Place and route homework S'14

note: you may need to set up the environment after you start a terminal.

```
csh
source /apps/design_environment
```

First, create a directory to work in

```
mkdir pnrhw
```

Then copy the files required from Professor Jones account to your account.

```
cp -R ~morris/PnRhw/* pnrhw
```

Change inside the pnrhw directory, and you can synthesize the project and move on to place and route.

The next step is to synthesize the design to gates. These gates are for a simple 0.18u library from OSU. They are not a complete ASIC library, but the synthesizer can build almost anything using nothing more that about 20 gate types and a few flip flop primitives.

To perform the synthesis, you should issue the command:

```
./run5pnr.pl 25 hope.txt
```

if the command doesn't work, try entering the command

```
csh
```

and then try the command again.

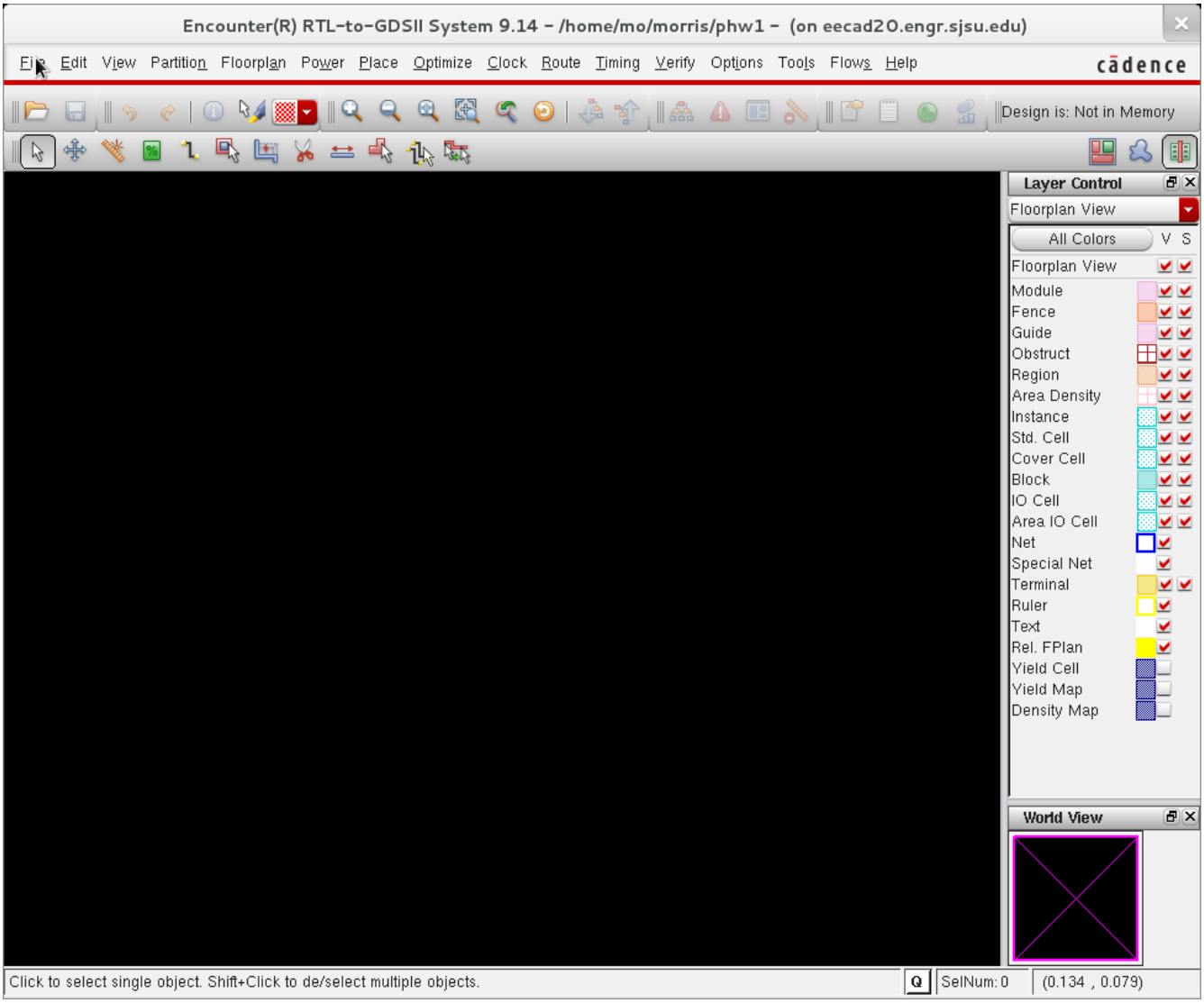
This will perform a synthesis of the design, and place the results in the hope.txt file. The synthesis script creates two files:

1. poly5_gates.v --- The synthesized gate level verilog netlist in the OSU library
2. poly5_gates.sdc --- A delay constraints file that contains the clock and delay constraints

You are now ready to run the place and route program. This is started by running the encounter startup script. (Copied earlier into your working directory). Enter the command:

```
./run_encounter
```

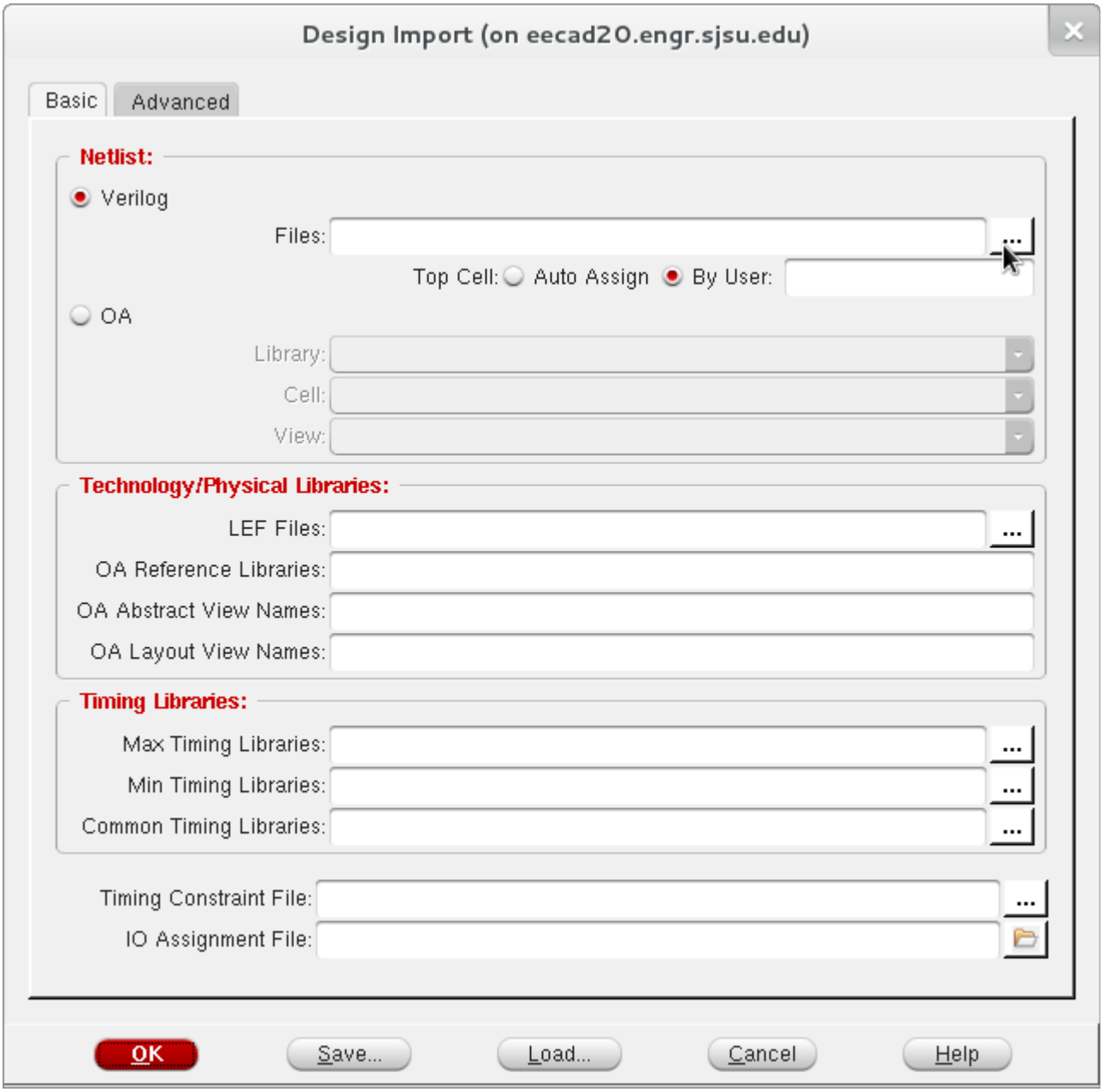
Do NOT place a '&' after this command. Encounter seems to have problems if started in the background. You should get a screen somewhat like:



Now, you need to setup the file information. There are several items to specify. These include:

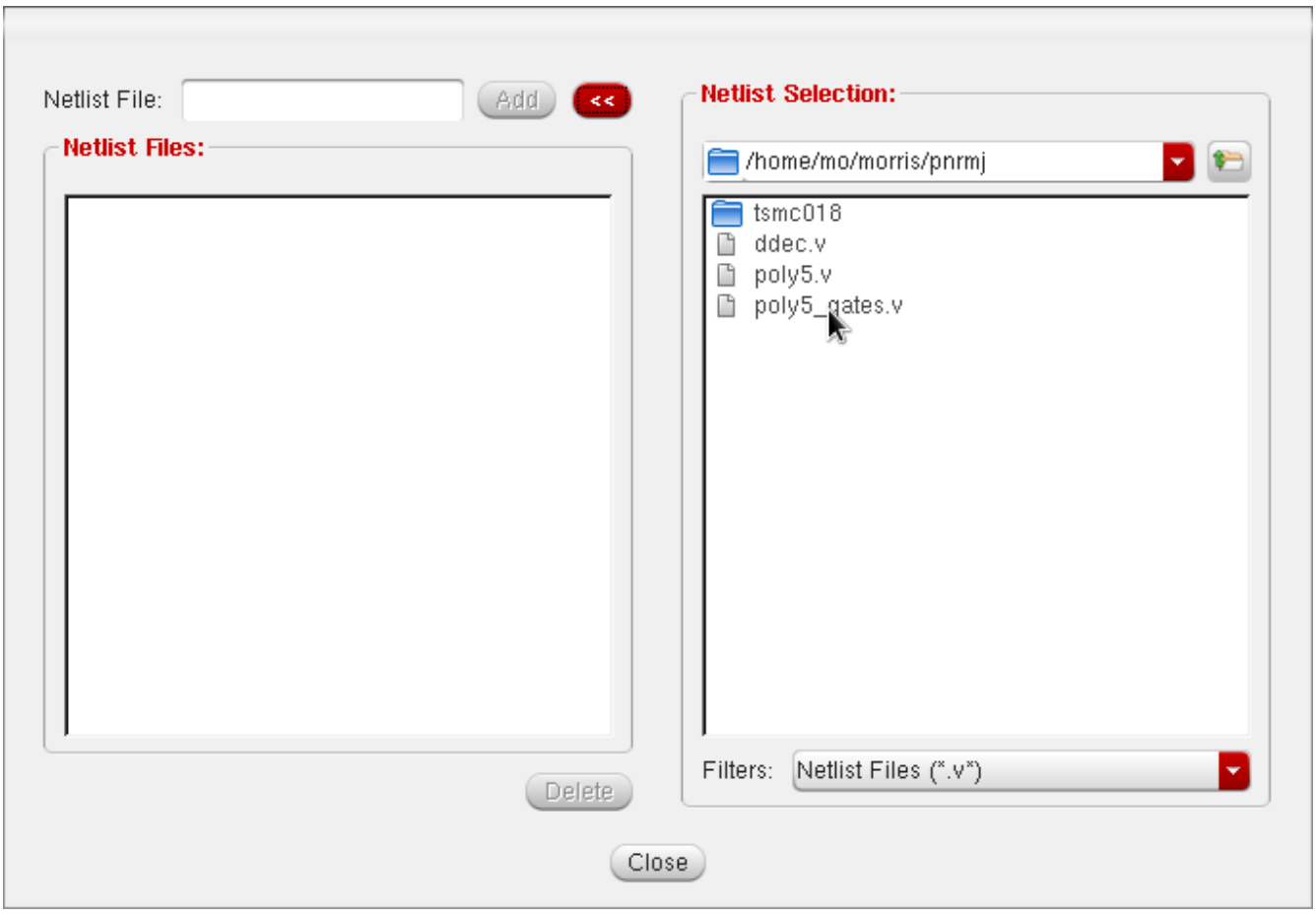
1. gate level netlist
2. The library of cells
3. Timing information for the cells
4. The timing constraints for the design
5. Where power and ground are located

Place the cursor on the <File> menu item in the upper left corner of the encounter screen. Click on File, and you then clock on <Import Design>. This will bring up the Design import window.

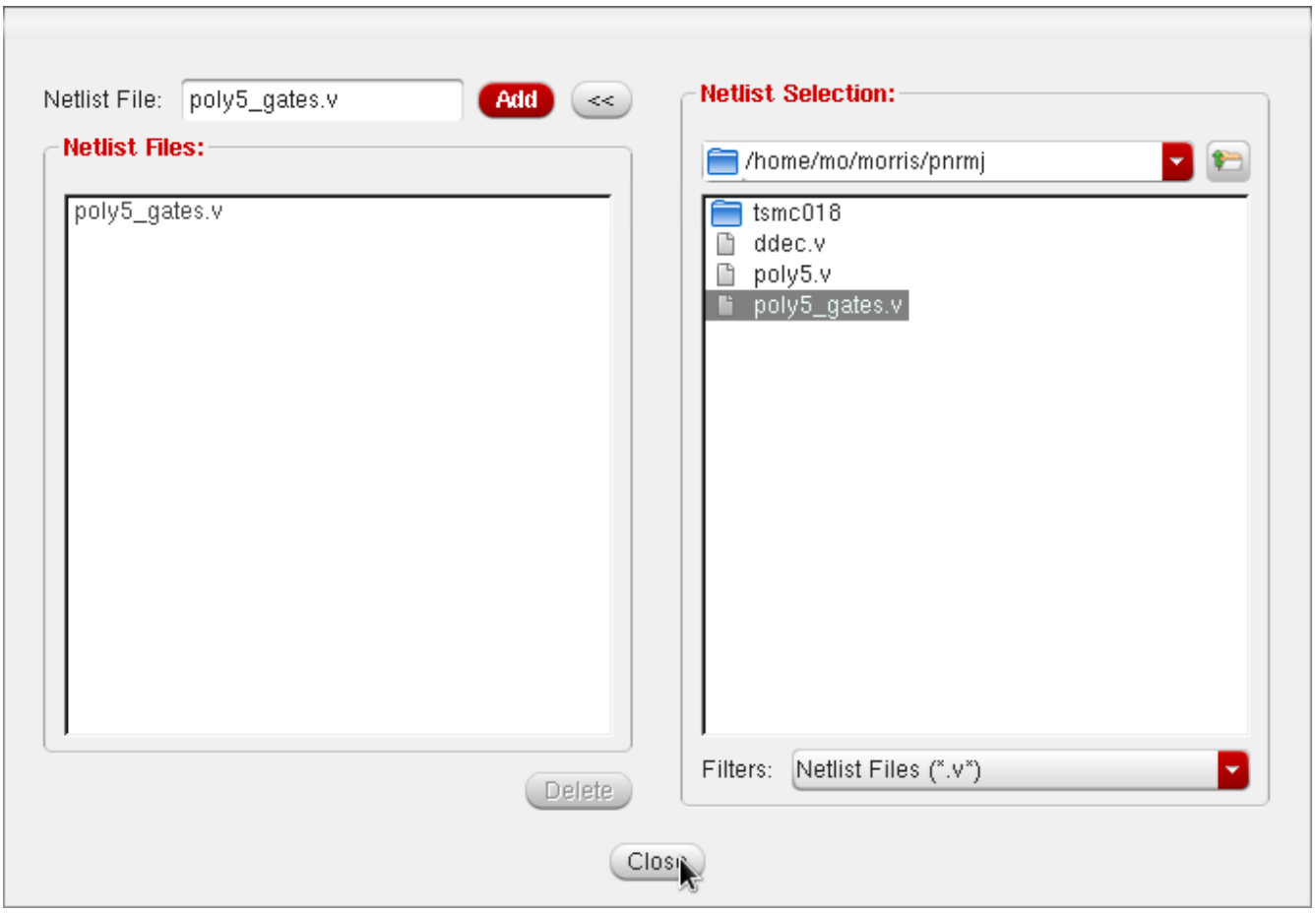


Click by the three dots '...' by the Verilog Files area. This will open a menu where a file will be selected.

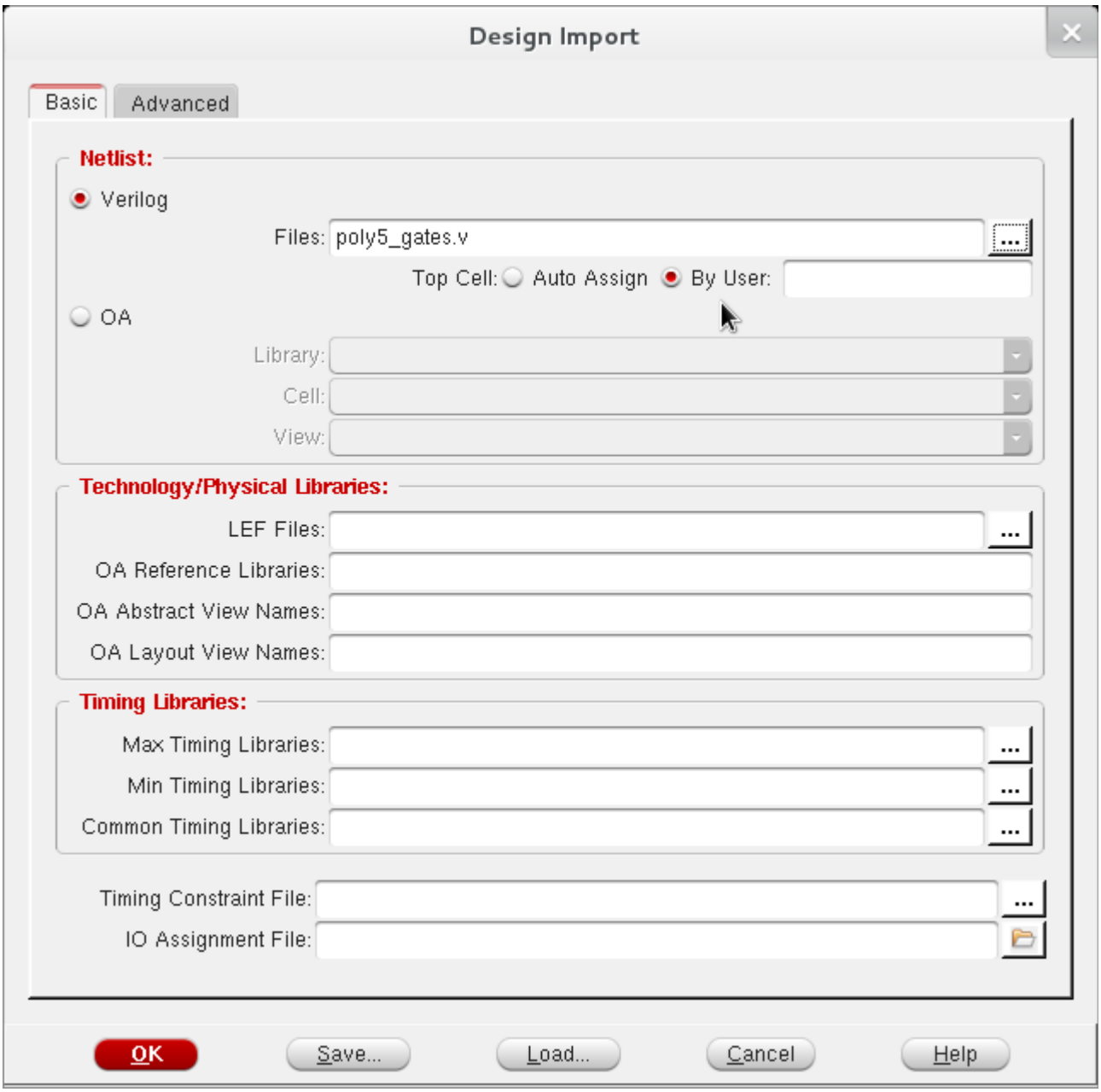
Click on the '>>' portion of the menu to open the file browsing menu.



Double click on the poly5_gates.v file (The netlist created by the Synopsys synthesis step) It will transfer the name to the netlist files area.



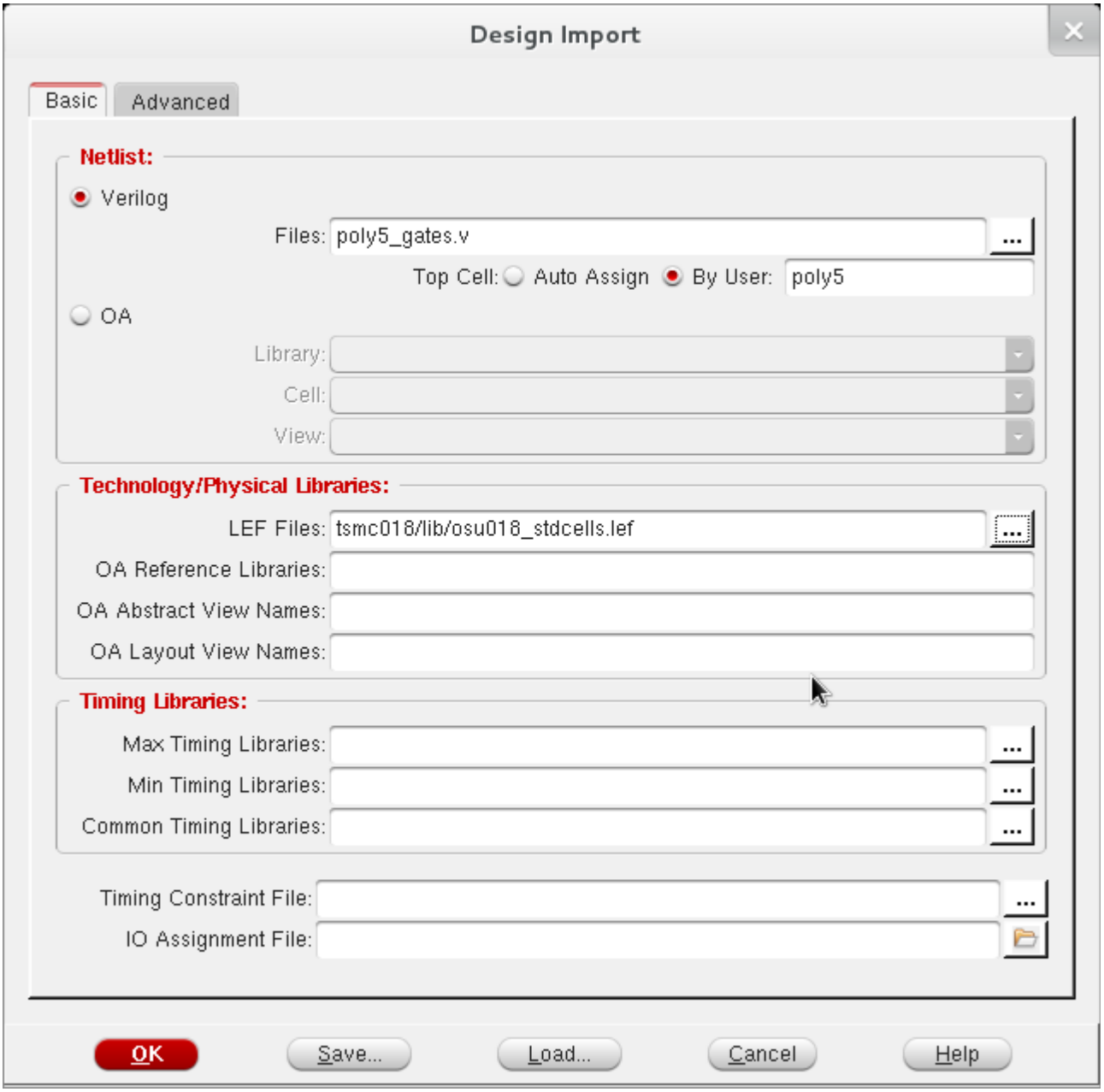
Click close, you should now have the poly5_gates.v file in the Netlist Files: area. (You could have typed it there, but you now know how to find files).
Your screen should now look something like:



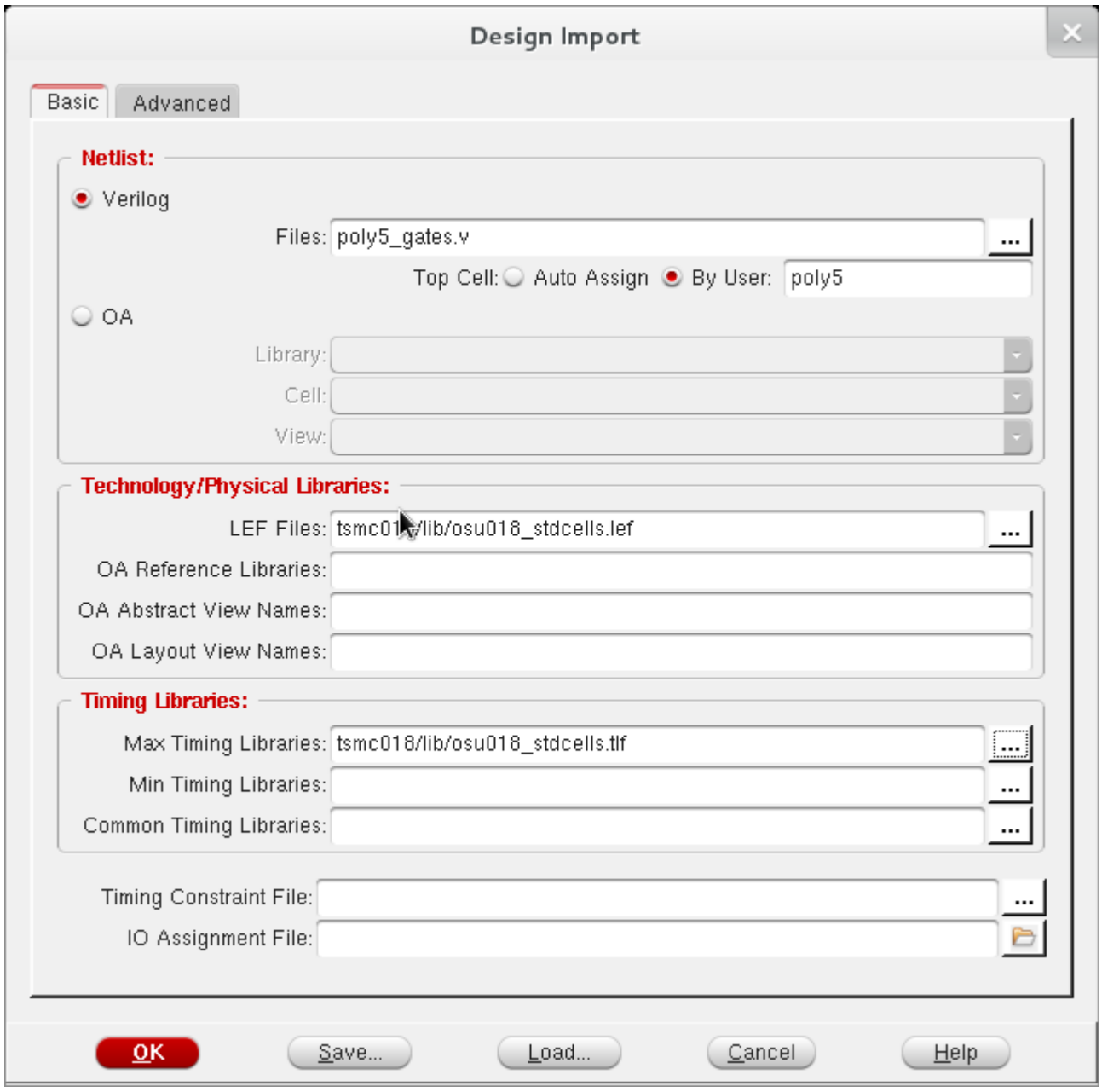
Specify the Module Name now. ust set it to poly5

Next, select the LEF files. These files tell the system about the physical design of the cells. (Not the transistors, but how to use the cells in the place and route). Click on the '...' and select the

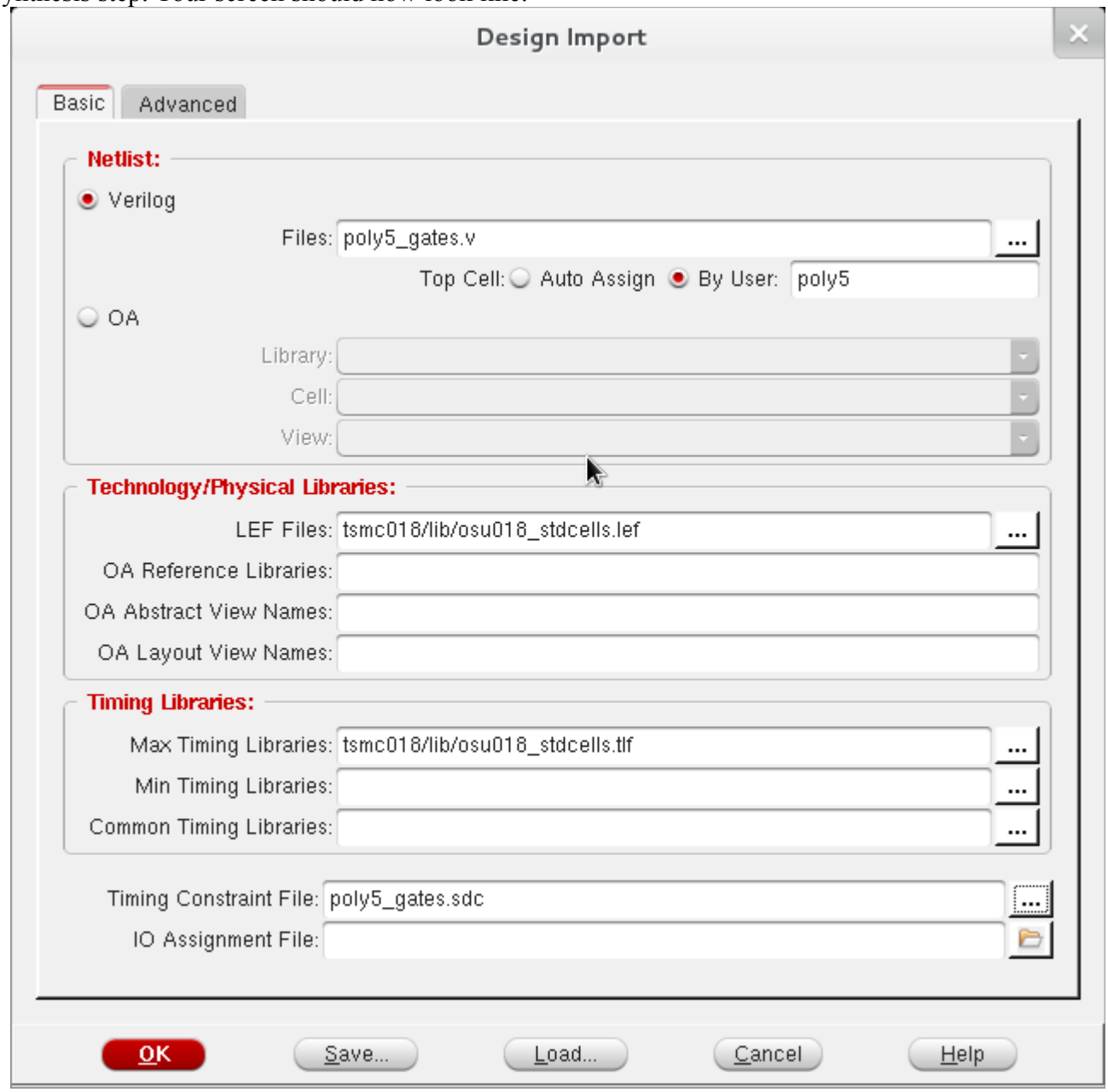
osu018_stdcells.lef file. This is inside the tsmc018/lib directories. You can double click on tsmc018 and then lib to move into that library. When you are finished, your screen should look something like:



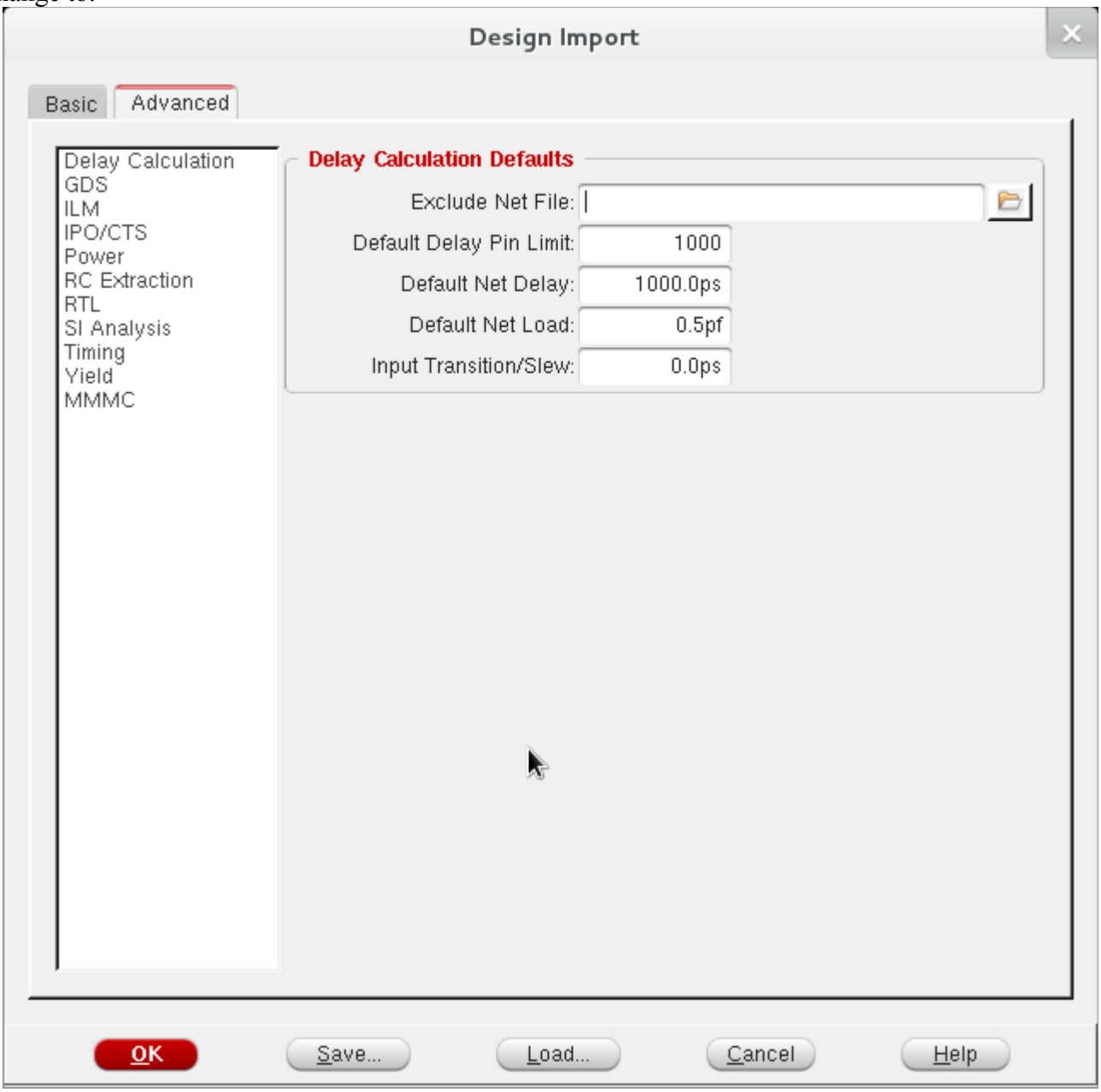
Next, get the max timing libraries. (The only ones out there). They are also in the tsmc018/lib area, but have a .tlf extension.
Your screen should now look something like:


Design Import
Basic
Advanced
Netlist:
Verilog
Files: poly5_gates.v
Top Cell: Auto Assign By User: poly5
OA
Library:
Cell:
View:
Technology/Physical Libraries:
LEF Files: tsmc018/lib/osu018_stdcells.lef
OA Reference Libraries:
OA Abstract View Names:
OA Layout View Names:
Timing Libraries:
Max Timing Libraries: tsmc018/lib/osu018_stdcells.tlf
Min Timing Libraries:
Common Timing Libraries:
Timing Constraint File:
IO Assignment File:
OK
Save...
Load...
Cancel
Help

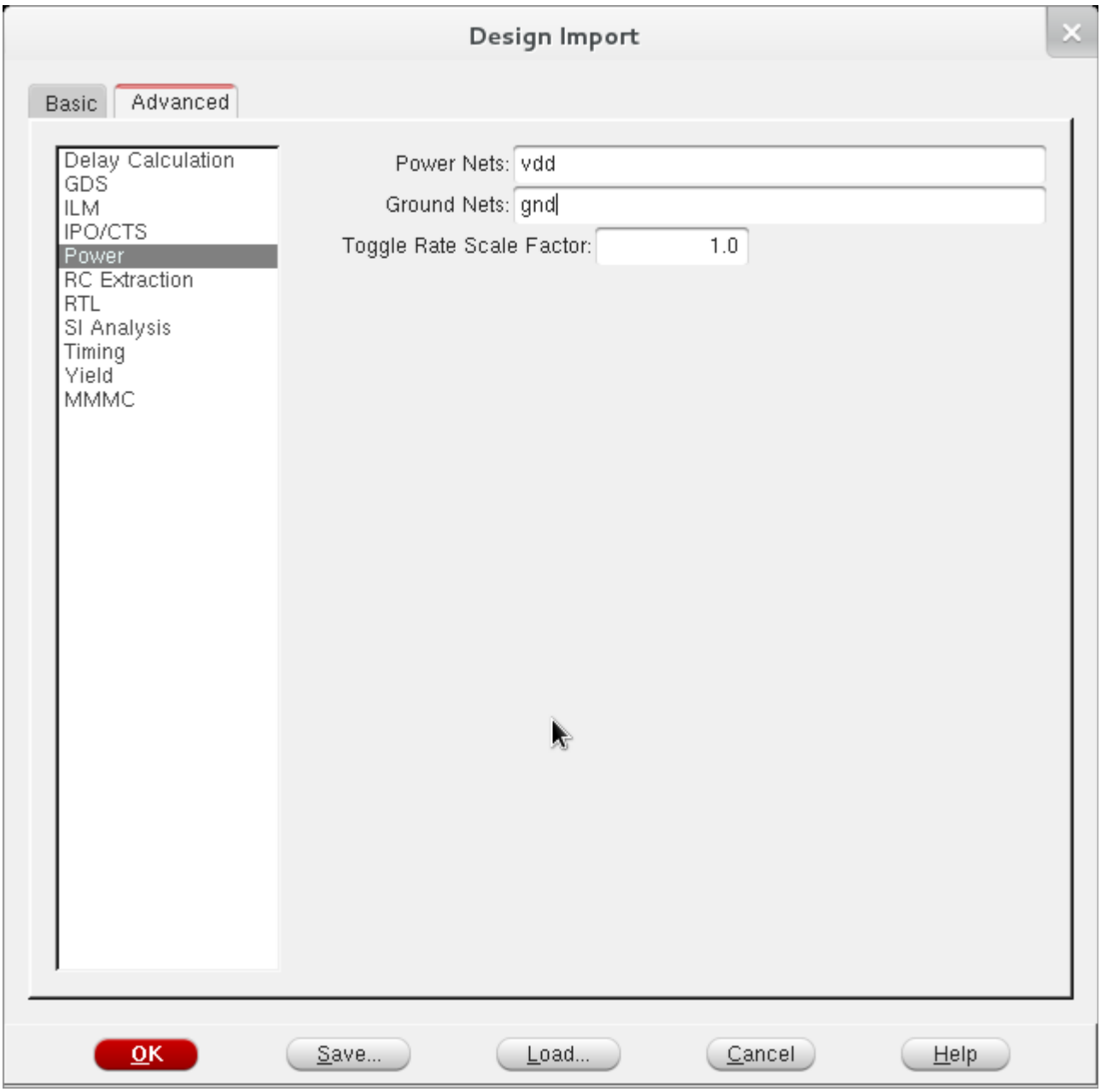
Next, get the timing constraint file. (poly5_gates.sdc). This should be in your directory from the synthesis step. Your screen should now look like:



Now click on the <advanced> tab. Click on the item to the left that says <Power>. Your screen should change to:



Click on Power. Then an area will appear to place the names of the power and ground pins. In the power nets area, type vdd. In the ground area, type gnd. Your screen should now look like:

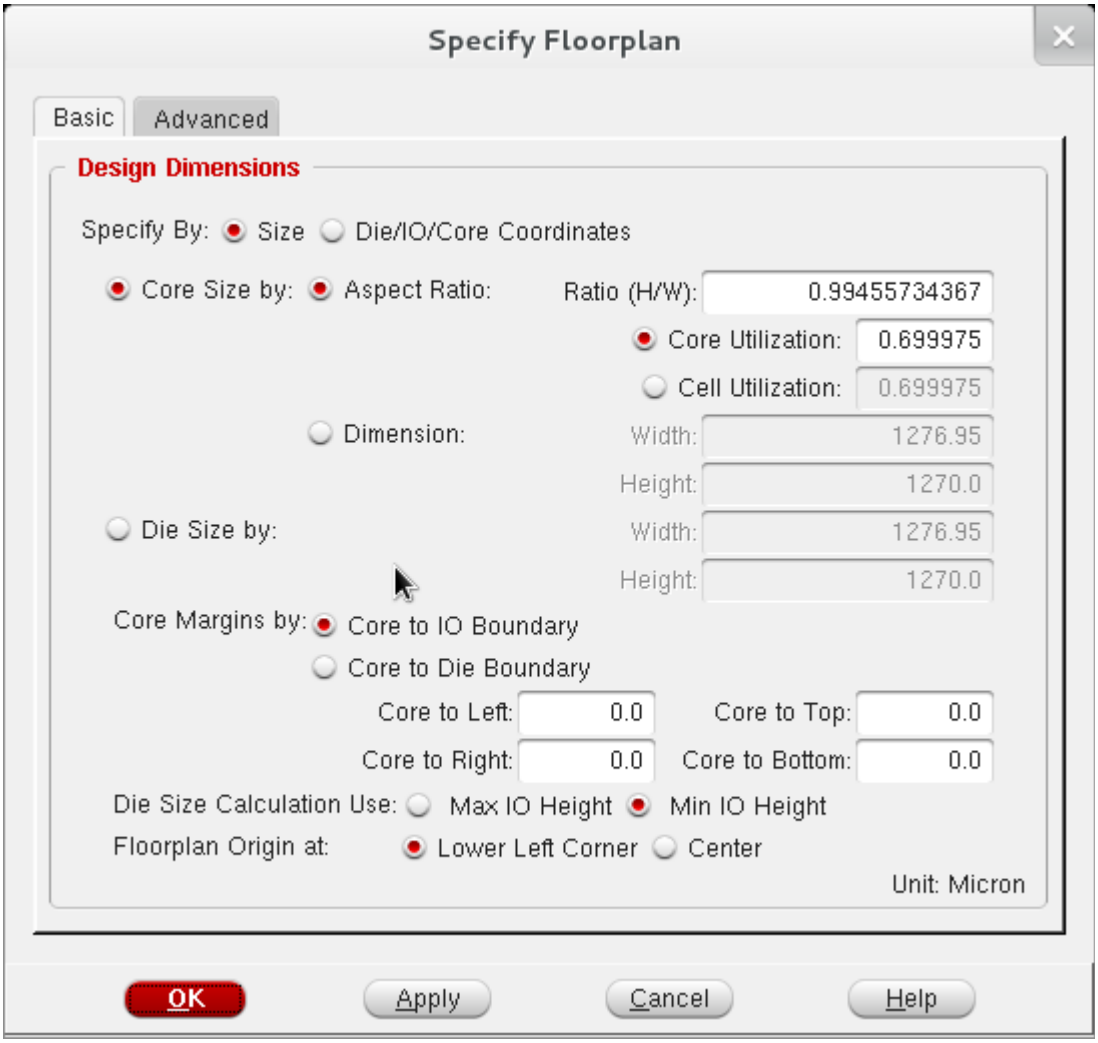


go back to the basic tab

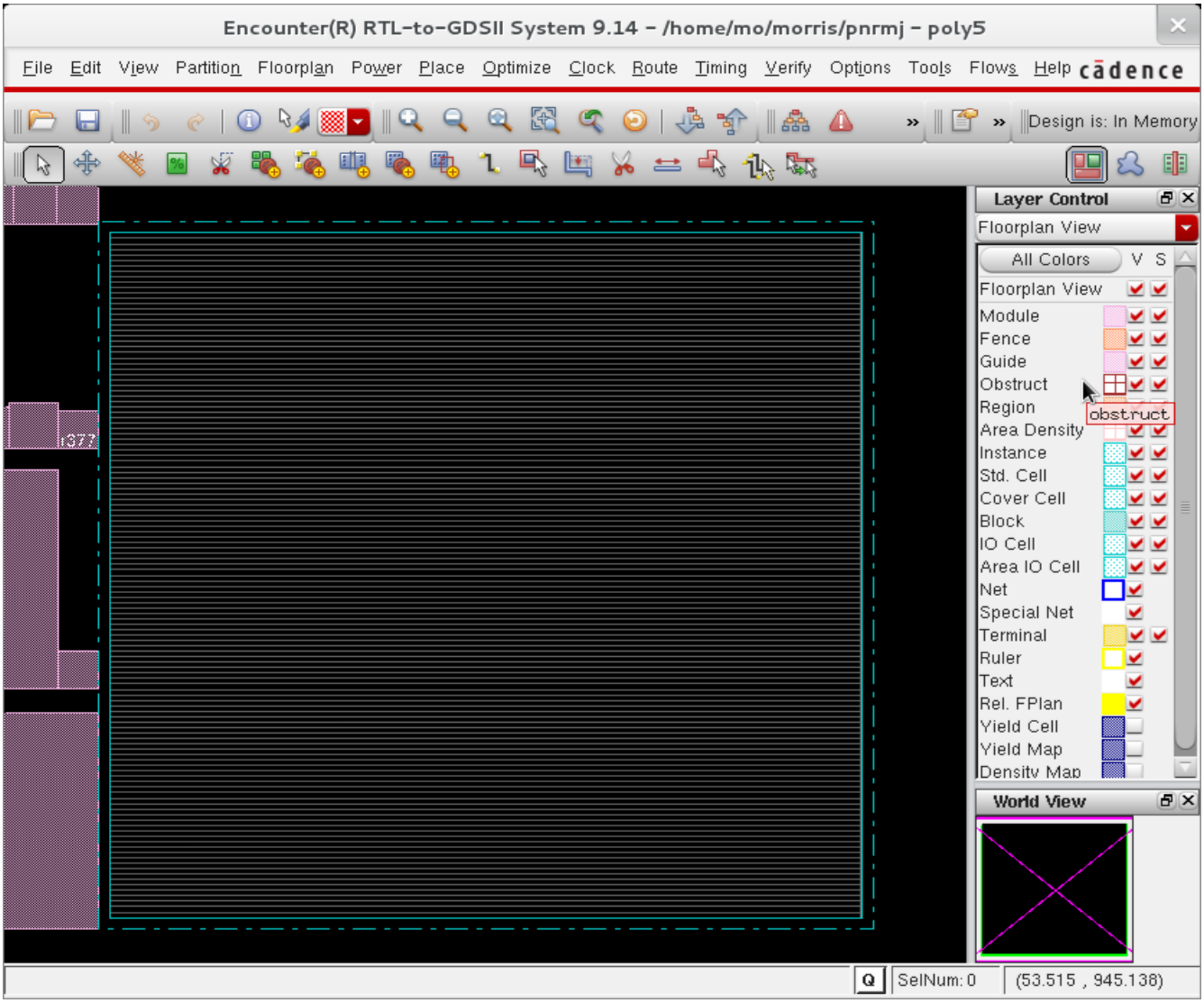
click OK.

You should now have the main window with some layout area presented. (There are no cells in it yet).

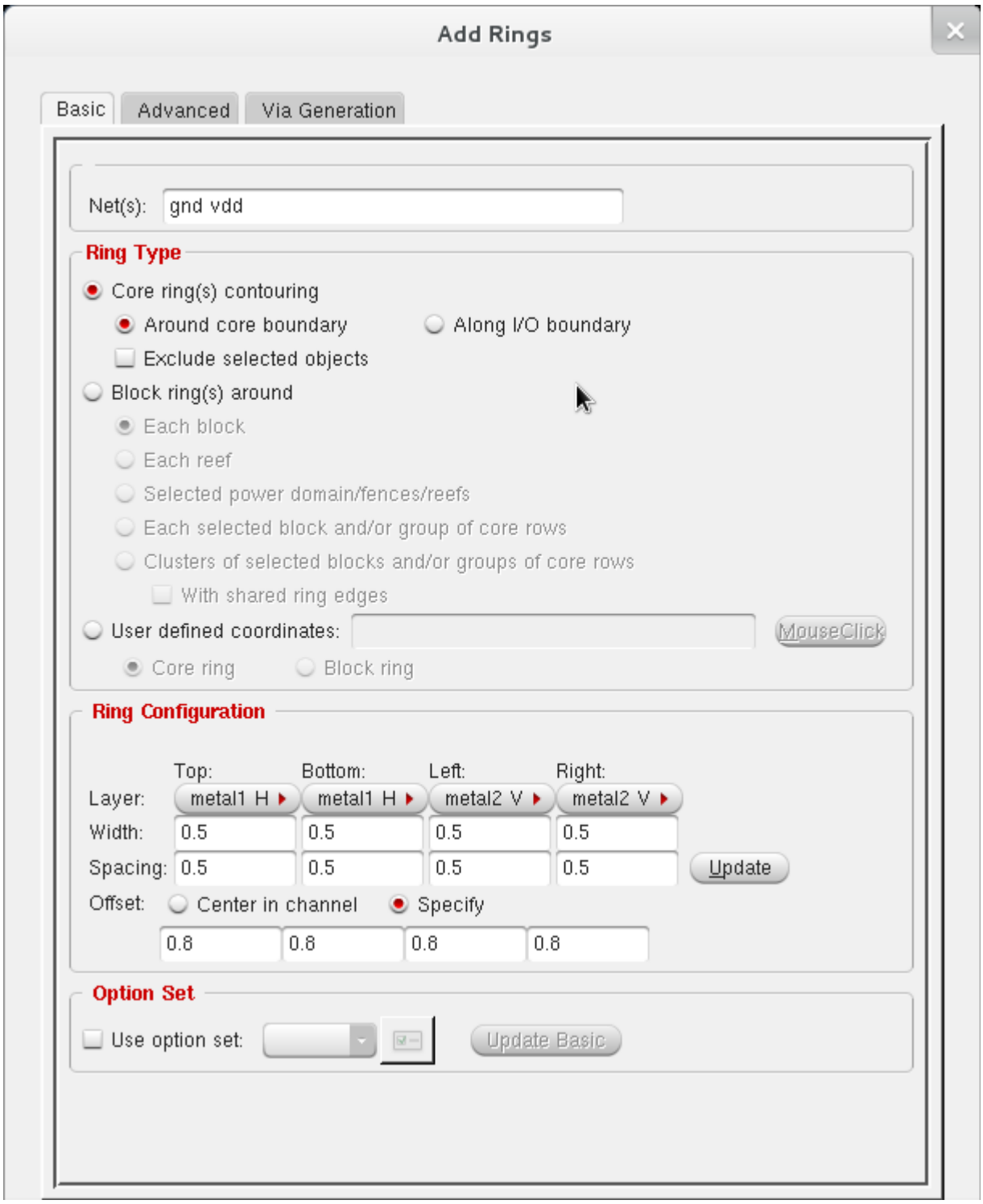
In the next steps, we will create some room for power and ground lines around the core of gates. Click on <Floorplan> then <Specify Floorplan> This should bring up a screen like:



Change the Core to Left, Core to Top, Core to Right, and Core to Bottom to values of 20, and click OK. If you did it correctly, you should now have some space around the area allotted for gates.

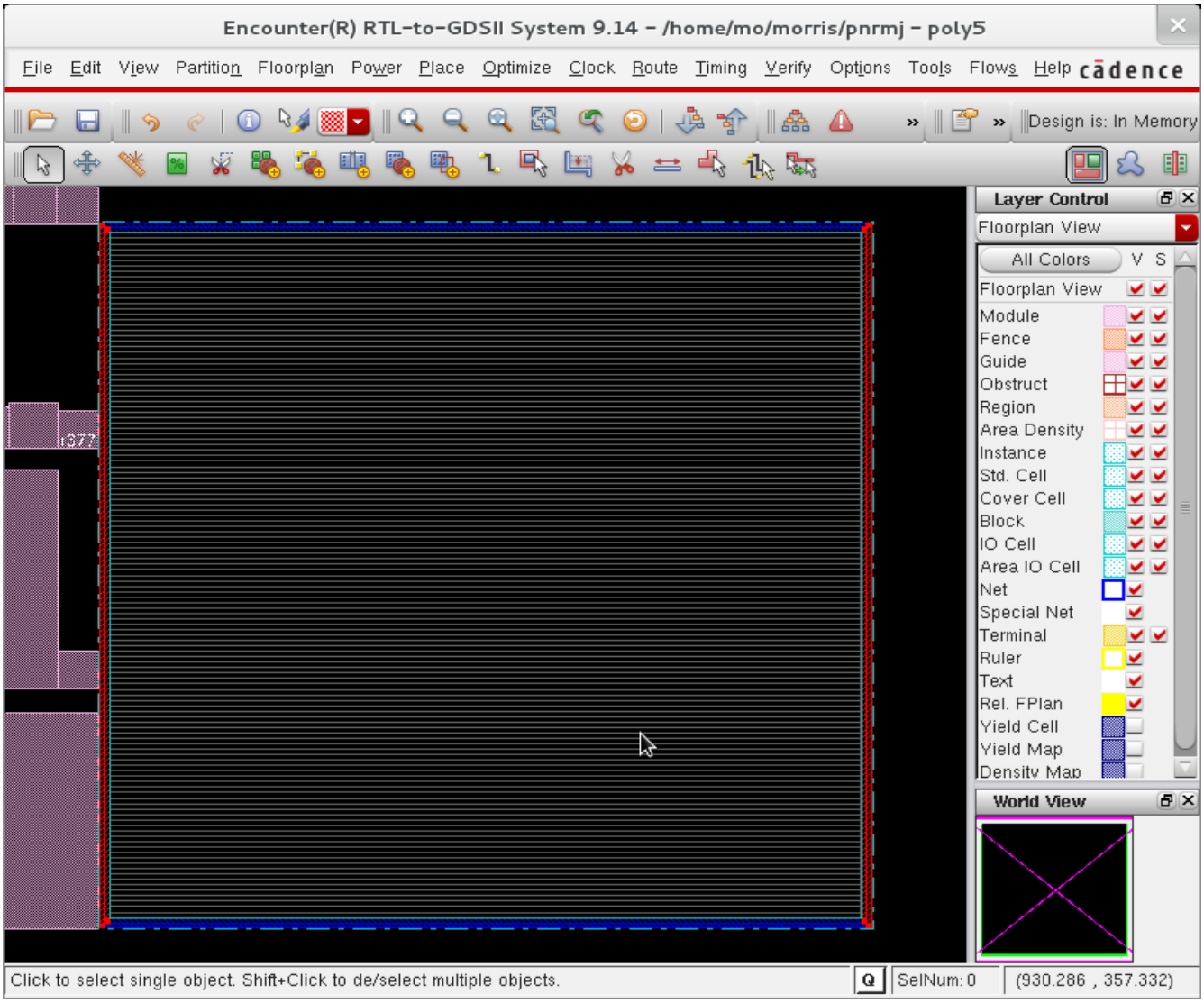


Click on the <Power> menu item, and then on <Power planning> and then on <add Ring>. You should get a menu like:

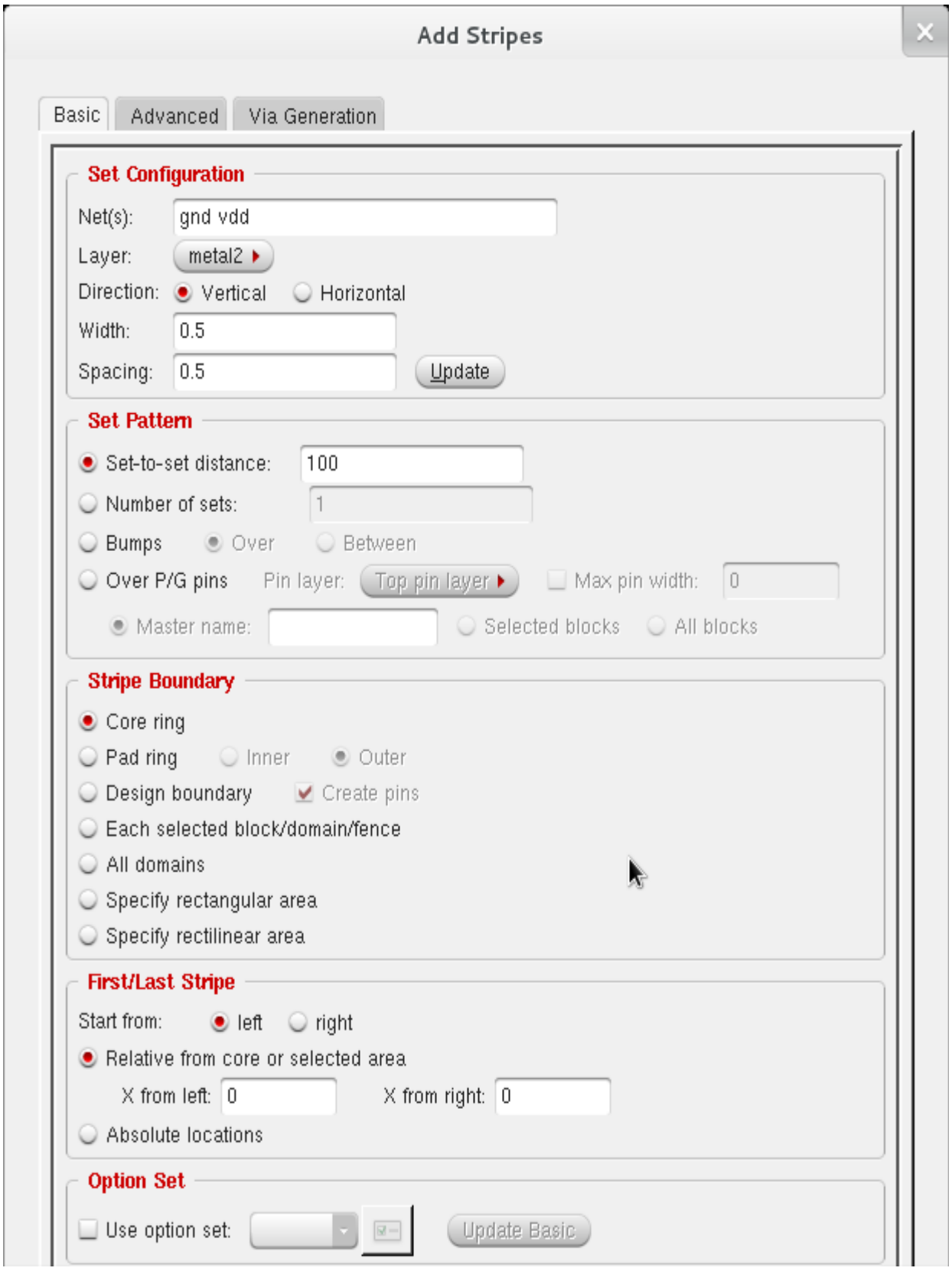


Change the width fields to '9' for the Top, Bottom, Left, and Right, and click OK.
On some monitors, the OK may be off the bottom of the screen. If this happens, then place the cursor after the last 0.8, and hit tab twice. Then hit enter.

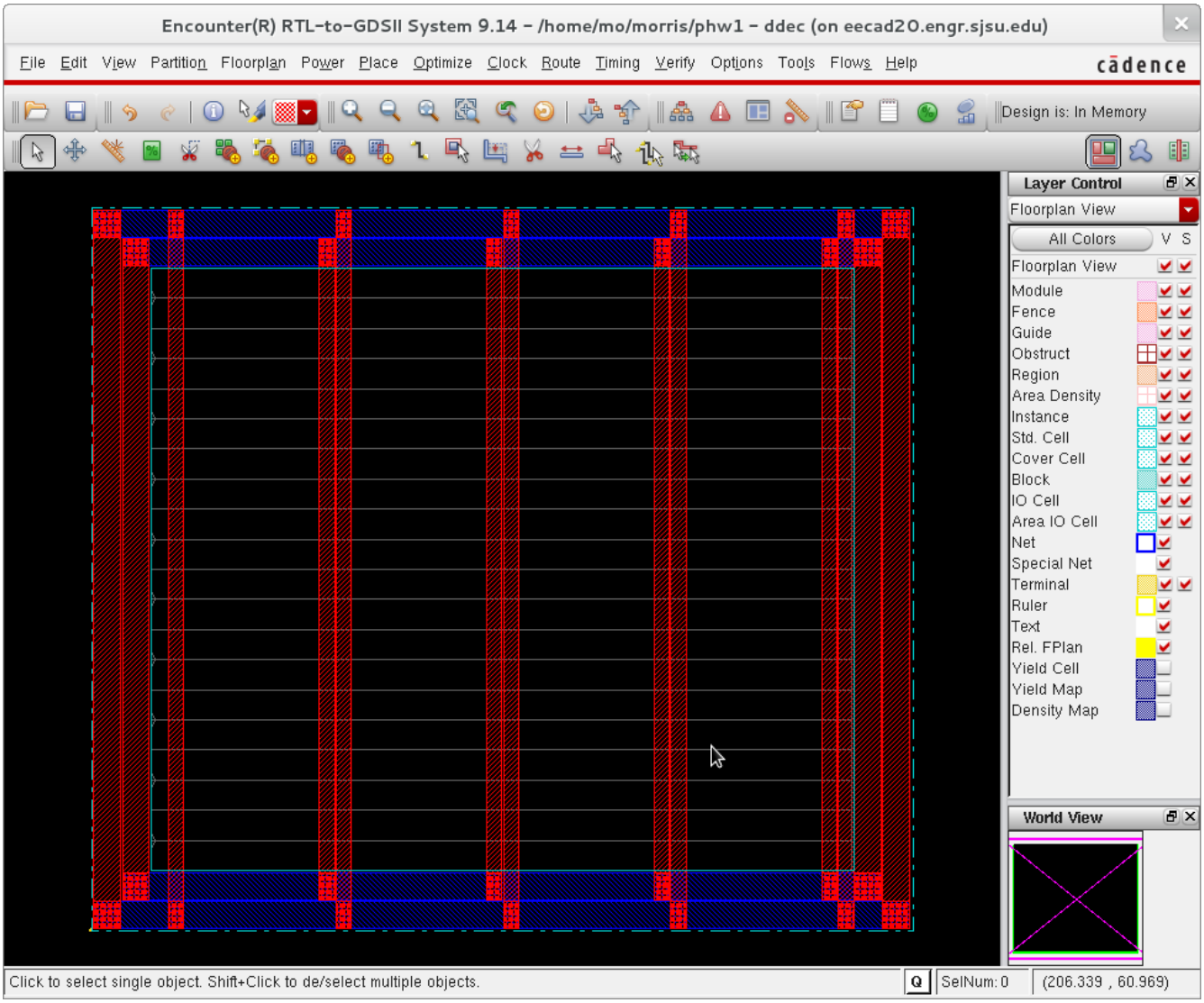
You will now have a ring of power and ground around your gates:



The wires running through the gates are not very big. We add some stripes of power running through the gates to improve the voltage drops in the design. Click on <Power>, and then on <Power planning> and finally on <add stripes>. This will bring up the striping screen.

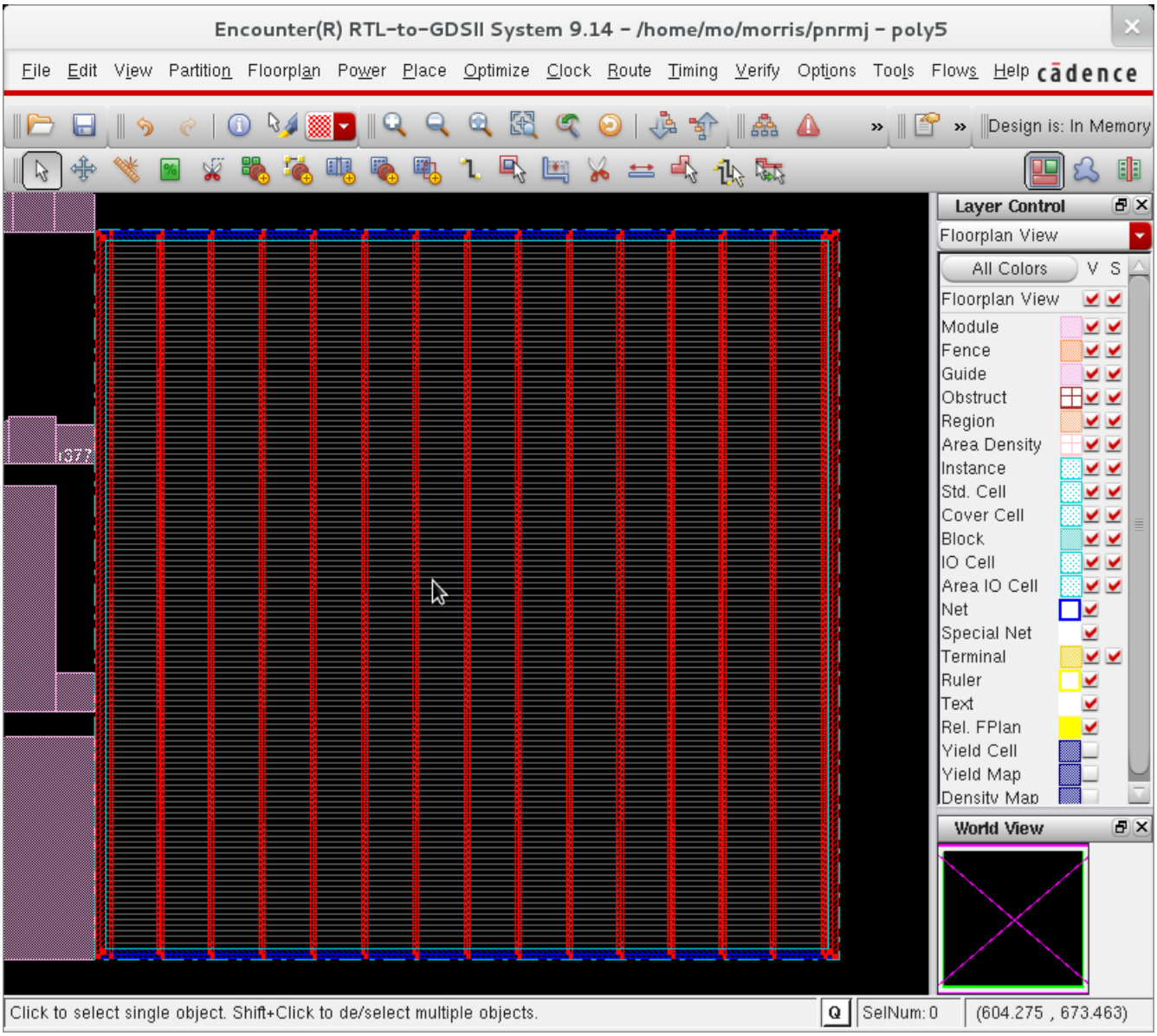


Change the width to 5, and click on Number of stripes, and set the data field to 15. Then click on OK



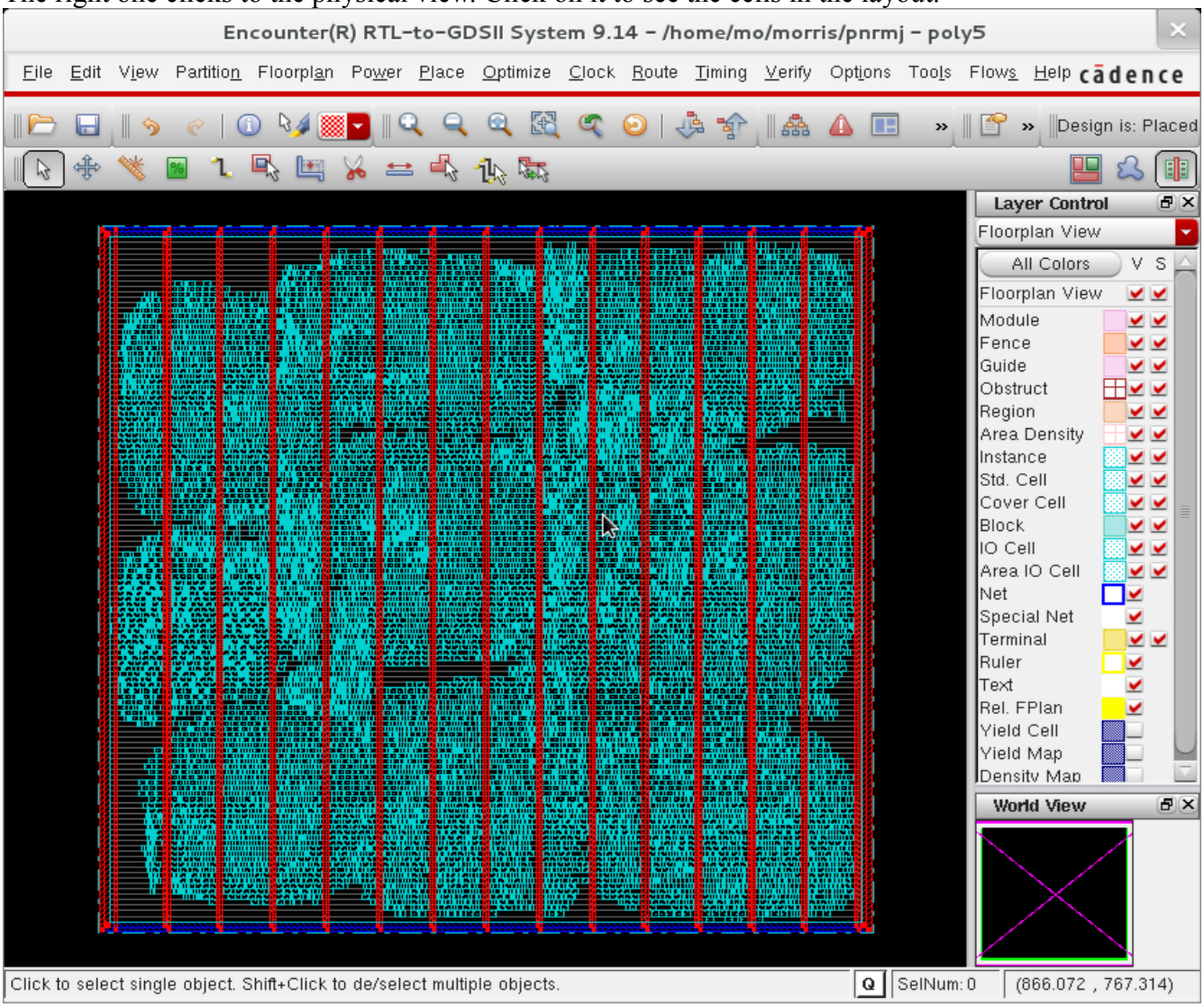
(again it may be off screen requiring the use of the tab key from the last entry field)

This should have added some power and ground stripes to your design:



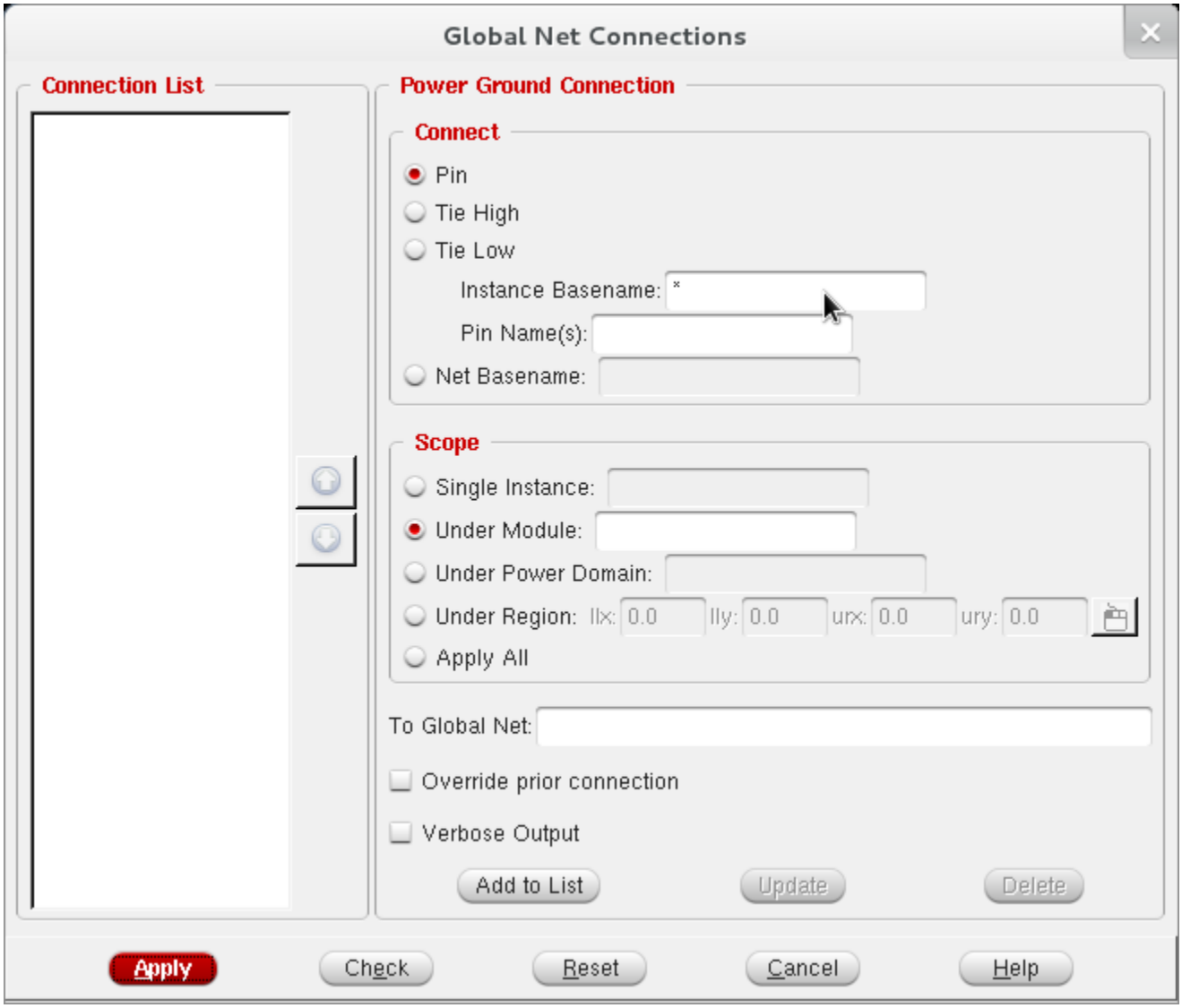
Now is the time to place the gates. Click on <Place> and then on <standard cells>. A menu will pop up. You can just click on OK here. It may take many minutes to get the design placed. When it is finished, you probably don't see anything different. That is because we are now viewing the design in floor planning mode. The are in the upper right has three icons that change the view.

The right one clicks to the physical view. Click on it to see the cells in the layout.

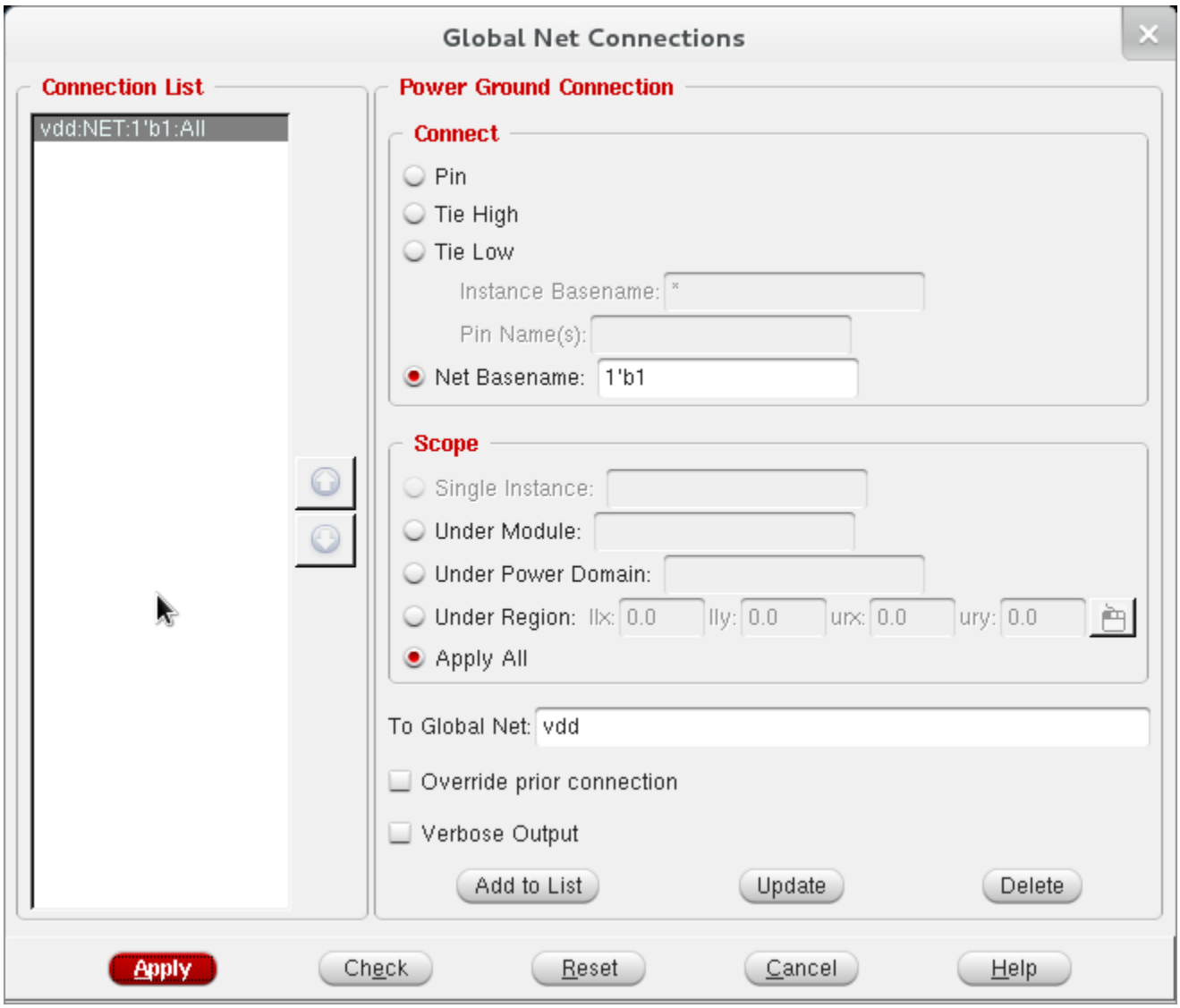


Each box represents a different type of gate. You can use the Zoom commands to zoom in and out of the design. If you get close enough to the boxes, you will see the name of the box, and the pins on the box. (There are no wires yet.) Next, you will connect the power and ground signals in the design. Before doing that, we need to tell the system that the verilog signal 1'b1 is connected to vdd in the design. (Some systems use a special cell to connect to logical 1 or zero).

To do this, click on <Power> and then on <Connect Global nets>. You will get a selection screen:

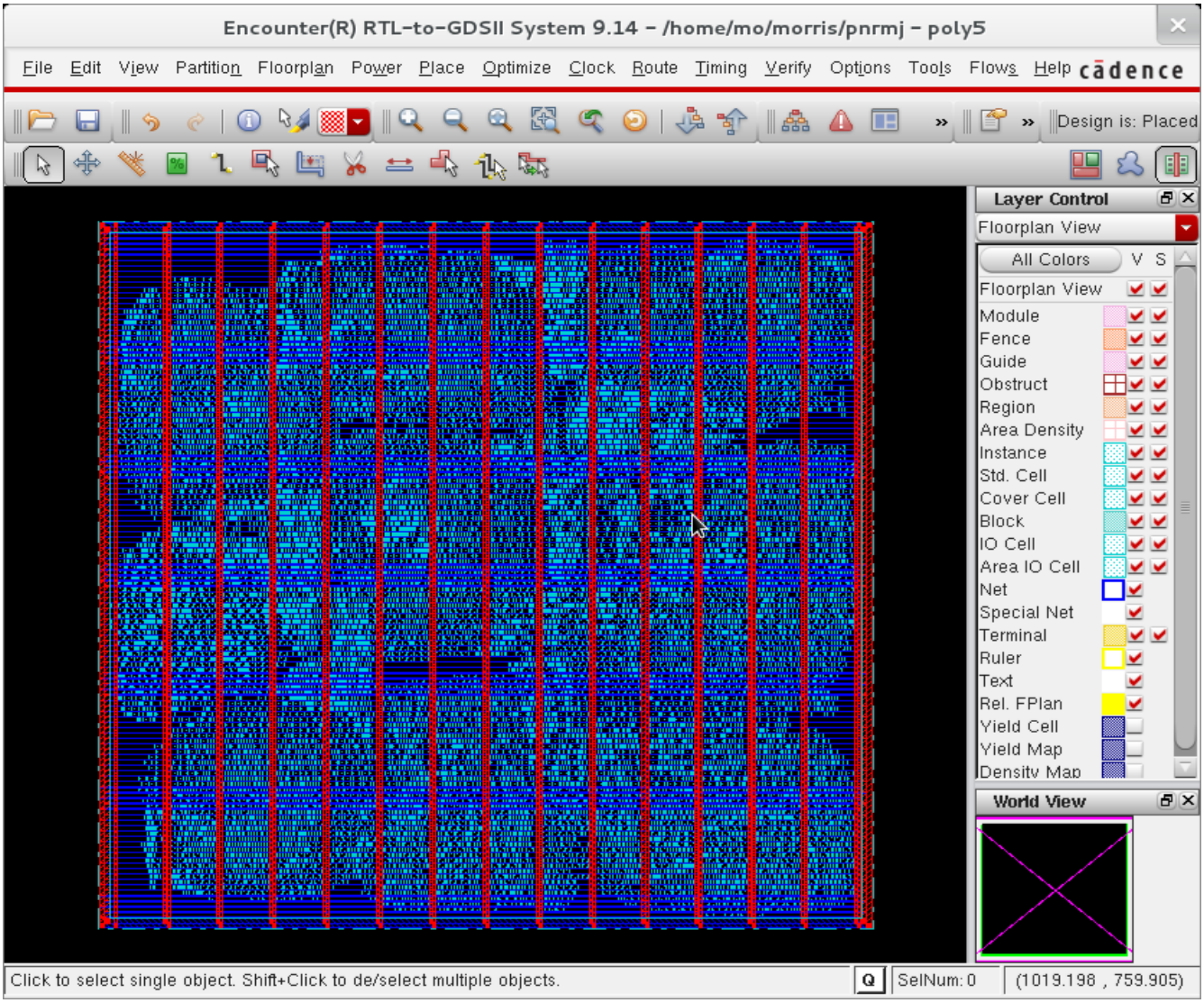


Click on the dot next to Net Basename, and enter 1'b1 then click on the dot next to “Apply all” under scope. In the space next to To Global net:, enter vdd then click <add to list>. Next click on Apply:



Next click on Cancel.

Now, click on <route> then <special route> (This will route the power and ground). When the menu comes up, just click on OK. You should see power and ground routed in the design.



You need to tell encounter to route the 1'b1 pins also. On the terminal where you launched the encounter tool, there is an area to enter a command line. It will say encounter 1> or some other number.

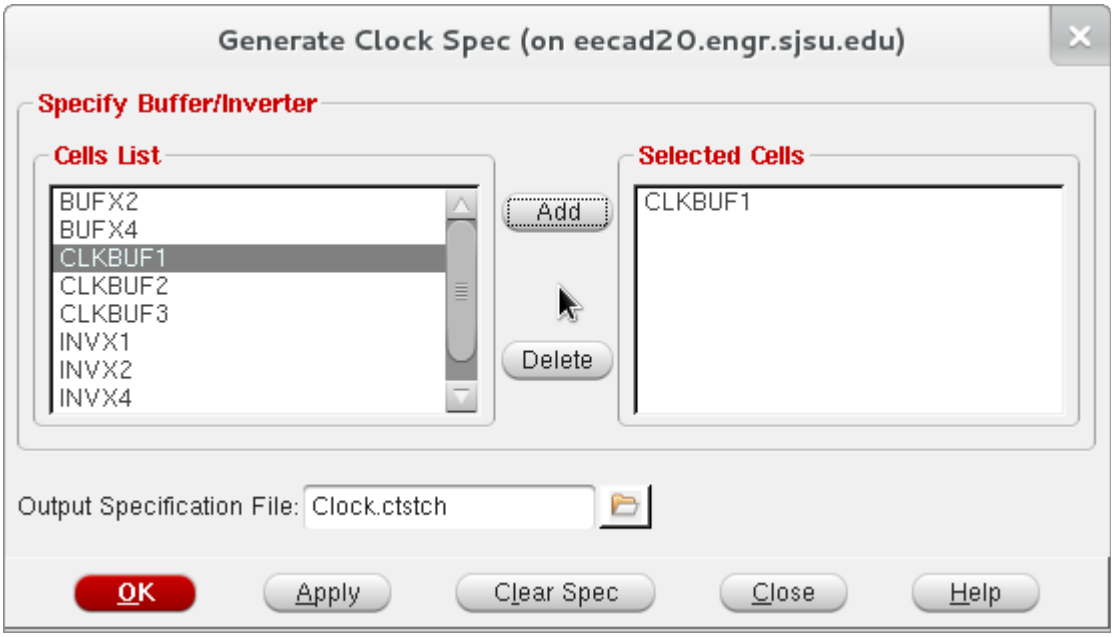
If you don't see this, place the cursor in the terminal window, and press enter. There may be other printout there at the moment...

On this line enter:

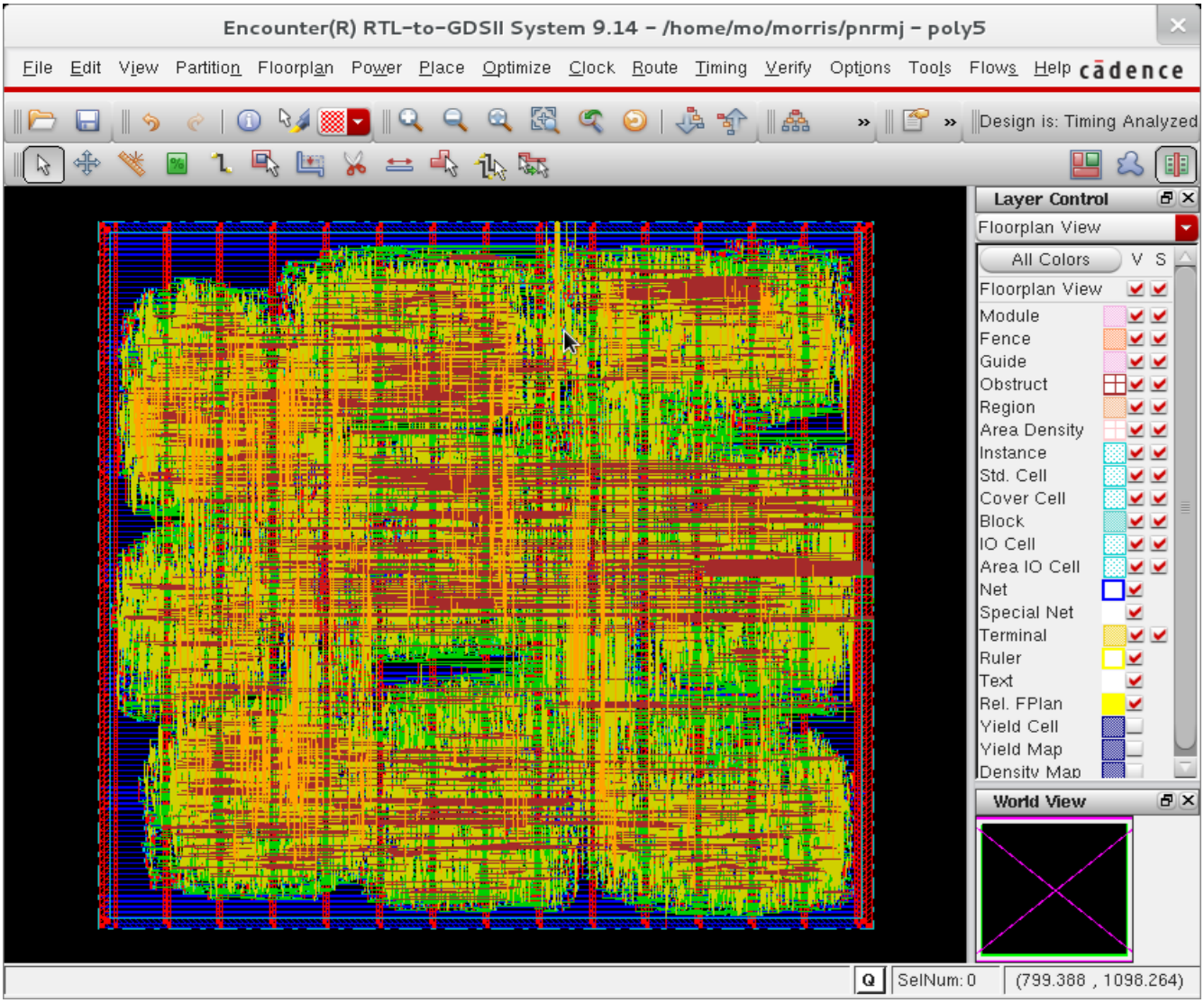
setNanoRouteMode -routeAllowPowerGroundPin true

then press return. This will tell it to route the Power and Ground Pins. (Other wise, the router assumes it has already been taken care of)

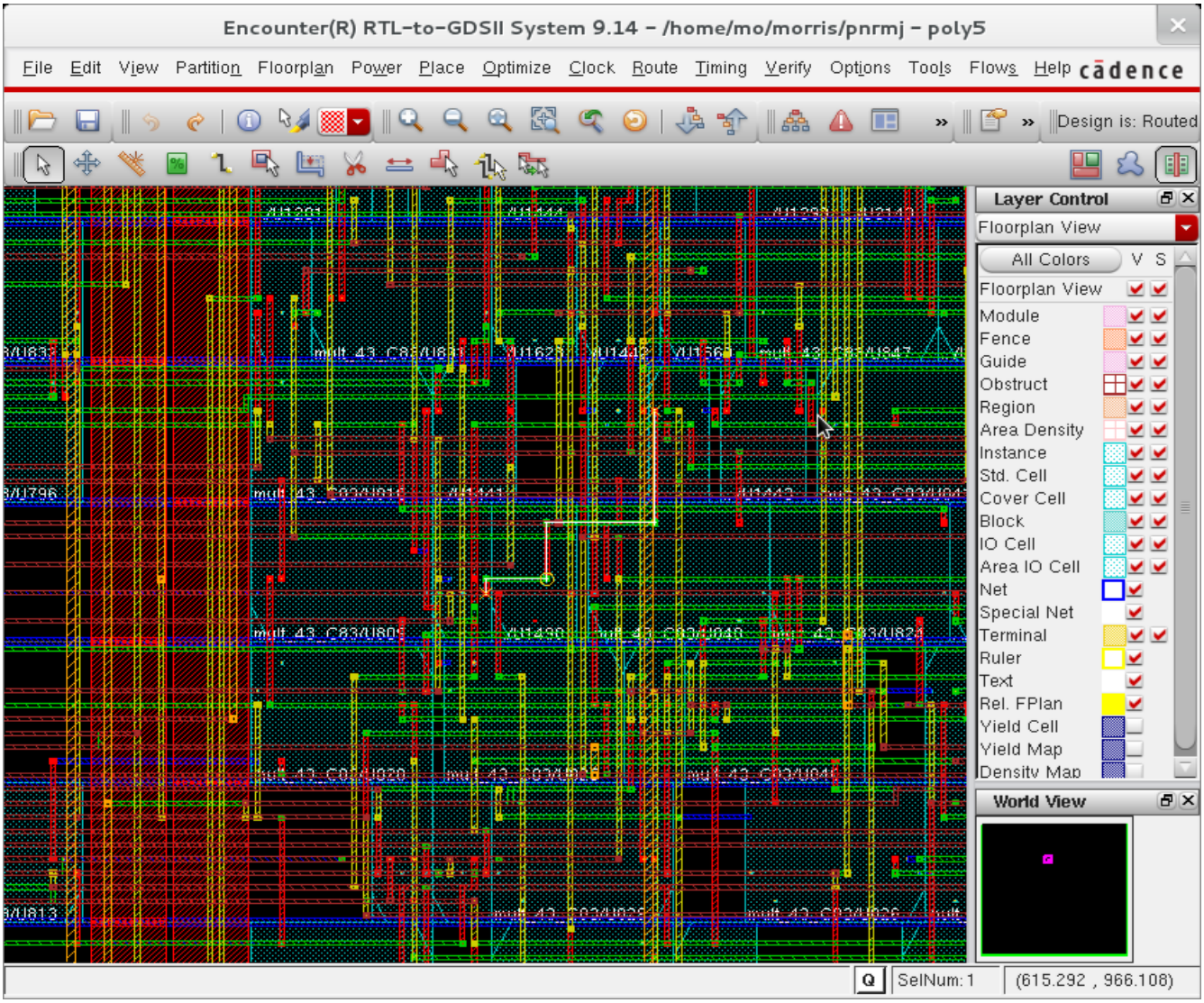
Next, route the clocks. Click on <clocks> then on <synthesize clock tree>. This will bring up a menu. Click on gen spec which brings up another menu. Pick CLKBUF1 and then add. After this, click on OK.



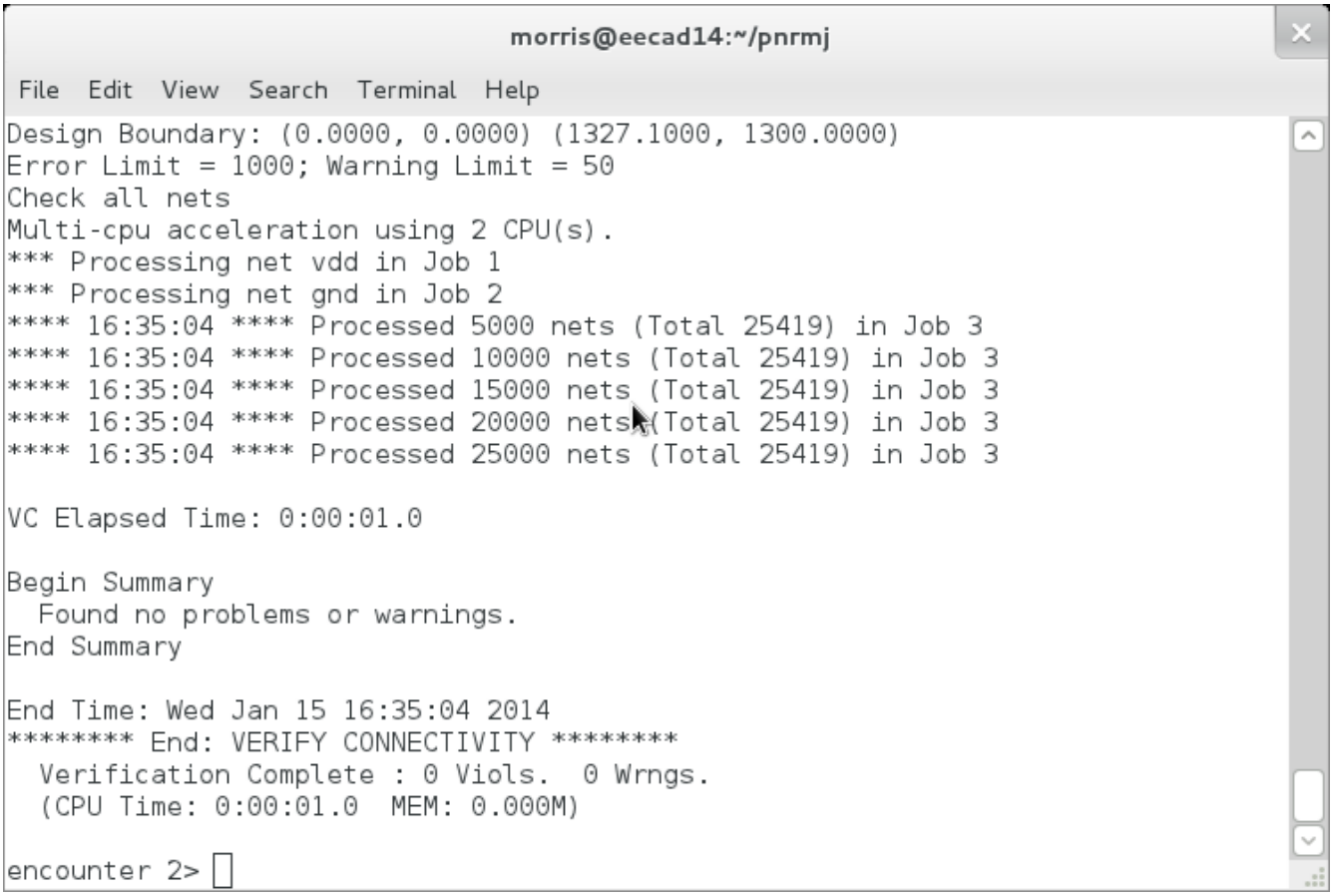
Now click <OK> on the synthesize menu.
Anything connected to a clock tree has probably been routed at this point.



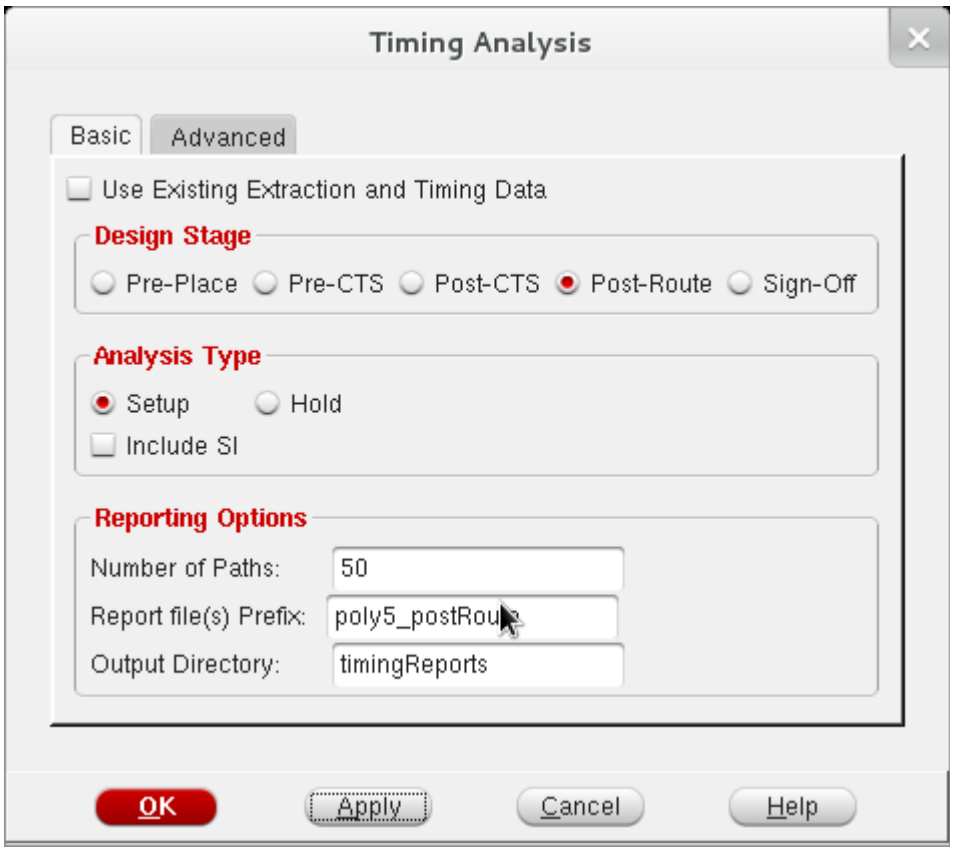
Now, click on <route> <trial route> and then <OK> This routes some more. Finally, click on <route> <nano route> <route> <OK> to complete the route. You now have a routed design. You can zoom in and look at the wires. The colors on the right let you know what you are looking at.



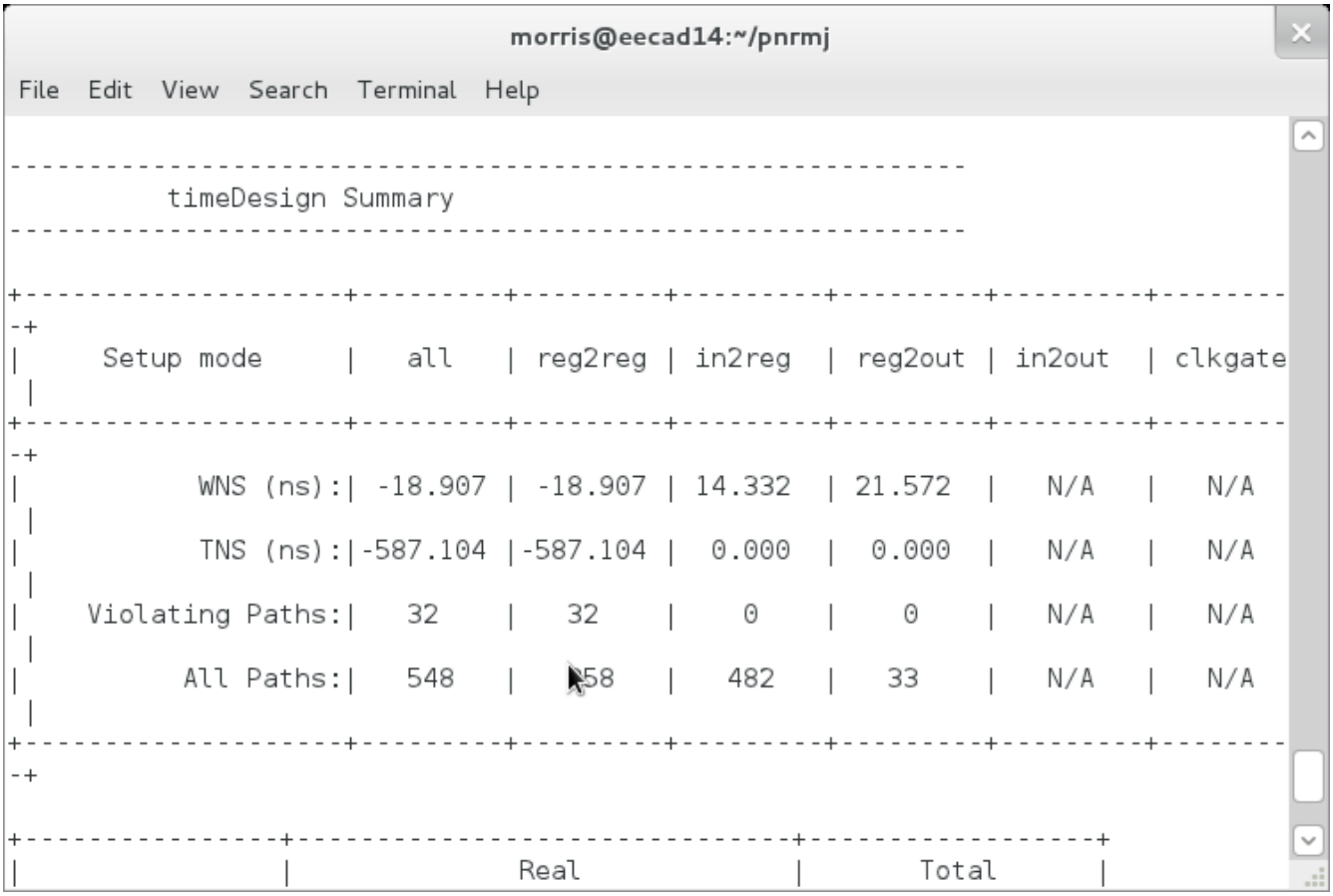
Next, click on verify then verify connectivity. This will bring up a menu, click OK. You should now see the report on your terminal window...



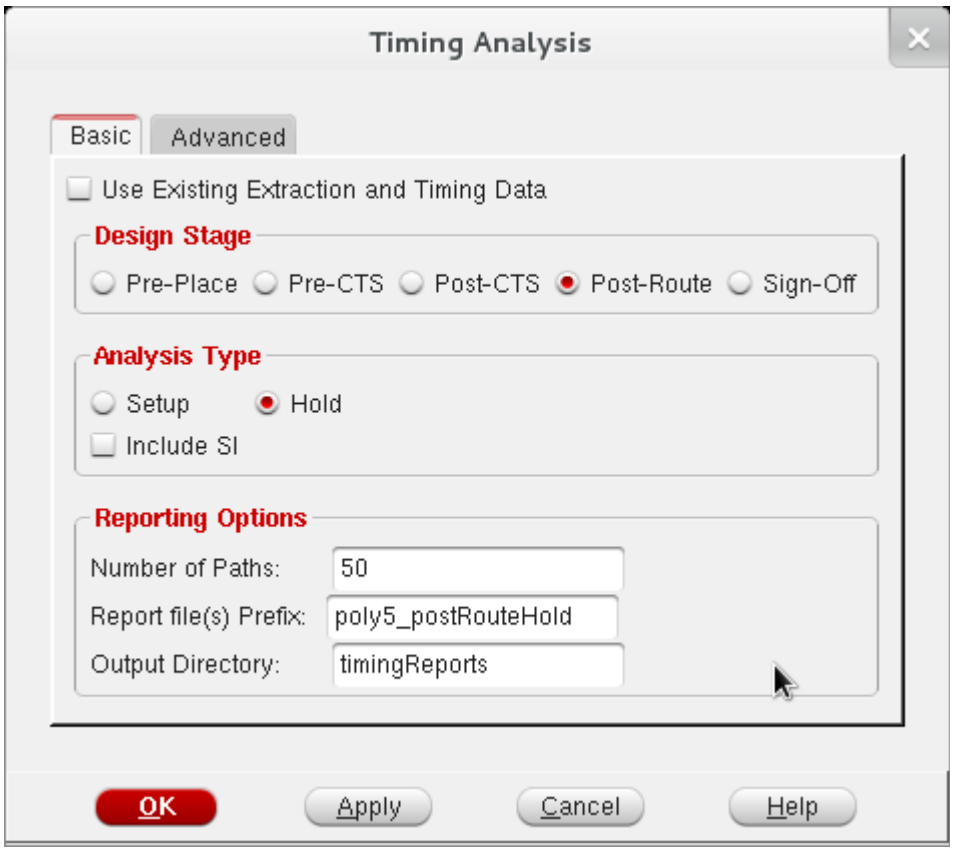
Now click on Timing, and then on Timing Analysis. This will bring up a menu.



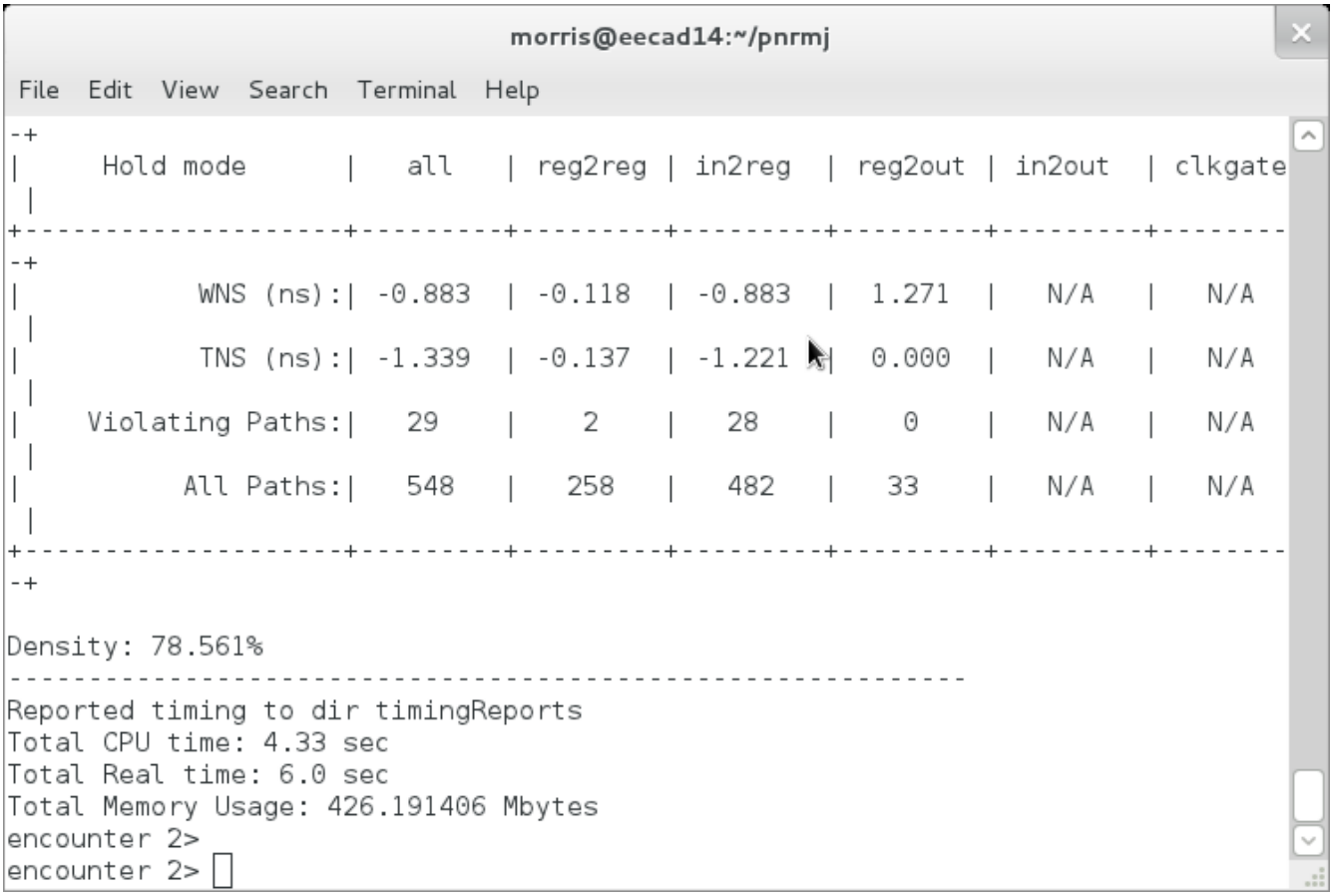
Click on Post-Route, and then clock OK. This will create a timing summary in your terminal. It is larger than the terminal, but this gives you an idea. 32 Nets have a register to register setup timing problem. (I didn't check hold yet). Look with the file manager (file cabinet on the activities menu) and you should find a timingReports directory, and a file with reg2reg in the name. This is a file you need to submit. These paths were not long in synthesis, but are long after place and route. We won't try and fix them now, but in a real setting, these would be given higher priority, and the route redone.



Now clock Hold, and create a report I added Hold after the name:

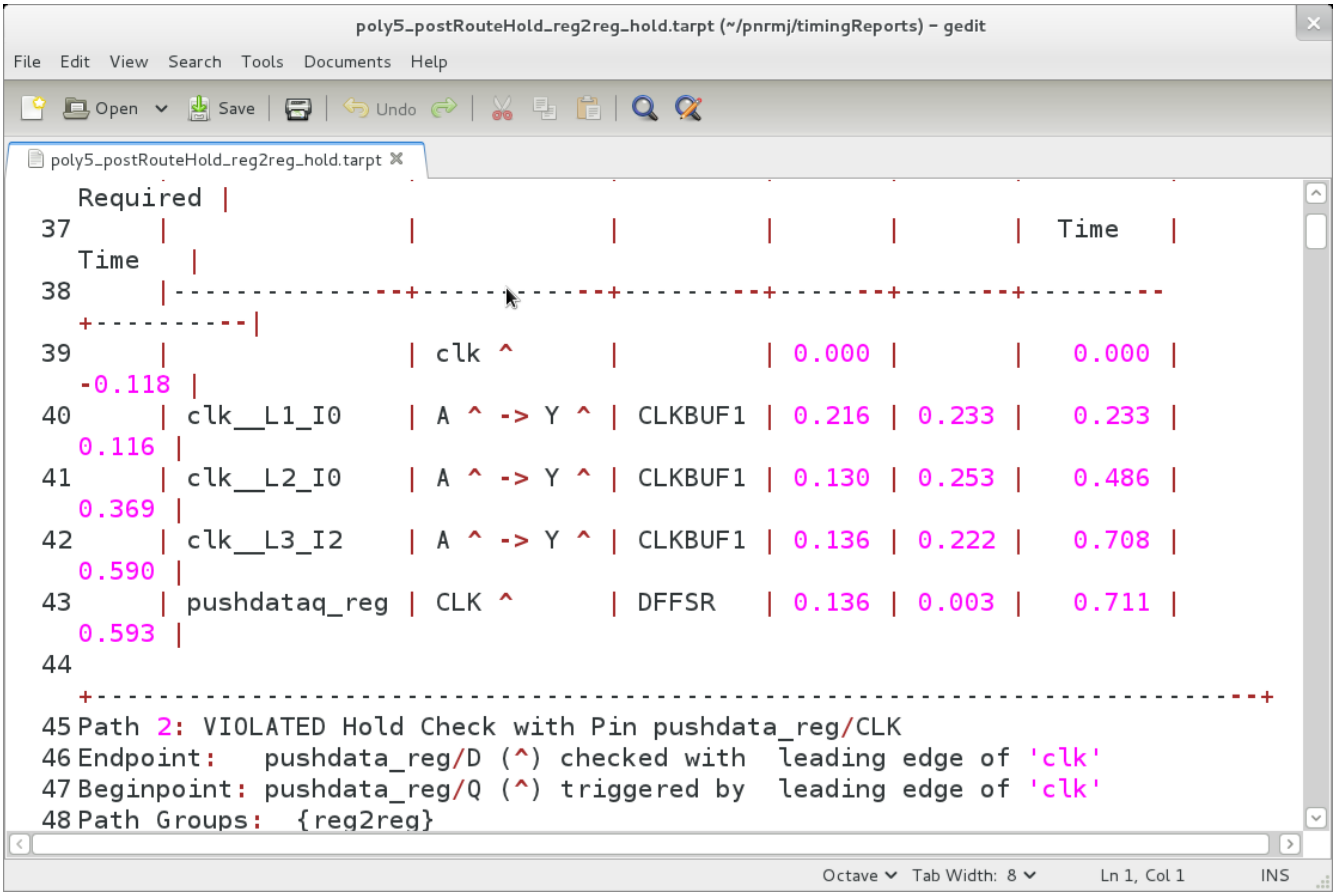


Click OK, this will generate a hold time violation report. In my example, I looked on the terminal and there are 29 race problems. These can be fixed by hand by adding more metal...

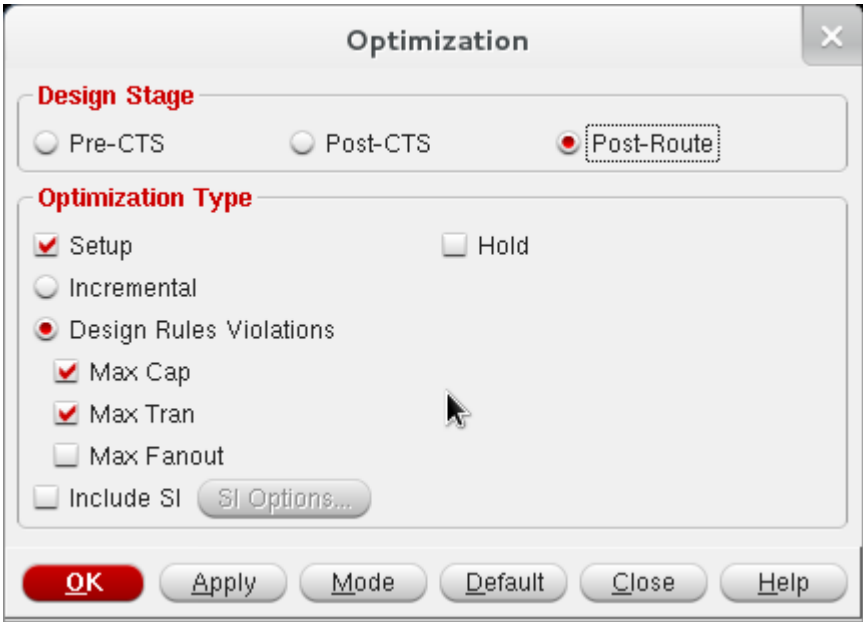


Only 2 of them are between flip flops, and these must be fixed. The others are due to the timing constraint given the block. They might not race when the other block is connected. (It will have some delay).

You will find these timing paths in a file reg2regHold. I have included an example. Submit your hold paths also...



Next, clock on optimize then optimize design... Clock on Post-Route, and then make sure setup is clicked.



Then click OK. This may take a while to run... (15 minutes or more) It will redo the routing and try and fix the nets with setup problems.

Create another timing report as above for long paths. (setup)

It may not be better. The paths were fairly well optimized in the beginning...

Report how many setup problems you have after optimization on Canvas.