North South University

Department of Electrical & Computer Engineering

LAB REPORT

Computer Organization and Architecture Lab

Experiment Number: **Lab - #03**

Experiment Name: **Design of a 4 bit Universal Shift Register**

Experiment Date: 10-11-2021

Report Submission Date: 16-11-2021

Section: **02**

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Remarks:	

Objectives

Here, a 4 bit universal shift register is being used, which is part of an arithmetic logic unit. The ALU here performs these microoperations: shift left, shift right, parallel load, and displaying same output as before (no change).

In the experiment, it is demonstrated that via selection bits into multiplexers, the ALU determines which of the four microoperations should take place, i.e. more than one microoperation out of the four listed cannot take place simultaneously.

List of Equipments

1. Trainer board
2. Power Supply
3. Four 4X1 MUX (Two 74153 ICs)
4. Four D Flip Flops (Two 7474 ICs)
5. Wires for connection

Theory

The 4 D FFs are connected to the same clock, so it is a synchronous circuit. If the clock is a positive edge clock, then the output can only be found at the rising edge. In the D FF, whatever is the input is the output.

There are a total of 4 MUXs, with 2 select bits, and 4 input bits. Each of these MUXs has a corresponding FF.

S=00. The 0^{th} input bit on each MUX is the output of MUX, and the 0^{th} input bit is connected to the output of the corresponding FF. Hence, when the output of MUX enters the input of FF, the previous output bit of FF is again its 'own input', so 'no change' is observed.

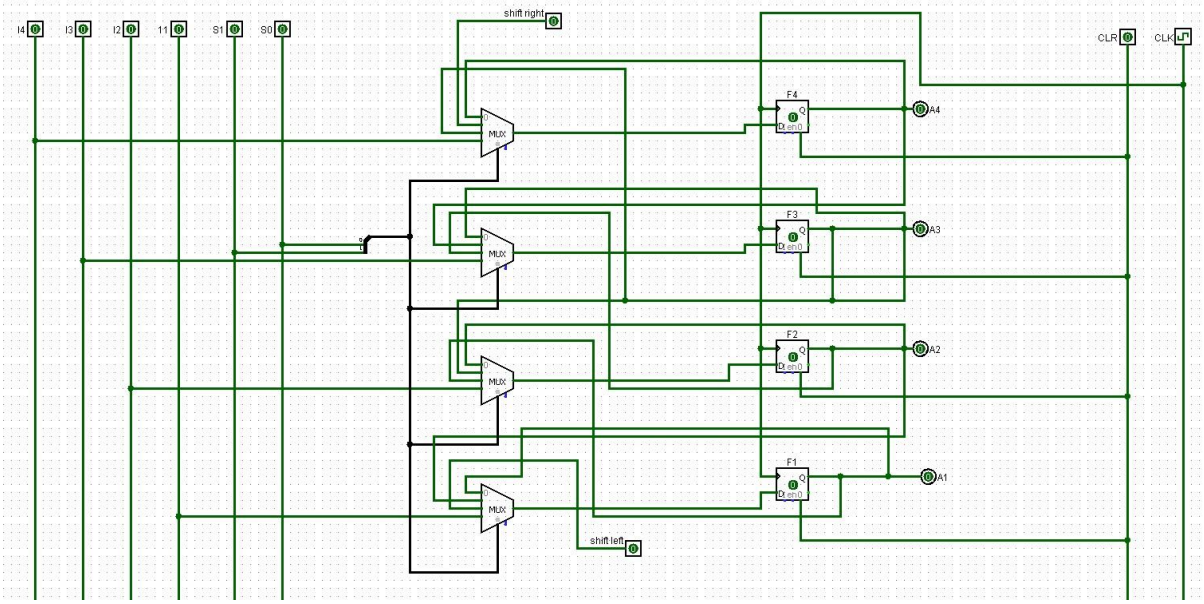
S=01. The 1^{st} input bit on each MUX is the output of MUX. MUX_4's 1^{st} input bit is shift right input, and the next FF's output is connected to the previous MUX's 1^{st} input bit for MUX_3 till MUX_1, e.g. A_4 from FF_4 is connected to the 1^{st} input bit of MUX_3. Hence, the outputs $A_4A_3A_2A_1$ are shift right outputs, since the values are shifted rightwards.

S=10. The 2^{nd} input bit on each MUX is the output of MUX. MUX_1's 2^{nd} input bit is shift left input, and the previous FF's output is connected to the next MUX's 2^{nd} input bit for MUX_2 till

MUX_4, e.g. A_1 from FF_1 is connected to the 2^{nd} input bit of MUX_2. Hence, the outputs $A_4A_3A_2A_1$ are shift left outputs, since the values are shifted leftwards.

S=11. The 3^{rd} input bit on each MUX is the output of MUX. This input bit is connected to parallel loads. Hence, the parallel load values are the outputs of the FFs.

Circuit Diagram



Function Table

S_1	S_0	Operation	I_4	I_3	I_2	I_1	A_4	A_3	A_2	A_1
0	0	No Change	0	1	1	0	0	0	0	0
0	1	SHR	1	1	0	0	1	0	0	0
1	0	SHL	1	1	0	0	0	0	0	1
1	1	Parallel Load	1	1	0	0	1	1	0	0

Discussion

At first, each equipment is discussed in details. The trainer board has the following features:

1. An on/off button
2. Vcc comes from 5V, and ground from GND
3. 16 input switches
4. The outputs are displayed by connecting the output pins of ICs to the output LED pins via wires.
5. A breadboard is located in the middle. The horizontal red line is the plus connection or Vcc connection. The horizontal blue line is the minus connection or ground. A, B, C, D, and E are vertically connected. There are 16 pins or rails for them.

6. ICs are connected to the breadboard.
7. Pulse switches – A' and B' give a negative phase, and A and B give a positive phase.

Secondly, ICs are discussed. Here are the pin numbers for IC 74F153, and a short description of each pin in the dual MUX:

1. Pins 1 and 15 are enable keys for Mux A and Mux B respectively.
2. The 2nd pin is S_1, and the 14th pin is S_0. S_1 is the most significant select bit (MSB), and S_0 is the least significant bit (LSB).
3. MUX A input pins (from pin no. 3 till 6) are as follows: 3rd pin is for 4th input bit or I_{3a} … 6th pin is for 1st input or I_{0a}. The output is 7th pin.
4. The 8th pin is GND, or 0 volts.
5. The 16th pin is Vcc, or 5V.
6. Mux B input pins (from pin no. 13 till 10) are as follows: 13th pin is for 4th input bit or I_{3b} … 10th pin is for 1st input or I_{0b}. The output is 9th pin.

IC 7474 has the following pins:

1. D FF1 – 1st pin is clear NOT, 2nd pin is input, 3rd pin is clock, 4th pin is preset NOT, 5th pin is output, and 6th pin is output NOT.
2. 7th pin is GND, and 14th pin is V_{cc}.
3. D FF2 – 13th pin is clear NOT, 12th pin is input, 11th pin is clock, 10th pin is preset NOT, 9th pin is output, 8th pin is output NOT.

Before the experiment even starts, the equipment must be checked to see if there are any troubles. The trainer board needs to be checked to see if 5V and ground are working properly or not. The power on trainer board is turned on. Next, the 5V supply is connected to breadboard first. A separate wire from here is then going into an output LED pin. LED turns on.

The GND is not working in the video, so an alternative has been used. The wire is connected to the 0-15V, and the knob is turned to 0V.

The input switches are checked to see if they are properly working or not. The input switch pin is connected to an output pin via a wire. The input switch is turned on to see if the output LED turns on. If the same input switch shows output for all other output pins except a particular output pin, that output pin is not properly working. Hence, this technique can be used to check whether input and output pins are working properly at the same time.

After checking all the equipment, the equipment is now being set up for the experiment. The Vcc is connected to the positive pin in the breadboard, and the 0-15V is connected to the minus pin.

The ICs are placed on the breadboard. The GND is taken from 0-15V of each IC, and V_{CC} is taken from the 5V. The preset deletes previous value stored in FF and saves a fixed 1. So, PRE' is connected to V_{cc}, so that the value in FF is not preset (because 1'=0, so PRE' is 0 throughout the experiment). The CLR', however, is connected to the turned on input switch pin on trainer board. This ensures:

1. 1'=0, so CLR' is 0 throughout most of the experiment, preventing deleting of values.
2. If ever needed, the CLR' can be turned on by turning off the switch.

At A' on trainer board, the clock starts at the rising edge, and releasing the button gives falling edge. In this circuit, the FFs are connected to A'. (In A, the clock starts at the falling edge, and releasing the button gives rising edge.) The inputs of MUXs are taken from the input switch pins on trainer board, and outputs of FFs are connected to output LED pins of trainer board.

Different input switch pins are turned on and off according to the function table, and the values are recorded onto the table.