North South University

Department of Electrical & Computer Engineering

LAB REPORT

Computer Organization and Architecture Lab

Experiment Number: **Lab - #04**

Experiment Name: **Design of a 4-bit Binary Up-Down counter**

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Section: **02**

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Remarks:	

Objectives

A counter is a type of register that goes through a specific sequence of states. Here, a 4 bit binary up-down counter is being built, in a synchronous circuit. If it is up, the 4 bit output increases by 1, and vice versa when down.

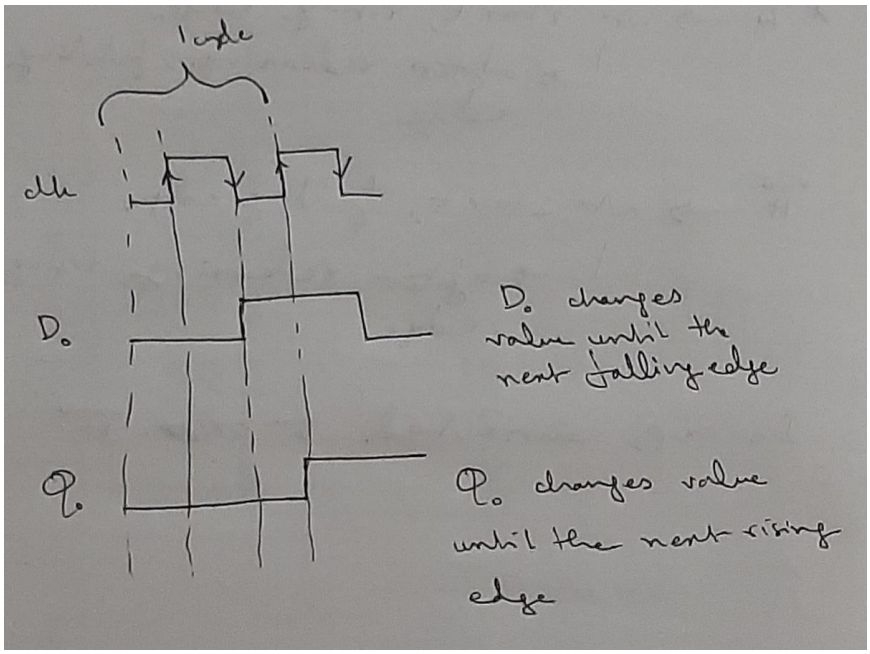
Counters generate time signals, which determines which operation takes place when in a computer.

List of Equipments

1. Trainer board
2. IC 7404, IC 7408, IC 7432, IC 7486, IC 7474
3. Wires for connection
4. Power supply

Theory

The states are 0 to 15. The FF changes output value in one clock cycle through the process shown in the diagram below.



The least significant bit is always complemented on every state.

The next significant bit only gets complemented if the previous bit becomes from 1 to 0.

In order to introduce complements, the counter circuit must have a flip flop that can complement, which is either T FF or JK FF. In T FF, an input of 0 causes no change. An input of 1 complements the output. T FF acts as a toggle switch. The following table shows how the T FF complements.

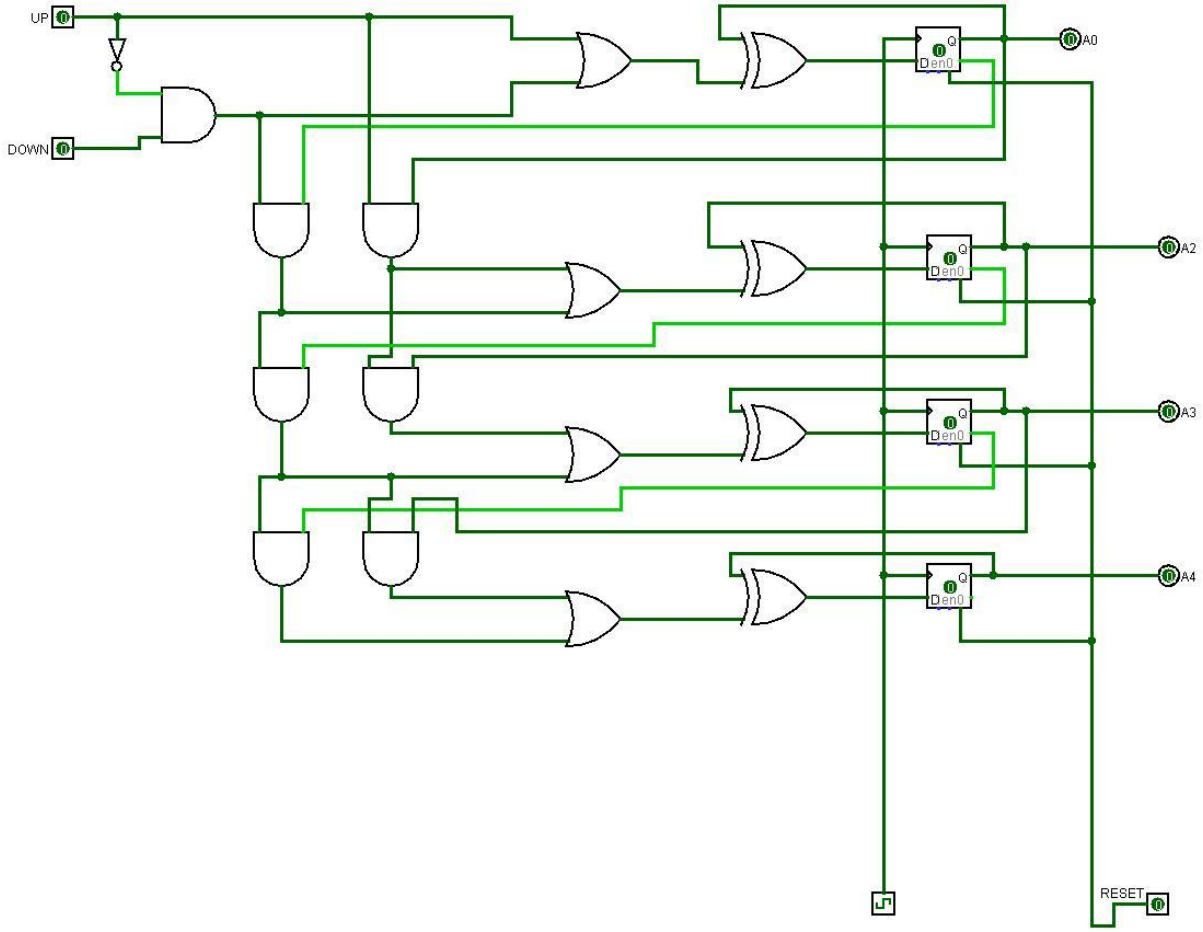
T	**Q(t+1)**
0	Q(t)
1	Q'(t)

For up counting, state change happens from 0 to 1. Q of previous FF is connected to the next FF. For down counting, the state transition takes place from 1 to 0. The Q' of previous FF is connected to next FF. This connection is summarized by the following equation:

$$Q(t+1) = T \oplus Q = TQ' + T'Q$$

Up Input	**Down Input**	**What Happens?**
0	0	No Change
0	1	Down Counter
1	0	Up Counter
1	1	Up Counter

Circuit Diagram



Truth Table

Clock Pulse	A	B	C	D
P_0	0	0	0	0
P_1	0	0	0	1
P_2	0	0	1	0
P_3	0	0	1	1
P_4	0	1	0	0
P_5	0	1	0	1
P_6	0	1	1	0
P_7	0	1	1	1
P_8	1	0	0	0
P_9	1	0	0	1
P_{10}	1	0	1	0
P_{11}	1	0	1	1
P_{12}	1	1	0	0
P_{13}	1	1	0	1
P_{14}	1	1	1	0
P_{15}	1	1	1	1

Discussion

Before the experiment even starts, the equipment must be checked to see if there are any troubles. The trainer board needs to be checked to see if 5V and ground are working properly or not. The power on trainer board is turned on. Next, the 5V supply is connected to breadboard first. A separate wire from here is then going into an output LED pin. LED turns on.

The GND is not working in the video, so an alternative has been used. The wire is connected to the 0-15V, and the knob is turned to 0V.

The input switches are checked to see if they are properly working or not. The input switch pin is connected to an output pin via a wire. The input switch is turned on to see if the output LED turns on. If the same input switch shows output for all other output pins except a particular output pin, that output pin is not properly working. Hence, this technique can be used to check whether input and output pins are working properly at the same time.

After checking all the equipment, the equipment is now being set up for the experiment. The V_{CC} is connected to the positive pin in the breadboard, and the 0-15V is connected to the minus pin.

The ICs are placed on the breadboard. The GND is taken from 0-15V of each IC, and V_{CC} is taken from the 5V.

The T FF is built using D FF. The input of D FF comes from the XOR output of Q and input to be given to FF. Each IC has 2 D FFs, so a total of 2 D FF ICs are used. These two ICs' clock connections need to be short, because they are all connected to the same synchronous circuit.

The preset deletes previous value stored in FF and saves a fixed 1. So, PRE' is connected to V_{CC}, so that the value in FF is not preset (because 1'=0, so PRE' is 0 throughout the experiment). The CLR', however, is connected to the turned on input switch pin on trainer board. This ensures:

1. 1'=0, so CLR' is 0 throughout most of the experiment, preventing deleting of values.
2. If ever needed, the CLR' can be turned on by turning off the switch.

At A' on trainer board, the clock starts at the rising edge, and releasing the button gives falling edge. In this circuit, the FFs are connected to A'. (In A, the clock starts at the falling edge, and releasing the button gives rising edge.) The inputs of up and down are taken from the input switch pins on trainer board, and outputs of FFs are connected to output LED pins of trainer board.

The reason why Up is connected to a NOT gate is so that Up and Down are never the 'same value' (or rather, Up NOT and Down are never the same value).

Different input switch pins (of Up and Down) are turned on and off as well as the A' switch, according to the truth table, and the values are recorded onto the table.