North South University

Department of Electrical & Computer Engineering

LAB REPORT

Computer Organization and Architecture Lab

Experiment Number: **Lab - #05**

Experiment Name: **Design of a Register File**

Experiment Date: 24-11-2021

Report Submission Date: 30-11-2021

Section: **02**

Student Name: **Asfaria Islam Chowdhury**	Score
Student ID: **1931741642**	
Remarks:	

Objectives

A register is a group of high speed storage cells inside CPU, where the storage is done with the help of flip-flops. Here, the experiment's goal is to build a 16 bit ISA using the following instruction formats:

R-type:

op (4 bit)	rs (4 bit)	rt (4 bit)	rd (4 bit)

I-type:

op (4 bit)	rs (4 bit)	rt (4 bit)	immediate (4 bit)

J-type:

op (4 bit)	target (12 bit)

Data can both be read and written to the registers.
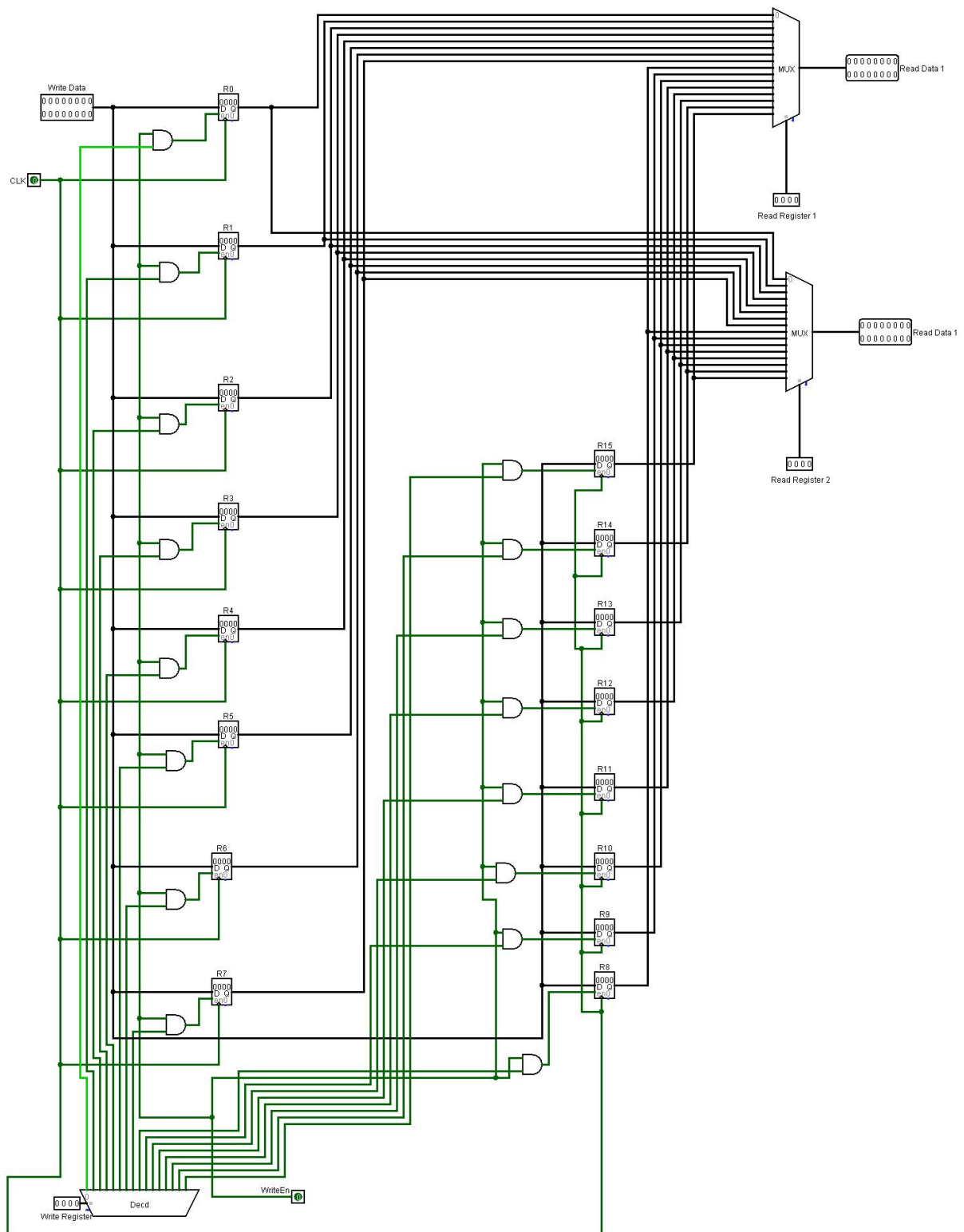
List of Equipment

Logisim

Theory

There is a common clock for all the 16 D flip flops because this is a synchronous circuit.

A common 16 bit write data input button is connected to all registers (made of D FFs). The enable key of register takes connection from a (4X16 decoder AND a write-enable button), the result of which if 1 allows data to be written to register (if both the input bits of decoder produces a particular minterm output 1 connected to corresponding register AND if write-enable is 1 – however, for other registers the minterm output of decoder is 0, so 0 AND 1 = 0, so data is only written to one register at a time). The input bits on the decoder are also called write register, and the enable key on the register is called load of the register, where it is observed that only load = 1 allows data to be written for only a single register while other registers have load = 0. (The write-enable is also common for all registers.)

All the outputs of the registers are connected to two 16X1 multiplexers. Each multiplexer has 4 bit selection bits, which are also known as Read Registers. The outputs of the multiplexers show the 16-bit values read from two different specific registers – the selection bits determine which registers to read from.

Logisim Diagram

Sub-circuit Diagram