North South University

Department of Electrical & Computer Engineering

LAB REPORT

Computer Organization and Architecture Lab

Experiment Number: **Lab - #02**

Experiment Name: **Design of a 2-bit Arithmetic unit**

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Section: **02**

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Remarks:	

Objectives

Here, a two bit arithmetic unit is being used, which is part of an arithmetic logic unit. The ALU here performs these microoperations: addition, addition with a carry, subtraction, and subtraction with a borrow on the two bit inputs $A=A_1A_0$ and $B=B_1B_0$; and transfer, increment and decrement on $A=A_1A_0$.

The description of each one of these microoperations is as follows:

1. Addition: A and B are added via two full adders, with a carry out.
2. Addition with a carry: Same as addition, but with a carry in of 1 into a full adder. The output is the summation of A+B+1, and C_{out} is displayed.
3. Subtraction: B is first 1's complemented, and then C_{in} is passed into FA as 1, hence making B into 2's complement. B is then added to A.
4. Subtraction with a borrow: B is only 1's complemented, i.e. $C_{in}=0$. Then, B is added to A.
5. Transfer: Whatever is the input of A is the output.
6. Increment: Increase A by 1.
7. Decrement: Decrease A by 1.

In the experiment, it is demonstrated that via selection bits into multiplexers and C_{in} in FA, the ALU determines which of the seven microoperations should take place, i.e. more than one microoperation out of the seven listed cannot take place simultaneously.

List of Equipments

1. Trainer board
2. IC 7404 - NOT, IC 7483 – 4-bit full adder, IC 74F153 – 4x1 Dual MUX
3. Wires for connection

Theory

There are two multiplexers in the dual MUX IC. In the *Circuit Diagram* section, they are labelled as MUX_0 and MUX_1, for the 0^{th} and 1^{st} bits of A and B respectively.

Each MUX has the following input pins (input pin no's as per Logisim screenshot in the *Circuit Diagram* section):

1. 0^{th} pin – B
2. 1^{st} pin – B's 1 complement (via B NOT). This step is useful for both subtraction and subtraction with borrow.
3. 2^{nd} pin – connected to 0

4. 3^{rd} pin – connected to 1

There are two selection pins, S_0 and S_1. The table below summarizes how S works.

S_1	S_0	Output
0	0	B
0	1	B NOT (1’s complement)
1	0	0
1	1	1

Addition

When S=00, B is output of MUX. Both B and A are connected to FA, with $C_{in}=0$. A_0 and B_0 are added in FA_0, and C_{out} of FA_0 is the C_{in} of FA_1. Here, C_{out} of FA_0 is added to A_1 and B_1, and the final carry out of the addition is displayed, along with $D_0=A_0+B_0$ and $D_1=A_1+B_1+(C_{out}$ of $FA_0)$.

Addition with Carry

S=00, output of MUX = B. $C_{in}=1$ for FA_0. The 0^{th} output, $D_0=A_0+B_0+1$, is displayed. The C_{out} of FA_0 is connected to C_{in} of FA_1. The 1^{st} output, $D_1=A_1+B_1+(C_{out}$ of $FA_0)$, is displayed, along with C_{out} of the entire addition.

Subtraction

S=01, output of MUX is 1’s complement of B. $C_{in}=1$ for FA_0. In FA_0, the output D_0 is $A_0+(B_0'+1)$, where B_0' is 1’s complement, and $(B_0'+1)$ is 2’s complement. The C_{out} of FA_0 goes to FA_1 as C_{in}, and the output is $D_1=A_1+B_1'+(C_{out}$ of $FA_0)$. The final carry out is also displayed.

Subtraction with Borrow

S=01, output of MUX is 1’s complement of B. $C_{in}=0$ for FA_0. In FA_0, the output D_0 is A_0+B_0', where B_0' is 1’s complement. The C_{out} of FA_0 goes to FA_1 as C_{in}, and the output is $D_1=A_1+B_1'+(C_{out}$ of $FA_0)$. The final carry out is also displayed.

The reason why $C_{in}=0$ is that B borrows from A, rather than taking an external 1. The following diagram explains this, along with comparing with decimal subtraction with borrow:

Decimal

$$\begin{array}{r} {}^{0}\cancel{1}0 \\ -\ 1 \\ \hline 09 \end{array}$$

Binary

* $A = 1010$
* $B = 0001$
* 1's complement of $B = B'$

$= 1110$

$$\begin{array}{r} 1010 \\ 1110 \\ \hline \underset{C_{out}}{1}\,\underbrace{1000}_{\text{8 in decimal}} \end{array}$$

We see that in binary subtraction with borrow, the result is 1 less than the decimal subtraction with borrow.

<u>Transfer A</u>

S=10, the output of MUX is 0. 0 is added with A to output A.

S=11, the output of MUX is 1. C_{in}=1. These two 1's cancel out each other (as shown in the diagram below), so the output of FAs is A_1A_0.

~~A=11~~

$A = A_1A_0 = 11$

MUX output, $Y = Y_1Y_0 = 11$ [because S = 11]

$$\begin{array}{r} 11 \\ +\ 11 \\ \hline 1\underbrace{10} \end{array}$$

C_{out} ← 1; 10 → A is decreased by 1

Because $C_{in} = 1$ during transfer when $S = 11$, A is again incremented by 1. Hence, A = 11, which is the same as the original value of A.

<u>Increment A</u>

S=10, the output of MUX is 0. C_{in} is 1. A+0+1=A+1, so A is incremented by 1.

<u>Decrement A</u>

S=11, output of MUX is 1. This is added to A and C_{in}, which is 0. The following diagram explains what happens:

$A = A_1 A_0 = 11$

MUX output, $Y = Y_1 Y_0 = 11$ [because $S = 11$]

$$
\begin{array}{r}
11 \\
+\ 11 \\
\hline
1\,10
\end{array}
$$

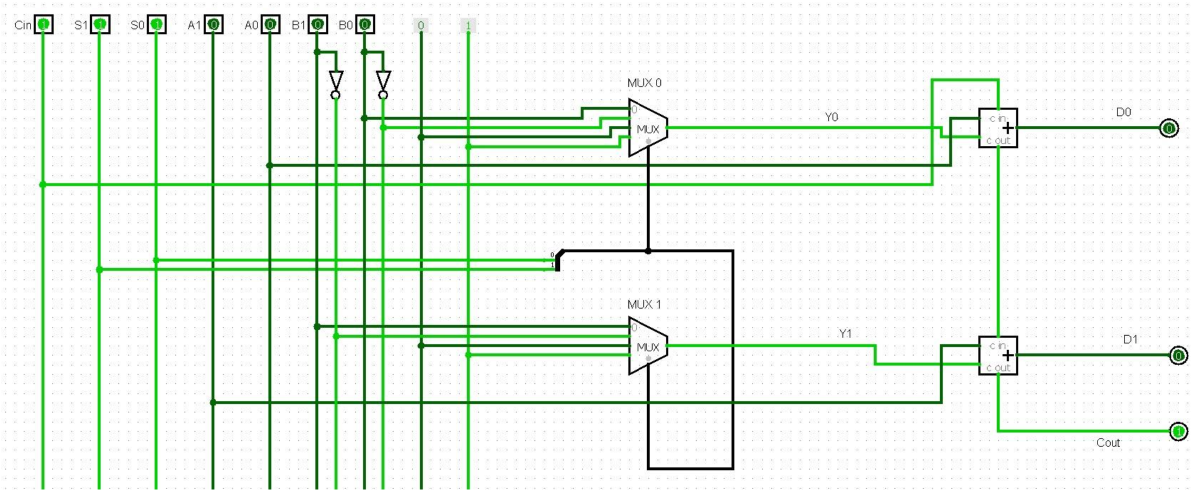
$1 \rightarrow C_{out}$

$10 \rightarrow$ A is decreased by 1

C_{out} is a signed bit. If C_{out}=1, the output D is positive. If C_{out}=0, the output D is negative.

Circuit Diagram

Here, the simulation is for S=11, C_{in}=1, A=00, and B=00.



Function Table

S_1	S_0	C_{in}	A_1	A_0	B_1	B_0	D_1	D_0	C_{out}	Microoperation
0	0	0	0	0	0	1	0	1	0	Add
0	0	1	0	1	0	1	1	1	0	Add with carry
0	1	0	1	0	0	0	0	1	1	Subtract with borrow
0	1	1	1	1	1	1	0	0	1	Subtract
1	0	0	1	1	0	1	1	1	0	Transfer A
1	0	1	0	0	1	0	0	1	0	Increment A
1	1	0	1	1	0	0	1	0	1	Decrement A
1	1	1	0	0	0	0	0	0	1	Transfer A

Discussion

At first, each equipment is discussed in details. The trainer board has the following features:

1. An on/off button
2. Vcc comes from 5V, and ground from GND
3. 16 input switches
4. The outputs are displayed by connecting the output pins of ICs to the output LED pins via wires.
5. A breadboard is located in the middle. The horizontal red line is the plus connection or Vcc connection. The horizontal blue line is the minus connection or ground. A, B, C, D, and E are vertically connected. There are 16 pins or rails for them.
6. ICs are connected to the breadboard.
7. Pulse switches – A’ and B’ give a negative phase, and A and B give a positive phase.

Secondly, ICs are discussed. Here are the pin numbers for IC 74F153, and a short description of each pin in the dual MUX:

1. Pins 1 and 15 are enable keys for Mux A and Mux B respectively.
2. The 2nd pin is S_1, and the 14th pin is S_0. S_1 is the most significant select bit (MSB), and S_0 is the least significant bit (LSB).
3. MUX A input pins (from pin no. 3 till 6) are as follows: 3rd pin is for 4th input bit or I_{3a} … 6th pin is for 1st input or I_{0a}. The output is 7th pin.
4. The 8th pin is GND, or 0 volts.
5. The 16th pin is Vcc, or 5V.
6. Mux B input pins (from pin no. 13 till 10) are as follows: 13th pin is for 4th input bit or I_{3b} … 10th pin is for 1st input or I_{0b}. The output is 9th pin.

The dual MUX already allows for both MUXs to have same select bit. However, if two separate MUXs were used, we would short the select bits.

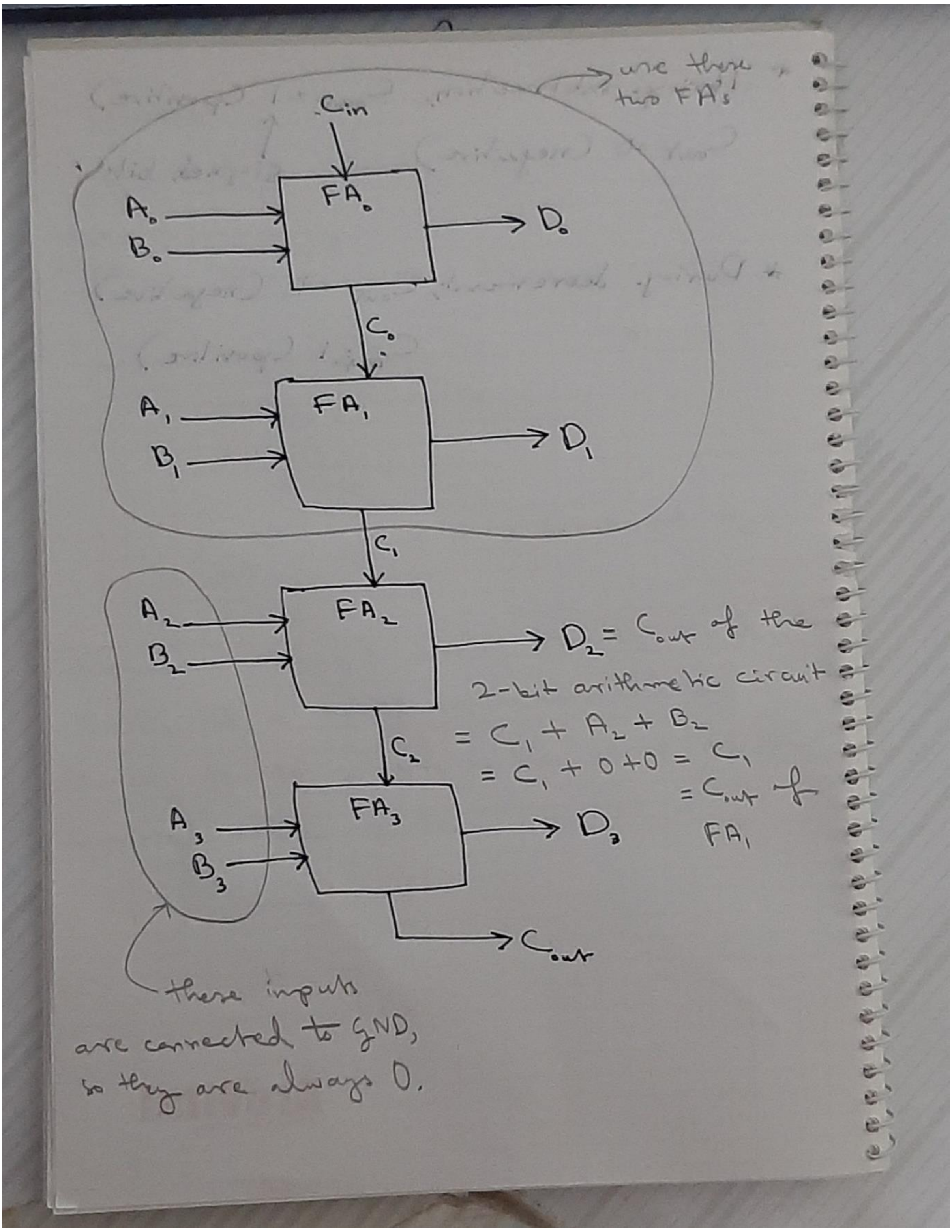
IC 7404, hex inverters, have a total of 6 NOT gates. Vcc is in 14^{th} pin, and GND at 7^{th}. The input-output pairs are as follows:

1. Input – 13^{th} pin, Output – 12^{th} pin
2. Input – 11^{th} pin, Output – 10^{th} pin
3. Input – 9^{th} pin, Output – 8^{th} pin
4. Input – 1^{st} pin, Output – 2^{nd} pin
5. Input – 3^{rd} pin, Output – 4^{th} pin
6. Input – 5^{th} pin, Output – 6^{th} pin

IC74283 is a 4-bit full adder. There are 4 FAs here. The pins are described as follows:

1. FA_1: pin 1 – summation of A_1 and B_1 or $\sum_1$, pin 2 - B_1, pin 3 - A_1
2. FA_0: pin 4 –$\sum_0$, pin 5 – A_0, pin 6 – B_0
3. FA_2: pin 15 – B_2, pin 14 – A_2, pin 13 – $\sum_2$
4. FA_3: pin 12 – A_3, pin 11 – B_3, pin 10 – $\sum_3$
5. Pin 16 – Vcc, pin 8 – GND
6. Pin 7 – C_{in}, pin 9 - C_{out}

The following block diagram shows how the 4 FAs connect with each other and work:



Before the experiment even starts, the equipment must be checked to see if there are any troubles. The trainer board needs to be checked to see if 5V and ground are working properly or not. The power on trainer board is turned on. Next, the 5V supply is connected to breadboard first. A separate wire from here is then going into an output LED pin. LED turns on.

The GND is not working in the video, so an alternative has been used. The wire is connected to the 0-15V, and the knob is turned to 0V.

The input switches are checked to see if they are properly working or not. The input switch pin is connected to an output pin via a wire. The input switch is turned on to see if the output LED turns on. If the same input switch shows output for all other output pins except a particular output pin, that output pin is not properly working. Hence, this technique can be used to check whether input and output pins are working properly at the same time.

After checking all the equipment, the equipment is now being set up for the experiment. The Vcc is connected to the positive pin in the breadboard, and the 0-15V is connected to the minus pin.

The ICs are placed on the breadboard. The Vccs on the IC pins are connected to 5V, and GND to the 0-15V (pin no's according to equipment description). Then, the input switches and other connections are as follows:

1. C_{in} is the 1st input switch pin on the trainer board, connected to the 7th pin to the FA IC.
2. S_1 and S_0 are 2nd and 3rd input switch pins on the trainer board, connected to 2nd and 14th pins of MUX IC respectively.
3. A_1 and A_0 are 4th and 5th input switch pins on the trainer board are connected to 3rd and 5th pins of FA IC respectively.
4. B_1 and B_0 are 6th and 7th input switch pins on the trainer board are connected to 10th and 6th pins of MUX IC respectively. From the MUX IC, these 'same' inputs are connected to 3rd and 1st pins of NOT IC (rather than taking connection from input switch pins 6 and 7 to NOT IC, because they have already been used for the MUX IC). The 4th and 2nd output pins are connected to 11th and 5th pins of MUX IC.
5. The GND is connected to the following pins (for constant 0):
   a. 12th and 4th pins on MUX IC
   b. Pins 11, 12, 14, 15 on FA IC
6. The 5V is connected to these pins (for constant 1): 13th and 3rd pins on MUX IC.
7. 9th and 7th pins are Y_0 and Y_1 respectively, the output pins on MUX IC. These are connected to the FA IC via 2nd and 6th pins of FA IC.
8. The outputs D_0, D_1, and C_{out} are from 4th, 1st, and 13th pins respectively in the FA IC, which are connected each to output LED pins 1, 2, 3.

Different input switch pins are turned on and off according to the function table, and the values are recorded onto the table.

Whenever C_{out}=1, the output LED is on in the 3rd pin, and the output D is positive because the signed bit indicates a positive number. Whenever C_{out}=0, the output LED is off in the 3rd pin, and the output D is negative because the signed bit indicates a negative number.

An example would be the simulation shown in the *Circuit Diagram* section, for S=11 (turned on 2nd and 3rd input switch pins), C_{in}=1 (turned on 1st input switch pin), A=00 (turned off 4th and 5th input switch pins), and B=00 (turned off 6th and 7th input switch pins). D_0=0 (output LED 1 is off), D_1=0 (output LED 2 is off), and C_{out}=1 (output LED 3 is on).The signed bit indicates that D=00 is a positive number.