Lab Manual

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Experiment No: 04
Experiment Name: Design of a 4-bit Binary Up-Down counter.

Introduction:

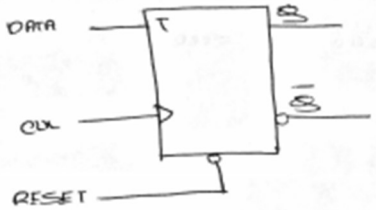
A register that goes through a predetermined sequence of states upon the application of input pulses, is called a counter. The input pulses may be clock pulses or may originate from an external source. They may occur at uniform intervals of time or at random. They are used for generating time signals to control the sequence of operations in digital computers.

A counter that follows the binary number sequence is called a binary counter. A 4-bit binary counter is a register of 4 flip-flops and associated gates that follows a sequence of states according to the binary count of 4 bits, from 0 to 15. We assume that the LSB is always complemented on every state. The sequence works on the fact that the next significant bit will be complemented only when a previous bit makes a transition from 1 to 0. For example, in case of transition from binary 0011 to 0100(4 to 5), 3^{rd} bit does transition from 0 to 1. So, the 4^{th} bit isn't complemented.

A counter circuit will usually employ flip-flops with complimenting capabilities. T and JK flip flops have this capability. Here we are going to use T flip-flops, which are built using D flip-flops. The T flip-flops act as a toggle switch. When the input is 0, there is no change in the output of the T flip-flops. It retains the previous value. But when the input is 1, the output is complemented. A XOR gate combined with a D flip-flop can be used to create a T flip-flop.

As we are going to design a 4 bit binary up down counter which is synchronous, so all of the flip-flops will have a common clock pulse. For counting up, the next flip-flop will change state when there is a transition from 0 to 1. Then we use the Q output and connect it to the next flip-flop. For counting down, the next flip-flop will change state when there is a transition from 1 to 0. Then we use the Q' output and connect it to the next flip-flop.

Diagram of a T-Type Flip-Flop:



(Fig-1)

Characteristic Equation:

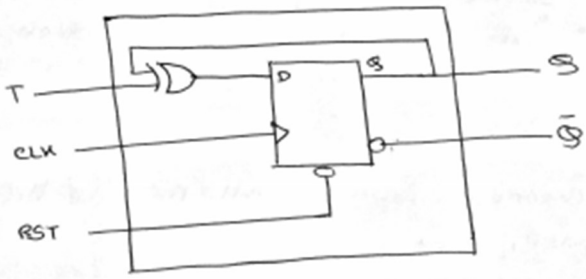
$$Q(t+1) = T \oplus Q = TQ' + T'Q \quad \text{(EQ-1)}.$$

Characteristic Table:

T	Q(t+1)
0	Q(t)
1	$\bar{Q}(t)$

(Table-1)

Creating a T-Flip Flop Using a D-Flip Flop:



(Fig-2).

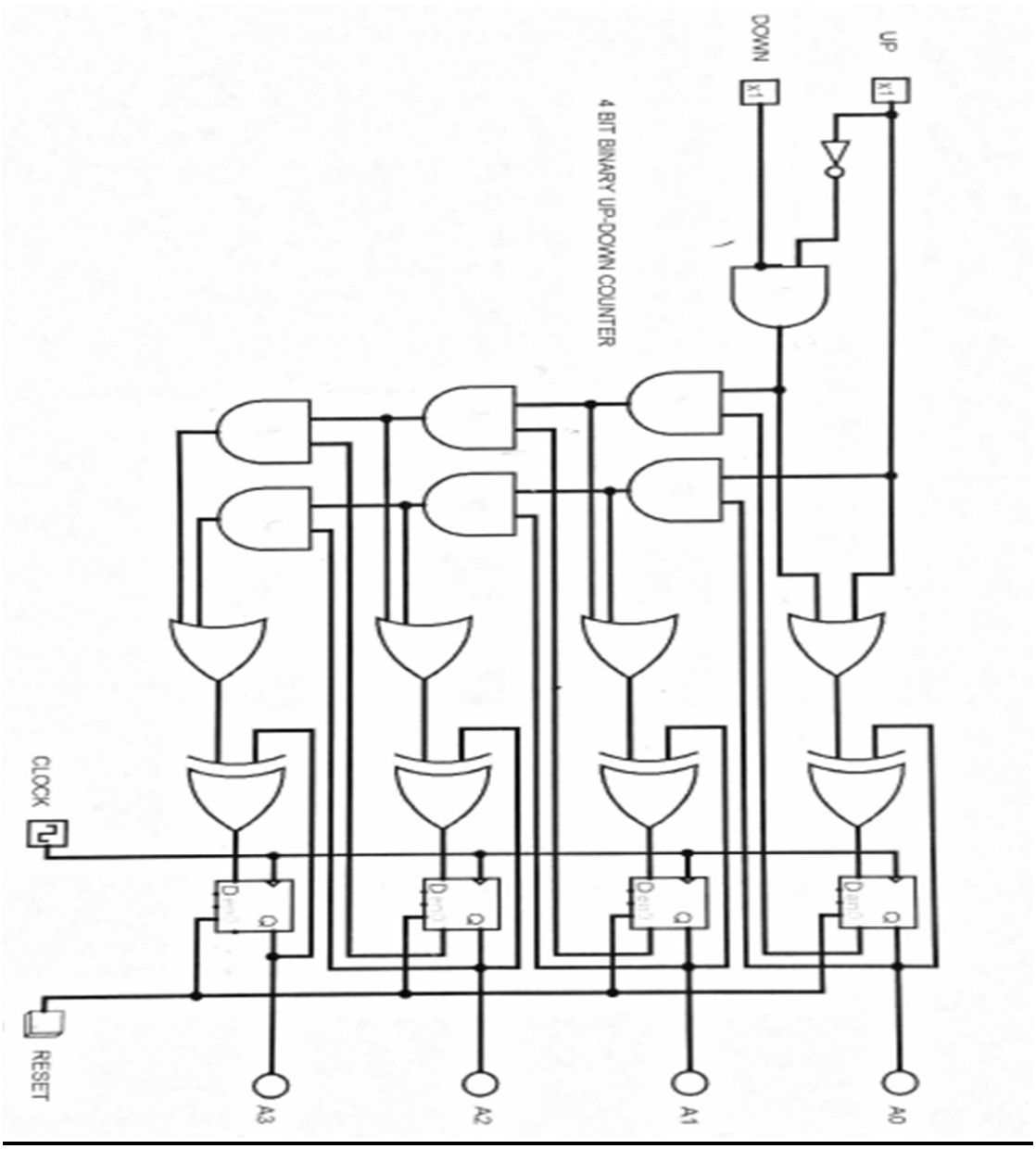
Equipments:

- Trainer board
- IC 7404,7408,7432,7486, 7474
- Wires for connection.
- Power supply

Truth Table:

Clock pulse	A	B	C	D
P0	0	0	0	0
P1	0	0	0	1
P2	0	0	1	0
P3	0	0	1	1
P4	0	1	0	0
P5	0	1	0	1
P6	0	1	1	0
P7	0	1	1	1
P8	1	0	0	0
P9	1	0	0	1
P10	1	0	1	0
P11	1	0	1	1
P12	1	1	0	0
P13	1	1	0	1
P14	1	1	1	0
P15	1	1	1	1

Logic Diagram:



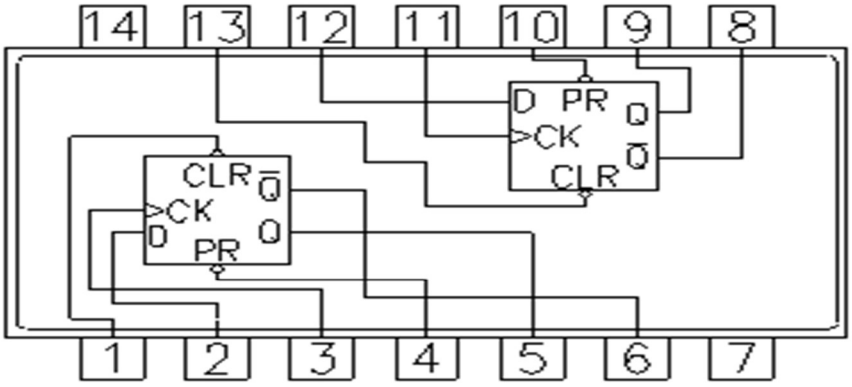
Procedure:

1) Place the ICs on the trainer board.
2) Connect V_{cc} and ground to the respective pins of IC.
3) Connect the inputs with the switches (UP, DOWN, CLOCK, RESET) and the outputs(A0, A1, A2, A3) with LEDs.
4) Apply various combinations of inputs and observe the outputs.
5) Verify the experimental outputs with the Truth Table.

Assignment:

1) Prepare the lab report.
2) Implement the circuit in Logisim. Take a screenshot and include it in your lab report.

Pin configuration of IC-7474:



7474
Dual D Flip–Flop
with Preset and Clear