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| nsu-logo  **North South University**  Department of Electrical & Computer Engineering    **LAB REPORT**  **Computer Organization and Architecture Lab**  Experiment Number: **Lab -** **#02**   |  | | --- | | Experiment Name: **Design of a 2-bit Arithmetic unit** |     Experiment Date: 03-11-2021  Report Submission Date: 09-11-2021  Section: **02** | |
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| Remarks: |

**Objectives**

Here, a two bit arithmetic unit is being used, which is part of an arithmetic logic unit. The ALU here performs addition, addition with a carry, subtraction, and subtraction with a borrow on the two bit inputs A=A1A0 and B=B1B0; and transfer, increment and decrement on A=A1A0.

The description of each one of these microoperations is as follows:

1. Addition: A and B are added via two full adders, with a carry out.
2. Addition with a carry: Same as addition, but with a carry in of 1 into a full adder. The output is the summation of A+B+1, and Cout is displayed.
3. Subtraction: B is first 1’s complemented, and then Cin is passed into FA as 1, hence making B into 2’s complement. B is then added to A.
4. Subtraction with a borrow: B is only 1’s complemented, i.e. Cin=0. Then, B is added to A.
5. Transfer: Whatever is the input of A is the output.
6. Increment: Increase A by 1.
7. Decrement: Decrease A by 1.

In the experiment, it is demonstrated that via selection bits into multiplexers and Cin in FA, the ALU determines which of the seven microoperations should take place, i.e. more than one microoperation out of the seven listed cannot take place simultaneously.

**List of Equipments**

1. Trainer board
2. IC 7404 - NOT, IC 7483 – 4-bit full adder, IC 74F153 – 4x1 Dual MUX
3. Wires for connection

**Theory**

There are two multiplexers in the dual MUX IC. In the *Circuit Diagram* section, they are labelled as MUX0 and MUX1, for the 0th and 1st bits of A and B respectively.

Each MUX has the following input pins:

1. 0th pin – B
2. 1st pin – B’s 1 complement (via B NOT). This step is useful for both subtraction and subtraction with borrow.
3. 2nd pin – is connected to 0, so that A is transferred.
4. 3rd pin – is connected to 1, for both increment and decrement.

There are two selection pins, S0 and S1. The table below summarizes how S works.

|  |  |  |
| --- | --- | --- |
| **S1** | **S0** | **Output** |
| 0 | 0 | B |
| 0 | 1 | B NOT (1’s complement) |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Addition

When S=00, B is output of MUX. Both B and A are connected to FA, with Cin=0. A0 and B0 are added in FA0, and Cout of FA0 is the Cin of FA1. Here, Cout of FA0 is added to A1 and B1, and the final carry out of the addition is displayed, along with D0=A0+B0 and D1=A1+B1+(Cout of FA0).

Addition with Carry

S=00, output of MUX = B. Cin=1 for FA0. The 0th output, D0=A0+B0+1, is displayed. The Cout of FA0 is connected to Cin of FA1. The 1st output, D1=A1+B1+(Cout of FA0), is displayed, along with Cout of the entire addition.

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The following are first performed (to later connect to multiplexer):

1. A0 AND B0 , A1 AND B1
2. A0 OR B0 , A1 OR B1
3. A0 XOR B0 , A1 XOR B1
4. A0 NOT, A1 NOT

The four output lines from the 0th bit are connected as inputs for a 4x1 MUX0, and the four output lines from the 1st bit are connected as inputs for a 4x1 MUX1. The outputs of the multiplexers are labeled as F0 and F1 respectively in the Logisim simulation.

The two multiplexers must have the same 2 selection bits, S0 and S1. The values for these selection bits are provided by the ALU in order to choose which microoperation to perform. The table drawn on the next page lists down which combination of selection bits perform which microoperation.

|  |  |  |
| --- | --- | --- |
| **S0** | **S1** | **Microoperation** |
| 0 | 0 | AND |
| 0 | 1 | OR |
| 1 | 0 | XOR |
| 0 | 1 | NOT |

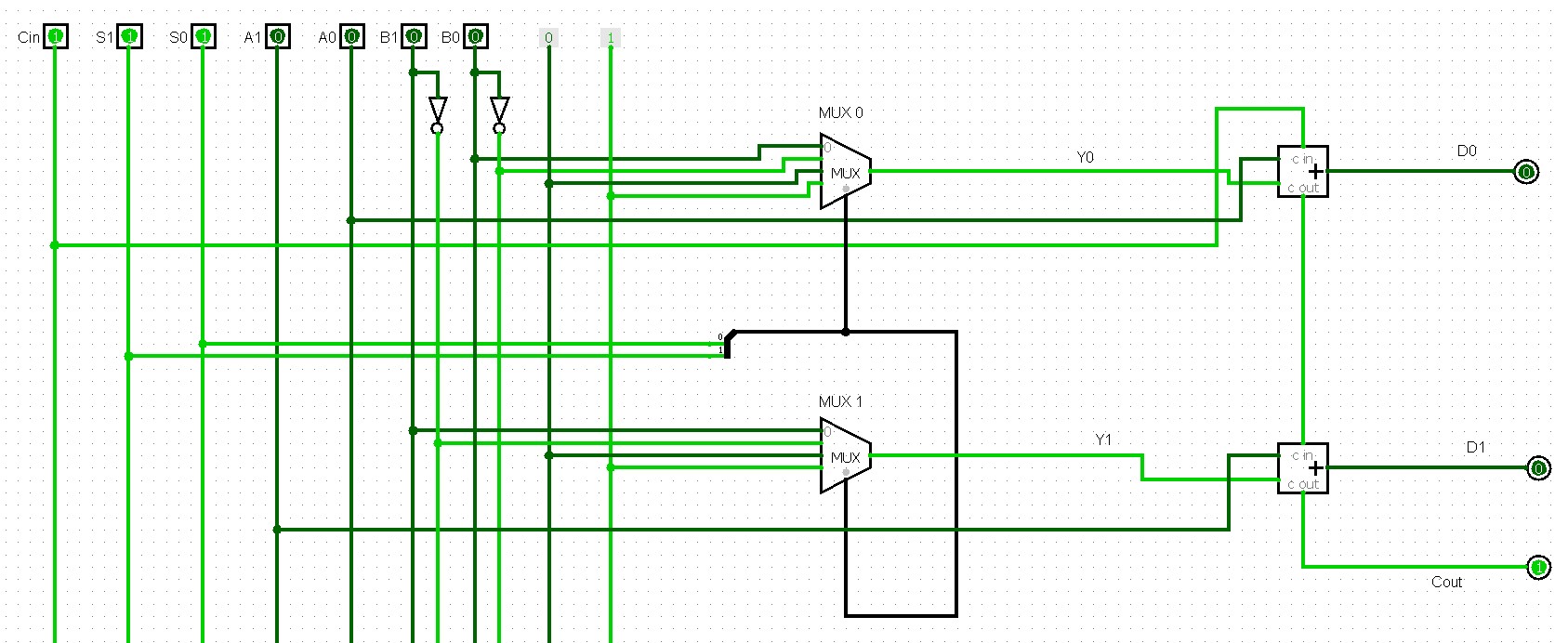
An example would be to choose to see OR microoperation when A = 11 and B = 00. First, all of the four logical functions are performed before even connecting to MUX and before even choosing the desired microoperation:

1. A0 AND B0 = 1, A1 AND B1 = 1
2. A0 OR B0 = 1, A1 OR B1 = 1
3. A0 XOR B0 = 0, A1 XOR B1 = 0
4. A0 NOT = 0, A1 NOT = 0

In order to perform OR microoperation, the selection bits according to the table above must be 01. The output of the multiplexers is the output of A OR B.

**Circuit Diagram**

Here, the simulation is for S=11, Cin=1, A=00, and B=00.



**Function Table**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **S1** | **S0** | **Cin** | **A1** | **A0** | **B1** | **B0** | **D1** | **D0** | **Cout** | **Microoperation** |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | Add |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | Add with carry |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | Subtract with borrow |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | Subtract |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Transfer A |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | Increment A |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | Decrement A |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Transfer A |

**Discussion**

At first, each equipment is discussed in details. The video first shows a trainer board. It has the following features:

1. An on/off button
2. Vcc comes from 5V, and ground from GND
3. 16 input switches
4. The outputs are displayed by connecting the output pins of ICs to the output LED pins via wires.
5. A breadboard is located in the middle. The horizontal red line is the plus connection or Vcc connection. The horizontal blue line is the minus connection or ground. A, B, C, D, and E are vertically connected. There are 16 pins or rails for them.
6. ICs are connected to the breadboard.
7. Pulse switches – A’ and B’ give a negative phase, and A and B give a positive phase.

Secondly, ICs are discussed in the video. Here are the pin numbers for IC 74F153, and a short description of each pin in the dual MUX:

1. Pins 1 and 15 are enable keys for Mux A and Mux B respectively.
2. The 2nd pin is S1, and the 14th pin is S0. S1 is the most significant select bit (MSB), and S0 is the least significant bit (LSB).
3. MUX A input pins (from pin no. 3 till 6) are as follows: 3rd pin is for 4th input bit or I3a … 6th pin is for 1st input or I0a. The output is 7th pin.
4. The 8th pin is GND, or 0 volts.
5. The 16th pin is Vcc, or 5V.
6. Mux B input pins (from pin no. 13 till 10) are as follows: 13th pin is for 4th input bit or I3b … 10th pin is for 1st input or I0b. The output is 9th pin.

IC 7404, hex inverters, have a total of 6 NOT gates. Vcc is in 14th pin, and GND at 7th. The input-output pairs are as follows:

1. Input – 13th pin, Output – 12th pin
2. Input – 11th pin, Output – 10th pin
3. Input – 9th pin, Output – 8th pin
4. Input – 1st pin, Output – 2nd pin
5. Input – 3rd pin, Output – 4th pin
6. Input – 5th pin, Output – 6th pin

IC 7408 has a total of 4 AND gates. IC 7432 has a total of 4 OR gates. IC 7486 has a total of 4 XOR gates. They have the 14th pin as Vcc, and the 7th pin as GND. The following are input-output pins:

1. 13th and 12th pins are input, 11th pin is output
2. 10th and 9th pins are input, 8th pin is output
3. 1st and 2nd pins are input, 3rd pin is output
4. 4th and 5th pins are input, 6th pin is output

The dual MUX already allows for both MUXs to have same select bit. However, if two separate MUXs were used, we would short the select bits.

Before the experiment even starts, the equipment must be checked to see if there are any troubles. The trainer board needs to be checked to see if 5V and ground are working properly or not. The power on trainer board is turned on. Next, the 5V supply is connected to breadboard first. A separate wire from here is then going into an output LED pin. LED turns on.

The GND is not working in the video, so an alternative has been used. The wire is connected to the 0-15V, and the knob is turned to 0V.

The input switches are checked to see if they are properly working or not. The input switch pin is connected to an output pin via a wire. The input switch is turned on to see if the output LED turns on. If the same input switch shows output for all other output pins except a particular output pin, that output pin is not properly working. Hence, this technique can be used to check whether input and output pins are working properly at the same time.

After checking all the equipment, the equipment is now being set up. The Vcc is connected to the positive pin in the breadboard, and the 0-15V is connected to the minus pin.

The ICs for the 0th bit (LSB) are placed on the breadboard (except MUX, it will be done later). Before wiring any other pin, the GND and Vcc are wired. The first and second input switches are wired to the first and second pins of IC 7408. The connection of inputs from AND IC are taken to OR IC’s 1st and 2nd pins. The same is done from OR IC to XOR IC. The NOT IC just takes the first input from XOR IC to the 1st pin. The outputs from each IC (except NOT), are connected from 3rd pin to an output LED pin each. This ensure whether IC is working properly or not for all combinations of inputs of A0 and B0, or the input-output wires have been set up properly or not, as shown in the following table.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **A** | **B** | **Check if output LED for AND …** | **Check if output LED for OR …** | **Check if output LED for XOR …** | **Check if output LED for NOT …** |
| 0 | 0 | … is off | … is off | … is off | … is on |
| 0 | 1 | … is off | … is on | … is on | … is on |
| 1 | 0 | … is off | … is on | … is on | … is off |
| 1 | 1 | … is on | … is on | … is off | … is off |

Next, the outputs are recorded in the truth table for A0 and B0.

The multiplexer is connected to the breadboard. It is currently in active low. The active pin must be connected to the GND. After connecting Vcc and GND, the output A0 AND B0 are connected to the 6th pin as LSB, A0 OR B0 as 5th pin, A0 XOR B0 as 4th pin, and A0 NOT as 3rd pin (MSB). The first MUX output, 7th pin in IC 74F153, is connected to an output LED pin. S0 and S1 from 14th and 2nd pins respectively are connected to the 3rd and 4th input switches. Then, it is observed for S=00, AND0 output is found, S=01 for OR0 output, S=10 for XOR0 output, and S=11 for NOT0 output.

After connecting 0th bits of A and B, the 1st bit is connected. The 5th and 6th input switches are used for A1 and B1 respectively. The wire connects from the 5th and 6th input switches to the 4th and 5th pins of IC 7408. The output from 6th pin is connected to an output LED pin and checked for LED turning on as per the table drawn above. The inputs from AND IC are taken to OR IC’s 4th and 5th pins, and the 6th output pin is connected to an output LED pin. The same is repeated from OR IC to XOR IC. From the XOR IC, only the A1 input is taken to NOT IC’s 3rd pin, and the 4th output pin is connected to an output LED pin. These values are recorded in the truth table – this time for A1 and B1.

Next, A1­ AND B1, A1­ OR B1, A1­ XOR B1 and A1­ NOT are connected to IC 74F153’s 10th, 11th, 12th and 13th pins respectively. The output at the 9th pin is connected to an output LED pin. It is observed for S=00, AND1 output is found, S=01 for OR1 output, S=10 for XOR1 output, and S=11 for NOT1 output.