Lime microsystems

LimeSDR Mini 1v0

CONTROLLED IMPEDANCE

GENERAL PARAMETERS:

Top layer copper foil thickness: 17.5 um
Dielectric thickness from Top to L2 = 173um (6.8 mils)
Dielectric between Top layer and 2nd layer relative permittivity (Er): 4.2

CALCULATIONS:

RF (Top)

50 Ohm coplanar waveguide (Top layer, without GND) characteristics:
Top layer copper foil thickness: 17.5 um
Track width = 0.309 mm (12.165 mils)
Dielectric thickness from Top to L2 = 173um (6.8 mils)
Dielectric between Top layer and 2nd layer relative permittivity (Er): 4.2

Approximate microstrip line impedance = 49.99 Ohms (+/- 10% tolerance)

RF (Top)

100 Ohm coplanar differential pair (Top layer, without GND) characteristics:
Top layer copper foil thickness: 17.5 um
Track width = 0.2 mm (7.874 mils)
Track spacing = 0.14 mm (5.511 mils)
Track width/spacing ratio = 1.43
Dielectric thickness from top to L2 = 173um (6.8 mils)
Dielectric between Top layer and 2nd layer relative permittivity (Er): 4.2

Approximate coupled microstrip line impedance = 100.6 Ohms (+/- 10% tolerance)

USB3.0 (Top)

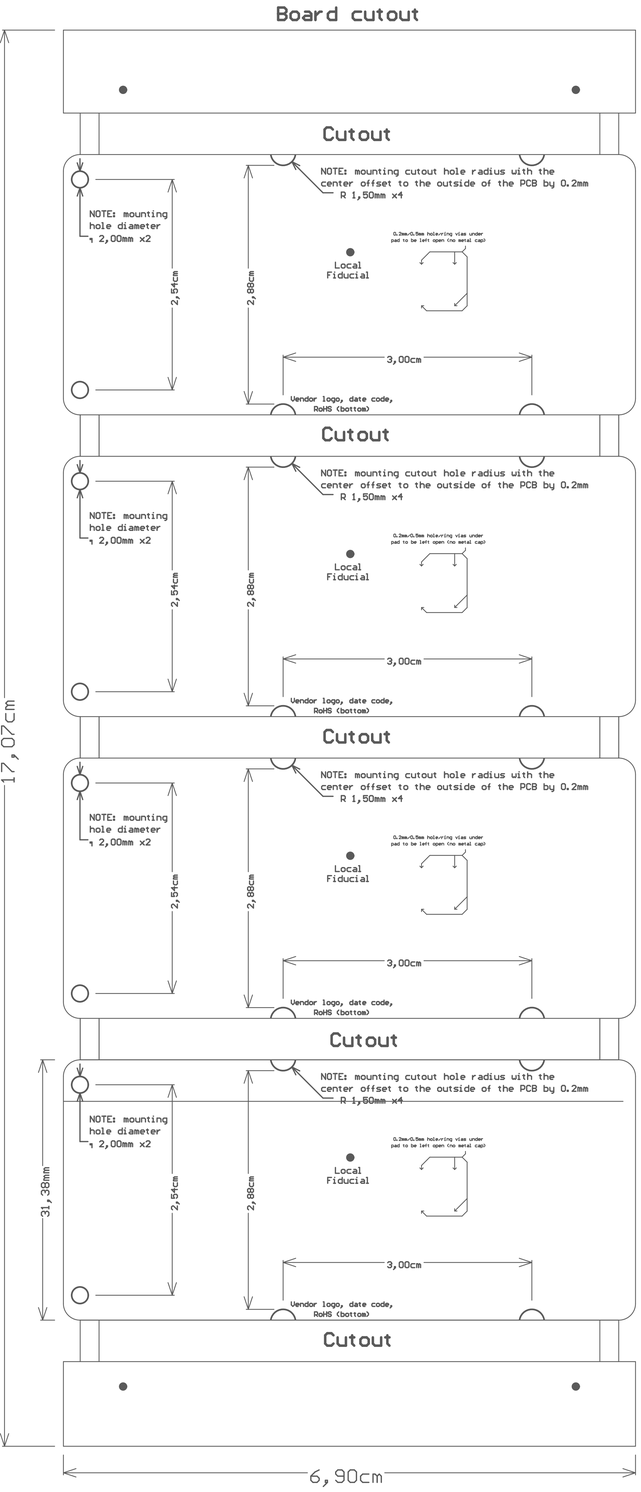
90 Ohm coupled microstrip line (Top layer, without GND) characteristics:
Top layer copper foil thickness: 17.5 um
Track width = 0.2 mm (7.874 mils)
Track spacing = 0.1 mm (3.93 mils)
Track width/spacing ratio = 2
Dielectric thickness from Top to 2nd layer = 173um (6.8 mils)
Dielectric between Top layer and 2nd layer relative permittivity (Er): 4.2

Approximate coupled microstrip line impedance = 90.5 Ohms (+/- 10% tolerance)

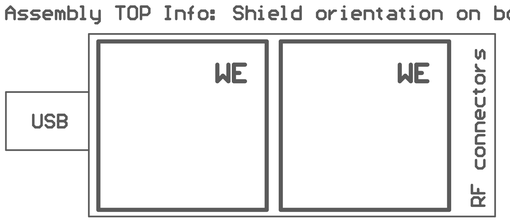
USB3.0 (Bottom)

90 Ohm coupled microstrip line (Bottom layer, without GND) characteristics:
Bottom layer copper foil thickness: 17.5 um
Track width = 0.2 mm (7.874 mils)
Track spacing = 0.1 mm (3.93 mils)
Track width/spacing ratio = 2
Dielectric thickness from Bottom to 7th layer = 173um (6.8 mils)
Dielectric between Bottom layer and 7th layer relative permittivity (Er): 4.2

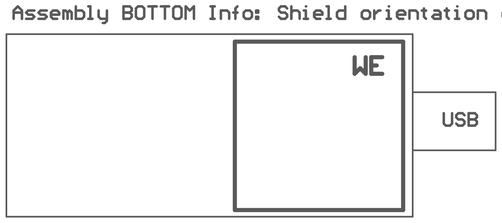
Approximate coupled microstrip line impedance = 90.5 Ohms (+/- 10% tolerance)



Assembly TOP Info: Shield orientation on board



Assembly BOTTOM Info: Shield orientation on board



Single board size: 69 x 31.37 mm2
Total panel size: 69 x 170.68 mm2

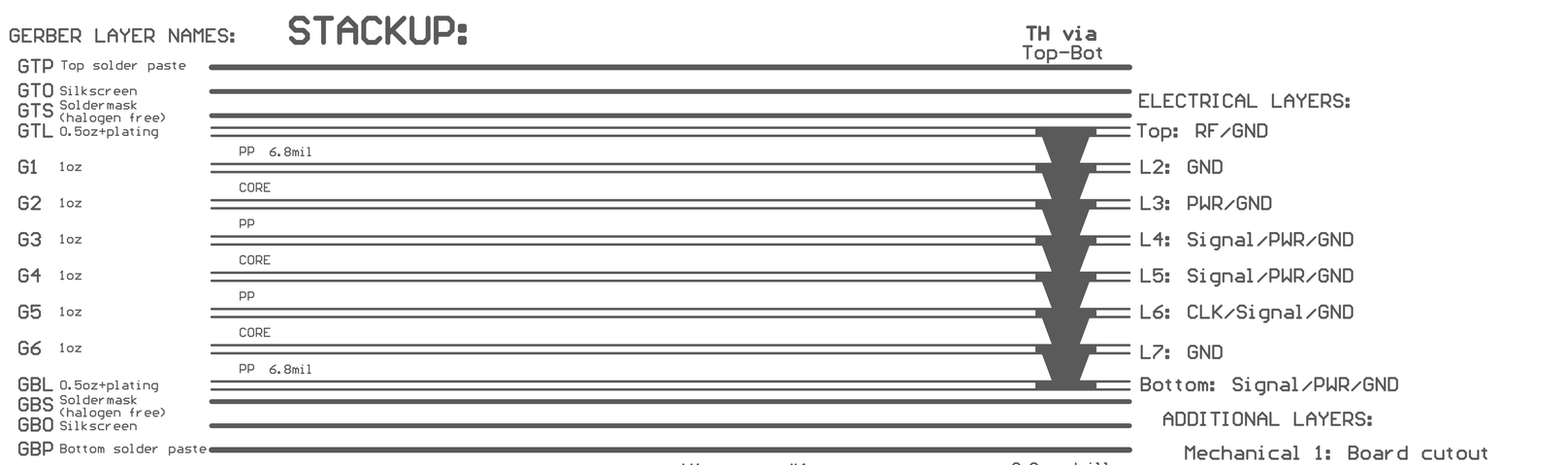
VERY IMPORTANT NOTES:

1) All 0.2mm vias including 0.35mm ring and 0.2mm drill via-in-pads (IC1) must be resin filled with metal cap
2) IC1 thermal pad vias with 0.4mm ring and 0.2mm drill must be resin filled with metal cap.
   IC1 thermal pad vias with 0.5mm ring and 0.2mm drill must be left open (NO resin fill with metal cap). 4 vias in total, marked with note
3) Solder mask : DARK BLUE, both sides, halogen free, glossy finish (NOT matte)
4) Silkscreen : white epoxy ink, halogen free, both sides. No silkscreen on pads.
5) DRCs must be run on Gerber files before building boards
6) Hole diameters are final manufactured diameters INCLUDING HOLE METALIZATION.
7) Minimum track spacing: 0.1 mm
   Minimum track width: 0.1 mm
8) There are plated and non-plated holes on the PCB
9) Material:
   - IT-180A
   - PCB vendor to silkscreen UL and RoHS compliance marks, vendor logo and date code on bottom where shown (ignore if none of the info will be placed on PCB)
   - Copper weight: External layers 0.5 oz+plating
     Internal layers 1 oz
10) Electrical test : 100 % netlist.
11) Boards are to be individually bagged.
12) Assembly note: Assembly house MUST provide notes in paper with shipped board if there were any changes during assembly and the board is not assembled 100% according to BOM and P&P files. Note example:

Part	Initial BOM asm. note	Status on board	Comment
R1	FIT	NF	Not mounted due to bad footprint
IC5	FIT	NF	Not mounted due to part shortage

GERBER LAYER NAMES:

STACKUP:



Total PCB thickness:
1.6mm +/- 10%

Via type #1 — 0.2mm drill, 0.4mm ring

Via type #2 (In pad, resin filled with metal cap) — 0.2mm drill, 0.35mm ring