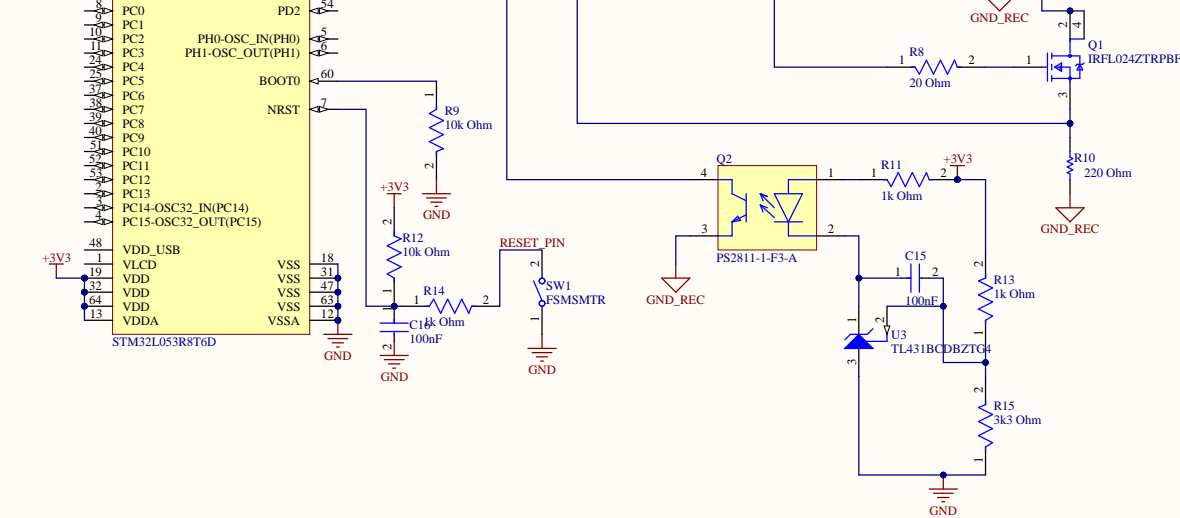
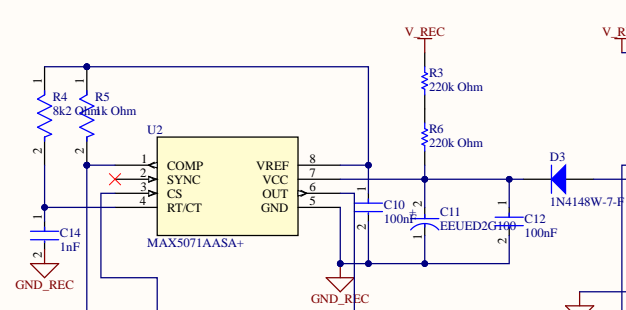


The diagram shows a 5-stage pipeline. Each stage consists of a PMOS transistor (top) and an NMOS transistor (bottom) connected in series. The gates of the PMOS transistors are connected to a common bus labeled $+3V3$. The gates of the NMOS transistors are connected to a common bus labeled **GND**. The drains of the PMOS transistors are connected to the gates of the NMOS transistors in the next stage. Each gate is connected to a capacitor labeled 100mF . The output of the fifth stage is labeled **OUT**.



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