Basys3 vs VTR Earch comparison
Design: 4 bit counter

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Post implementation Timing

With a clock period of 10ns or frequency of 100MHz

Parameter	Slack with Basys3	Slack with VTR Earch
Technology	**28nm**	**40nm [Earch]**
Worst Negative Slack (WNS)- Setup	5.77ns	8.54ns
Worst Negative Slack (WNS)- Hold	0.23ns	0.293ns

Clock frequency varied to get minimum slack

Parameter	with Basys3	with VTR Earch
Max freq	285MHz (period 3.5ns)	555MHz (period 1.8ns)
Worst Negative Slack (WNS)- Setup	0.41ns	0.34ns
Worst Negative Slack (WNS)- Hold	0.33ns	0.293ns

VTR Earch: Worst case setup path
Design: counter: 555MHz

```
#Path 1
Startpoint: up_counter^out~0_FF.Q[0] (.latch clocked by up_counter_clk)
Endpoint  : up_counter^out~3_FF.D[0] (.latch clocked by up_counter_clk)
Path Type : setup

Point                                                                    Incr      Path
-------------------------------------------------------------------------------------
clock up_counter_clk (rise edge)                                        0.000     0.000
clock source latency                                                    0.000     0.000
up_counter_clk.inpad[0] (.input)                                        0.000     0.000
up_counter^out~0_FF.clk[0] (.latch)                                     0.042     0.042
up_counter^out~0_FF.Q[0] (.latch) [clock-to-output]                     0.124     0.166
up_counter^ADD~4-1[0].a[0] (adder)                                      0.315     0.481
up_counter^ADD~4-1[0].cout[0] (adder)                                   0.300     0.781
up_counter^ADD~4-2[0].cin[0] (adder)                                    0.000     0.781
up_counter^ADD~4-2[0].cout[0] (adder)                                   0.010     0.791
up_counter^ADD~4-3[0].cin[0] (adder)                                    0.000     0.791
up_counter^ADD~4-3[0].cout[0] (adder)                                   0.010     0.801
up_counter^ADD~4-4[0].cin[0] (adder)                                    0.000     0.801
up_counter^ADD~4-4[0].sumout[0] (adder)                                 0.300     1.101
n27.in[1] (.names)                                                      0.100     1.201
n27.out[0] (.names)                                                     0.235     1.436
up_counter^out~3_FF.D[0] (.latch)                                       0.000     1.436
data arrival time                                                                 1.436

clock up_counter_clk (rise edge)                                        1.800     1.800
clock source latency                                                    0.000     1.800
up_counter_clk.inpad[0] (.input)                                        0.000     1.800
up_counter^out~3_FF.clk[0] (.latch)                                     0.042     1.842
clock uncertainty                                                       0.000     1.842
cell setup time                                                        -0.066     1.776
data required time                                                                1.776
-------------------------------------------------------------------------------------
data required time                                                                1.776
data arrival time                                                                -1.436
-------------------------------------------------------------------------------------
slack (MET)                                                                       0.340
```

VTR Earch: Worst case hold path
Design: counter: 555MHz

```
#Path 1
Startpoint: up_counter^out~0_FF.Q[0] (.latch clocked by up_counter_clk)
Endpoint  : up_counter^out~0_FF.D[0] (.latch clocked by up_counter_clk)
Path Type : hold

Point                                                                  Incr      Path
-------------------------------------------------------------------------------------
clock up_counter_clk (rise edge)                                      0.000     0.000
clock source latency                                                  0.000     0.000
up_counter_clk.inpad[0] (.input)                                      0.000     0.000
up_counter^out~0_FF.clk[0] (.latch)                                   0.000     0.000
up_counter^out~0_FF.Q[0] (.latch) [clock-to-output]                   0.124     0.124
n22.in[0] (.names)                                                    0.000     0.124
n22.out[0] (.names)                                                   0.235     0.359
up_counter^out~0_FF.D[0] (.latch)                                     0.000     0.359
data arrival time                                                               0.359

clock up_counter_clk (rise edge)                                      0.000     0.000
clock source latency                                                  0.000     0.000
up_counter_clk.inpad[0] (.input)                                      0.000     0.000
up_counter^out~0_FF.clk[0] (.latch)                                   0.000     0.000
clock uncertainty                                                     0.000     0.000
cell hold time                                                        0.066     0.066
data required time                                                              0.066
-------------------------------------------------------------------------------------
data required time                                                             -0.066
data arrival time                                                               0.359
-------------------------------------------------------------------------------------
slack (MET)                                                                     0.293
```

Basys3: Worst case setup path

Summary

Name	Path 1
Slack	0.412ns
Source	delay_count_reg[3]/C (rising edge-triggered cell FDRE clocked by clk
Destination	delay_count_reg[24]/D (rising edge-triggered cell FDRE clocked by cl
Path Group	clk
Path Type	Setup (Max at Slow Process Corner)
Requirement	3.500ns (clk rise@3.500ns - clk rise@0.000ns)
Data Path Delay	3.052ns (logic 2.115ns (69.290%) route 0.937ns
Logic Levels	7 (CARRY4=6 LUT3=1)
Clock Path Skew	-0.029ns
Clock Un...rtainty	0.035ns

Source Clock Path

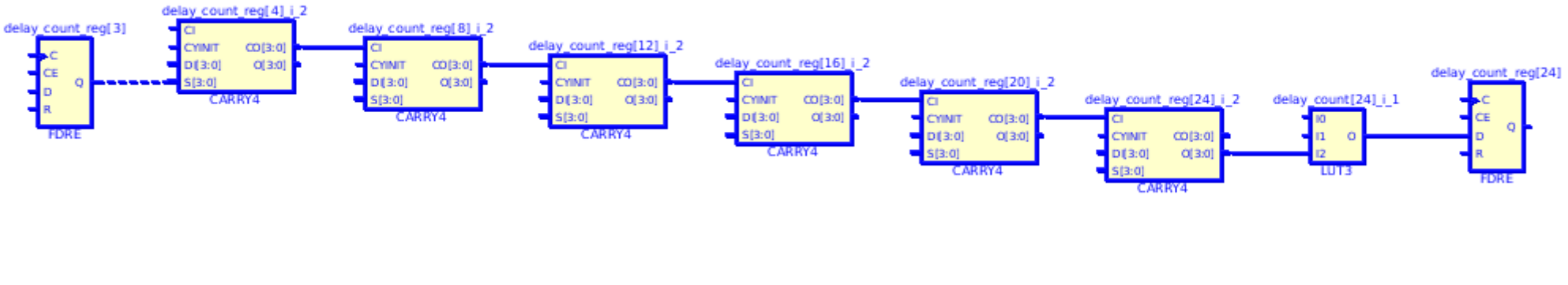
Delay Type	Incr (ns)	Path (ns)	Location	Netlist Resource(s)
(clock clk rise edge)	(r) 0.000	0.000		
	(r) 0.000	0.000	Site: W5	clk
net (fo=0)	0.000	0.000		clk
IBUF (Prop_ibuf_I_O)	(r) 1.458	1.458	Site: W5	clk_IBUF_inst/O
net (fo=1, routed)	1.967	3.425		clk_IBUF
BUFG (Prop_bufg_I_O)	(r) 0.096	3.521	Site: BU...RL_X0Y0	clk_IBUF_BUFG_inst/O
net (fo=27, routed)	1.619	5.140		clk_IBUF_BUFG
FDRE			Site: SLICE_X64Y65	delay_count_reg[3]/C

Data Path

Delay Type	Incr (ns)	Path (ns)	Location	Netlist Resource(s)
FDRE (Prop_fdre_C_Q)	(r) 0.518	5.658	Site: SLICE_X64Y65	delay_count_reg[3]/Q
net (fo=2, routed)	0.540	6.198		delay_count_reg_n_0_[3]
CARRY4 (Prop_c...4_S[2]_CO[3])	(r) 0.522	6.720	Site: SLICE_X65Y65	delay_count_reg[4]_i_2/CO[3]
net (fo=1, routed)	0.000	6.720		delay_count_reg[4]_i_2_n_0
CARRY4 (Prop_carry4_CI_CO[3])	(r) 0.114	6.834	Site: SLICE_X65Y66	delay_count_reg[8]_i_2/CO[3]
net (fo=1, routed)	0.000	6.834		delay_count_reg[8]_i_2_n_0
CARRY4 (Prop_carry4_CI_CO[3])	(r) 0.114	6.948	Site: SLICE_X65Y67	delay_count_reg[12]_i_2/CO[3]
net (fo=1, routed)	0.000	6.948		delay_count_reg[12]_i_2_n_0
CARRY4 (Prop_carry4_CI_CO[3])	(r) 0.114	7.062	Site: SLICE_X65Y68	delay_count_reg[16]_i_2/CO[3]
net (fo=1, routed)	0.000	7.062		delay_count_reg[16]_i_2_n_0
CARRY4 (Prop_carry4_CI_CO[3])	(r) 0.114	7.176	Site: SLICE_X65Y69	delay_count_reg[20]_i_2/CO[3]
net (fo=1, routed)	0.000	7.176		delay_count_reg[20]_i_2_n_0
CARRY4 (Prop_carry4_CI_O[3])	(r) 0.313	7.489	Site: SLICE_X65Y70	delay_count_reg[24]_i_2/O[3]
net (fo=1, routed)	0.398	7.886		data0[24]
LUT3 (Prop_lut3_I2_O)	(r) 0.306	8.192	Site: SLICE_X63Y70	delay_count[24]_i_1/O
net (fo=1, routed)	0.000	8.192		delay_count[24]
FDRE			Site: SLICE_X63Y70	delay_count_reg[24]/D
Arrival Time		8.192		

Basys3: Worst case setup path

Path schematics

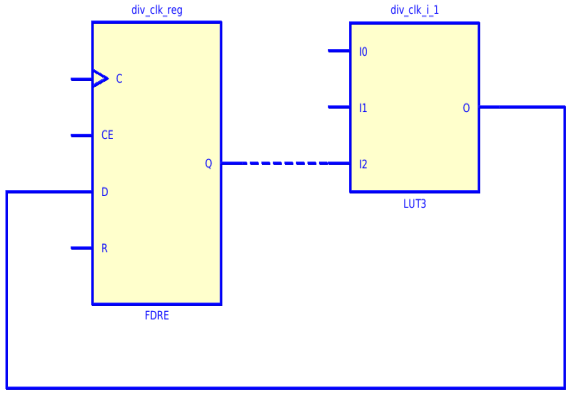


Basys3: Worst case hold path

Summary	
Name	Path 11
Slack (Hold)	0.334ns
Source	div_clk_reg/C (rising edge-triggered cell FDRE clocked by clk {ri
Destination	div_clk_reg/D (rising edge-triggered cell FDRE clocked by clk {ri
Path Group	clk
Path Type	Hold (Min at Fast Process Corner)
Requirement	0.000ns (clk rise@0.000ns - clk rise@0.000ns)
Data P...Delay	0.455ns (logic 0.209ns (45.985%) route 0.246ns (54.015%))
Logic Levels	1 (LUT3=1)
Clock ... Skew	0.000ns

Source Clock Path

Delay Type	Incr (ns)	Path (ns)	Location	Netlist Resource(s)
(clock clk rise edge)	(r) 0.000	0.000		
	(r) 0.000	0.000	Site: W5	clk
net (fo=0)	0.000	0.000		clk
IBUF (Prop_ibuf_I_O)	(r) 0.226	0.226	Site: W5	clk_IBUF_inst/O
net (fo=1, routed)	0.631	0.858		clk_IBUF
BUFG (Pr...ufg_I_O)	(r) 0.026	0.884	Site: BU...RL_X0Y0	clk_IBUF_BUFG_inst/O
net (fo=27, routed)	0.586	1.469		clk_IBUF_BUFG
FDRE			Site: SLICE_X64Y68	div_clk_reg/C



Data Path

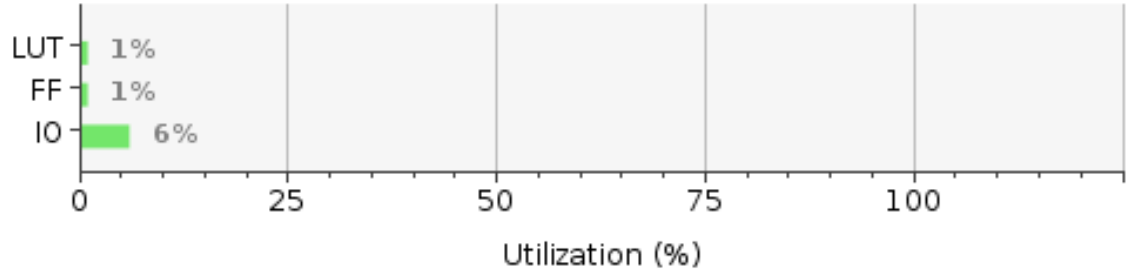
Delay Type	Incr (ns)	Path (ns)	Location	Netlist Resource(s)
FDRE (Pr...dre_C_Q)	(r) 0.164	1.633	Site: SLICE_X64Y68	div_clk_reg/Q
net (fo=5, routed)	0.246	1.879		div_clk_reg_n_0
LUT3 (Pro...t3_I2_O)	(r) 0.045	1.924	Site: SLICE_X64Y68	div_clk_i_1/O
net (fo=1, routed)	0.000	1.924		div_clk_i_1_n_0
FDRE			Site: SLICE_X64Y68	div_clk_reg/D
Arrival Time		1.924		

Area and power

Area

Basys3

Resource	Utilization	Available	Utilization %
LUT	23	20800	0.11
FF	31	41600	0.07
IO	6	106	5.66



VTR

```
Pb types usage...
  io                : 7
   inpad            : 3
   outpad           : 4
  clb               : 1
   fle              : 6
    lut5inter       : 6
     ble5           : 11
      flut5         : 6
       lut5         : 6
        lut         : 6
       ff           : 4
      arithmetic    : 5
       adder        : 5
```

Parameter	Resources on Basys3	Resources with VTR
LUTs	23	18
I/O	6	7
Flip-flops	31	4

```
Circuit Statistics:
  Blocks: 22
    .input :       3
    .latch :       4
    .output:       4
    0-LUT  :       2
    6-LUT  :       4
    adder  :       5
  Nets  : 21
    Avg Fanout:     2.0
    Max Fanout:     4.0
    Min Fanout:     1.0
```

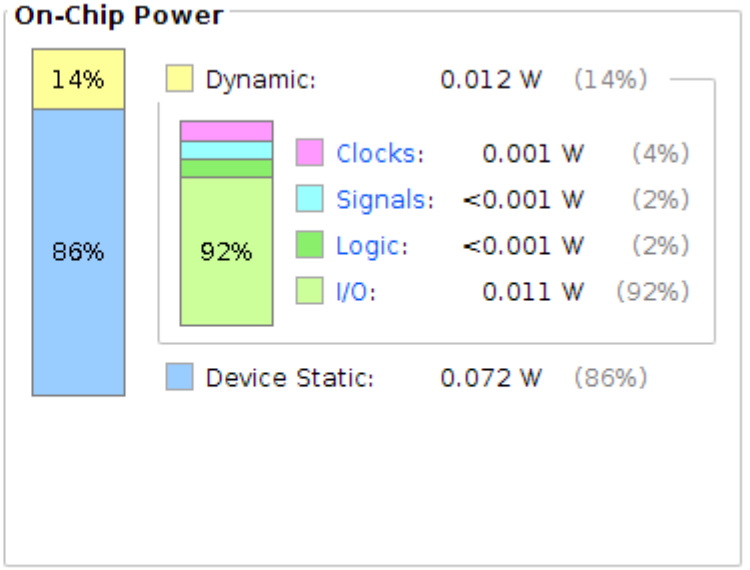
Power

Basys3

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.084 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.4°C**
Thermal Margin:	59.6°C (11.9 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium

Launch Power Constraint Advisor to find and fix invalid switching activity



VTR

```
-------------------------------- Power Breakdown ------------------------------
Component                        Power (W)   %-Total     %-Dynamic   Method

Total                            0.0003212   1           0.7689
 Routing                         0.0001066   0.3319      0.4223
  Switch Box                     9.697e-05   0.3019      0.3837
  Connection Box                 5.033e-06   0.01567     0.6368
  Global Wires                   4.617e-06   0.01437     1
 PB Types                        8.287e-05   0.258       0.8582
  Primitives                     6.158e-05   0.1917      0.9314
  Interc Structures              7.248e-06   0.02256     0.6487
  Buffers and Wires              1.404e-05   0.0437      0.6451
  Other Estimation Methods       0           0           -nan
 Clock                           0.0001317   0.4101      0.9932
```

Power

Parameter	Power with Basys3 (W)	Power with VTR (W)
Clocks	0.001	0.0001
Signals	0.001	1.4e-5
Logic	0.001	8.2e-5
I/O	0.011	0
Dynamic	0.012	