

FPGAs - Fabric, Design and Architecture

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Agenda

- Module 1
 - FPGA Introduction
 - Design of a 4-bit counter through Vivado on Basys3 FPGA
 - Use of Virtual Input/Output (VIO)
- Module 2
 - OpenFPGA Introduction (<https://openfpga.readthedocs.io/en/master/overview/motivation/>)
 - VTR Flow (<https://docs.verilogtorouting.org/en/latest/quickstart/>)
 - Demos:
 - VPR flow: tseng on Earch
 - VTR flow: 4 bit counter on Earch
 - Timing, area, power and post implementation simulation
 - Basys3 vs VTR results

Agenda

- Module 3:
 - Explain RISC-V RVMyth processor code
 - Run it till bitstream on Basys3
- Module 4:
 - Skywater OpenSource FPGA (SOFA): 4-bit counter on SOFA
 - Area, timing and post implementation
- Module 5:
 - Skywater OpenSource FPGA (SOFA): RVMyth on SOFA (<https://github.com/Inis-uofu/SOFA>)
 - Area, timing and post implementation

Collaterals

- Needed for the workshop
 - https://github.com/nandithaec/fpga_workshop_collaterals

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