# SOFA overview

https://github.com/lnis-uofu/SOFA

https://skywater-openfpga.readthedocs.io/en/latest/

# Skywater Opensource FPGAs

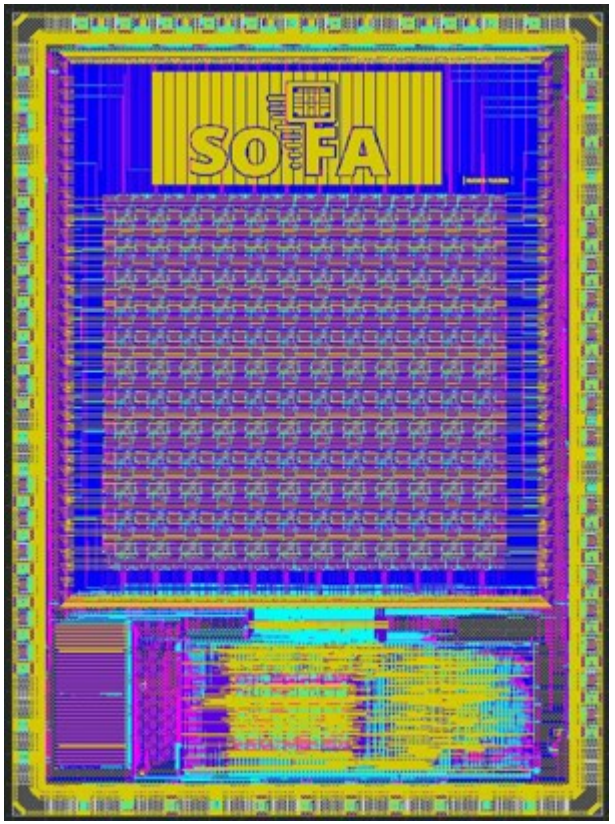
- SOFA (Skywater Opensource FPGAs) are a series of open-source FPGA IPs using the open-source Skywater 130nm PDK and OpenFPGA framework.
- Open-source embedded FPGA IP library, from the architecture description to production ready layouts.

# HD eFPGAs

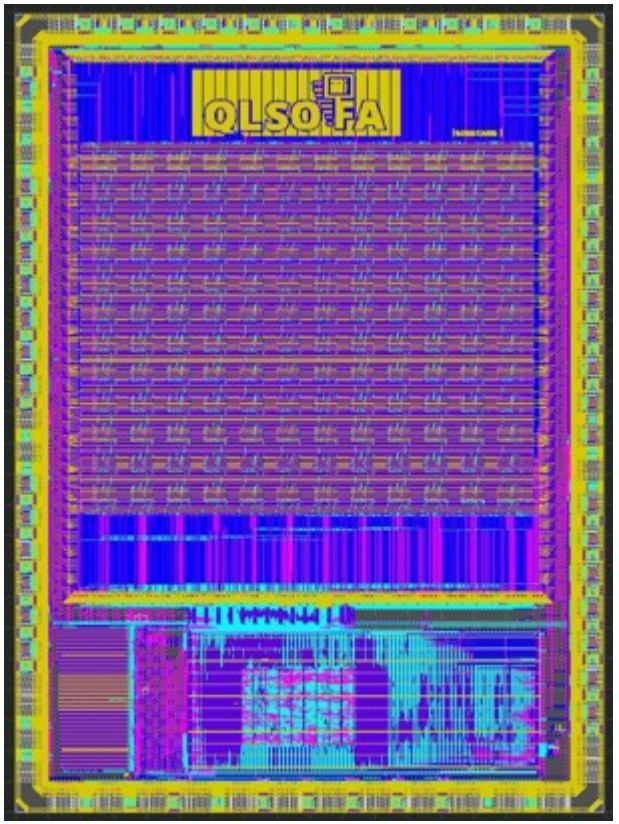
The High Density (HD) FPGAs are embedded FPGAs built with the Skywater 130nm High Density Standard Cell library (Sky130_fd_SC_HD).

| Resource/Capacity | SOFA HD | QLSOFA HD | SOFA CHD |
|---|---|---|---|
| Look-Up Tables [1] | 1152 | 1152 | 1152 |
| Flip-flops | 2304 | 2304 | 2304 |
| Soft Adders [2] | N/A | 1152 | 1152 |
| Routing Channel Width [3] | 40 | 60 | 60 |
| Max. Configuration Speed [4] | 50MHz | 50MHz | 50MHz |
| Max. Operating Speed [4] | 50MHz | 50 MHz | 50MHz |
| User I/O Pins [5] | 144 | 144 | 144 |
| Max. I/O Speed [4] | 33MHz | 33MHz | 33MHz |
| Core Voltage | 1.8V | 1.8V | 1.8V |

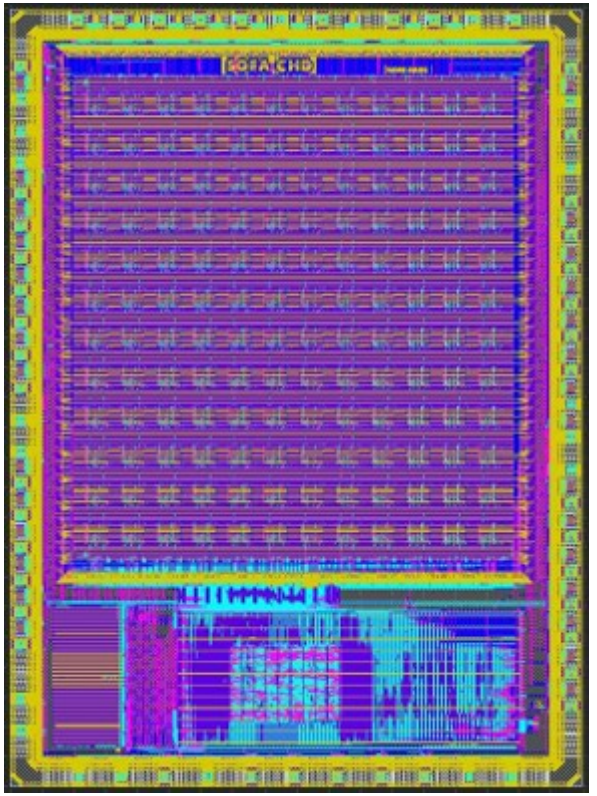
# Layout views




SOFA HD is the base design of the SOFA high-density eFPGA IPs




QLSOFA HD is the arithmetic-enhanced design




SOFA CHD is the performance-optimized design

https://skywater-openfpga.readthedocs.io/en/latest/device/hd_fpga/hd_device_gallery/

# Commands to be run by user on cloud

- We assume that OpenFPGA is already installed and its path is exported
- Now run the following to install SOFA and make sure it is working:
  - git clone https://github.com/lnis-uofu/SOFA.git
  - cd FPGA1212_QLSOFA_HD_PNR
  - make runOpenFPGA

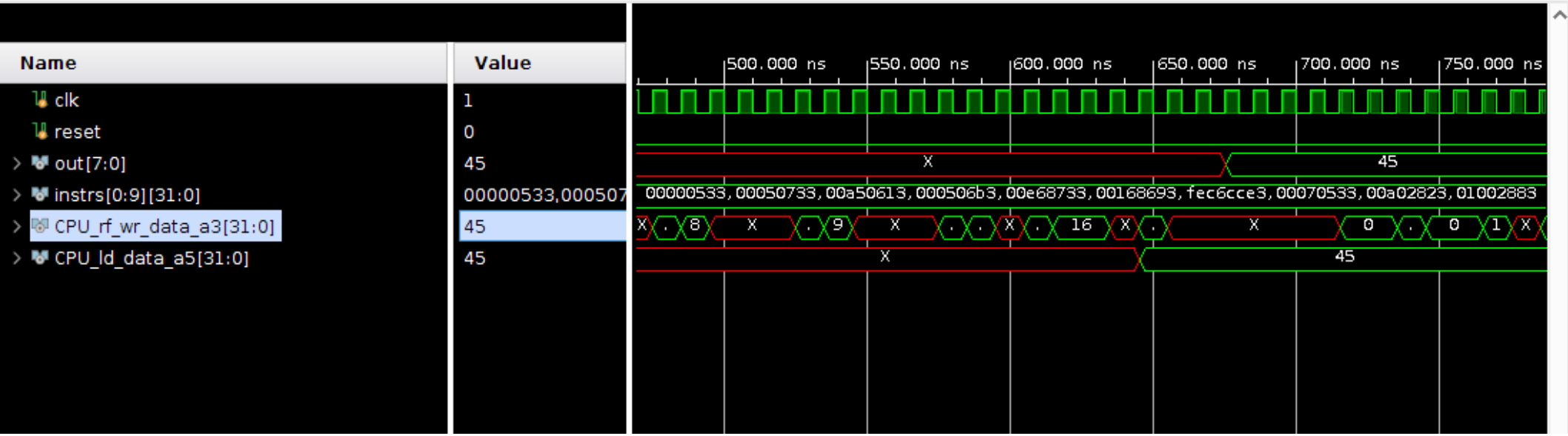
# RVMyth

Instr memory in
mythcore_test.v

```
`
  /*SV_plus*/
     // The program in an instruction memory.
     wire [31:0] instrs [0:10-1];
     assign instrs[0] = {7'b0000000, 5'd0, 5'd0, 3'b000, 5'd10, 7'b0110011};
     assign instrs[1] = {7'b0000000, 5'd0, 5'd10, 3'b000, 5'd14, 7'b0110011};
     assign instrs[2] = {12'b1010, 5'd10, 3'b000, 5'd12, 7'b0010011};
     assign instrs[3] = {7'b0000000, 5'd0, 5'd10, 3'b000, 5'd13, 7'b0110011};
     assign instrs[4] = {7'b0000000, 5'd14, 5'd13, 3'b000, 5'd14, 7'b0110011};
     assign instrs[5] = {12'b1, 5'd13, 3'b000, 5'd13, 7'b0010011};
     assign instrs[6] = {1'b1, 6'b111111, 5'd12, 5'd13, 3'b100, 4'b1100, 1'b1, 7'b1100011};
     assign instrs[7] = {7'b0000000, 5'd0, 5'd14, 3'b000, 5'd10, 7'b0110011};
     assign instrs[8] = {7'b0000000, 5'd10, 5'd0, 3'b010, 5'b10000, 7'b0100011};
     assign instrs[9] = {12'b10000, 5'd0, 3'b010, 5'd17, 7'b0000011};

  for (imem   0; imem <  0; imem imem+1) begin : |  CPU_Imem // /imem
```

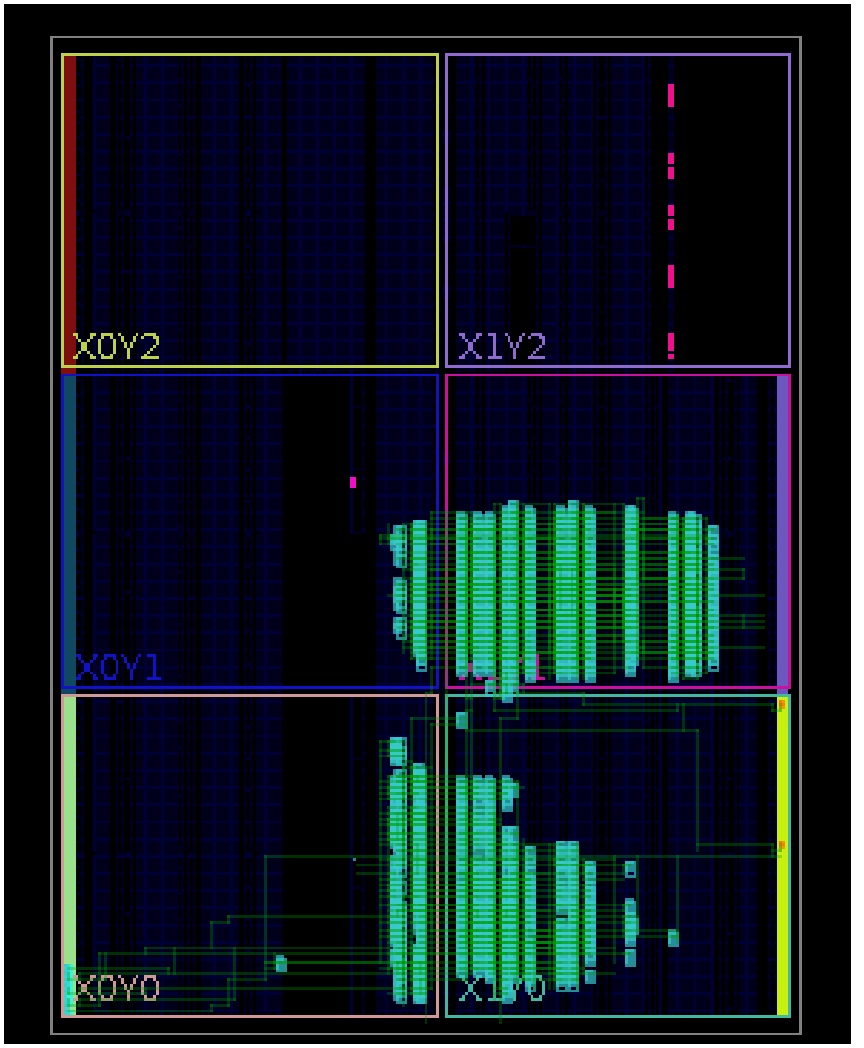
RVMyth Simulation output: Sum of first 9 numbers after running through Vivado



# Post implementation Area

## Without ILA

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 816 | 20800 | 3.92 |
| LUTRAM | 1 | 9600 | 0.01 |
| FF | 1770 | 41600 | 4.25 |
| IO | 10 | 106 | 9.43 |




## With ILA

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 1932 | 20800 | 9.29 |
| LUTRAM | 95 | 9600 | 0.99 |
| FF | 3578 | 41600 | 8.60 |
| BRAM | 0.50 | 50 | 1.00 |
| IO | 10 | 106 | 9.43 |

# Post implementation: Timing and Power (Without ILA)

**Design Timing Summary**

| Setup | | Hold | |
|---|---|---|---|
| Worst Negative Slack (WNS): | 2.472 ns | Worst Hold Slack (WHS): | 0.060 ns |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | 0.000 ns |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 4786 | Total Number of Endpoints: | 4786 |

**All user specified timing constraints are met.**

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

| | |
|---|---|
| **Total On-Chip Power:** | **0.094 W** |
| **Design Power Budget:** | **Not Specified** |
| **Power Budget Margin:** | **N/A** |
| **Junction Temperature:** | **25.5°C** |
| Thermal Margin: | 59.5°C (11.8 W) |
| Effective θJA: | 5.0°C/W |
| Power supplied to off-chip devices: | 0 W |
| Confidence level: | Medium |

**On-Chip Power**