Architecture of 8086

It is divided into 2 parts

1) Bus interface unit (BIU) and 2) Execution unit (EU)

BIU It acts as interface between system bus and the execution unit.

Fetches instruction from memory.

Reads data from I/O ports and memories.

Writes data to ports and memories

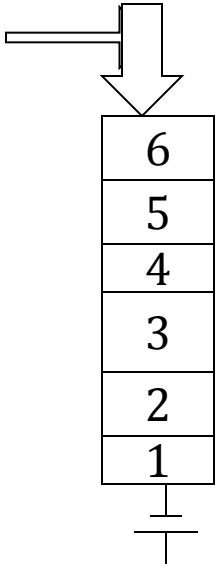
Supports pipelining.

BIU handles transfer of data on all the buses for the execution unit.

Queue: To speed up the program execution BIU fetches as many as 6 instruction bytes from memory. These pre-fetched instruction byte for execution unit in FIFO group of registers called a QUEUE.

Concept of pipelining

Fetching the next instruction while recent instruction executes is known as pipelining.



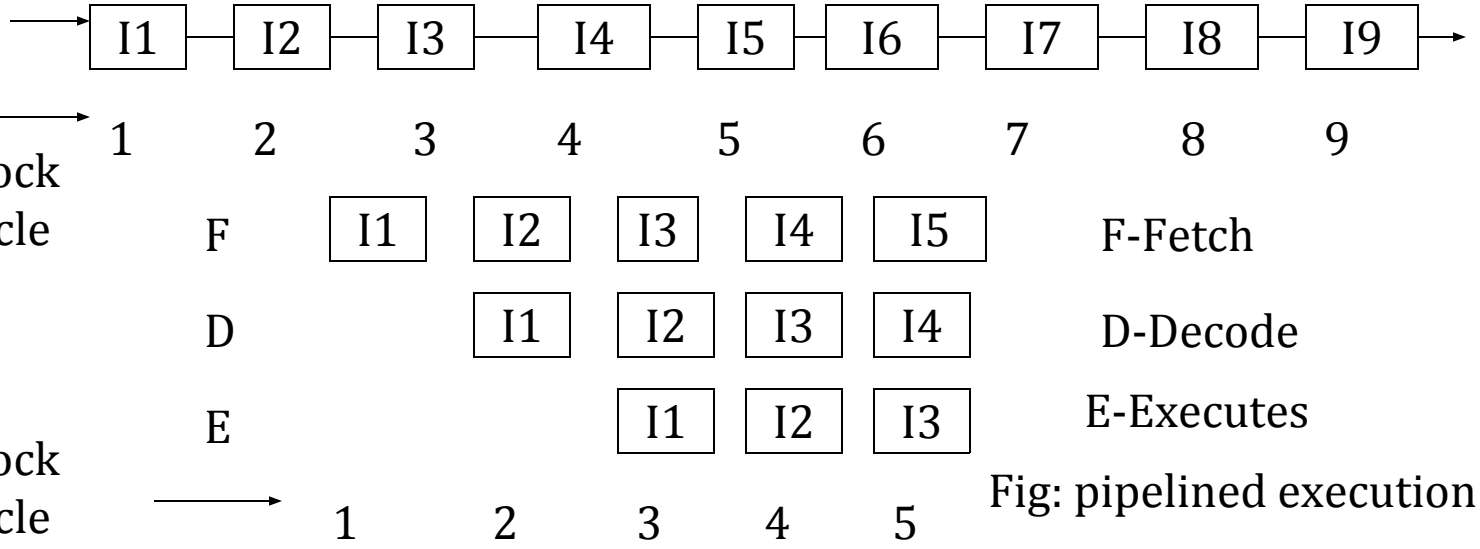


Fig: pipelined execution of 3 instruction

1. On non pipelined processor 9 clock cycle are required for individual fetch , decode & execute for 3 instruction.
2. On pipelined processor fetch, decode & execute operation are performed in parallel.
3. Only 5 cycle are required to execute 3 instruction.
4. 1 instruction requires -> 3 cycle to completes.
5. Additional instruction complete at rate of one per cycle.
6. During clock cycle 5 I_3 instruction executing , I_4 is decoding , I_5 instruction fetched.
7. If 1000 instruction it requires 3000 clock cycle on non pipelined processor then it requires 1002 clock cycle on pipelined processor.
8. In 8086 performs fetch , decode , & executes instruction in parallel.