8086 Microprocessor - Memory and IO Interfacing

Memory and I/O Interfacing

Interface is the path for communication between two components. Interfacing is of two types, memory interfacing and I/O interfacing.

Memory Interfacing

When we are executing any instruction, we need the microprocessor to access the memory for reading instruction codes and the data stored in the memory. For this, both the memory and the microprocessor requires some signals to read from and write to registers. The interfacing process includes some key factors to match with the memory requirements and microprocessor signals. The interfacing circuit therefore should be designed in such a way that it matches the memory signal requirements with the signals of the microprocessor.

I/O Interfacing

There are various communication devices like the keyboard, mouse, printer, etc. So, we need to interface the keyboard and other devices with the microprocessor by using latches and buffers. This type of interfacing is known as I/O interfacing.

In memory interfacing

8 bit data line, 16 bit address line, control signals are connected to corresponding lines of memory IC.

In I/O device interfacing

8 bit data line, only 8 bit address line, control signals are connected to corresponding lines of I/O devices.

Address connections: All memory devices have address inputs that select a memory location within the memory device. Address inputs are labeled (A0 – An).

Data connections: All memory devices have a set of data outputs or input/outputs. Today many of them have bi-directional common I/O pins.

Selection connections: Each memory device has an input that selects or enables the memory device. This kind of input is most often called a chip select (CS) , chip enable (CE) or simply select (S) input.

Control connections: The control input most often found on the ROM is the output enable (OE) or gate (G) this allows data to flow out of the output data pins of the ROM.

Minimum mode Memory and I/O Interfacing

- Address bus & Data bus are multiplexed on same lines (AD0 to AD15).
- During first clock cycle, it serves as a memory/ IO address bus.
- For second and third clock cycles it acts as data bus and carries data.
- Demultiplexing refers to separating Address & Data signals for read/write operations.

8086 Memory Organization

- The memory address space of the 8086-based microcomputers has different logical and physical organizations.
- Logically, memory is implemented as a single 1M × 8 memory bank. The byte-wide storage locations are assigned consecutive addresses over the range from 00000H through FFFFFH.
- Physically, memory is implemented as two independent 512 Kbyte banks: the low (even) bank and the high (odd) bank.

8086 Memory Organization

- To distinguish between odd and even bytes, the CPU provides a signal called BHE (bus high enable).
- BHE and A0 are used to select the odd and even byte, as shown in the table below.

BHE	A0	Function
0	0	Choose both odd and even memory bank
0	1	Choose only odd memory bank
1	0	Choose only even memory bank
1	1	None is chosen

Memory Expansion

- In many applications, the microcomputer system requirement for memory is greater than what is available in a single device. There are two basic reasons for expanding memory capacity:
    i. The byte-wide length is not large enough.
    ii. The total storage capacity is not enough bytes.
- Both of these expansion needs can be satisfied by interconnecting a number of ICs.

Interfacing I/O Devices

- Using I/O devices data can be transferred between the microprocessor and the outside world.
- This can be done in groups of 8 bits using the entire data bus. This is called parallel I/O.
- The other method is serial I/O where one bit is transferred at a time using the SID and SOD pins on the Microprocessor.
- 8088/8086 architecture implements independent memory and input/output address spaces.
- Memory address space - 1,048,576 bytes long (1MB): 00000H – FFFFFH
- Input/output address space - 65,536 bytes long (64KB): 0000H – FFFFH
- I/O devices can be interfaced in two ways
  - Isolated mapped I/O
  - Memory mapped I/O

Isolated Input/Output

- It treats them separately from memory.
- I/O devices are assigned a “port number” within the 8-bit address range of 00H to FFH.
- The user in this case would access these devices using the IN and OUT instructions only.

Advantages of isolated I/O

- Complete memory address space available for use by memory.
- Special instructions have been provided in the instruction set of the 8086 to perform isolated I/O operation. This instructions tailored to maximize performance.

Disadvantage of Isolated I/O

- All inputs/outputs must take place between an I/O port and accumulator (AL or AX) register