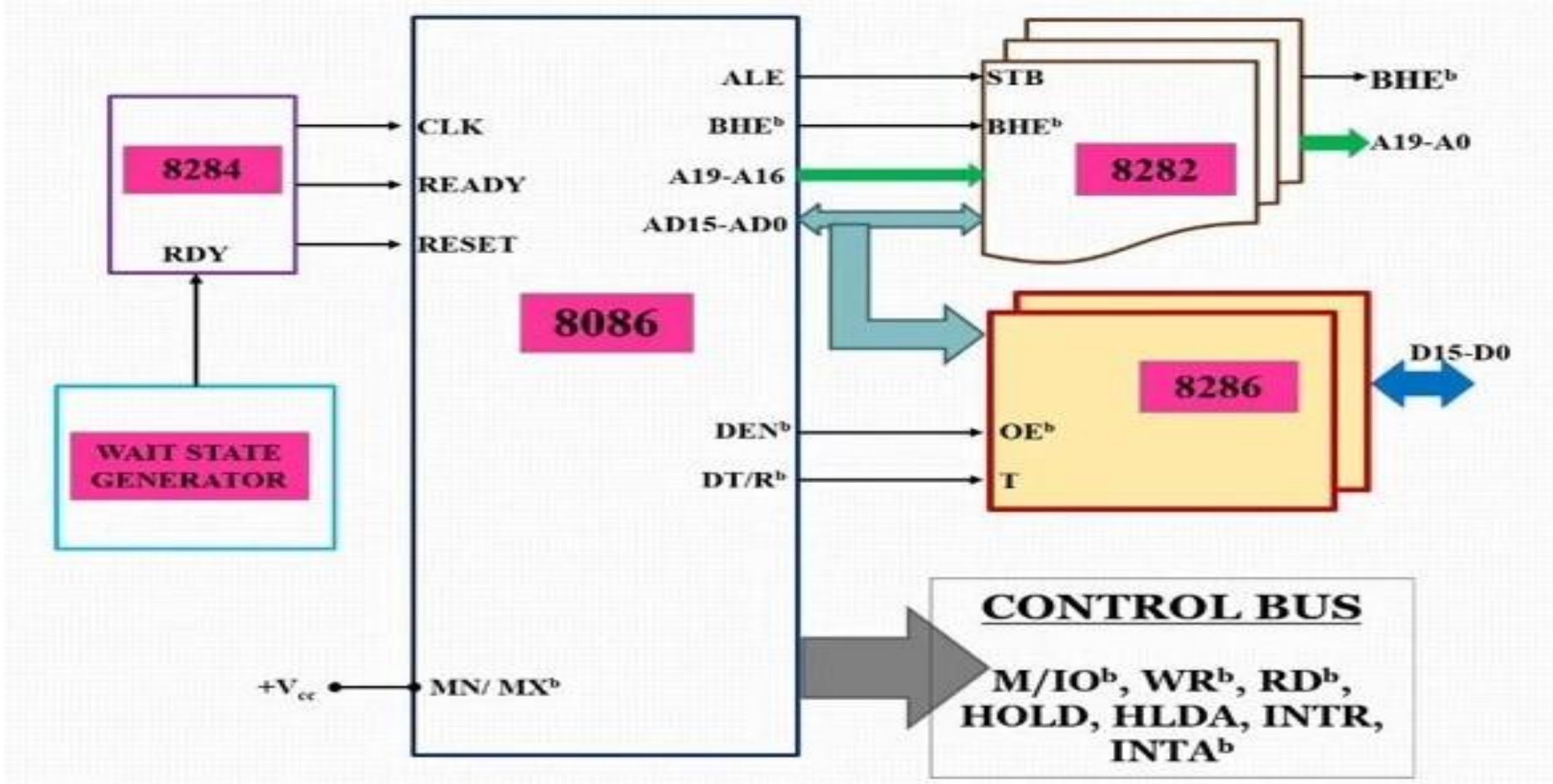
Minimum Mode and Maximum Mode of 8086 Microprocessor

The difference between minimum mode and maximum mode:

Minimum Mode	Maximum Mode
In minimum mode, there can be only one processor, i.e. 8086.	In maximum mode, there can be multiple processors with 8086, like 8087 and 8089.
Mn/Mx' is 1 to indicate minimum mode.	Mn/Mx' is 0 to indicate maximum mode.
ALE for the latch is given by 8086 as it is the only processor in the circuit.	ALE for the latch is given by 8288 bus controller as there can be multiple processors in the circuit.
DEN' and DT/R' for the trans-receivers are given by 8086 itself.	DT/R' for the trans-receivers are given by 8288 bus controller.
Direct control signals M/IO' , RD' and WR' are given by 8086.	Instead of control signals each processor generates status signals called S_2', S_1' and S_0'.

The difference between minimum mode and maximum mode:

Minimum Mode	Maximum Mode
Control signals M/IO’ , RD’ and WR’ are decoded by 3:8 decoder like 74138.	Status signals called S_2’, S_1’ and S_0’ are decoded by a bus controller like 8288 to produce control signals.
INTA’ is given by 8086 in response to an interrupt on INTR line.	INTA’ is given by bus controller 8288 in response to an interrupt on INTR line.
HOLD and HLDA signals are used for bus request with a DMA controller like 8237.	RQ’ or GT’ lines are used for bus request by other processors like 8087, 8089.
This circuit is simpler.	This circuit is more complex.
Performance is lower.	Performance is very high.


8284
RDY
WAIT STATE GENERATOR
CLK
READY
RESET
8086
ALE
BHE^b
A19-A16
AD15-AD0
DEN^b
DT/R^b
+V_cc
MN/ MX^b
STB
BHE^b
8282
BHE^b
A19-A0
8286
OE^b
T
D15-D0
CONTROL BUS
M/IO^b, WR^b, RD^b,
HOLD, HLDA, INTR,
INTA^b

- 8086 works in Minimum Mode, when $MN/\overline{MX} = 1$.
- The Minimum Mode is used for a small system with a single processor (8086) and in any system.
- 8086 itself generates all bus control signals in the minimum mode configuration of 8086.
- Clock is provided by the 8284 clock generator, it provides CLK, RESET and READY input to 8086.
- Address from the address bus is latched into 8282 8-bit latch. Three such latches are needed, as address bus is 20-bit. The ALE of 8086 is connected to STB of the latch. The ALE for this latch is given by 8086 itself.

- The data bus is driven through 8286 8-bit trans-receiver. Two such trans-receivers are needed, as the data bus is 16-bit. The trans-receivers are enabled through the $\overline{DEN}$ signal, while the direction of data is controlled by the DT/ $\overline{R}$ signal. $\overline{DEN}$ is connected to $\overline{OE}$ and DT/$\overline{R}$ is connected to T. Both $\overline{DEN}$ and DT/$\overline{R}$ are given by 8086 itself.

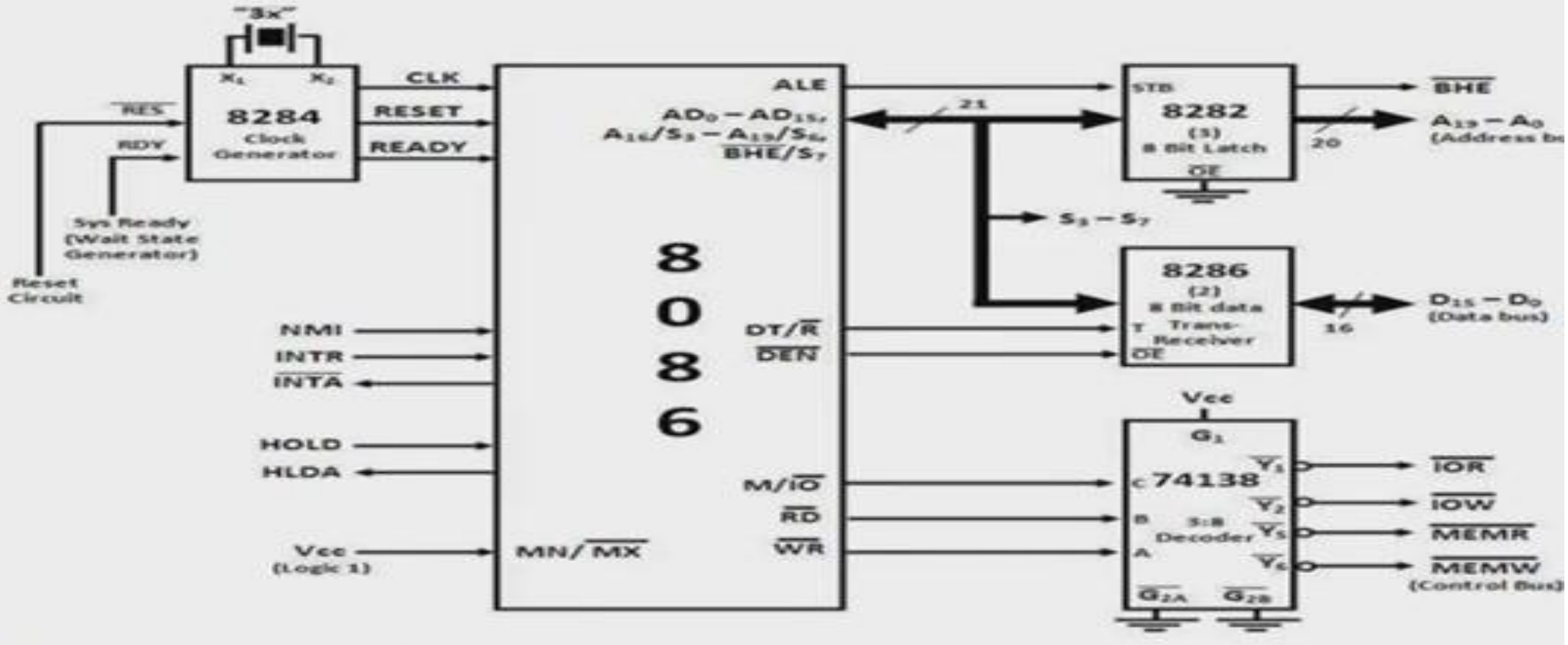
$\overline{DEN}$	DT/ $\overline{R}$	Action
1	X	Transreceiver is disabled
0	0	Receive data
0	1	Transmit data

- Minimum Mode, 8086 is the only processor in the system.
- Control signals for all operations are generated by decoding $M/\overline{IO}$, $\overline{RD}$ and $\overline{WR}$ signals.

$M/\overline{IO}$	$\overline{RD}$	$\overline{WR}$	Action
1	0	1	Memory Read
1	1	0	Memory Write
0	0	1	I/O Read
0	1	0	I/O Write

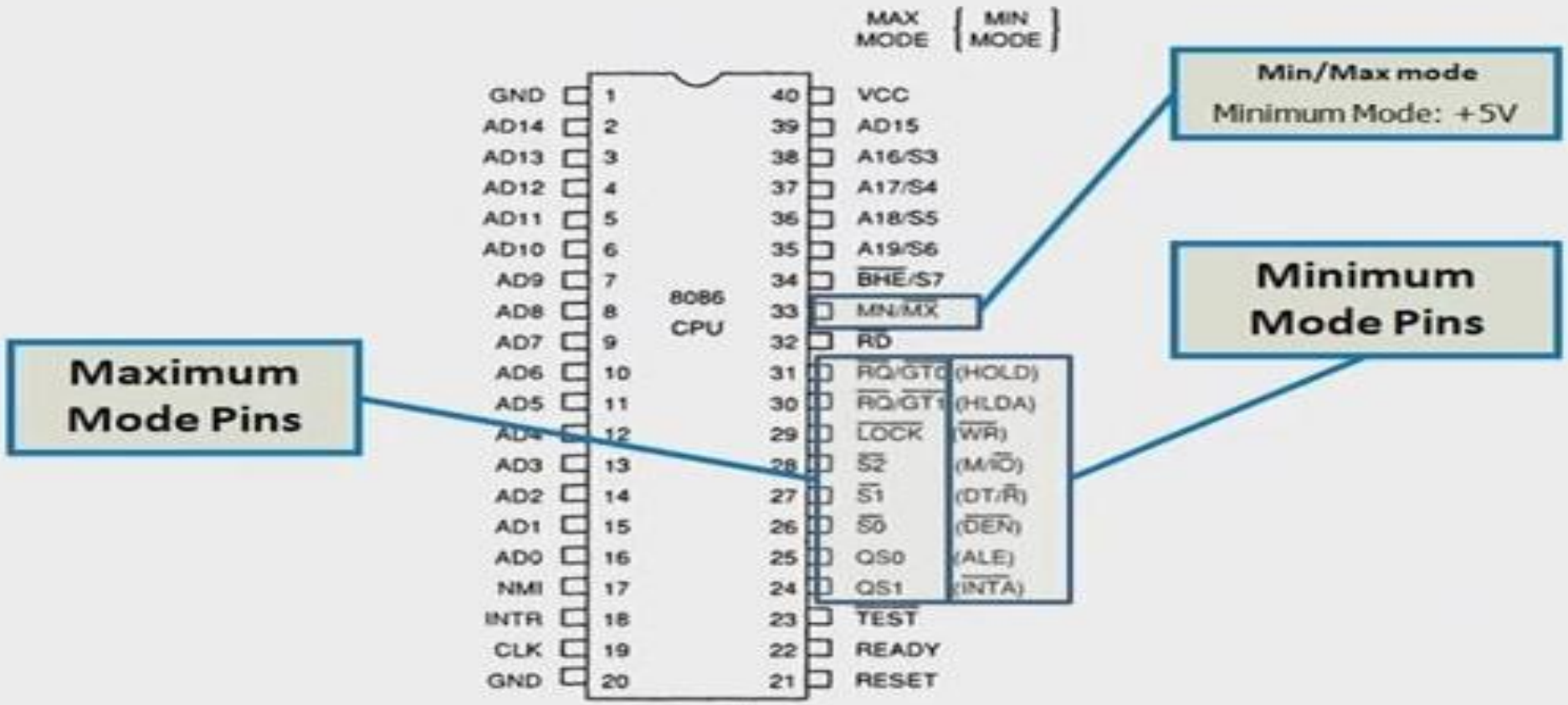
- $M/\overline{IO}$, $\overline{RD}$ and $\overline{WR}$ are decoded by a 3:8 decoder like IC 74138. Bus Request (DMA) is done using the HOLD and HLDA signals.
- $\overline{INTA}$ is given by 8086, in response to an interrupt on INTR line.

Minimum Mode 8086 System



INTEL 8086 - Pin Details

The microprocessor 8086 is operated in minimum mode by strapping to logic 1.



Minimum Mode Configuration of 8086:

- Pin definitions from 24 to 31 are different for minimum mode and maximum mode. By using these pins the 8086 itself generates all bus control signals in the Minimum Mode Configuration of 8086. These signals are:

Pin Definitions (24 to 31) in Minimum Mode:

- **INTA' (Interrupt Acknowledge) Output :** This indicates recognition of an interrupt request. It consists of two negative going pulses in two consecutive bus cycles. The first pulse informs the interface that its request has been recognized and upon receipt of the second pulse, the interface is to send the interrupt type to the processor over the data bus.

- **ALE (Address Latch Enable) output :** This signal is provided by 8086 to demultiplex the AD_0-AD_{15} into A_0-A_{15} and D_0-D_{15} using external latches.
- **DEN' (Data Enable) output :** This signal informs the transceivers that the CPU is ready to send or receive data.
- **DT/R' (Data transmit/Receive) output :** This signal is used to control data flow direction. High on this pin indicates that the 8086 is transmitting the data and low indicates that the 8086 is receiving the data.
- **M/IO' output :** It is used to distinguish memory data transfer, (M/I0 = HIGH) and I/O data transfer (M/I0 = LOW).

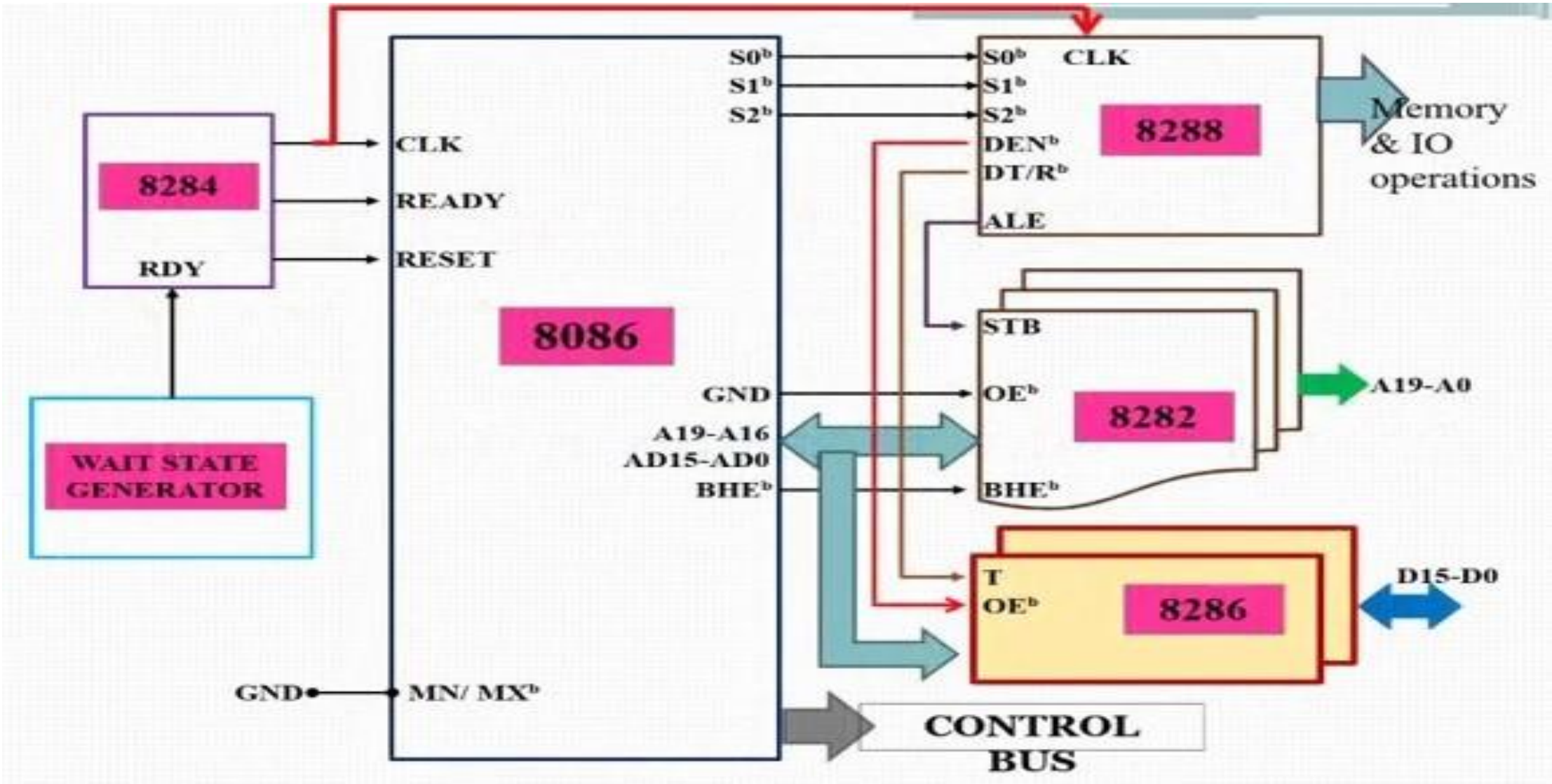
WR' : Write output : WR is low whenever the 8086 is writing data into memory or an I/O device.

HOLD input, HLDA output : A HIGH on HOLD pin indicates that another master (DMA) is requesting to take over the system bus. On receiving HOLD signal processor outputs HLDA signal HIGH as an acknowledgment. A low on HOLD gives the system bus control back to the processor. Processor then outputs low signal on HLDA.

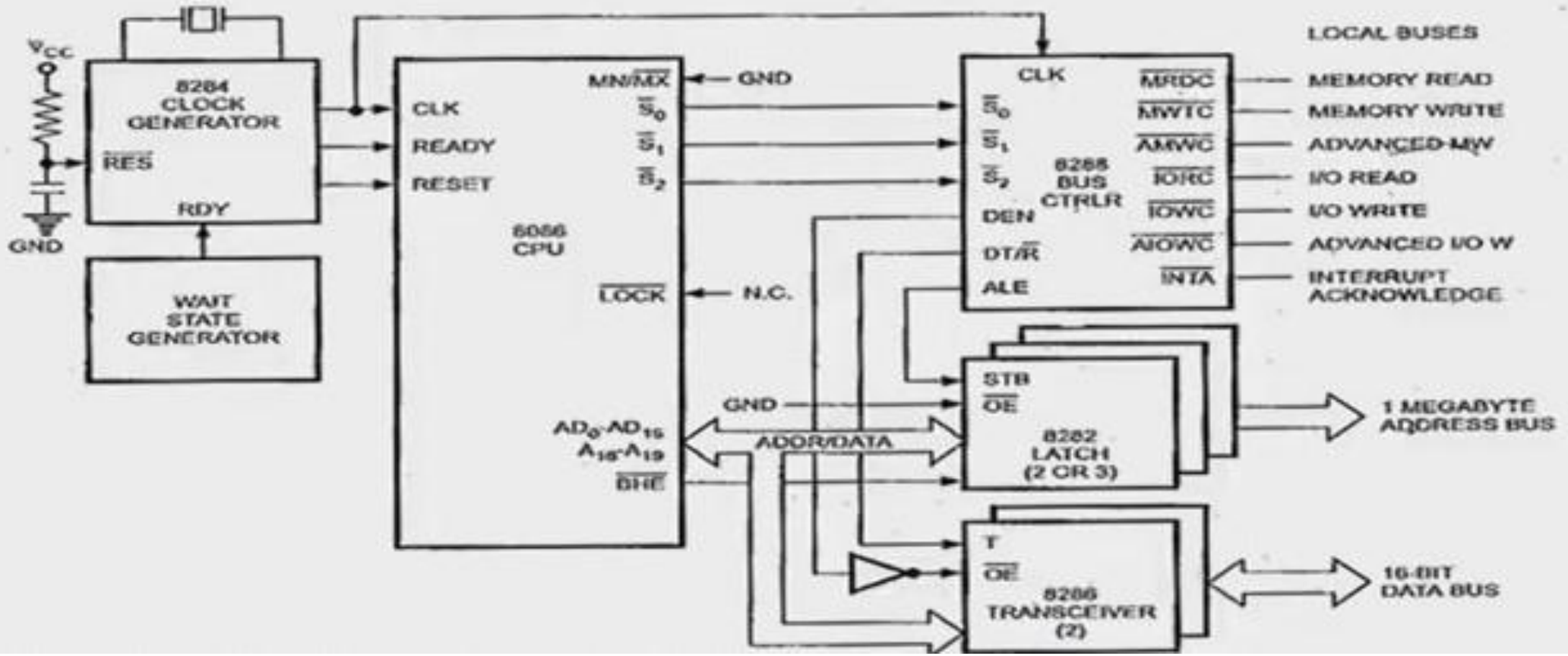
Maximum Mode 8086 System

When the pin 33 of the 8086 microprocessor is in the reset state, i.e. 0, then the **microprocessor functions in the Maximum Mode**.

- The maximum mode is for medium to large systems, which often use two or more processors.
- It also generates the control signals required to direct the data flow and for controlling 8282 latches and 8286 transceivers.
- The intel 8288 bus controller is used to implement this control circuitry.

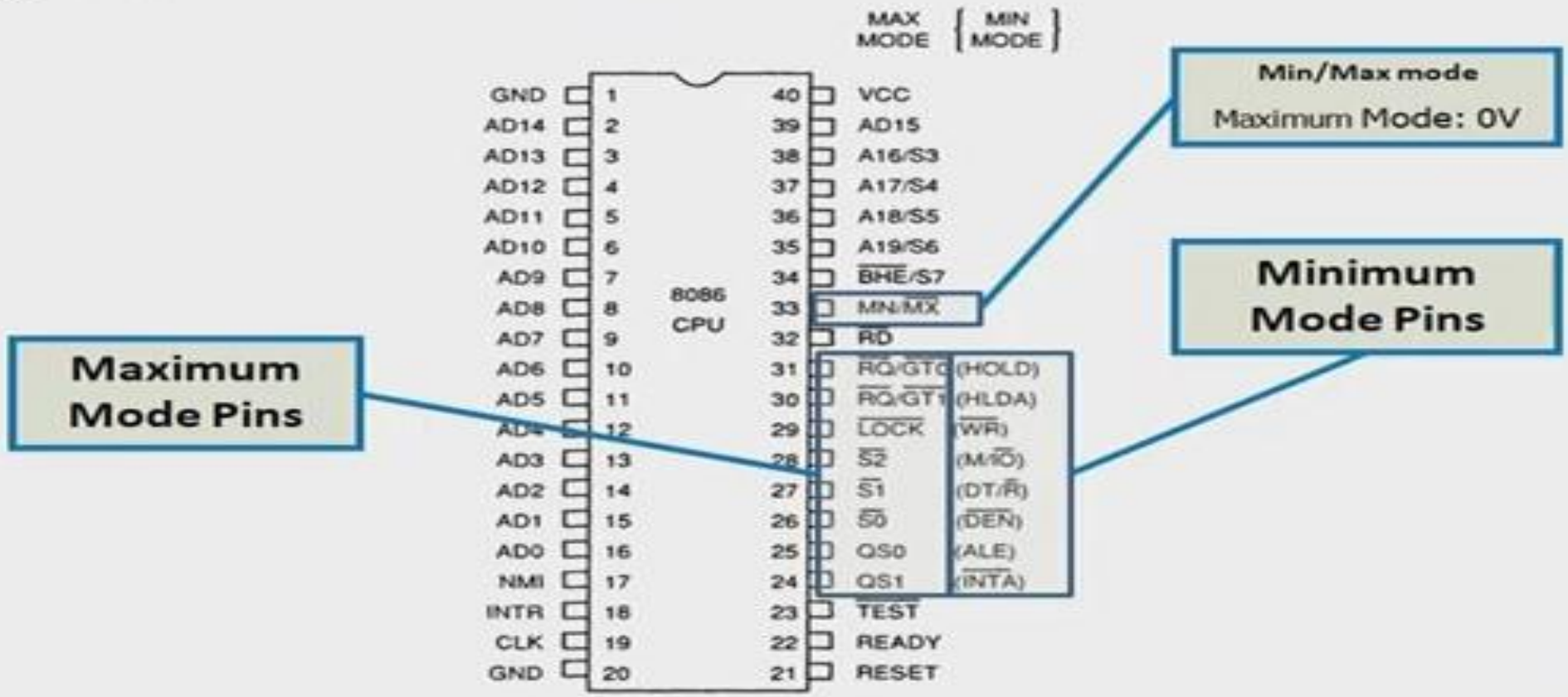

8284
RDY
WAIT STATE GENERATOR
CLK
READY
RESET
8086
GND
MN/ MX^b
S0^b
S1^b
S2^b
GND
A19-A16
AD15-AD0
BHE^b
S0^b
S1^b
S2^b
DEN^b
DT/R^b
ALE
CLK
8288
Memory & IO operations
STB
OE^b
8282
A19-A0
BHE^b
T
OE^b
8286
D15-D0
CONTROL BUS

Maximum Mode 8086 System



INTEL 8086 - Pin Details

The microprocessor 8086 is operated in maximum mode by strapping pin to logic 0.



Maximum Mode Configuration of 8086:

- Pin definitions from 24 to 31 are different for minimum mode and maximum mode. The pins form 24 to 31 are dedicated to these modes.. For maximum mode these signals are:

Pin Definitions (24 to 31) in Maximum Mode:

- **(RQ' / GT 0) and (RQ’ / GT 1):** These two pins are used for bus request and grant purpose. Through these pins, a connection is established between the external peripheral devices and the 8086 microprocessor. Among these two pins, the pin (RT / GT 0) has higher priority over (RT / GT 1).
- **LOCK’:** This pin is used to lock the internal buses of the microprocessor. When the control of buses is handed over to an external peripheral device, then the microprocessor is locked through this pin. It is an active low signal.

- **QS0 and QS1:** QS stands for Queue status, and as the name suggests, these two pins are used to tell the status of the queue. The status of the queue form the values of these pins is decided as follows:

QS1	QS0	Queue Status
0	0	No operation in queue
0	1	First byte form the instruction queue is fetched
1	0	Queue is empty
1	1	Subsequent byte from the instruction Queue is fetched

- **S2, S1 and S0:** Here, the S in each of these pins stands for Status. These three pins: S2, S1, and S0 together tell about the CPU cycle. The different of the values of these pins taken together tell about which CPU cycle is currently running.

S2	S1	S0	Current CPU Cycle Running
0	0	0	Interrupt Acknowledgement
0	0	1	Read from Input- Output devices
0	1	0	Write into Input- Output devices
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read from Memory
1	1	0	Write into Memory
1	1	1	Parsing Inactive

8288 Bus Controller: The 8288 bus controller is able to originate the address latch enable signal to the 8282's, the enable and direction signals to the 8286 transceivers, and the interrupt acknowledge signal to the interrupt controller. It also decodes the S_2-S_0 signals to generate MRDC, MWTC, IORC, IOWC, MCE/PDEN, AEN, IOB, CEN, AIOWC, and AMWC signals.

- **MRDC (M. Rd Comm) :** It instructs the memory to put the contents of the addressed location on the data bus.
- **MWTC (Memory Write Command) :** It instructs the memory to accept the data on the data bus and load the data into the addressed memory location.
- **IORC (I/O Rd Cm) :** It instructs an I/O device to put the data contained in the addressed port on the data bus.
- **IOWC (I/0 Write Command) :** It instructs an I/O device to accept the data on the data bus and load the data into the addressed port.

- **MCE/PDEN (Master Cascade Enable/Peripheral Data Enable):** It controls the mode of operation of 8259. It selects cascade operation for 8259 (interrupt controller) if IOB signal is grounded and enables the I/O bus transceivers if IOB is tied high.
- **AEN, IOB and CEN :** These pins are used in multiprocessor system. With a single processor in the system, AEN and IOB are grounded and CEN is tied high. AEN causes the 8288 to enable the memory control signals. IOB (I/O bus mode) signal selects either the I/O bus mode or system bus mode operation. CEN (control enable) input enables the command output pins on the 8288.
- **AIOWC/AMWC (Advance I/O Write Command/Advance Memory Write Command):** These signals are similar to IOWC and MWTC except that they are activated one clock pulse earlier. This gives slow interfaces an extra clock cycle to prepare to input the data.