

# Interfacing Memory with 8086

## Address decoding

- In general all the address lines are not used by the memory devices to select particular memory locations.
- The remaining line are used to generate chip select logic.
- Following two techniques are used to decode the address:
  - 1) Absolute or Full decoding
  - 2) Linear or Partial decoding

## Absolute or full decoding

- All the higher address lines are decoded to select the memory chip.
- The memory chip is selected only for the specified logic levels on these higher order address lines.
- So each location have fixed address.
- This technique is expensive
- It needs more hardware than partial decoding.

## **Partial or Linear Decoding**

- This technique is used in the small system
- All the address lines are not used to generate chip select logic
- Individual High order address lines are used to decode the chip select for the memory chips.
- Less hardware is required.
- Drawback is address of location is not fixed, so each location may have multiple address.

**Q. 1:** Interface 32 KB of RAM memory to the 8086 microprocessor system using absolute decoding with the suitable address.

**Step\_1:** Total RAM memory = 32 KB

Half RAM capacity = 16 KB

hence,

number of RAM IC required = 2 ICs of 16 KB

so,

**EVEN** Bank = 1 ICs of 16 KB RAM

**ODD** Bank = 1 ICs of 16 KB RAM

Even bank	Odd bank
<b>RAM _1 (16KB)</b>	<b>RAM _2 (16KB)</b>

**Step\_2:** Number of address lines required = 15 address lines

### Step\_3: Address decoding table

MEMOR Y IC	HEX ADDRESS	BINARY ADDRESS																		
		A 19	A 18	A 17	A 16	A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1
16 K x 8 RAM-(1)	00000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	07FFE	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0

To decoder                          To 16 K IC

RAM-2 <  
00001H  
07FFFH

**Q. 2:** Interface 32 K word of memory to the 8086 microprocessor system . Available memory chips are 16 K x 8 RAM. Use suitable decoder for generating chip select logic.

**Step\_1:** Total memory = 32 K word =  $32 * 2 \text{ K} = 64 \text{ K}$

IC available = 16 K

hence,

number of RAM IC required =  $64 \text{ K} \times 8 / 16 \text{ K} \times 8 = 4 \text{ ICs}$

so,

**EVEN** Bank = 2 ICs of 16 Kx8 RAM

**ODD** Bank = 2 ICs of 16 Kx8 RAM

Even bank	Odd bank
<b>RAM _1 (16K)</b>	<b>RAM _2 (16K)</b>
<b>RAM _3 (16K)</b>	<b>RAM _4 (16K)</b>

**Step\_2:** Number of address lines required = 15 address lines

### Step\_3: Address decoding table

MEMORY IC	HEX ADDRESS	BINARY ADDRESS																			
		A <sub>19</sub>	A <sub>18</sub>	A <sub>17</sub>	A <sub>16</sub>	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>12</sub>	A <sub>11</sub>	A <sub>10</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>
16 K x 8 RAM-(1)	00000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	07FFE	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
16 K x 8 RAM-(3)	08000	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0FFE	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

To decoder    To 16 K IC

**Q. 3:** Interface the following memory ICs with the 8086 microprocessor system in minimum mode configuration.

**ROM 4K-2 Numbers**

**EPROM 64K-1 Numbers**

**RAM 32K- 1Number . Use partial decoding.**

**Step\_1: Total ROM memory = 4 KB --- 2 ICs**

**EVEN Bank = 1 ICs of 4 KB ROM**

**ODD Bank = 1 ICs of 4 KB ROM**

**Total EPROM memory = 64 KB**

**EVEN Bank = 1 ICs of 32 KB EPROM**

**ODD Bank = 1 ICs of 32 KB EPROM**

**Total RAM memory = 64 KB**

**EVEN Bank = 1 ICs of 16 KB RAM**

**ODD Bank = 1 ICs of 16 KB RAM**

<b>Even bank</b>	<b>Odd bank</b>
<b>ROM _1 (4KB)</b>	<b>ROM _2 (4KB)</b>
<b>EPROM _1 (32KB)</b>	<b>EPROM _2 (32KB)</b>
<b>RAM _1 (16KB)</b>	<b>RAM _2 (16KB)</b>

Step 2:

Number of address lines required for ROM = 13 address lines

Number of address lines required for EPROM = 16 address lines

Number of address lines required for RAM = 15 address lines

### Step\_3: Address decoding table

MEMORY IC	HEX ADDRESS	BINARY ADDRESS																			
		A <sub>19</sub>	A <sub>18</sub>	A <sub>17</sub>	A <sub>16</sub>	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>12</sub>	A <sub>11</sub>	A <sub>10</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>
4 K x 8 ROM-(1)	<b>FFFFE</b>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
	<b>FE000</b>	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
32 K x 8 EPROM-(1)	<b>EFFFFE</b>	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
	<b>E0000</b>	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16 K x 8 RAM-(1)	<b>D0000</b>	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	<b>D7FFE</b>	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
					To decoder					To RAM IC											