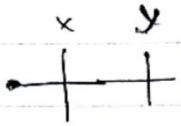
26977

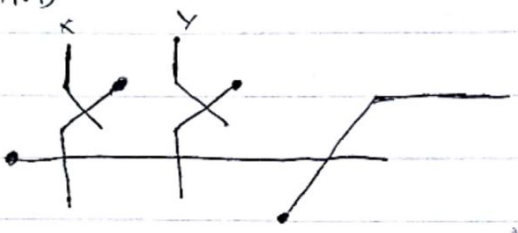
Pset 7

a) NOR



2 switches
t = 2t

b) NAND



5 switches

c) 3 way

3 switches time = 3t

d) DECODER

~~78 switches~~ 36 switches (counted from diagram)
~~time = 78t~~ time = 36 t

e) DEMUX

52 switches (counted from diagram)
time = 52t

f) MUX

61 switches (52 from DEMUX + 8 OR + 1 OR (additional)
hence 61

counted from diagram

~~Maj~~

g) MAJ switches = 26 counted from diagram
time = 26t

h) ODD switches = 23 counted from diagram
time = 23t

i) nbit adder adder consist of
both ODD and MAJ
hence 23 + 26
= 49 switches
time = 49t