Initialized B with 1
ashant@Ashant:~/ChampSim$ bin/champsim_ashant --warmup_instructions 200000
--simulation_instructions 5
00000 "traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 200000
Simulation Instructions: 500000
Number of CPUs: 1
Page size: 4096

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Warmup finished CPU 0 instructions: 200001 cycles: 64012 cumulative IPC: 3.124 (Simulation time: 00 hr 00 min 03 sec)
Warmup complete CPU 0 instructions: 200001 cycles: 64012 cumulative IPC: 3.124 (Simulation time: 00 hr 00 min 03 sec)
Simulation finished CPU 0 instructions: 500001 cycles: 389666 cumulative IPC: 1.283 (Simulation time: 00 hr 00 min 15 sec)
Simulation complete CPU 0 instructions: 500001 cycles: 389666 cumulative IPC: 1.283 (Simulation time: 00 hr 00 min 15 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics

CPU 0 cumulative IPC: 1.283 instructions: 500001 cycles: 389666
CPU 0 Branch Prediction Accuracy: 96.46% MPKI: 5.352 Average ROB Occupancy at Mispredict: 84.04
Branch type MPKI
BRANCH_DIRECT_JUMP: 0.102
BRANCH_INDIRECT: 0.028
BRANCH_CONDITIONAL: 5.018
BRANCH_DIRECT_CALL: 0.06
BRANCH_INDIRECT_CALL: 0.06
BRANCH_RETURN: 0.084

cpu0->cpu0_STLB TOTAL ACCESS: 475 HIT: 341 MISS: 134
MSHR_MERGE: 0

cpu0->cpu0_STLB LOAD ACCESS: 475 HIT: 341 MISS: 134 MSHR_MERGE: 0
cpu0->cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_STLB AVERAGE MISS LATENCY: 466.3 cycles
cpu0->cpu0_L2C TOTAL ACCESS: 946 HIT: 89 MISS: 857 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 764 HIT: 70 MISS: 694 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 32 HIT: 5 MISS: 27 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 12 HIT: 12 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 138 HIT: 2 MISS: 136 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 189.4 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 19617 HIT: 19312 MISS: 305 MSHR_MERGE: 33
cpu0->cpu0_L1I LOAD ACCESS: 19617 HIT: 19312 MISS: 305 MSHR_MERGE: 33
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: 178.7 cycles

cpu0->cpu0_L1D TOTAL ACCESS: 155830 HIT: 154589 MISS: 1241
MSHR_MERGE: 579
cpu0->cpu0_L1D LOAD ACCESS: 68426 HIT: 67491 MISS: 935
MSHR_MERGE: 443
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_L1D WRITE ACCESS: 87230 HIT: 87062 MISS: 168
MSHR_MERGE: 136
cpu0->cpu0_L1D TRANSLATION ACCESS: 174 HIT: 36 MISS: 138
MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
USELESS: 0
cpu0->cpu0_L1D AVERAGE MISS LATENCY: 184 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 18136 HIT: 18100 MISS: 36
MSHR_MERGE: 12
cpu0->cpu0_ITLB LOAD ACCESS: 18136 HIT: 18100 MISS: 36
MSHR_MERGE: 12
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: 268 cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 140124 HIT: 139425 MISS: 699
MSHR_MERGE: 248
cpu0->cpu0_DTLB LOAD ACCESS: 140124 HIT: 139425 MISS: 699
MSHR_MERGE: 248
cpu0->cpu0_DTLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0
MSHR_MERGE: 0
cpu0->cpu0_DTLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
USELESS: 0

cpu0->cpu0_DTLB AVERAGE MISS LATENCY: 129.9 cycles
cpu0->LLC TOTAL ACCESS: 857 HIT: 0 MISS: 857 MSHR_MERGE: 0
cpu0->LLC LOAD ACCESS: 694 HIT: 0 MISS: 694 MSHR_MERGE: 0
cpu0->LLC RFO ACCESS: 27 HIT: 0 MISS: 27 MSHR_MERGE: 0
cpu0->LLC PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC TRANSLATION ACCESS: 136 HIT: 0 MISS: 136 MSHR_MERGE: 0
cpu0->LLC PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->LLC AVERAGE MISS LATENCY: 173.4 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT: 5
ROW_BUFFER_MISS: 852
AVG DBUS CONGESTED CYCLE: 2.771
Channel 0 WQ ROW_BUFFER_HIT: 0
ROW_BUFFER_MISS: 0
FULL: 0
Channel 0 REFRESHES ISSUED: 32

Original perceptron

ashant@Ashant:~/ChampSim$ bin/champsim_perceptron --warmup_instructions 200000 --simulation_instructio
ns 500000 "traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 200000
Simulation Instructions: 500000
Number of CPUs: 1
Page size: 4096

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Warmup finished CPU 0 instructions: 200001 cycles: 64012 cumulative IPC: 3.124 (Simulation time: 00 hr 00 min 03 sec)
Warmup complete CPU 0 instructions: 200001 cycles: 64012 cumulative IPC: 3.124 (Simulation time: 00 hr 00 min 03 sec)
Simulation finished CPU 0 instructions: 500001 cycles: 370660 cumulative IPC: 1.349 (Simulation time: 00 hr 00 min 14 sec)

Simulation complete CPU 0 instructions: 500001 cycles: 370660 cumulative IPC: 1.349 (Simulation time: 00 hr 00 min 14 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics

CPU 0 cumulative IPC: 1.349 instructions: 500001 cycles: 370660
CPU 0 Branch Prediction Accuracy: 97.29% MPKI: 4.094 Average ROB Occupancy at Mispredict: 110.4
Branch type MPKI
BRANCH_DIRECT_JUMP: 0.102
BRANCH_INDIRECT: 0.028
BRANCH_CONDITIONAL: 3.76
BRANCH_DIRECT_CALL: 0.06
BRANCH_INDIRECT_CALL: 0.06
BRANCH_RETURN: 0.084

cpu0->cpu0_STLB TOTAL ACCESS: 473 HIT: 339 MISS: 134 MSHR_MERGE: 0
cpu0->cpu0_STLB LOAD ACCESS: 473 HIT: 339 MISS: 134 MSHR_MERGE: 0
cpu0->cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_STLB AVERAGE MISS LATENCY: 473.6 cycles
cpu0->cpu0_L2C TOTAL ACCESS: 946 HIT: 89 MISS: 857 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 764 HIT: 70 MISS: 694 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 32 HIT: 5 MISS: 27 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0

cpu0->cpu0_L2C WRITE ACCESS: 12 HIT: 12 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 138 HIT: 2 MISS: 136 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 192.7 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 21224 HIT: 20921 MISS: 303 MSHR_MERGE: 31
cpu0->cpu0_L1I LOAD ACCESS: 21224 HIT: 20921 MISS: 303 MSHR_MERGE: 31
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: 178.9 cycles
cpu0->cpu0_L1D TOTAL ACCESS: 154809 HIT: 153560 MISS: 1249 MSHR_MERGE: 587
cpu0->cpu0_L1D LOAD ACCESS: 67309 HIT: 66367 MISS: 942 MSHR_MERGE: 450
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D WRITE ACCESS: 87326 HIT: 87157 MISS: 169 MSHR_MERGE: 137
cpu0->cpu0_L1D TRANSLATION ACCESS: 174 HIT: 36 MISS: 138 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1D AVERAGE MISS LATENCY: 188.2 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 19592 HIT: 19556 MISS: 36 MSHR_MERGE: 12
cpu0->cpu0_ITLB LOAD ACCESS: 19592 HIT: 19556 MISS: 36 MSHR_MERGE: 12
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0

cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: 270.5 cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 139060 HIT: 138369 MISS: 691 MSHR_MERGE: 242
cpu0->cpu0_DTLB LOAD ACCESS: 139060 HIT: 138369 MISS: 691 MSHR_MERGE: 242
cpu0->cpu0_DTLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: 132.5 cycles
cpu0->LLC TOTAL ACCESS: 857 HIT: 0 MISS: 857 MSHR_MERGE: 0
cpu0->LLC LOAD ACCESS: 694 HIT: 0 MISS: 694 MSHR_MERGE: 0
cpu0->LLC RFO ACCESS: 27 HIT: 0 MISS: 27 MSHR_MERGE: 0
cpu0->LLC PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC TRANSLATION ACCESS: 136 HIT: 0 MISS: 136 MSHR_MERGE: 0
cpu0->LLC PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->LLC AVERAGE MISS LATENCY: 176.7 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT: 5
 ROW_BUFFER_MISS: 852
 AVG DBUS CONGESTED CYCLE: 2.745
Channel 0 WQ ROW_BUFFER_HIT: 0
 ROW_BUFFER_MISS: 0
 FULL: 0
Channel 0 REFRESHES ISSUED: 31

With B=0.5

```
ashant@Ashant:~/ChampSim$ bin/champsim_ashant --warmup_instructions 200000
--simulation_instructions 500000 "traces/ChampSim
Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 200000
Simulation Instructions: 500000
Number of CPUs: 1
Page size: 4096

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Warmup finished CPU 0 instructions: 200001 cycles: 64012 cumulative IPC: 3.124 (Simulation
time: 00 hr 00 min 04 sec)
Warmup complete CPU 0 instructions: 200001 cycles: 64012 cumulative IPC: 3.124 (Simulation
time: 00 hr 00 min 04 sec)
Simulation finished CPU 0 instructions: 500001 cycles: 389666 cumulative IPC: 1.283
(Simulation time: 00 hr 00 min 15 sec)
Simulation complete CPU 0 instructions: 500001 cycles: 389666 cumulative IPC: 1.283
(Simulation time: 00 hr 00 min 15 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics

CPU 0 cumulative IPC: 1.283 instructions: 500001 cycles: 389666
CPU 0 Branch Prediction Accuracy: 96.46% MPKI: 5.352 Average ROB Occupancy at
Mispredict: 84.04
Branch type MPKI
BRANCH_DIRECT_JUMP: 0.102
BRANCH_INDIRECT: 0.028
BRANCH_CONDITIONAL: 5.018
BRANCH_DIRECT_CALL: 0.06
BRANCH_INDIRECT_CALL: 0.06
BRANCH_RETURN: 0.084

cpu0->cpu0_STLB TOTAL        ACCESS:        475 HIT:        341 MISS:        134
MSHR_MERGE:          0
```

cpu0->cpu0_STLB LOAD ACCESS: 475 HIT: 341 MISS: 134 MSHR_MERGE: 0
cpu0->cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_STLB AVERAGE MISS LATENCY: 466.3 cycles
cpu0->cpu0_L2C TOTAL ACCESS: 946 HIT: 89 MISS: 857 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 764 HIT: 70 MISS: 694 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 32 HIT: 5 MISS: 27 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 12 HIT: 12 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 138 HIT: 2 MISS: 136 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 189.4 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 19617 HIT: 19312 MISS: 305 MSHR_MERGE: 33
cpu0->cpu0_L1I LOAD ACCESS: 19617 HIT: 19312 MISS: 305 MSHR_MERGE: 33
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: 178.7 cycles

cpu0->cpu0_L1D TOTAL ACCESS: 155830 HIT: 154589 MISS: 1241
MSHR_MERGE: 579
cpu0->cpu0_L1D LOAD ACCESS: 68426 HIT: 67491 MISS: 935
MSHR_MERGE: 443
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_L1D WRITE ACCESS: 87230 HIT: 87062 MISS: 168
MSHR_MERGE: 136
cpu0->cpu0_L1D TRANSLATION ACCESS: 174 HIT: 36 MISS: 138
MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
USELESS: 0
cpu0->cpu0_L1D AVERAGE MISS LATENCY: 184 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 18136 HIT: 18100 MISS: 36
MSHR_MERGE: 12
cpu0->cpu0_ITLB LOAD ACCESS: 18136 HIT: 18100 MISS: 36
MSHR_MERGE: 12
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: 268 cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 140124 HIT: 139425 MISS: 699
MSHR_MERGE: 248
cpu0->cpu0_DTLB LOAD ACCESS: 140124 HIT: 139425 MISS: 699
MSHR_MERGE: 248
cpu0->cpu0_DTLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0
MSHR_MERGE: 0
cpu0->cpu0_DTLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
USELESS: 0

```
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: 129.9 cycles
cpu0->LLC TOTAL        ACCESS:       857 HIT:         0 MISS:       857 MSHR_MERGE:         0
cpu0->LLC LOAD         ACCESS:       694 HIT:         0 MISS:       694 MSHR_MERGE:         0
cpu0->LLC RFO          ACCESS:        27 HIT:         0 MISS:        27 MSHR_MERGE:         0
cpu0->LLC PREFETCH     ACCESS:         0 HIT:         0 MISS:         0 MSHR_MERGE:         0
cpu0->LLC WRITE        ACCESS:         0 HIT:         0 MISS:         0 MSHR_MERGE:         0
cpu0->LLC TRANSLATION  ACCESS:       136 HIT:         0 MISS:       136 MSHR_MERGE:
0
cpu0->LLC PREFETCH REQUESTED:         0 ISSUED:         0 USEFUL:         0 USELESS:
0
cpu0->LLC AVERAGE MISS LATENCY: 173.4 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT:         5
  ROW_BUFFER_MISS:       852
  AVG DBUS CONGESTED CYCLE: 2.771
Channel 0 WQ ROW_BUFFER_HIT:         0
  ROW_BUFFER_MISS:         0
  FULL:         0
Channel 0 REFRESHES ISSUED:        32
ashant@Ashant:~/ChampSim$
```

With B=2

```
ashant@Ashant:~/ChampSim$ bin/champsim_ashant --warmup_instructions 2000000
--simulation_instructions
5000000 "traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 2000000
Simulation Instructions: 5000000
Number of CPUs: 1
Page size: 4096

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Warmup finished CPU 0 instructions: 2000000 cycles: 584938 cumulative IPC: 3.419
(Simulation time: 00 hr 00 min 32 sec)
Warmup complete CPU 0 instructions: 2000000 cycles: 584938 cumulative IPC: 3.419
(Simulation time: 00 hr 00 min 32 sec)
```

Simulation finished CPU 0 instructions: 5000004 cycles: 2753823 cumulative IPC: 1.816 (Simulation time: 00 hr 01 min 56 sec)
Simulation complete CPU 0 instructions: 5000004 cycles: 2753823 cumulative IPC: 1.816 (Simulation time: 00 hr 01 min 56 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics

CPU 0 cumulative IPC: 1.816 instructions: 5000004 cycles: 2753823
CPU 0 Branch Prediction Accuracy: 94.19% MPKI: 10.16 Average ROB Occupancy at Mispredict: 56.41
Branch type MPKI
BRANCH_DIRECT_JUMP: 0.1264
BRANCH_INDIRECT: 0.0238
BRANCH_CONDITIONAL: 9.996
BRANCH_DIRECT_CALL: 0.0064
BRANCH_INDIRECT_CALL: 0.0034
BRANCH_RETURN: 0.0066

cpu0->cpu0_STLB TOTAL ACCESS: 2474 HIT: 2365 MISS: 109 MSHR_MERGE: 0
cpu0->cpu0_STLB LOAD ACCESS: 2474 HIT: 2365 MISS: 109 MSHR_MERGE: 0
cpu0->cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_STLB AVERAGE MISS LATENCY: 424.3 cycles
cpu0->cpu0_L2C TOTAL ACCESS: 1458 HIT: 593 MISS: 865 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 1179 HIT: 470 MISS: 709 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 68 HIT: 9 MISS: 59 MSHR_MERGE: 0

cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 97 HIT: 97 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 114 HIT: 17 MISS: 97 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 192.1 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 73468 HIT: 73042 MISS: 426 MSHR_MERGE: 53
cpu0->cpu0_L1I LOAD ACCESS: 73468 HIT: 73042 MISS: 426 MSHR_MERGE: 53
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: 96.53 cycles
cpu0->cpu0_L1D TOTAL ACCESS: 1498378 HIT: 1496641 MISS: 1737 MSHR_MERGE: 749
cpu0->cpu0_L1D LOAD ACCESS: 782170 HIT: 780944 MISS: 1226 MSHR_MERGE: 420
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D WRITE ACCESS: 716087 HIT: 715690 MISS: 397 MSHR_MERGE: 329
cpu0->cpu0_L1D TRANSLATION ACCESS: 121 HIT: 7 MISS: 114 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1D AVERAGE MISS LATENCY: 143.3 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 64868 HIT: 64792 MISS: 76 MSHR_MERGE: 42
cpu0->cpu0_ITLB LOAD ACCESS: 64868 HIT: 64792 MISS: 76 MSHR_MERGE: 42

cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: 155 cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 1372826 HIT: 1369652 MISS: 3174 MSHR_MERGE: 734
cpu0->cpu0_DTLB LOAD ACCESS: 1372826 HIT: 1369652 MISS: 3174 MSHR_MERGE: 734
cpu0->cpu0_DTLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: 21.91 cycles
cpu0->LLC TOTAL ACCESS: 865 HIT: 0 MISS: 865 MSHR_MERGE: 0
cpu0->LLC LOAD ACCESS: 709 HIT: 0 MISS: 709 MSHR_MERGE: 0
cpu0->LLC RFO ACCESS: 59 HIT: 0 MISS: 59 MSHR_MERGE: 0
cpu0->LLC PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC TRANSLATION ACCESS: 97 HIT: 0 MISS: 97 MSHR_MERGE: 0
cpu0->LLC PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->LLC AVERAGE MISS LATENCY: 176.1 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT: 5
ROW_BUFFER_MISS: 860
AVG DBUS CONGESTED CYCLE: 2.717
Channel 0 WQ ROW_BUFFER_HIT: 0
ROW_BUFFER_MISS: 0

FULL: 0
Channel 0 REFRESHES ISSUED: 230
ashant@Ashant:~/ChampSim$

With B=0.05

Comparison based on 500,5000,50000,500000,500000,...., 500000000instructions on both ashant,perceptron

ashant@Ashant:~/ChampSim$ bin/champsim_ashant --warmup_instructions 200
--simulation_instructions 500
"traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 200
Simulation Instructions: 500
Number of CPUs: 1
Page size: 4096

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Warmup finished CPU 0 instructions: 204 cycles: 2309 cumulative IPC: 0.08835 (Simulation time: 00 hr 00 min 02 sec)
Warmup complete CPU 0 instructions: 204 cycles: 2309 cumulative IPC: 0.08835 (Simulation time: 00 hr 00 min 02 sec)
Simulation finished CPU 0 instructions: 501 cycles: 849 cumulative IPC: 0.5901 (Simulation time: 00 hr 00 min 02 sec)
Simulation complete CPU 0 instructions: 501 cycles: 849 cumulative IPC: 0.5901 (Simulation time: 00 hr 00 min 02 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics

CPU 0 cumulative IPC: 0.5901 instructions: 501 cycles: 849
CPU 0 Branch Prediction Accuracy: 73.68% MPKI: 9.98 Average ROB Occupancy at Mispredict: 205.2
Branch type MPKI

BRANCH_DIRECT_JUMP: 0
BRANCH_INDIRECT: 1.996
BRANCH_CONDITIONAL: 7.984
BRANCH_DIRECT_CALL: 0
BRANCH_INDIRECT_CALL: 0
BRANCH_RETURN: 0

cpu0->cpu0_STLB TOTAL ACCESS: 2 HIT: 0 MISS: 2 MSHR_MERGE: 0
cpu0->cpu0_STLB LOAD ACCESS: 2 HIT: 0 MISS: 2 MSHR_MERGE: 0
cpu0->cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_STLB AVERAGE MISS LATENCY: 410.8 cycles
cpu0->cpu0_L2C TOTAL ACCESS: 19 HIT: 0 MISS: 19 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 12 HIT: 0 MISS: 12 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 3 HIT: 0 MISS: 3 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 197 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 3 HIT: 3 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I LOAD ACCESS: 3 HIT: 3 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0

cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: - cycles
cpu0->cpu0_L1D TOTAL ACCESS: 139 HIT: 113 MISS: 26 MSHR_MERGE: 7
cpu0->cpu0_L1D LOAD ACCESS: 39 HIT: 23 MISS: 16 MSHR_MERGE: 4
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D WRITE ACCESS: 96 HIT: 90 MISS: 6 MSHR_MERGE: 3
cpu0->cpu0_L1D TRANSLATION ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1D AVERAGE MISS LATENCY: 206.4 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 3 HIT: 3 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB LOAD ACCESS: 3 HIT: 3 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: - cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 113 HIT: 108 MISS: 5 MSHR_MERGE: 3
cpu0->cpu0_DTLB LOAD ACCESS: 113 HIT: 108 MISS: 5 MSHR_MERGE: 3

```
cpu0->cpu0_DTLB RFO          ACCESS:          0 HIT:          0 MISS:          0 MSHR_MERGE:
0
cpu0->cpu0_DTLB PREFETCH     ACCESS:          0 HIT:          0 MISS:          0
MSHR_MERGE:          0
cpu0->cpu0_DTLB WRITE        ACCESS:          0 HIT:          0 MISS:          0 MSHR_MERGE:
0
cpu0->cpu0_DTLB TRANSLATION  ACCESS:          0 HIT:          0 MISS:          0
MSHR_MERGE:          0
cpu0->cpu0_DTLB PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:          0
USELESS:          0
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: 413.2 cycles
cpu0->LLC TOTAL        ACCESS:         18 HIT:          0 MISS:         18 MSHR_MERGE:          0
cpu0->LLC LOAD         ACCESS:         12 HIT:          0 MISS:         12 MSHR_MERGE:          0
cpu0->LLC RFO          ACCESS:          3 HIT:          0 MISS:          3 MSHR_MERGE:          0
cpu0->LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:          0 MSHR_MERGE:          0
cpu0->LLC WRITE        ACCESS:          0 HIT:          0 MISS:          0 MSHR_MERGE:          0
cpu0->LLC TRANSLATION  ACCESS:          3 HIT:          0 MISS:          3 MSHR_MERGE:
0
cpu0->LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:          0 USELESS:
0
cpu0->LLC AVERAGE MISS LATENCY: 181 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT:          0
  ROW_BUFFER_MISS:         18
  AVG DBUS CONGESTED CYCLE: 2.935
Channel 0 WQ ROW_BUFFER_HIT:          0
  ROW_BUFFER_MISS:          0
  FULL:          0
Channel 0 REFRESHES ISSUED: -
ashant@Ashant:~/ChampSim$ bin/champsim_perceptron --warmup_instructions 200
--simulation_instructions
500 "traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 200
Simulation Instructions: 500
Number of CPUs: 1
Page size: 4096
```

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Warmup finished CPU 0 instructions: 204 cycles: 2309 cumulative IPC: 0.08835 (Simulation time: 00 hr 00 min 00 sec)
Warmup complete CPU 0 instructions: 204 cycles: 2309 cumulative IPC: 0.08835 (Simulation time: 00 hr 00 min 00 sec)
Simulation finished CPU 0 instructions: 501 cycles: 849 cumulative IPC: 0.5901 (Simulation time: 00 hr 00 min 00 sec)
Simulation complete CPU 0 instructions: 501 cycles: 849 cumulative IPC: 0.5901 (Simulation time: 00 hr 00 min 00 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics

CPU 0 cumulative IPC: 0.5901 instructions: 501 cycles: 849
CPU 0 Branch Prediction Accuracy: 73.68% MPKI: 9.98 Average ROB Occupancy at Mispredict: 205.2
Branch type MPKI
BRANCH_DIRECT_JUMP: 0
BRANCH_INDIRECT: 1.996
BRANCH_CONDITIONAL: 7.984
BRANCH_DIRECT_CALL: 0
BRANCH_INDIRECT_CALL: 0
BRANCH_RETURN: 0

cpu0->cpu0_STLB TOTAL ACCESS: 2 HIT: 0 MISS: 2 MSHR_MERGE: 0
cpu0->cpu0_STLB LOAD ACCESS: 2 HIT: 0 MISS: 2 MSHR_MERGE: 0
cpu0->cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_STLB AVERAGE MISS LATENCY: 410.8 cycles

cpu0->cpu0_L2C TOTAL ACCESS: 19 HIT: 0 MISS: 19 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 12 HIT: 0 MISS: 12 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 3 HIT: 0 MISS: 3 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 197 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 3 HIT: 3 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I LOAD ACCESS: 3 HIT: 3 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: - cycles
cpu0->cpu0_L1D TOTAL ACCESS: 139 HIT: 113 MISS: 26 MSHR_MERGE: 7
cpu0->cpu0_L1D LOAD ACCESS: 39 HIT: 23 MISS: 16 MSHR_MERGE: 4
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D WRITE ACCESS: 96 HIT: 90 MISS: 6 MSHR_MERGE: 3
cpu0->cpu0_L1D TRANSLATION ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0

cpu0->cpu0_L1D AVERAGE MISS LATENCY: 206.4 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 3 HIT: 3 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB LOAD ACCESS: 3 HIT: 3 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: - cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 113 HIT: 108 MISS: 5 MSHR_MERGE: 3
cpu0->cpu0_DTLB LOAD ACCESS: 113 HIT: 108 MISS: 5 MSHR_MERGE: 3
cpu0->cpu0_DTLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: 413.2 cycles
cpu0->LLC TOTAL ACCESS: 18 HIT: 0 MISS: 18 MSHR_MERGE: 0
cpu0->LLC LOAD ACCESS: 12 HIT: 0 MISS: 12 MSHR_MERGE: 0
cpu0->LLC RFO ACCESS: 3 HIT: 0 MISS: 3 MSHR_MERGE: 0
cpu0->LLC PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC TRANSLATION ACCESS: 3 HIT: 0 MISS: 3 MSHR_MERGE: 0
cpu0->LLC PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->LLC AVERAGE MISS LATENCY: 181 cycles

DRAM Statistics

```
Channel 0 RQ ROW_BUFFER_HIT:          0
  ROW_BUFFER_MISS:         18
  AVG DBUS CONGESTED CYCLE: 2.935
Channel 0 WQ ROW_BUFFER_HIT:          0
  ROW_BUFFER_MISS:          0
  FULL:          0
Channel 0 REFRESHES ISSUED: -
ashant@Ashant:~/ChampSim$ bin/champsim_ashant --warmup_instructions 2000
--simulation_instructions 500
0 "traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 2000
Simulation Instructions: 5000
Number of CPUs: 1
Page size: 4096

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Warmup finished CPU 0 instructions: 2003 cycles: 3123 cumulative IPC: 0.6414 (Simulation
time: 00 hr 00 min 01 sec)
Warmup complete CPU 0 instructions: 2003 cycles: 3123 cumulative IPC: 0.6414 (Simulation
time: 00 hr 00 min 01 sec)
Simulation finished CPU 0 instructions: 5004 cycles: 2444 cumulative IPC: 2.047 (Simulation
time: 00 hr 00 min 01 sec)
Simulation complete CPU 0 instructions: 5004 cycles: 2444 cumulative IPC: 2.047 (Simulation
time: 00 hr 00 min 01 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics

CPU 0 cumulative IPC: 2.047 instructions: 5004 cycles: 2444
CPU 0 Branch Prediction Accuracy: 98.19% MPKI: 2.598 Average ROB Occupancy at
Mispredict: 152.9
Branch type MPKI
BRANCH_DIRECT_JUMP: 0
BRANCH_INDIRECT: 0
BRANCH_CONDITIONAL: 2.598
```

BRANCH_DIRECT_CALL: 0
BRANCH_INDIRECT_CALL: 0
BRANCH_RETURN: 0

cpu0->cpu0_L2C TOTAL ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 156.5 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 291 HIT: 291 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I LOAD ACCESS: 291 HIT: 291 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: - cycles
cpu0->cpu0_L1D TOTAL ACCESS: 1523 HIT: 1518 MISS: 5 MSHR_MERGE: 1
cpu0->cpu0_L1D LOAD ACCESS: 617 HIT: 612 MISS: 5 MSHR_MERGE: 1
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D WRITE ACCESS: 906 HIT: 906 MISS: 0 MSHR_MERGE: 0

cpu0->cpu0_L1D TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1D AVERAGE MISS LATENCY: 165.5 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 277 HIT: 277 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB LOAD ACCESS: 277 HIT: 277 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: - cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 1361 HIT: 1361 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB LOAD ACCESS: 1361 HIT: 1361 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: - cycles
cpu0->LLC TOTAL ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->LLC LOAD ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->LLC RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0

cpu0->LLC AVERAGE MISS LATENCY: 140.5 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT: 0
 ROW_BUFFER_MISS: 4
 AVG DBUS CONGESTED CYCLE: -
Channel 0 WQ ROW_BUFFER_HIT: 0
 ROW_BUFFER_MISS: 0
 FULL: 0
Channel 0 REFRESHES ISSUED: -
ashant@Ashant:~/ChampSim$ bin/champsim_perceptron --warmup_instructions 2000
--simulation_instructions
 5000 "traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 2000
Simulation Instructions: 5000
Number of CPUs: 1
Page size: 4096

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Warmup finished CPU 0 instructions: 2003 cycles: 3123 cumulative IPC: 0.6414 (Simulation
time: 00 hr 00 min 00 sec)
Warmup complete CPU 0 instructions: 2003 cycles: 3123 cumulative IPC: 0.6414 (Simulation
time: 00 hr 00 min 00 sec)
Simulation finished CPU 0 instructions: 5004 cycles: 2444 cumulative IPC: 2.047 (Simulation
time: 00 hr 00 min 01 sec)
Simulation complete CPU 0 instructions: 5004 cycles: 2444 cumulative IPC: 2.047 (Simulation
time: 00 hr 00 min 01 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics

CPU 0 cumulative IPC: 2.047 instructions: 5004 cycles: 2444
CPU 0 Branch Prediction Accuracy: 98.19% MPKI: 2.598 Average ROB Occupancy at
Mispredict: 152.9

Branch type MPKI
BRANCH_DIRECT_JUMP: 0
BRANCH_INDIRECT: 0
BRANCH_CONDITIONAL: 2.598
BRANCH_DIRECT_CALL: 0
BRANCH_INDIRECT_CALL: 0
BRANCH_RETURN: 0

cpu0->cpu0_L2C TOTAL ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 156.5 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 291 HIT: 291 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I LOAD ACCESS: 291 HIT: 291 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: - cycles
cpu0->cpu0_L1D TOTAL ACCESS: 1523 HIT: 1518 MISS: 5 MSHR_MERGE: 1
cpu0->cpu0_L1D LOAD ACCESS: 617 HIT: 612 MISS: 5 MSHR_MERGE: 1
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0

cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D WRITE ACCESS: 906 HIT: 906 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1D AVERAGE MISS LATENCY: 165.5 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 277 HIT: 277 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB LOAD ACCESS: 277 HIT: 277 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: - cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 1361 HIT: 1361 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB LOAD ACCESS: 1361 HIT: 1361 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: - cycles
cpu0->LLC TOTAL ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->LLC LOAD ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->LLC RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0

```
cpu0->LLC TRANSLATION  ACCESS:          0 HIT:          0 MISS:          0 MSHR_MERGE:
0
cpu0->LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:          0 USELESS:
0
cpu0->LLC AVERAGE MISS LATENCY: 140.5 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT:          0
  ROW_BUFFER_MISS:          4
  AVG DBUS CONGESTED CYCLE: -
Channel 0 WQ ROW_BUFFER_HIT:          0
  ROW_BUFFER_MISS:          0
  FULL:          0
Channel 0 REFRESHES ISSUED: -
ashant@Ashant:~/ChampSim$ bin/champsim_ashant --warmup_instructions 20000
--simulation_instructions 50
000 "traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 20000
Simulation Instructions: 50000
Number of CPUs: 1
Page size: 4096

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Warmup finished CPU 0 instructions: 20001 cycles: 8325 cumulative IPC: 2.403 (Simulation
time: 00 hr 00 min 01 sec)
Warmup complete CPU 0 instructions: 20001 cycles: 8325 cumulative IPC: 2.403 (Simulation
time: 00 hr 00 min 01 sec)
Simulation finished CPU 0 instructions: 50004 cycles: 60523 cumulative IPC: 0.8262
(Simulation time: 00 hr 00 min 02 sec)
Simulation complete CPU 0 instructions: 50004 cycles: 60523 cumulative IPC: 0.8262
(Simulation time: 00 hr 00 min 02 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics
```

CPU 0 cumulative IPC: 0.8262 instructions: 50004 cycles: 60523
CPU 0 Branch Prediction Accuracy: 95.66% MPKI: 6.399 Average ROB Occupancy at Mispredict: 61.84
Branch type MPKI
BRANCH_DIRECT_JUMP: 0.44
BRANCH_INDIRECT: 0.14
BRANCH_CONDITIONAL: 5.24
BRANCH_DIRECT_CALL: 0.14
BRANCH_INDIRECT_CALL: 0.16
BRANCH_RETURN: 0.28

cpu0->cpu0_STLB TOTAL ACCESS: 34 HIT: 1 MISS: 33 MSHR_MERGE: 0
cpu0->cpu0_STLB LOAD ACCESS: 34 HIT: 1 MISS: 33 MSHR_MERGE: 0
cpu0->cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_STLB AVERAGE MISS LATENCY: 487.9 cycles
cpu0->cpu0_L2C TOTAL ACCESS: 211 HIT: 0 MISS: 211 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 171 HIT: 0 MISS: 171 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 36 HIT: 0 MISS: 36 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 195.8 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 2671 HIT: 2559 MISS: 112 MSHR_MERGE: 8

cpu0->cpu0_L1I LOAD ACCESS: 2671 HIT: 2559 MISS: 112 MSHR_MERGE: 8
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: 203.6 cycles
cpu0->cpu0_L1D TOTAL ACCESS: 15515 HIT: 15386 MISS: 129 MSHR_MERGE: 22
cpu0->cpu0_L1D LOAD ACCESS: 6508 HIT: 6419 MISS: 89 MSHR_MERGE: 22
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D WRITE ACCESS: 8966 HIT: 8962 MISS: 4 MSHR_MERGE: 0
cpu0->cpu0_L1D TRANSLATION ACCESS: 41 HIT: 5 MISS: 36 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1D AVERAGE MISS LATENCY: 205.1 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 2518 HIT: 2497 MISS: 21 MSHR_MERGE: 5
cpu0->cpu0_ITLB LOAD ACCESS: 2518 HIT: 2497 MISS: 21 MSHR_MERGE: 5
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: 417.2 cycles

```
cpu0->cpu0_DTLB TOTAL        ACCESS:      13872 HIT:      13854 MISS:         18
MSHR_MERGE:         0
cpu0->cpu0_DTLB LOAD         ACCESS:      13872 HIT:      13854 MISS:         18
MSHR_MERGE:         0
cpu0->cpu0_DTLB RFO          ACCESS:          0 HIT:          0 MISS:          0 MSHR_MERGE:
0
cpu0->cpu0_DTLB PREFETCH     ACCESS:          0 HIT:          0 MISS:          0
MSHR_MERGE:         0
cpu0->cpu0_DTLB WRITE        ACCESS:          0 HIT:          0 MISS:          0 MSHR_MERGE:
0
cpu0->cpu0_DTLB TRANSLATION  ACCESS:          0 HIT:          0 MISS:          0
MSHR_MERGE:         0
cpu0->cpu0_DTLB PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:          0
USELESS:          0
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: 534.9 cycles
cpu0->LLC TOTAL        ACCESS:        211 HIT:          0 MISS:        211 MSHR_MERGE:          0
cpu0->LLC LOAD         ACCESS:        171 HIT:          0 MISS:        171 MSHR_MERGE:          0
cpu0->LLC RFO          ACCESS:          4 HIT:          0 MISS:          4 MSHR_MERGE:          0
cpu0->LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:          0 MSHR_MERGE:          0
cpu0->LLC WRITE        ACCESS:          0 HIT:          0 MISS:          0 MSHR_MERGE:          0
cpu0->LLC TRANSLATION  ACCESS:         36 HIT:          0 MISS:         36 MSHR_MERGE:
0
cpu0->LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:          0 USELESS:
0
cpu0->LLC AVERAGE MISS LATENCY: 179.8 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT:          0
  ROW_BUFFER_MISS:        211
  AVG DBUS CONGESTED CYCLE: 2.738
Channel 0 WQ ROW_BUFFER_HIT:          0
  ROW_BUFFER_MISS:          0
  FULL:          0
Channel 0 REFRESHES ISSUED:          5
ashant@Ashant:~/ChampSim$ bin/champsim_perceptron --warmup_instructions 20000
--simulation_instruction
s 50000 "traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 20000
```

Simulation Instructions: 50000
Number of CPUs: 1
Page size: 4096

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Warmup finished CPU 0 instructions: 20001 cycles: 8325 cumulative IPC: 2.403 (Simulation time: 00 hr 00 min 01 sec)
Warmup complete CPU 0 instructions: 20001 cycles: 8325 cumulative IPC: 2.403 (Simulation time: 00 hr 00 min 01 sec)
Simulation finished CPU 0 instructions: 50004 cycles: 60333 cumulative IPC: 0.8288 (Simulation time: 00 hr 00 min 02 sec)
Simulation complete CPU 0 instructions: 50004 cycles: 60333 cumulative IPC: 0.8288 (Simulation time: 00 hr 00 min 02 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics

CPU 0 cumulative IPC: 0.8288 instructions: 50004 cycles: 60333
CPU 0 Branch Prediction Accuracy: 95.65% MPKI: 6.419 Average ROB Occupancy at Mispredict: 62.47
Branch type MPKI
BRANCH_DIRECT_JUMP: 0.44
BRANCH_INDIRECT: 0.14
BRANCH_CONDITIONAL: 5.26
BRANCH_DIRECT_CALL: 0.14
BRANCH_INDIRECT_CALL: 0.16
BRANCH_RETURN: 0.28

cpu0->cpu0_STLB TOTAL ACCESS: 34 HIT: 1 MISS: 33 MSHR_MERGE: 0
cpu0->cpu0_STLB LOAD ACCESS: 34 HIT: 1 MISS: 33 MSHR_MERGE: 0
cpu0->cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0

cpu0->cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_STLB AVERAGE MISS LATENCY: 478.2 cycles
cpu0->cpu0_L2C TOTAL ACCESS: 211 HIT: 0 MISS: 211 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 171 HIT: 0 MISS: 171 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 36 HIT: 0 MISS: 36 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 192.1 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 2592 HIT: 2480 MISS: 112 MSHR_MERGE: 8
cpu0->cpu0_L1I LOAD ACCESS: 2592 HIT: 2480 MISS: 112 MSHR_MERGE: 8
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: 199.5 cycles
cpu0->cpu0_L1D TOTAL ACCESS: 15521 HIT: 15392 MISS: 129 MSHR_MERGE: 22
cpu0->cpu0_L1D LOAD ACCESS: 6513 HIT: 6424 MISS: 89 MSHR_MERGE: 22
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D WRITE ACCESS: 8967 HIT: 8963 MISS: 4 MSHR_MERGE: 0

cpu0->cpu0_L1D TRANSLATION ACCESS: 41 HIT: 5 MISS: 36 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1D AVERAGE MISS LATENCY: 201.7 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 2451 HIT: 2431 MISS: 20 MSHR_MERGE: 4
cpu0->cpu0_ITLB LOAD ACCESS: 2451 HIT: 2431 MISS: 20 MSHR_MERGE: 4
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: 385.9 cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 13879 HIT: 13861 MISS: 18 MSHR_MERGE: 0
cpu0->cpu0_DTLB LOAD ACCESS: 13879 HIT: 13861 MISS: 18 MSHR_MERGE: 0
cpu0->cpu0_DTLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: 545.1 cycles
cpu0->LLC TOTAL ACCESS: 211 HIT: 0 MISS: 211 MSHR_MERGE: 0
cpu0->LLC LOAD ACCESS: 171 HIT: 0 MISS: 171 MSHR_MERGE: 0
cpu0->LLC RFO ACCESS: 4 HIT: 0 MISS: 4 MSHR_MERGE: 0
cpu0->LLC PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC TRANSLATION ACCESS: 36 HIT: 0 MISS: 36 MSHR_MERGE: 0
cpu0->LLC PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0

cpu0->LLC AVERAGE MISS LATENCY: 176.1 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT: 0
 ROW_BUFFER_MISS: 211
 AVG DBUS CONGESTED CYCLE: 2.763
Channel 0 WQ ROW_BUFFER_HIT: 0
 ROW_BUFFER_MISS: 0
 FULL: 0
Channel 0 REFRESHES ISSUED: 5
ashant@Ashant:~/ChampSim$ bin/champsim_ashant --warmup_instructions 200000
--simulation_instructions 5
00000 "traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 200000
Simulation Instructions: 500000
Number of CPUs: 1
Page size: 4096

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Warmup finished CPU 0 instructions: 200001 cycles: 64012 cumulative IPC: 3.124 (Simulation
time: 00 hr 00 min 04 sec)
Warmup complete CPU 0 instructions: 200001 cycles: 64012 cumulative IPC: 3.124 (Simulation
time: 00 hr 00 min 04 sec)
Simulation finished CPU 0 instructions: 500001 cycles: 389666 cumulative IPC: 1.283
(Simulation time: 00 hr 00 min 14 sec)
Simulation complete CPU 0 instructions: 500001 cycles: 389666 cumulative IPC: 1.283
(Simulation time: 00 hr 00 min 14 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics

CPU 0 cumulative IPC: 1.283 instructions: 500001 cycles: 389666
CPU 0 Branch Prediction Accuracy: 96.46% MPKI: 5.352 Average ROB Occupancy at
Mispredict: 84.04

Branch type MPKI
BRANCH_DIRECT_JUMP: 0.102
BRANCH_INDIRECT: 0.028
BRANCH_CONDITIONAL: 5.018
BRANCH_DIRECT_CALL: 0.06
BRANCH_INDIRECT_CALL: 0.06
BRANCH_RETURN: 0.084

cpu0->cpu0_STLB TOTAL ACCESS: 475 HIT: 341 MISS: 134 MSHR_MERGE: 0
cpu0->cpu0_STLB LOAD ACCESS: 475 HIT: 341 MISS: 134 MSHR_MERGE: 0
cpu0->cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_STLB AVERAGE MISS LATENCY: 466.3 cycles
cpu0->cpu0_L2C TOTAL ACCESS: 946 HIT: 89 MISS: 857 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 764 HIT: 70 MISS: 694 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 32 HIT: 5 MISS: 27 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 12 HIT: 12 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 138 HIT: 2 MISS: 136 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 189.4 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 19617 HIT: 19312 MISS: 305 MSHR_MERGE: 33
cpu0->cpu0_L1I LOAD ACCESS: 19617 HIT: 19312 MISS: 305 MSHR_MERGE: 33
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0

cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: 178.7 cycles
cpu0->cpu0_L1D TOTAL ACCESS: 155830 HIT: 154589 MISS: 1241 MSHR_MERGE: 579
cpu0->cpu0_L1D LOAD ACCESS: 68426 HIT: 67491 MISS: 935 MSHR_MERGE: 443
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D WRITE ACCESS: 87230 HIT: 87062 MISS: 168 MSHR_MERGE: 136
cpu0->cpu0_L1D TRANSLATION ACCESS: 174 HIT: 36 MISS: 138 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1D AVERAGE MISS LATENCY: 184 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 18136 HIT: 18100 MISS: 36 MSHR_MERGE: 12
cpu0->cpu0_ITLB LOAD ACCESS: 18136 HIT: 18100 MISS: 36 MSHR_MERGE: 12
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: 268 cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 140124 HIT: 139425 MISS: 699 MSHR_MERGE: 248
cpu0->cpu0_DTLB LOAD ACCESS: 140124 HIT: 139425 MISS: 699 MSHR_MERGE: 248

```
cpu0->cpu0_DTLB RFO          ACCESS:          0 HIT:          0 MISS:          0 MSHR_MERGE:
0
cpu0->cpu0_DTLB PREFETCH     ACCESS:          0 HIT:          0 MISS:          0
MSHR_MERGE:          0
cpu0->cpu0_DTLB WRITE        ACCESS:          0 HIT:          0 MISS:          0 MSHR_MERGE:
0
cpu0->cpu0_DTLB TRANSLATION  ACCESS:          0 HIT:          0 MISS:          0
MSHR_MERGE:          0
cpu0->cpu0_DTLB PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:          0
USELESS:          0
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: 129.9 cycles
cpu0->LLC TOTAL        ACCESS:        857 HIT:          0 MISS:        857 MSHR_MERGE:          0
cpu0->LLC LOAD         ACCESS:        694 HIT:          0 MISS:        694 MSHR_MERGE:          0
cpu0->LLC RFO          ACCESS:         27 HIT:          0 MISS:         27 MSHR_MERGE:          0
cpu0->LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:          0 MSHR_MERGE:          0
cpu0->LLC WRITE        ACCESS:          0 HIT:          0 MISS:          0 MSHR_MERGE:          0
cpu0->LLC TRANSLATION  ACCESS:        136 HIT:          0 MISS:        136 MSHR_MERGE:
0
cpu0->LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:          0 USELESS:
0
cpu0->LLC AVERAGE MISS LATENCY: 173.4 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT:          5
  ROW_BUFFER_MISS:        852
  AVG DBUS CONGESTED CYCLE: 2.771
Channel 0 WQ ROW_BUFFER_HIT:          0
  ROW_BUFFER_MISS:          0
  FULL:          0
Channel 0 REFRESHES ISSUED:         32
ashant@Ashant:~/ChampSim$ bin/champsim_perceptron --warmup_instructions 200000
--simulation_instructio
ns 500000 "traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 200000
Simulation Instructions: 500000
Number of CPUs: 1
Page size: 4096
```

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Warmup finished CPU 0 instructions: 200001 cycles: 64012 cumulative IPC: 3.124 (Simulation time: 00 hr 00 min 04 sec)
Warmup complete CPU 0 instructions: 200001 cycles: 64012 cumulative IPC: 3.124 (Simulation time: 00 hr 00 min 04 sec)
Simulation finished CPU 0 instructions: 500001 cycles: 370660 cumulative IPC: 1.349 (Simulation time: 00 hr 00 min 15 sec)
Simulation complete CPU 0 instructions: 500001 cycles: 370660 cumulative IPC: 1.349 (Simulation time: 00 hr 00 min 15 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics

CPU 0 cumulative IPC: 1.349 instructions: 500001 cycles: 370660
CPU 0 Branch Prediction Accuracy: 97.29% MPKI: 4.094 Average ROB Occupancy at Mispredict: 110.4
Branch type MPKI
BRANCH_DIRECT_JUMP: 0.102
BRANCH_INDIRECT: 0.028
BRANCH_CONDITIONAL: 3.76
BRANCH_DIRECT_CALL: 0.06
BRANCH_INDIRECT_CALL: 0.06
BRANCH_RETURN: 0.084

cpu0->cpu0_STLB TOTAL ACCESS: 473 HIT: 339 MISS: 134 MSHR_MERGE: 0
cpu0->cpu0_STLB LOAD ACCESS: 473 HIT: 339 MISS: 134 MSHR_MERGE: 0
cpu0->cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_STLB AVERAGE MISS LATENCY: 473.6 cycles

cpu0->cpu0_L2C TOTAL ACCESS: 946 HIT: 89 MISS: 857 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 764 HIT: 70 MISS: 694 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 32 HIT: 5 MISS: 27 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 12 HIT: 12 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 138 HIT: 2 MISS: 136 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 192.7 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 21224 HIT: 20921 MISS: 303 MSHR_MERGE: 31
cpu0->cpu0_L1I LOAD ACCESS: 21224 HIT: 20921 MISS: 303 MSHR_MERGE: 31
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: 178.9 cycles
cpu0->cpu0_L1D TOTAL ACCESS: 154809 HIT: 153560 MISS: 1249 MSHR_MERGE: 587
cpu0->cpu0_L1D LOAD ACCESS: 67309 HIT: 66367 MISS: 942 MSHR_MERGE: 450
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D WRITE ACCESS: 87326 HIT: 87157 MISS: 169 MSHR_MERGE: 137
cpu0->cpu0_L1D TRANSLATION ACCESS: 174 HIT: 36 MISS: 138 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0

cpu0->cpu0_L1D AVERAGE MISS LATENCY: 188.2 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 19592 HIT: 19556 MISS: 36 MSHR_MERGE: 12
cpu0->cpu0_ITLB LOAD ACCESS: 19592 HIT: 19556 MISS: 36 MSHR_MERGE: 12
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: 270.5 cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 139060 HIT: 138369 MISS: 691 MSHR_MERGE: 242
cpu0->cpu0_DTLB LOAD ACCESS: 139060 HIT: 138369 MISS: 691 MSHR_MERGE: 242
cpu0->cpu0_DTLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: 132.5 cycles
cpu0->LLC TOTAL ACCESS: 857 HIT: 0 MISS: 857 MSHR_MERGE: 0
cpu0->LLC LOAD ACCESS: 694 HIT: 0 MISS: 694 MSHR_MERGE: 0
cpu0->LLC RFO ACCESS: 27 HIT: 0 MISS: 27 MSHR_MERGE: 0
cpu0->LLC PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC TRANSLATION ACCESS: 136 HIT: 0 MISS: 136 MSHR_MERGE: 0
cpu0->LLC PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->LLC AVERAGE MISS LATENCY: 176.7 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT: 5
 ROW_BUFFER_MISS: 852
 AVG DBUS CONGESTED CYCLE: 2.745
Channel 0 WQ ROW_BUFFER_HIT: 0
 ROW_BUFFER_MISS: 0
 FULL: 0
Channel 0 REFRESHES ISSUED: 31
ashant@Ashant:~/ChampSim$ bin/champsim_ashant --warmup_instructions 2000000
--simulation_instructions
5000000 "traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 2000000
Simulation Instructions: 5000000
Number of CPUs: 1
Page size: 4096

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Warmup finished CPU 0 instructions: 2000000 cycles: 584938 cumulative IPC: 3.419
(Simulation time: 00 hr 00 min 29 sec)
Warmup complete CPU 0 instructions: 2000000 cycles: 584938 cumulative IPC: 3.419
(Simulation time: 00 hr 00 min 29 sec)
Simulation finished CPU 0 instructions: 5000004 cycles: 2753823 cumulative IPC: 1.816
(Simulation time: 00 hr 01 min 51 sec)
Simulation complete CPU 0 instructions: 5000004 cycles: 2753823 cumulative IPC: 1.816
(Simulation time: 00 hr 01 min 51 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics

CPU 0 cumulative IPC: 1.816 instructions: 5000004 cycles: 2753823
CPU 0 Branch Prediction Accuracy: 94.19% MPKI: 10.16 Average ROB Occupancy at
Mispredict: 56.41
Branch type MPKI
BRANCH_DIRECT_JUMP: 0.1264
BRANCH_INDIRECT: 0.0238
BRANCH_CONDITIONAL: 9.996

BRANCH_DIRECT_CALL: 0.0064
BRANCH_INDIRECT_CALL: 0.0034
BRANCH_RETURN: 0.0066

cpu0->cpu0_STLB TOTAL ACCESS: 2474 HIT: 2365 MISS: 109 MSHR_MERGE: 0
cpu0->cpu0_STLB LOAD ACCESS: 2474 HIT: 2365 MISS: 109 MSHR_MERGE: 0
cpu0->cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_STLB AVERAGE MISS LATENCY: 424.3 cycles
cpu0->cpu0_L2C TOTAL ACCESS: 1458 HIT: 593 MISS: 865 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 1179 HIT: 470 MISS: 709 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 68 HIT: 9 MISS: 59 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 97 HIT: 97 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 114 HIT: 17 MISS: 97 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 192.1 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 73468 HIT: 73042 MISS: 426 MSHR_MERGE: 53
cpu0->cpu0_L1I LOAD ACCESS: 73468 HIT: 73042 MISS: 426 MSHR_MERGE: 53
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0

cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: 96.53 cycles
cpu0->cpu0_L1D TOTAL ACCESS: 1498378 HIT: 1496641 MISS: 1737
MSHR_MERGE: 749
cpu0->cpu0_L1D LOAD ACCESS: 782170 HIT: 780944 MISS: 1226
MSHR_MERGE: 420
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_L1D WRITE ACCESS: 716087 HIT: 715690 MISS: 397
MSHR_MERGE: 329
cpu0->cpu0_L1D TRANSLATION ACCESS: 121 HIT: 7 MISS: 114
MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
USELESS: 0
cpu0->cpu0_L1D AVERAGE MISS LATENCY: 143.3 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 64868 HIT: 64792 MISS: 76
MSHR_MERGE: 42
cpu0->cpu0_ITLB LOAD ACCESS: 64868 HIT: 64792 MISS: 76
MSHR_MERGE: 42
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: 155 cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 1372826 HIT: 1369652 MISS: 3174
MSHR_MERGE: 734
cpu0->cpu0_DTLB LOAD ACCESS: 1372826 HIT: 1369652 MISS: 3174
MSHR_MERGE: 734
cpu0->cpu0_DTLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0
MSHR_MERGE: 0

cpu0->cpu0_DTLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: 21.91 cycles
cpu0->LLC TOTAL ACCESS: 865 HIT: 0 MISS: 865 MSHR_MERGE: 0
cpu0->LLC LOAD ACCESS: 709 HIT: 0 MISS: 709 MSHR_MERGE: 0
cpu0->LLC RFO ACCESS: 59 HIT: 0 MISS: 59 MSHR_MERGE: 0
cpu0->LLC PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC TRANSLATION ACCESS: 97 HIT: 0 MISS: 97 MSHR_MERGE: 0
cpu0->LLC PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->LLC AVERAGE MISS LATENCY: 176.1 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT: 5
 ROW_BUFFER_MISS: 860
 AVG DBUS CONGESTED CYCLE: 2.717
Channel 0 WQ ROW_BUFFER_HIT: 0
 ROW_BUFFER_MISS: 0
 FULL: 0
Channel 0 REFRESHES ISSUED: 230
ashant@Ashant:~/ChampSim$ bin/champsim_perceptron --warmup_instructions 2000000 --simulation_instructi
ons 5000000 "traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 2000000
Simulation Instructions: 5000000
Number of CPUs: 1
Page size: 4096

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Warmup finished CPU 0 instructions: 2000000 cycles: 584918 cumulative IPC: 3.419
(Simulation time: 00 hr 00 min 29 sec)

Warmup complete CPU 0 instructions: 2000000 cycles: 584918 cumulative IPC: 3.419 (Simulation time: 00 hr 00 min 29 sec)
Simulation finished CPU 0 instructions: 5000004 cycles: 2332853 cumulative IPC: 2.143 (Simulation time: 00 hr 01 min 46 sec)
Simulation complete CPU 0 instructions: 5000004 cycles: 2332853 cumulative IPC: 2.143 (Simulation time: 00 hr 01 min 46 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics

CPU 0 cumulative IPC: 2.143 instructions: 5000004 cycles: 2332853
CPU 0 Branch Prediction Accuracy: 97.48% MPKI: 4.41 Average ROB Occupancy at Mispredict: 109.1
Branch type MPKI
BRANCH_DIRECT_JUMP: 0.1264
BRANCH_INDIRECT: 0.0238
BRANCH_CONDITIONAL: 4.243
BRANCH_DIRECT_CALL: 0.0064
BRANCH_INDIRECT_CALL: 0.0034
BRANCH_RETURN: 0.0066

cpu0->cpu0_STLB TOTAL ACCESS: 2453 HIT: 2344 MISS: 109 MSHR_MERGE: 0
cpu0->cpu0_STLB LOAD ACCESS: 2453 HIT: 2344 MISS: 109 MSHR_MERGE: 0
cpu0->cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_STLB AVERAGE MISS LATENCY: 414.5 cycles
cpu0->cpu0_L2C TOTAL ACCESS: 1452 HIT: 587 MISS: 865 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 1175 HIT: 466 MISS: 709 MSHR_MERGE: 0

cpu0->cpu0_L2C RFO ACCESS: 68 HIT: 9 MISS: 59 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 95 HIT: 95 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 114 HIT: 17 MISS: 97 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 191 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 128194 HIT: 127764 MISS: 430 MSHR_MERGE: 60
cpu0->cpu0_L1I LOAD ACCESS: 128194 HIT: 127764 MISS: 430 MSHR_MERGE: 60
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: 94.84 cycles
cpu0->cpu0_L1D TOTAL ACCESS: 1441234 HIT: 1439466 MISS: 1768 MSHR_MERGE: 781
cpu0->cpu0_L1D LOAD ACCESS: 730810 HIT: 729553 MISS: 1257 MSHR_MERGE: 452
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D WRITE ACCESS: 710303 HIT: 709906 MISS: 397 MSHR_MERGE: 329
cpu0->cpu0_L1D TRANSLATION ACCESS: 121 HIT: 7 MISS: 114 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1D AVERAGE MISS LATENCY: 143.3 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 113616 HIT: 113532 MISS: 84 MSHR_MERGE: 50

cpu0->cpu0_ITLB LOAD ACCESS: 113616 HIT: 113532 MISS: 84 MSHR_MERGE: 50
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: 130.9 cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 1304663 HIT: 1301430 MISS: 3233 MSHR_MERGE: 814
cpu0->cpu0_DTLB LOAD ACCESS: 1304663 HIT: 1301430 MISS: 3233 MSHR_MERGE: 814
cpu0->cpu0_DTLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: 21.96 cycles
cpu0->LLC TOTAL ACCESS: 865 HIT: 0 MISS: 865 MSHR_MERGE: 0
cpu0->LLC LOAD ACCESS: 709 HIT: 0 MISS: 709 MSHR_MERGE: 0
cpu0->LLC RFO ACCESS: 59 HIT: 0 MISS: 59 MSHR_MERGE: 0
cpu0->LLC PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC TRANSLATION ACCESS: 97 HIT: 0 MISS: 97 MSHR_MERGE: 0
cpu0->LLC PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->LLC AVERAGE MISS LATENCY: 175 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT: 4
 ROW_BUFFER_MISS: 861
 AVG DBUS CONGESTED CYCLE: 2.701

```
Channel 0 WQ ROW_BUFFER_HIT:          0
  ROW_BUFFER_MISS:          0
  FULL:          0
Channel 0 REFRESHES ISSUED:        195
ashant@Ashant:~/ChampSim$ bin/champsim_perceptron --warmup_instructions 20000000
--simulation_instruct
ions 50000000 "traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 20000000
Simulation Instructions: 50000000
Number of CPUs: 1
Page size: 4096

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Heartbeat CPU 0 instructions: 10000002 cycles: 2792634 heartbeat IPC: 3.581 cumulative IPC:
3.581 (Simulation time: 00 hr 02 min 19 sec)
Warmup finished CPU 0 instructions: 20000000 cycles: 5644725 cumulative IPC: 3.543
(Simulation time: 00 hr 04 min 42 sec)
Warmup complete CPU 0 instructions: 20000000 cycles: 5644725 cumulative IPC: 3.543
(Simulation time: 00 hr 04 min 42 sec)
Heartbeat CPU 0 instructions: 20000004 cycles: 5644726 heartbeat IPC: 3.506 cumulative IPC:
4 (Simulation time: 00 hr 04 min 42 sec)
Heartbeat CPU 0 instructions: 30000004 cycles: 9589808 heartbeat IPC: 2.535 cumulative IPC:
2.535 (Simulation time: 00 hr 07 min 16 sec)
Heartbeat CPU 0 instructions: 40000008 cycles: 13915696 heartbeat IPC: 2.312 cumulative
IPC: 2.418 (Simulation time: 00 hr 09 min 49 sec)
Heartbeat CPU 0 instructions: 50000008 cycles: 18146308 heartbeat IPC: 2.364 cumulative
IPC: 2.4 (Simulation time: 00 hr 12 min 21 sec)
Heartbeat CPU 0 instructions: 60000009 cycles: 22638280 heartbeat IPC: 2.226 cumulative
IPC: 2.354 (Simulation time: 00 hr 14 min 58 sec)
Simulation finished CPU 0 instructions: 50000002 cycles: 20975120 cumulative IPC: 2.384
(Simulation time: 00 hr 17 min 23 sec)
Simulation complete CPU 0 instructions: 50000002 cycles: 20975120 cumulative IPC: 2.384
(Simulation time: 00 hr 17 min 23 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz
```

Region of Interest Statistics

CPU 0 cumulative IPC: 2.384 instructions: 50000002 cycles: 20975120
CPU 0 Branch Prediction Accuracy: 98.14% MPKI: 2.535 Average ROB Occupancy at Mispredict: 149.5
Branch type MPKI
BRANCH_DIRECT_JUMP: 0.0292
BRANCH_INDIRECT: 0.3349
BRANCH_CONDITIONAL: 2.17
BRANCH_DIRECT_CALL: 0.00052
BRANCH_INDIRECT_CALL: 8e-05
BRANCH_RETURN: 0.00052

cpu0->cpu0_STLB TOTAL ACCESS: 31863 HIT: 31673 MISS: 190 MSHR_MERGE: 0
cpu0->cpu0_STLB LOAD ACCESS: 31863 HIT: 31673 MISS: 190 MSHR_MERGE: 0
cpu0->cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_STLB AVERAGE MISS LATENCY: 311.5 cycles
cpu0->cpu0_L2C TOTAL ACCESS: 4115 HIT: 2134 MISS: 1981 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 3316 HIT: 1620 MISS: 1696 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 233 HIT: 41 MISS: 192 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 388 HIT: 388 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 178 HIT: 85 MISS: 93 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 191 cycles

cpu0->cpu0_L1I TOTAL ACCESS: 2523138 HIT: 2522023 MISS: 1115
MSHR_MERGE: 241
cpu0->cpu0_L1I LOAD ACCESS: 2523138 HIT: 2522023 MISS: 1115
MSHR_MERGE: 241
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: 13.97 cycles
cpu0->cpu0_L1D TOTAL ACCESS: 16098517 HIT: 16093385 MISS: 5132
MSHR_MERGE: 2279
cpu0->cpu0_L1D LOAD ACCESS: 6297340 HIT: 6293717 MISS: 3623
MSHR_MERGE: 1181
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_L1D WRITE ACCESS: 9800983 HIT: 9799652 MISS: 1331
MSHR_MERGE: 1098
cpu0->cpu0_L1D TRANSLATION ACCESS: 194 HIT: 16 MISS: 178
MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
USELESS: 0
cpu0->cpu0_L1D AVERAGE MISS LATENCY: 139.2 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 2191391 HIT: 2191162 MISS: 229
MSHR_MERGE: 144
cpu0->cpu0_ITLB LOAD ACCESS: 2191391 HIT: 2191162 MISS: 229
MSHR_MERGE: 144
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE:
0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
USELESS: 0

cpu0->cpu0_ITLB AVERAGE MISS LATENCY: 5 cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 14337814 HIT: 14302441 MISS: 35373 MSHR_MERGE: 3595
cpu0->cpu0_DTLB LOAD ACCESS: 14337814 HIT: 14302441 MISS: 35373 MSHR_MERGE: 3595
cpu0->cpu0_DTLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: 6.869 cycles
cpu0->LLC TOTAL ACCESS: 1985 HIT: 6 MISS: 1979 MSHR_MERGE: 0
cpu0->LLC LOAD ACCESS: 1696 HIT: 2 MISS: 1694 MSHR_MERGE: 0
cpu0->LLC RFO ACCESS: 192 HIT: 0 MISS: 192 MSHR_MERGE: 0
cpu0->LLC PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC WRITE ACCESS: 4 HIT: 4 MISS: 0 MSHR_MERGE: 0
cpu0->LLC TRANSLATION ACCESS: 93 HIT: 0 MISS: 93 MSHR_MERGE: 0
cpu0->LLC PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->LLC AVERAGE MISS LATENCY: 175.2 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT: 21
 ROW_BUFFER_MISS: 1958
 AVG DBUS CONGESTED CYCLE: 2.574
Channel 0 WQ ROW_BUFFER_HIT: 0
 ROW_BUFFER_MISS: 0
 FULL: 0
Channel 0 REFRESHES ISSUED: 1748

```
ashant@Ashant:~/ChampSim$ bin/champsim_perceptron --warmup_instructions 200000000
--simulation_instruc
tions 500000000 "traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz"
[VMEM] WARNING: physical memory size is smaller than virtual memory size.
WARNING: option --warmup_instructions is deprecated. Use --warmup-instructions instead.
WARNING: option --simulation_instructions is deprecated. Use --simulation-instructions instead.

*** ChampSim Multicore Out-of-Order Simulator ***
Warmup Instructions: 200000000
Simulation Instructions: 500000000
Number of CPUs: 1
Page size: 4096

Off-chip DRAM Size: 16 GiB Channels: 1 Width: 64-bit Data Rate: 3205 MT/s
Heartbeat CPU 0 instructions: 10000002 cycles: 2792634 heartbeat IPC: 3.581 cumulative IPC:
3.581 (Simulation time: 00 hr 02 min 18 sec)
Heartbeat CPU 0 instructions: 20000004 cycles: 5644726 heartbeat IPC: 3.506 cumulative IPC:
3.543 (Simulation time: 00 hr 04 min 41 sec)
Heartbeat CPU 0 instructions: 30000007 cycles: 8497473 heartbeat IPC: 3.505 cumulative IPC:
3.53 (Simulation time: 00 hr 07 min 08 sec)
Heartbeat CPU 0 instructions: 40000010 cycles: 11353601 heartbeat IPC: 3.501 cumulative
IPC: 3.523 (Simulation time: 00 hr 09 min 29 sec)
Heartbeat CPU 0 instructions: 50000010 cycles: 14193242 heartbeat IPC: 3.522 cumulative
IPC: 3.523 (Simulation time: 00 hr 11 min 52 sec)
Heartbeat CPU 0 instructions: 60000013 cycles: 17004732 heartbeat IPC: 3.557 cumulative
IPC: 3.528 (Simulation time: 00 hr 14 min 12 sec)
Heartbeat CPU 0 instructions: 70000013 cycles: 19901404 heartbeat IPC: 3.452 cumulative
IPC: 3.517 (Simulation time: 00 hr 16 min 34 sec)
Heartbeat CPU 0 instructions: 80000015 cycles: 22802593 heartbeat IPC: 3.447 cumulative
IPC: 3.508 (Simulation time: 00 hr 18 min 55 sec)
Heartbeat CPU 0 instructions: 90000016 cycles: 25582501 heartbeat IPC: 3.597 cumulative
IPC: 3.518 (Simulation time: 00 hr 21 min 14 sec)
Heartbeat CPU 0 instructions: 100000018 cycles: 28399923 heartbeat IPC: 3.549 cumulative
IPC: 3.521 (Simulation time: 00 hr 23 min 34 sec)
Heartbeat CPU 0 instructions: 110000018 cycles: 31287158 heartbeat IPC: 3.464 cumulative
IPC: 3.516 (Simulation time: 00 hr 25 min 59 sec)
Heartbeat CPU 0 instructions: 120000018 cycles: 34186401 heartbeat IPC: 3.449 cumulative
IPC: 3.51 (Simulation time: 00 hr 28 min 22 sec)
Heartbeat CPU 0 instructions: 130000021 cycles: 36988292 heartbeat IPC: 3.569 cumulative
IPC: 3.515 (Simulation time: 00 hr 30 min 47 sec)
Heartbeat CPU 0 instructions: 140000025 cycles: 39779980 heartbeat IPC: 3.582 cumulative
IPC: 3.519 (Simulation time: 00 hr 33 min 07 sec)
```

Heartbeat CPU 0 instructions: 150000025 cycles: 42612731 heartbeat IPC: 3.53 cumulative IPC: 3.52 (Simulation time: 00 hr 35 min 29 sec)
Heartbeat CPU 0 instructions: 160000029 cycles: 45507048 heartbeat IPC: 3.455 cumulative IPC: 3.516 (Simulation time: 00 hr 37 min 53 sec)
Heartbeat CPU 0 instructions: 170000032 cycles: 48336598 heartbeat IPC: 3.534 cumulative IPC: 3.517 (Simulation time: 00 hr 40 min 16 sec)
Heartbeat CPU 0 instructions: 180000035 cycles: 51197010 heartbeat IPC: 3.496 cumulative IPC: 3.516 (Simulation time: 00 hr 42 min 43 sec)
Heartbeat CPU 0 instructions: 190000037 cycles: 54090103 heartbeat IPC: 3.457 cumulative IPC: 3.513 (Simulation time: 00 hr 45 min 04 sec)
Warmup finished CPU 0 instructions: 200000001 cycles: 56917825 cumulative IPC: 3.514 (Simulation time: 00 hr 47 min 22 sec)
Warmup complete CPU 0 instructions: 200000001 cycles: 56917825 cumulative IPC: 3.514 (Simulation time: 00 hr 47 min 22 sec)
Heartbeat CPU 0 instructions: 200000041 cycles: 56917836 heartbeat IPC: 3.536 cumulative IPC: 3.636 (Simulation time: 00 hr 47 min 22 sec)
Heartbeat CPU 0 instructions: 210000042 cycles: 61229162 heartbeat IPC: 2.319 cumulative IPC: 2.319 (Simulation time: 00 hr 49 min 52 sec)
Heartbeat CPU 0 instructions: 220000042 cycles: 65501738 heartbeat IPC: 2.341 cumulative IPC: 2.33 (Simulation time: 00 hr 52 min 26 sec)
Heartbeat CPU 0 instructions: 230000042 cycles: 69643217 heartbeat IPC: 2.415 cumulative IPC: 2.357 (Simulation time: 00 hr 54 min 58 sec)
Heartbeat CPU 0 instructions: 240000044 cycles: 73917204 heartbeat IPC: 2.34 cumulative IPC: 2.353 (Simulation time: 00 hr 57 min 34 sec)
Heartbeat CPU 0 instructions: 250000048 cycles: 78110974 heartbeat IPC: 2.384 cumulative IPC: 2.359 (Simulation time: 01 hr 00 min 17 sec)
Heartbeat CPU 0 instructions: 260000048 cycles: 82370952 heartbeat IPC: 2.347 cumulative IPC: 2.357 (Simulation time: 01 hr 02 min 48 sec)
Heartbeat CPU 0 instructions: 270000049 cycles: 86533389 heartbeat IPC: 2.402 cumulative IPC: 2.364 (Simulation time: 01 hr 05 min 17 sec)
Heartbeat CPU 0 instructions: 280000051 cycles: 90644915 heartbeat IPC: 2.432 cumulative IPC: 2.372 (Simulation time: 01 hr 07 min 47 sec)
Heartbeat CPU 0 instructions: 290000051 cycles: 94819153 heartbeat IPC: 2.396 cumulative IPC: 2.375 (Simulation time: 01 hr 10 min 19 sec)
Heartbeat CPU 0 instructions: 300000052 cycles: 99195856 heartbeat IPC: 2.285 cumulative IPC: 2.365 (Simulation time: 01 hr 12 min 56 sec)
Heartbeat CPU 0 instructions: 310000055 cycles: 103612583 heartbeat IPC: 2.264 cumulative IPC: 2.356 (Simulation time: 01 hr 15 min 28 sec)
Heartbeat CPU 0 instructions: 320000058 cycles: 107894176 heartbeat IPC: 2.336 cumulative IPC: 2.354 (Simulation time: 01 hr 18 min 00 sec)
Heartbeat CPU 0 instructions: 330000059 cycles: 112097450 heartbeat IPC: 2.379 cumulative IPC: 2.356 (Simulation time: 01 hr 20 min 47 sec)
Heartbeat CPU 0 instructions: 340000060 cycles: 116362637 heartbeat IPC: 2.345 cumulative IPC: 2.355 (Simulation time: 01 hr 23 min 18 sec)

Heartbeat CPU 0 instructions: 350000061 cycles: 120674628 heartbeat IPC: 2.319 cumulative IPC: 2.353 (Simulation time: 01 hr 25 min 49 sec)
Heartbeat CPU 0 instructions: 360000063 cycles: 125088774 heartbeat IPC: 2.265 cumulative IPC: 2.347 (Simulation time: 01 hr 28 min 26 sec)
Heartbeat CPU 0 instructions: 370000064 cycles: 129138490 heartbeat IPC: 2.469 cumulative IPC: 2.354 (Simulation time: 01 hr 30 min 58 sec)
Heartbeat CPU 0 instructions: 380000064 cycles: 133345400 heartbeat IPC: 2.377 cumulative IPC: 2.355 (Simulation time: 01 hr 33 min 30 sec)
Heartbeat CPU 0 instructions: 390000068 cycles: 137657995 heartbeat IPC: 2.319 cumulative IPC: 2.353 (Simulation time: 01 hr 36 min 00 sec)
Heartbeat CPU 0 instructions: 400000070 cycles: 141891014 heartbeat IPC: 2.362 cumulative IPC: 2.354 (Simulation time: 01 hr 38 min 29 sec)
Heartbeat CPU 0 instructions: 410000074 cycles: 145961576 heartbeat IPC: 2.457 cumulative IPC: 2.358 (Simulation time: 01 hr 41 min 29 sec)
Heartbeat CPU 0 instructions: 420000075 cycles: 150161517 heartbeat IPC: 2.381 cumulative IPC: 2.359 (Simulation time: 01 hr 45 min 46 sec)
Heartbeat CPU 0 instructions: 430000076 cycles: 154465724 heartbeat IPC: 2.323 cumulative IPC: 2.358 (Simulation time: 01 hr 49 min 32 sec)
Heartbeat CPU 0 instructions: 440000078 cycles: 158816256 heartbeat IPC: 2.299 cumulative IPC: 2.355 (Simulation time: 01 hr 52 min 09 sec)
Heartbeat CPU 0 instructions: 450000078 cycles: 162907276 heartbeat IPC: 2.444 cumulative IPC: 2.359 (Simulation time: 01 hr 54 min 54 sec)
Heartbeat CPU 0 instructions: 460000080 cycles: 167287561 heartbeat IPC: 2.283 cumulative IPC: 2.356 (Simulation time: 01 hr 58 min 23 sec)
Heartbeat CPU 0 instructions: 470000084 cycles: 174741642 heartbeat IPC: 1.342 cumulative IPC: 2.292 (Simulation time: 02 hr 02 min 47 sec)
Heartbeat CPU 0 instructions: 480000088 cycles: 181235264 heartbeat IPC: 1.54 cumulative IPC: 2.252 (Simulation time: 02 hr 07 min 04 sec)
Heartbeat CPU 0 instructions: 490000089 cycles: 186312275 heartbeat IPC: 1.97 cumulative IPC: 2.241 (Simulation time: 02 hr 10 min 39 sec)
Heartbeat CPU 0 instructions: 500000090 cycles: 191445912 heartbeat IPC: 1.948 cumulative IPC: 2.23 (Simulation time: 02 hr 14 min 35 sec)
Heartbeat CPU 0 instructions: 510000090 cycles: 200517585 heartbeat IPC: 1.102 cumulative IPC: 2.159 (Simulation time: 02 hr 19 min 32 sec)
Heartbeat CPU 0 instructions: 520000090 cycles: 212822792 heartbeat IPC: 0.8127 cumulative IPC: 2.053 (Simulation time: 02 hr 26 min 04 sec)
Heartbeat CPU 0 instructions: 530000093 cycles: 223002424 heartbeat IPC: 0.9824 cumulative IPC: 1.987 (Simulation time: 02 hr 31 min 41 sec)
Heartbeat CPU 0 instructions: 540000096 cycles: 232667529 heartbeat IPC: 1.035 cumulative IPC: 1.935 (Simulation time: 02 hr 36 min 22 sec)
Heartbeat CPU 0 instructions: 550000096 cycles: 245051495 heartbeat IPC: 0.8075 cumulative IPC: 1.86 (Simulation time: 02 hr 40 min 50 sec)
Heartbeat CPU 0 instructions: 560000100 cycles: 250487962 heartbeat IPC: 1.839 cumulative IPC: 1.86 (Simulation time: 02 hr 43 min 34 sec)

Heartbeat CPU 0 instructions: 570000101 cycles: 255663283 heartbeat IPC: 1.932 cumulative IPC: 1.862 (Simulation time: 02 hr 46 min 27 sec)
Heartbeat CPU 0 instructions: 580000104 cycles: 261121871 heartbeat IPC: 1.832 cumulative IPC: 1.861 (Simulation time: 02 hr 49 min 25 sec)
Heartbeat CPU 0 instructions: 590000105 cycles: 266654347 heartbeat IPC: 1.808 cumulative IPC: 1.859 (Simulation time: 02 hr 53 min 04 sec)
Heartbeat CPU 0 instructions: 600000105 cycles: 276586989 heartbeat IPC: 1.007 cumulative IPC: 1.821 (Simulation time: 02 hr 59 min 03 sec)
Heartbeat CPU 0 instructions: 610000108 cycles: 288804574 heartbeat IPC: 0.8185 cumulative IPC: 1.768 (Simulation time: 03 hr 05 min 32 sec)
Heartbeat CPU 0 instructions: 620000112 cycles: 300800202 heartbeat IPC: 0.8336 cumulative IPC: 1.722 (Simulation time: 03 hr 12 min 37 sec)
Heartbeat CPU 0 instructions: 630000114 cycles: 309988339 heartbeat IPC: 1.088 cumulative IPC: 1.699 (Simulation time: 03 hr 18 min 16 sec)
Heartbeat CPU 0 instructions: 640000114 cycles: 320424361 heartbeat IPC: 0.9582 cumulative IPC: 1.67 (Simulation time: 03 hr 23 min 46 sec)
Heartbeat CPU 0 instructions: 650000114 cycles: 333312712 heartbeat IPC: 0.7759 cumulative IPC: 1.628 (Simulation time: 03 hr 28 min 22 sec)
Heartbeat CPU 0 instructions: 660000115 cycles: 345405172 heartbeat IPC: 0.827 cumulative IPC: 1.595 (Simulation time: 03 hr 32 min 47 sec)
Heartbeat CPU 0 instructions: 670000116 cycles: 353218482 heartbeat IPC: 1.28 cumulative IPC: 1.586 (Simulation time: 03 hr 36 min 12 sec)
Heartbeat CPU 0 instructions: 680000116 cycles: 368061047 heartbeat IPC: 0.6737 cumulative IPC: 1.543 (Simulation time: 03 hr 41 min 23 sec)
Heartbeat CPU 0 instructions: 690000116 cycles: 380434550 heartbeat IPC: 0.8082 cumulative IPC: 1.515 (Simulation time: 03 hr 45 min 51 sec)
Simulation finished CPU 0 instructions: 500000004 cycles: 327907529 cumulative IPC: 1.525 (Simulation time: 03 hr 48 min 13 sec)
Simulation complete CPU 0 instructions: 500000004 cycles: 327907529 cumulative IPC: 1.525 (Simulation time: 03 hr 48 min 13 sec)

ChampSim completed all CPUs

=== Simulation ===
CPU 0 runs traces/ChampSim Traces/600.perlbench_s-210B.champsimtrace.xz

Region of Interest Statistics

CPU 0 cumulative IPC: 1.525 instructions: 500000004 cycles: 327907529
CPU 0 Branch Prediction Accuracy: 95.53% MPKI: 7.07 Average ROB Occupancy at Mispredict: 57.8
Branch type MPKI
BRANCH_DIRECT_JUMP: 0.06608
BRANCH_INDIRECT: 0.3866

BRANCH_CONDITIONAL: 6.301
BRANCH_DIRECT_CALL: 0.02277
BRANCH_INDIRECT_CALL: 0.2705
BRANCH_RETURN: 0.0235

cpu0->cpu0_STLB TOTAL ACCESS: 1106347 HIT: 1074460 MISS: 31887 MSHR_MERGE: 0
cpu0->cpu0_STLB LOAD ACCESS: 1106347 HIT: 1074460 MISS: 31887 MSHR_MERGE: 0
cpu0->cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_STLB AVERAGE MISS LATENCY: 174 cycles
cpu0->cpu0_L2C TOTAL ACCESS: 2988893 HIT: 2534296 MISS: 454597 MSHR_MERGE: 0
cpu0->cpu0_L2C LOAD ACCESS: 2602061 HIT: 2199969 MISS: 402092 MSHR_MERGE: 0
cpu0->cpu0_L2C RFO ACCESS: 84477 HIT: 56499 MISS: 27978 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L2C WRITE ACCESS: 269181 HIT: 267887 MISS: 1294 MSHR_MERGE: 0
cpu0->cpu0_L2C TRANSLATION ACCESS: 33174 HIT: 9941 MISS: 23233 MSHR_MERGE: 0
cpu0->cpu0_L2C PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L2C AVERAGE MISS LATENCY: 145.3 cycles
cpu0->cpu0_L1I TOTAL ACCESS: 36160454 HIT: 34151655 MISS: 2008799 MSHR_MERGE: 369212
cpu0->cpu0_L1I LOAD ACCESS: 36160454 HIT: 34151655 MISS: 2008799 MSHR_MERGE: 369212
cpu0->cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0

cpu0->cpu0_L1I WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1I AVERAGE MISS LATENCY: 9.691 cycles
cpu0->cpu0_L1D TOTAL ACCESS: 163633075 HIT: 162133156 MISS: 1499919 MSHR_MERGE: 419789
cpu0->cpu0_L1D LOAD ACCESS: 71145900 HIT: 69926217 MISS: 1219683 MSHR_MERGE: 257207
cpu0->cpu0_L1D RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_L1D WRITE ACCESS: 92450819 HIT: 92203764 MISS: 247055 MSHR_MERGE: 162575
cpu0->cpu0_L1D TRANSLATION ACCESS: 36356 HIT: 3175 MISS: 33181 MSHR_MERGE: 7
cpu0->cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_L1D AVERAGE MISS LATENCY: 65.64 cycles
cpu0->cpu0_ITLB TOTAL ACCESS: 31506665 HIT: 31230178 MISS: 276487 MSHR_MERGE: 158793
cpu0->cpu0_ITLB LOAD ACCESS: 31506665 HIT: 31230178 MISS: 276487 MSHR_MERGE: 158793
cpu0->cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_ITLB AVERAGE MISS LATENCY: 7.021 cycles
cpu0->cpu0_DTLB TOTAL ACCESS: 148342009 HIT: 147098776 MISS: 1243233 MSHR_MERGE: 254580
cpu0->cpu0_DTLB LOAD ACCESS: 148342009 HIT: 147098776 MISS: 1243233 MSHR_MERGE: 254580
cpu0->cpu0_DTLB RFO ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0

cpu0->cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB WRITE ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->cpu0_DTLB AVERAGE MISS LATENCY: 10.41 cycles
cpu0->LLC TOTAL ACCESS: 543217 HIT: 210331 MISS: 332886 MSHR_MERGE: 0
cpu0->LLC LOAD ACCESS: 402092 HIT: 108942 MISS: 293150 MSHR_MERGE: 0
cpu0->LLC RFO ACCESS: 27977 HIT: 8054 MISS: 19923 MSHR_MERGE: 0
cpu0->LLC PREFETCH ACCESS: 0 HIT: 0 MISS: 0 MSHR_MERGE: 0
cpu0->LLC WRITE ACCESS: 89915 HIT: 89094 MISS: 821 MSHR_MERGE: 0
cpu0->LLC TRANSLATION ACCESS: 23233 HIT: 4241 MISS: 18992 MSHR_MERGE: 0
cpu0->LLC PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 USELESS: 0
cpu0->LLC AVERAGE MISS LATENCY: 176.9 cycles

DRAM Statistics

Channel 0 RQ ROW_BUFFER_HIT: 5840
 ROW_BUFFER_MISS: 326220
 AVG DBUS CONGESTED CYCLE: 20.98
Channel 0 WQ ROW_BUFFER_HIT: 19604
 ROW_BUFFER_MISS: 37559
 FULL: 0
Channel 0 REFRESHES ISSUED: 27325
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