74HC138; 74HCT138

3-to-8 line decoder/demultiplexer; inverting

Rev. 5 — 26 January 2015 Product data sheet

1. General description

The 74HC138; 74HCT138 decodes three binary weighted address inputs (A0, A1 and A2) to eight mutually exclusive outputs ($\overline{Y}0$ to $\overline{Y}7$). The device features three enable inputs ($\overline{E}1$, $\overline{E}2$ and E3). Every output will be HIGH unless $\overline{E}1$ and $\overline{E}2$ are LOW and E3 is HIGH. This multiple enable function allows easy parallel expansion to a 1-of-32 (5 to 32 lines) decoder with just four '138' ICs and one inverter. The '138' can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Complies with JEDEC standard no. 7A
- Input levels:
  - For 74HC138: CMOS level
  - For 74HCT138: TTL level
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC138N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT138N				
74HC138D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74 HCT138D				
74HC138DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT138DB				

Table 1. Ordering information *…continued*

Type number	Package			
	Temperature range	Name	Description	Version
74HC138PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT138PW				
74HC138BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT138BQ				

4. Functional diagram

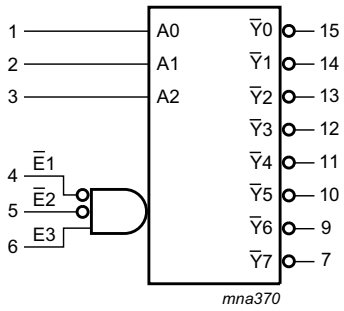

Fig 1. Logic symbol

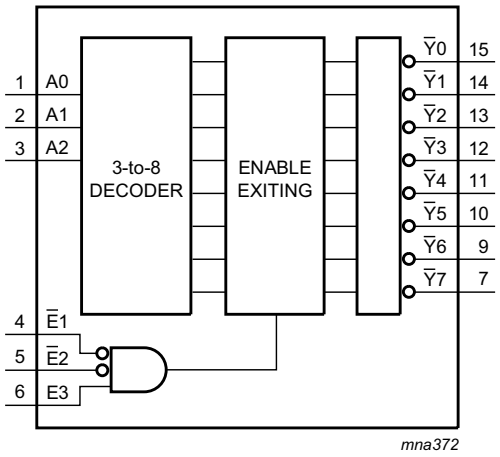

Fig 2. Functional diagram

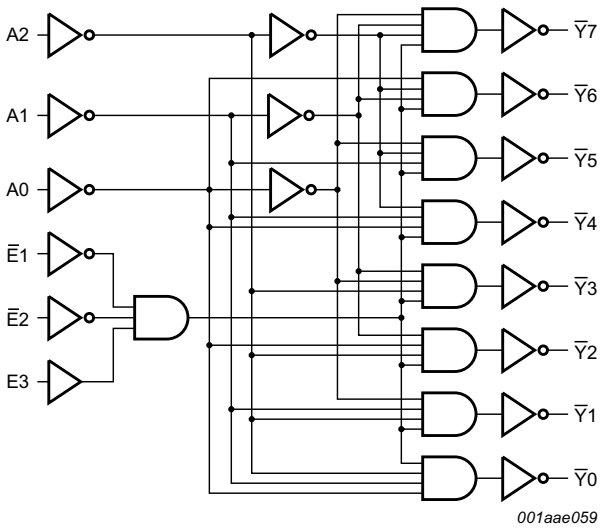

Fig 3. Logic diagram

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5. Pinning information

5.1 Pinning

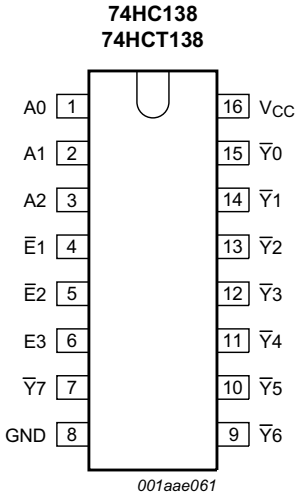
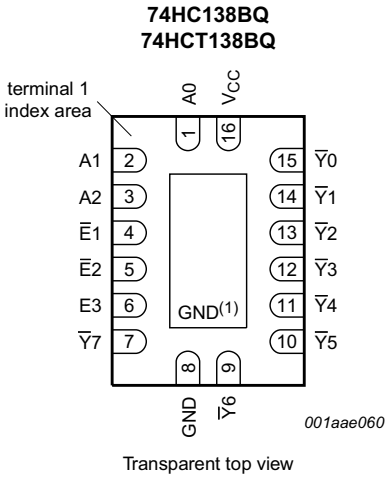


Fig 4. Pin configuration DIP16, SO16, SSOP16 and TSSOP16



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration DHVQFN16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0, A1, A2	1, 2, 3	address input A0, A1, A2
$\overline{E}1$, $\overline{E}2$	4, 5	enable input $\overline{E}1$, $\overline{E}2$ (active LOW)
E3	6	enable input E3 (active HIGH)
$\overline{Y}0$, $\overline{Y}1$, $\overline{Y}2$, $\overline{Y}3$, $\overline{Y}4$, $\overline{Y}5$, $\overline{Y}6$, $\overline{Y}7$	15, 14, 13, 12, 11, 10, 9, 7	output $\overline{Y}0$, $\overline{Y}1$, $\overline{Y}2$, $\overline{Y}3$, $\overline{Y}4$, $\overline{Y}5$, $\overline{Y}6$, $\overline{Y}7$ (active LOW)
GND	8	ground (0 V)
V_{CC}	16	positive supply voltage

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6. Functional description

Table 3. Function table[1]

Control			Input			Output							
$\overline{E1}$	$\overline{E2}$	E3	A2	A1	A0	$\overline{Y7}$	$\overline{Y6}$	$\overline{Y5}$	$\overline{Y4}$	$\overline{Y3}$	$\overline{Y2}$	$\overline{Y1}$	$\overline{Y0}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X											
X	X	L											
L	L	H	L	L	L	H	H	H	H	H	H	H	L
			L	L	H	H	H	H	H	H	H	L	H
			L	H	L	H	H	H	H	H	L	H	H
			L	H	H	H	H	H	H	L	H	H	H
			H	L	L	H	H	H	L	H	H	H	H
			H	L	H	H	H	L	H	H	H	H	H
			H	H	L	H	L	H	H	H	H	H	H
			H	H	H	L	H	H	H	H	H	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-	±25	mA
I_{CC}	quiescent supply current		-	50	mA
I_{GND}	ground current		-	−50	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation				
	DIP16 package	[1]	-	750	mW
	SO16 package	[2]	-	500	mW
	SSOP16 package	[3]	-	500	mW
	TSSOP16 package	[3]	-	500	mW
	DHVQFN16 package	[4]	-	500	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN16 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC138			74HCT138			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC138										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA

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Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_I	input capacitance		-	3.5	-					pF
74HCT138										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = –20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	V_I = V_{CC} – 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A								
		per input pin; An inputs	-	150	540	-	675	-	735	μA
		per input pin; $\overline{E}n$ inputs	-	125	450	-	562.5	-	612.5	μA
		per input pin; E3 input	-	100	360	-	450	-	490	μA
C_I	input capacitance		-	3.5	-					pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 8.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC138										
t_{pd}	propagation delay	An to $\overline{Y}$n; see Figure 6 [1]								
		V_{CC} = 2.0 V	-	41	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	15	30	-	38	-	45	ns
		V_{CC} = 5 V; C_L = 15 pF	-	12	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	12	26	-	33	-	38	ns
		E3 to $\overline{Y}$n; see Figure 6 [1]								
		V_{CC} = 2.0 V	-	47	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	17	20	-	38	-	45	ns
		V_{CC} = 5 V; C_L = 15 pF	-	14	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	26	-	33	-	38	ns
		$\overline{E}$n to $\overline{Y}$n; see Figure 7 [1]								
		V_{CC} = 2.0 V	-	47	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	17	20	-	38	-	45	ns
		V_{CC} = 5 V; C_L = 15 pF	-	14	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	26	-	33	-	38	ns
t_t	transition time	$\overline{Y}$n; see Figure 6 and Figure 7 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} [3]	-	67	-	-	-	-	-	pF

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 8.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT138										
t_{pd}	propagation delay	An to $\overline{Y}$n; see Figure 6 [1]								
		V_{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
		E3 to $\overline{Y}$n; see Figure 6 [1]								
		V_{CC} = 4.5 V	-	18	40	-	50	-	60	ns
		V_{CC} = 5 V; C_L = 15 pF	-	19	-	-	-	-	-	ns
		$\overline{E}$n to $\overline{Y}$n; see Figure 7 [1]								
		V_{CC} = 4.5 V	-	19	40	-	50	-	60	ns
		V_{CC} = 5 V; C_L = 15 pF	-	19	-	-	-	-	-	ns
t_t	transition time	$\overline{Y}$n; see Figure 6 and Figure 7 [2]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} − 1.5 V [3]	-	67	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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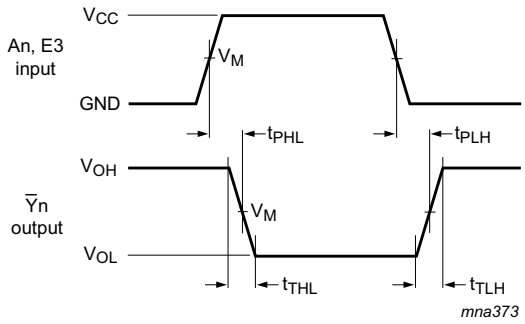
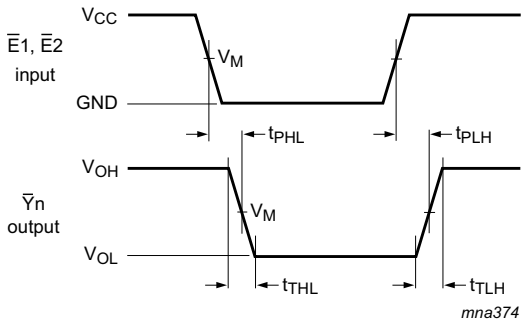
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delay input (An) and enable input (E3) to output ($\overline{Y}$n) and transition time output ($\overline{Y}$n)



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Propagation delay enable input ($\overline{E}$n) to output ($\overline{Y}$n) and transition time output ($\overline{Y}$n)

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC138	$0.5V_{CC}$	$0.5V_{CC}$
74HCT138	1.3 V	1.3 V

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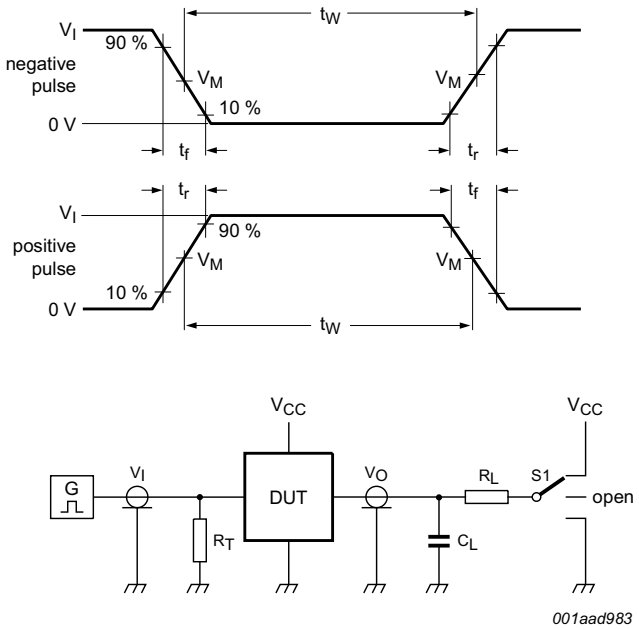

Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC138	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74HCT138	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

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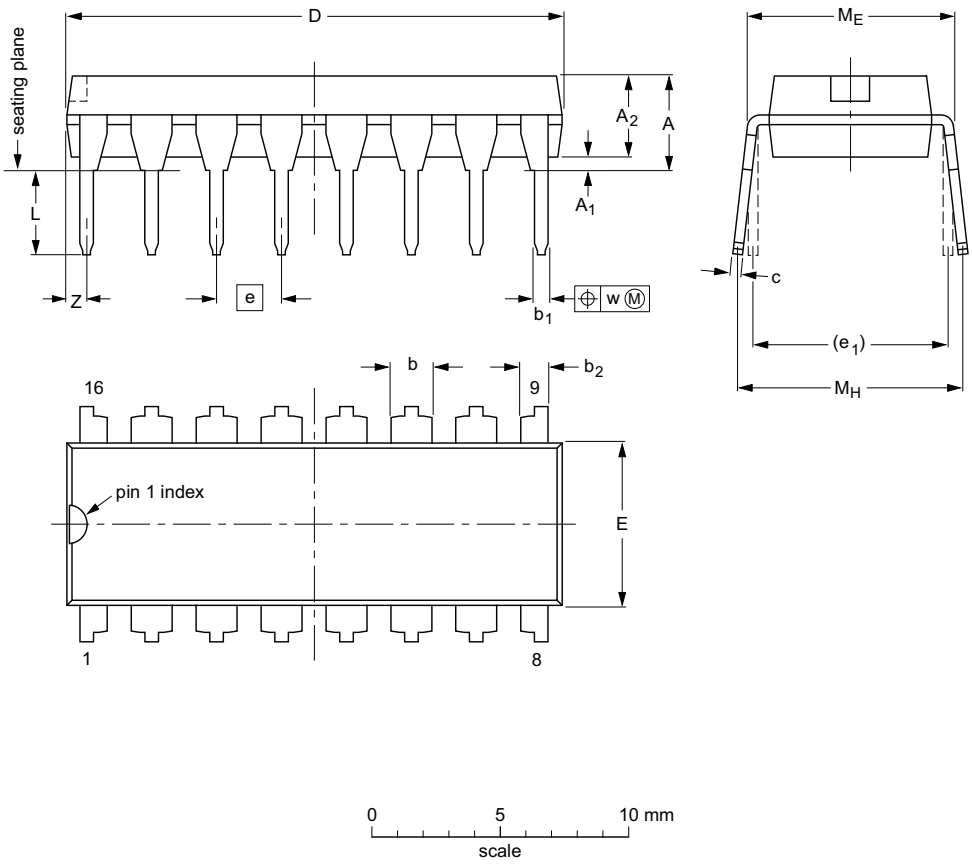
12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 9. Package outline SOT38-4 (DIP16)

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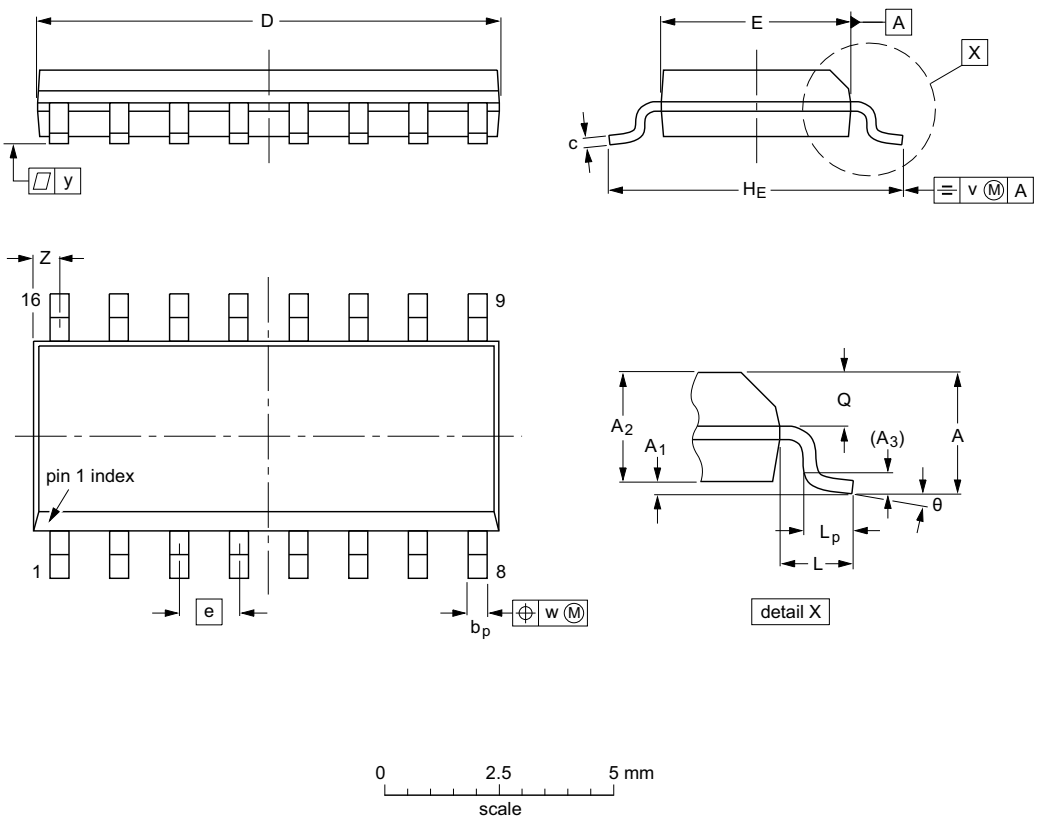
SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT109-1 (SO16)

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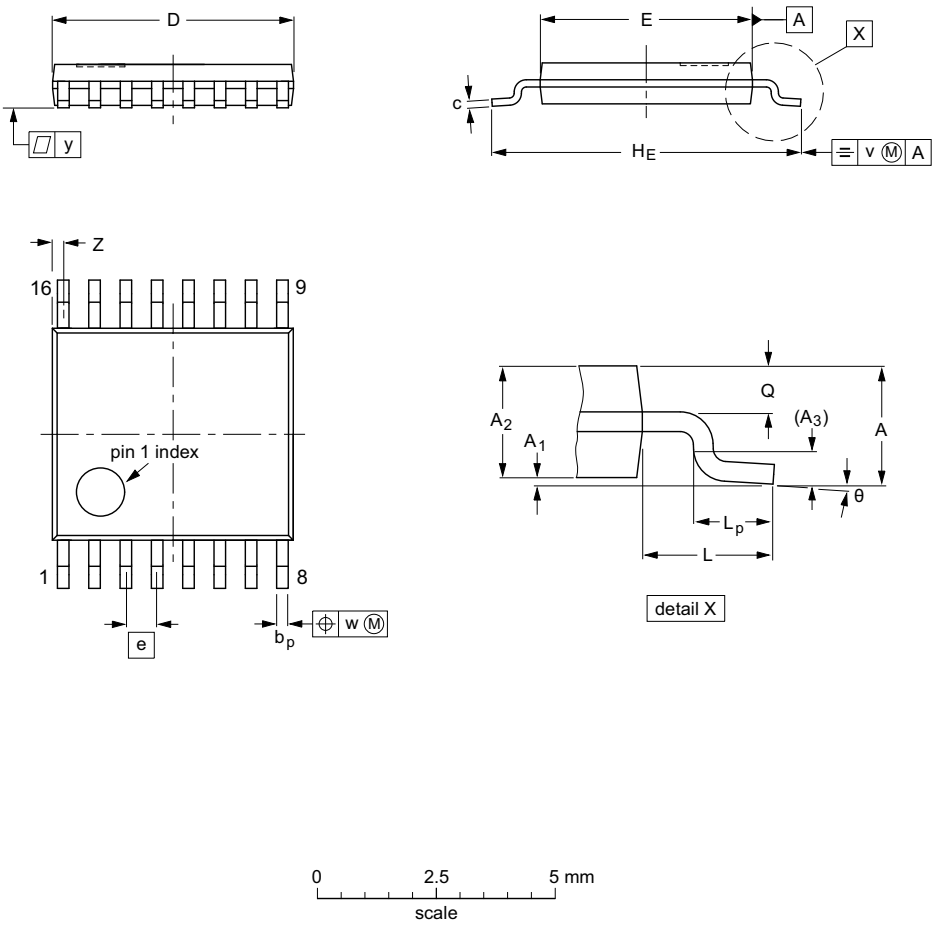
TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT403-1 (TSSOP16)

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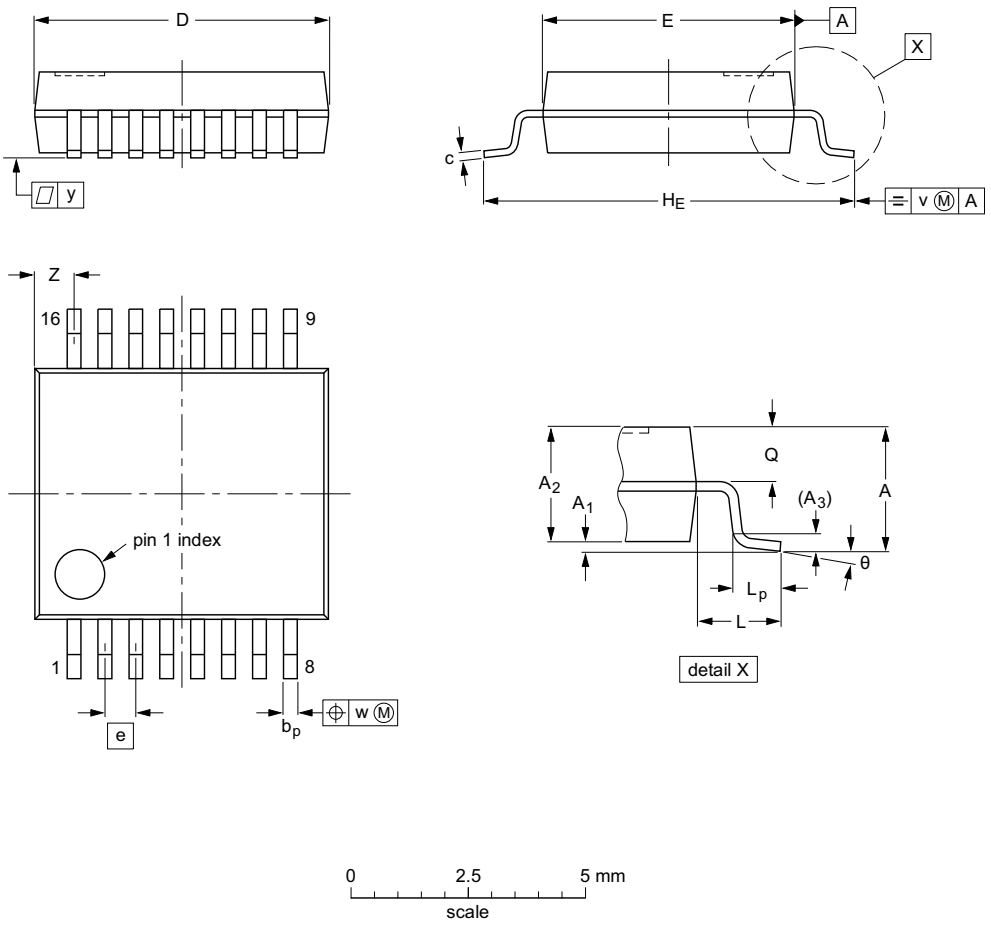
SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT338-1 (SSOP16)

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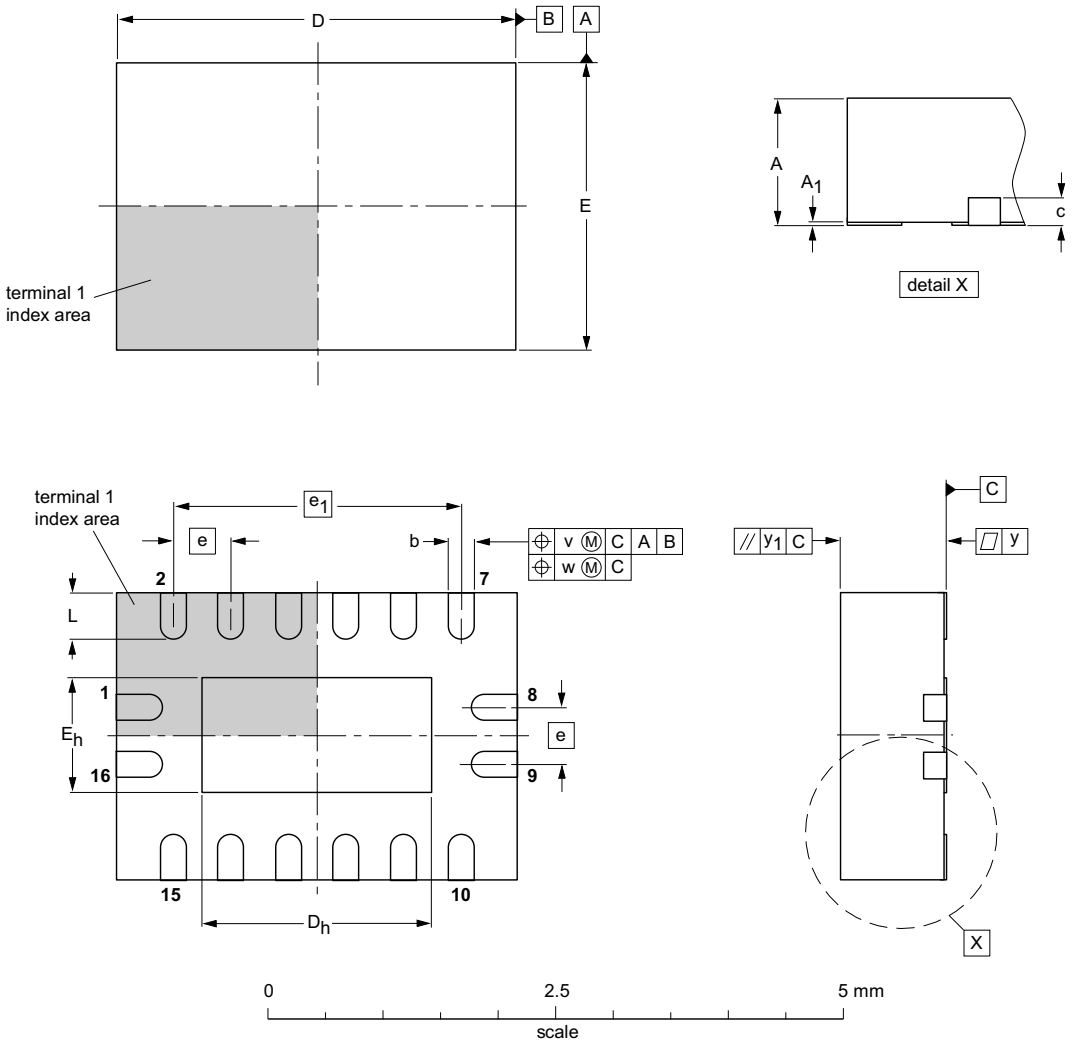
DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 13. Package outline SOT763-1 (DHVQFN16)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT138 v.5	20150126	Product data sheet	-	74HC_HCT138 v.4
Modifications:	• Table 6: OFF-state output current removed because device has no 3-state outputs. • Table 7: Power dissipation capacitance condition for 74HCT138 is corrected.			
74HC_HCT138 v.4	20120627	Product data sheet	-	74HC_HCT138 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • SOT38-1 changed to SOT38-4.			
74HC_HCT138 v.3	20051223	Product data sheet	-	74HC_HCT138_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 3 “Ordering information”, Section 5 “Pinning information” and Section 12 “Package outline”: Added DHVQFN package information • Section 9 “Static characteristics”: Added from the family specification			
74HC_HCT138_CNV v.2	19970827	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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