Synthesizer Design Report

ELEC 40006-Electronics Design Project

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Word count: 10,275

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Abstract

An analogue synthesizer is a device which enables the user to electronically generate sounds. Generated soundwaves can then be modulated to modify their pitch (frequency), loudness (amplitude), intensity (power per area) or timbre (frequency composition) [1]. This is achieved by passing the soundwave through filters and amplifiers which can be controlled by user inputs or functional inputs generated in envelope generators or oscillators.

Over recent years synthesizer technology has advanced greatly, causing analogue synthesizers, which rely on circuitry to create and modulate the soundwaves, to be replaced by their digital counterparts, using digital computers instead of actual circuitry. This paper shows a possible design solution for an analogue synthesizer, satisfying the design criteria and product design specifications outlined below.

Outline of the technical problem and Design Criteria

Technical problem:

The input voltage that is generated when the user presses a key on the keyboard should be related to the output frequency of the soundwave in the following way:

$$f = 2^{V+4.781}$$

This equation should be used to relate input voltages generated by an 88-key piano to frequencies in the frequency range of $27.5Hz - 4.186kHz$.

All used components in the design should be real components, *i.e.* passive components or semiconductors with the exception of voltage sources or voltage-controlled resistors to model user inputs or potentiometers.

The design should also be able to drive a loudspeaker with an impedance of $Z = 8\Omega$.

Process Design System

The following Design Criteria were formulated for the design of the synthesizer.

Performance

The user should be able to choose between triangle wave, square wave, sine wave or sawtooth wave as the desired input to the synthesizer. Filtering and amplification stages should be controlled by either a user input or a functional user input, generated by an envelope generator or a low frequency oscillator. The overall design must satisfy the technical problem.

Maintenance

The design should be modular, split into different building blocks/ stages. These should be able to be exchanged easily, possible through implementation into integrated circuitry when produced.

Size

Components should be chosen to keep size to a minimum. Casing of the synthesizer should not exceed: $w\ x\ h\ x\ d$: $1{,}300mm\ x\ 120mm\ x\ 300mm$. Internal circuits should ideally be integrable on circuit boards.

Target production cost

Production cost should be kept to a functional minimum. A market price of around £200 should not be exceeded.

Environment

The design should perform best at room temperature. Performance should be maintained in conditions of 5 – 40 °C surrounding temperature.

Testing

Output waveforms should be audible and able to drive an $8\ \Omega$ loudspeaker. The design should be power efficient with a high power-factor. The circuit should be driven by a 10W power supply. The design should be resilient to unwanted short connections to ground.

Implementation and Design Process

The Integrated Synthesizer

The integrated synthesizer design should be based on the fundamental building blocks of oscillator (VCO), filtering stage (VCF), and amplifying stage (VCA). These stages are responsible for the general pitch, timbre and loudness of the generated sounds. Their effect can be determined from user inputs or functional inputs of other building blocks (ADSR, LFO).

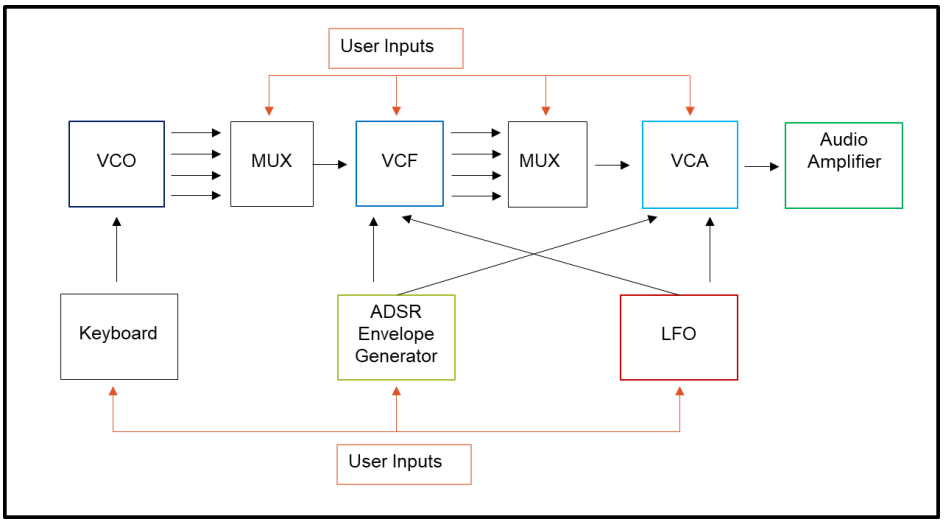


Figure 1: Block diagram of the synthesizer design

Functional inputs to the design like this, can be adjusted again to achieve a desired input or a certain sound effect, such as to emulate the mechanical generation of a sound on a piano (ADSR). The working principle of each block, together with its effect on the generated output soundwave is highlighted in the corresponding sections below.

Overview of VCO Function

The Voltage Controlled Oscillator (VCO) is the core of the synth. It generates the wave that will then be processed by the Voltage Controlled Filter (VCF), and the Voltage Controlled Amplifier (VCA). It receives as inputs a DC voltage from the keyboard controller, which it relates to the frequency of the output wave according to the relationship $f = 2^{V+4.781}$. It consists of the exponential converter and the oscillator core itself. The output wave it generates can have one of four shapes: triangle, square, sawtooth, or sine wave, from which the user can select. The different wave shapes have different timbres, meaning "the quality given to a sound by its overtones" [2], which is defined by frequencies present in the wave. The sine wave is the purest wave, only containing the fundamental frequency. The square wave also contains odd harmonics at high frequencies, which contribute to shaping the "jump" between the low and high state. The triangle wave, too, contains odd harmonics, however they attenuate with increasing frequency. Finally, the sawtooth wave contains both even and odd frequencies [3].

As a block diagram, we would represent the VCO as follows:

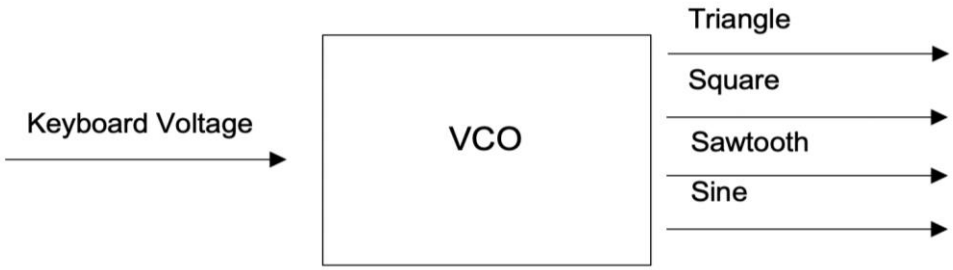
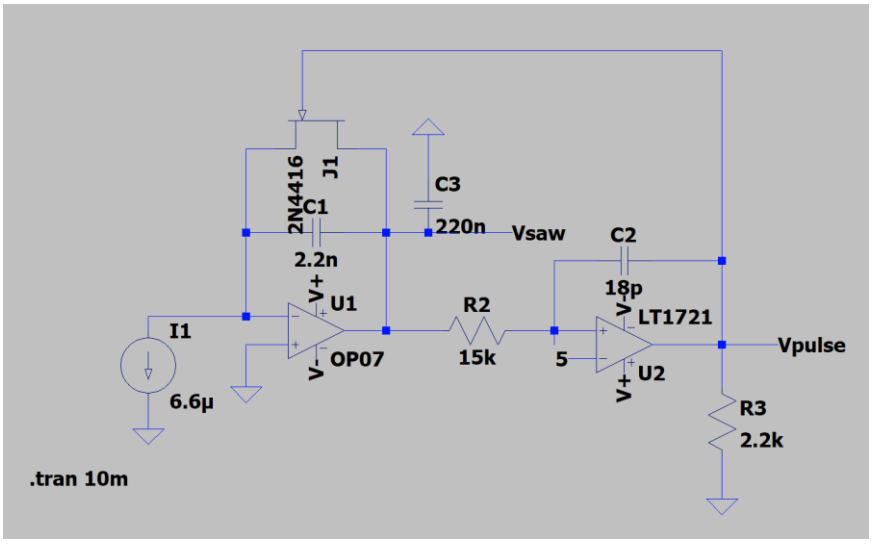


Figure 2: Inputs and outputs to the VCO

Design Process

To design the VCO, we divided the whole block into smaller tasks, specifically the task of relating the output frequency to the input voltage, and the task of generating every wave shape.

In the beginning, the task of figuring out possible designs for each waveform was the most important. We began with finding a design to generate a sawtooth wave, using a constant input current to an integrator, charging a capacitor, until it reached a threshold voltage at the input of a Schmitt trigger comparator, which would then output a spike, which would reset the process by instantaneously turning a JFET on, as shown in the following figure. However, this track did not prove to be easy for the generation of the rest of the waves based on the sawtooth, without using any other components, such as the NE555 timer, and it was also current-controlled instead of voltage-controlled. The following picture shows that first sawtooth design, which did not make it to the final design.



Schematic 1: First sawtooth generator design

We adopted another approach, and instead began with the generation of the triangle and square waves, which are directly related to each other through differentiation/integration. Their circuits therefore could be implemented using a feedback loop. Using these two waves we can generate a sawtooth by manipulating the triangle wave, and a sine by appropriate filtering.

At the same time, we had to figure out how to implement the exponential relationship between the voltage and the frequency. After conducting research, we found that this task is accomplished by the exponential converter, a circuit which takes linear changes in its input voltage and produces exponential changes in its output voltage [4]. For the design of the exponential converter, we had to keep in mind the range of input voltages that were required to generate the right wave frequency according to $f = 2^{V+4.781}$, so as to remain within the boundaries of the power rails and prevent the waves from clipping, while also using maximum amount of the voltage range available.

After deciding on the circuits, the design was straightforward; all we had to do was calculate and test the right component values. The following diagram shows how the blocks of the VCO connect:

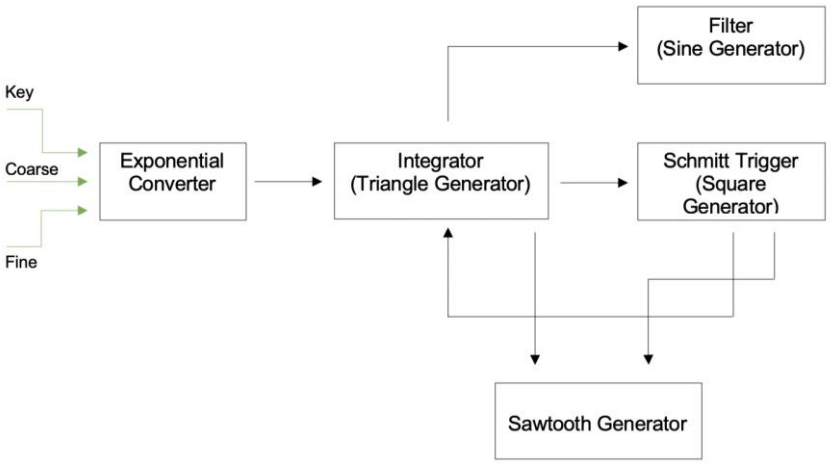
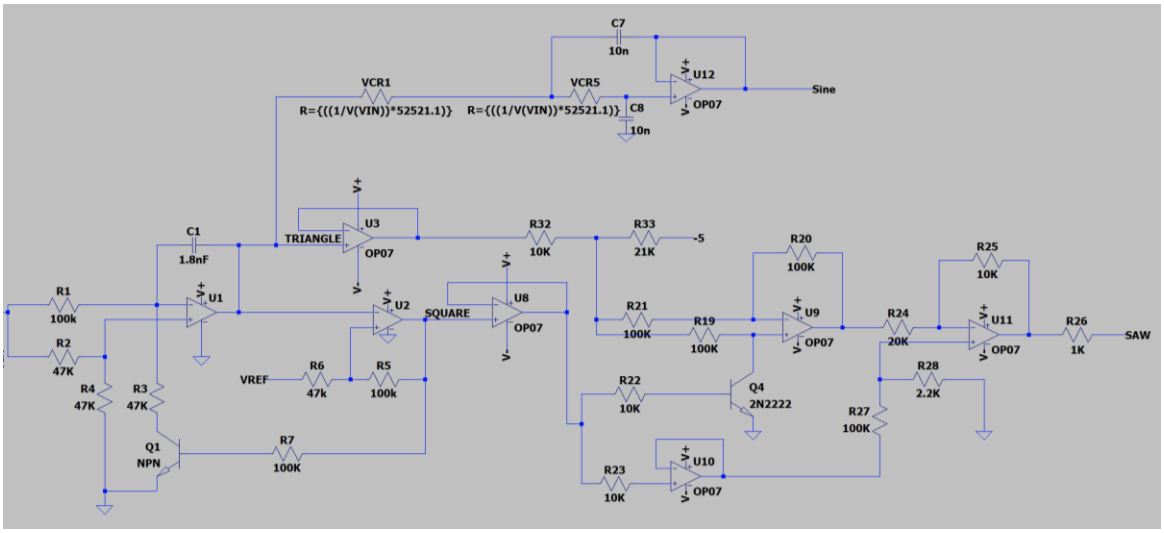


Figure 3: Connection of VCO circuits

On LT-Spice, the design of the VCO core is:



Schematic 2: VCO core

The Exponential Converter

The relationship between the input voltage to the VCO and the output frequency of the wave is exponential. This relates to the properties of human hearing, since humans do not perceive linear changes in frequency, but rather logarithmic. A note with double the frequency (one octave higher) has a higher pitch, but sounds the same as the note with half the frequency. For example, changing the frequency of a note from 55Hz (A1) to 110Hz (A2) is perceived to be a change of one octave, and A3 in the next octave is at 220Hz [5]. Using our formula, $f = 2^{V+4.781}$, we can create the following table relating the frequency of every note on the 88-key keyboard with the right input voltage to generate that note:

Note	Frequency (Hz)	Voltage
A0	27,50	0,000360
A#0/Bb0	29,14	0,083929
B0	30,87	0,167134
C1	32,70	0,250219
C#1/Db1	34,65	0,333783
D1	36,71	0,417101
D#1/Eb1	38,89	0,500327
E1	41,20	0,583572
F1	43,65	0,666910
F#1/Gb1	46,25	0,750381
G1	49,00	0,833710
G#1/Ab1	51,91	0,916941
A1	55,00	1,000360
A#1/Bb1	58,27	1,083681
B1	61,74	1,167134
C2	65,41	1,250439
C#2/Db2	69,30	1,333783
D2	73,42	1,417101
D#2/Eb2	77,78	1,500327
E2	82,41	1,583748
F2	87,31	1,667075
$F^{\#}{}_2/G^{b}{}_2$	92,50	1,750381
G2	98,00	1,833710
G#2/Ab2	103,83	1,917080
A2	110,00	2,000360
A#2/Bb2	116,54	2,083681
B2	123,47	2,167017
C3	130,81	2,250329
C#3/Db3	138,59	2,333679
D3	146,83	2,417003
D#3/Eb3	155,56	2,500327
E3	164,81	2,583660
F3	174,61	2,666992
F#3/Gb3	185,00	2,750381
G3	196,00	2,833710
G#3/Ab3	207,65	2,917010
A3	220,00	3,000360
A#3/Bb3	233,08	3,083681
B3	246,94	3,167017
C4	261,63	3,250384
C#4/Db4	277,18	3,333679
D4	293,66	3,417003
D#4/Eb4	311,13	3,500374
E4	329,63	3,583704
F4	349,23	3,667034
F#4/Gb4	369,99	3,750342
G4	392,00	3,833710
G#4/Ab4	415,30	3,917010
A4	440,00	4,000360
A#4/Bb4	466,16	4,083681
B4	493,88	4,167017
C5	523,25	4,250357
C#5/Db5	554,37	4,333705

D5	587,33	4,417028
D#5/Eb5	622,25	4,500351
E5	659,25	4,583682
F5	698,46	4,667034
F#5/Gb5	739,99	4,750362
G5	783,99	4,833691
G#5/Ab5	830,61	4,917027
A5	880,00	5,000360
A#5/Bb5	932,33	5,083697
B5	987,77	5,167031
C6	1046,5	5,250357
C#6/Db6	1108,73	5,333692
D6	1174,66	5,417028
D#6/Eb6	1244,51	5,500362
E6	1318,51	5,583693
F6	1396,91	5,667023
F#6/Gb6	1479,98	5,750362
G6	1567,98	5,833691
G#6/Ab6	1661,22	5,917027
A6	1760,00	6,000360
A#6/Bb6	1864,66	6,083697
B6	1975,53	6,167024
C7	2093,00	6,250357
C#7/Db7	2217,46	6,333692
D7	2349,32	6,417028
D#7/Eb7	2489,02	6,500362
E7	2637,02	6,583693
F7	2793,83	6,667029
F#7/Gb7	2959,96	6,750362
G7	3135,96	6,833691
G#7/Ab7	3322,44	6,917027
A7	3520,00	7,000360
A#7/Bb7	3729,31	7,083693
B7	3951,07	7,167028
C8	4186,01	7,250360

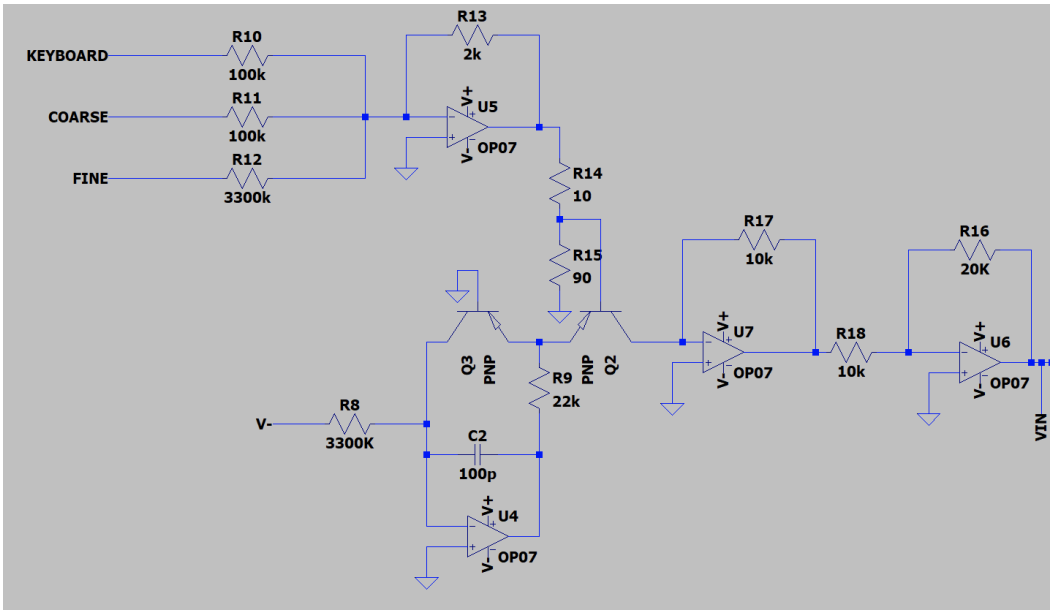
Table 1: Notes, frequencies, and required input voltages

We observe that for a 1V increase in input voltage the output frequency doubles (e.g. A4 at 440Hz, generated by a voltage of 4.000360V, and A5, at 880Hz, generated by 5.000360V). Given that the input voltage controls the output frequency, it is convenient to translate the linear input voltage into an exponential voltage, before feeding it into the oscillator, which will then be proportional to the output frequency by some constant. The most suitable component for this task would be a BJT, which is known for its exponential properties, using the Ebers-Moll equation [6]:

$$I_c = I_s \exp\left(\frac{V_{BE}}{V_T}\right)\left(1 + \frac{V_{CE}}{V_A}\right),$$

where $V_T = \frac{kT}{q}$, k the Boltzmann constant, T the temperature in Kelvin, q the electron charge, V_{BE} the base-emitter voltage, I_s the saturation current, I_c the collector current, and V_A the Early voltage. Therefore, using BJTs, we can approximate that for a linear increase in V_{BE}, there will approximately be a doubling in I_c, can cause a doubling in voltage, when driven through a resistance. Implementing this task is the function of the exponential converter [7].

The exponential converter takes as inputs the constant voltage generated by the keyboard when a key is pressed, as well as coarse and fine-tuning inputs, coming from potentiometers handled by the user. The resistance connected to the fine-tuning input is much higher than the other two, since it controls a more precise function. All three are inputted into an inverting summing amplifier, and then 90% of the amplifier's output is inputted into the base of a PNPBJT. We require small changes into the base of Q2, so as to keep the collector current in an operational range, and not damage the BJT. For the design of the exponential converter, we considered using NPN transistors instead of PNP, connecting the inputs to the reference transistor instead, and connecting R8 to the positive power rail. However, after experimenting with all these choices, we found that the one that worked best, and generated the right values of current and voltage, with the correct sign was the design below, which was based on designs from [7] and [8]:



Schematic 3: Exponential Converter schematic

The summing amplifier has negative feedback, which means we can approximate $V_+ = V_- = 0V$. Performing nodal analysis at the input of the summing amplifier:

$$\frac{-KEYBOARD}{100k} + \frac{-COARSE}{100k} + \frac{-FINE}{3300k} + \frac{OP07\_OUT}{2k} = 0$$

$$\therefore 33KEYBOARD + 33COARSE + FINE + 1650OP07\_OUT = 0$$

This relationship relates the output to the keyboard and the coarse and fine-tuning potentiometers, which are all user inputs. Coarse and fine tuning might be needed for the notes at the two extremes of the 88-key range, given that the doubling of the wave's frequency is only approximated by the BJT's properties, and not exactly met.

Assuming $COARSE = FINE = 0V$:

$$33KEYBOARD = -1650OP07\_OUT \ \therefore OP07\_OUT = -0.02KEYBOARD$$

And after the potential divider: $V_{B2} = -0.9 \times 0.02KEYBOARD = -0.018KEYBOARD$

Therefore, a 1V increase in the keyboard voltage causes an 18mV decrease of the voltage on the base of Q2. Every time V_{BE} doubles, I_c becomes $I_s(\exp\left(\frac{V_{BE}}{V_T}\right))^2$, and therefore is roughly doubled.

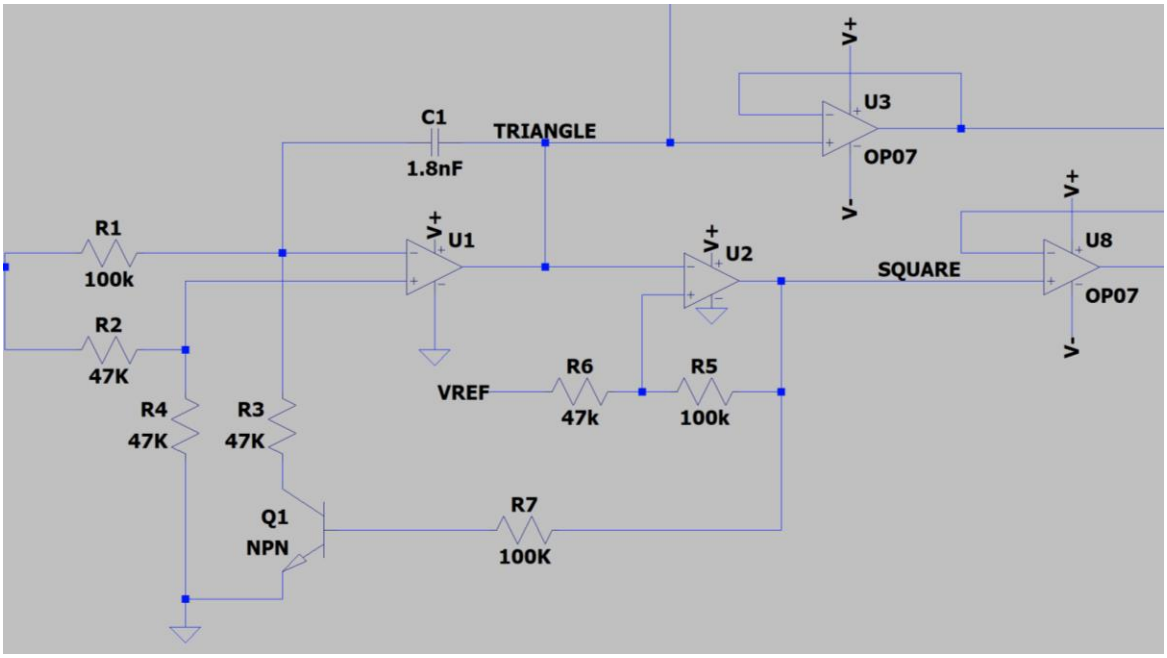
The left part of the exponential converter contains the reference transistor, which sets the current into the emitter of Q2. The amplifier U4 has negative feedback, therefore $V_+ = V_- = 0V$. The voltage drop across R8 equals $-15V$, and the current through it is -4.5μA. The function of the R8 resistor is to drive a constant current into Q2. Given that both the base and the collector of Q3 are grounded, the reference transistor is always biased at active mode. The op amp U4 ensures the emitters of the BJTs are biased so as to keep -4.5μA flowing through Q3. Changes in temperature will cause the op amp to drive its output to a new voltage to keep the same current flowing. R9 ensures that the current through the BJTs will not be too high [9].

Since Q2 has been biased on active mode, as we continue decreasing the voltage on the base, the output current I_c will keep doubling. This current will then flow through the inverting amplifier U7, causing a voltage drop across the 10k resistor,

which will be amplified with a gain of -2 by U6. Finally, U6's output is inputted into the core.

Although using two inverting op amps (U7 and U6) is slightly wasteful, we could not use a single non-inverting one, since that did not give a path for the current generated by the exponential converter to reach the oscillator core. We also required positive voltages into the core, and therefore we had to use two inverters. In a future design, we could find a solution that serves the same purpose more efficiently. Another important point to note is that the BJTs should ideally be matched and kept at the same temperature, which practically would be implemented by placing them as close as possible on the IC.

Triangle and Square Generator Design



Schematic 4: Triangle and Square generator

The triangle and square-generating circuits are connected in a feedback loop [7]. The triangle wave is obtained at the output of an integrator, through the charging and discharging of a capacitor. The square wave is obtained at the output of a Schmitt trigger connected to the output of the integrator. The Schmitt trigger uses positive feedback to act as a comparator. It seeks to maximize the difference between $V_+$and $V\_$:

$$Vout = A(V_+ - V\_)$$

where A is the gain of the op amp, ideally very large, and V_+ and V_- are the voltages at the input terminals of the trigger.

The Schmitt trigger is a bistable multivibrator, meaning it has two stable states, and it only changes from one to the other once appropriately triggered [10, p. 1217]. Here, the positive rail of the op amp is connected to $V_+ = 15V$, and the negative to ground. So the output switches between 15V and 0V. We need to find the values needed at V_- during the high and low stages of the square wave to cause the switching.

When the square wave is at 0V, for U2, $V_+ = V_{REF} \times \frac{100k}{147k} = 2.5 \times \frac{100k}{147k} = 1.701V$. Therefore, we need the output of U1 to reach 1.701V for the square wave to switch to 15V. When square is low, Q1, which here is used as a switch, does not conduct. This C1 is charging through R1, causing the output of U1 to fall, according to the equation:

$$i(t) = C\frac{dV}{dt} \therefore v(t) = \frac{1}{C}\int i(t)dt$$

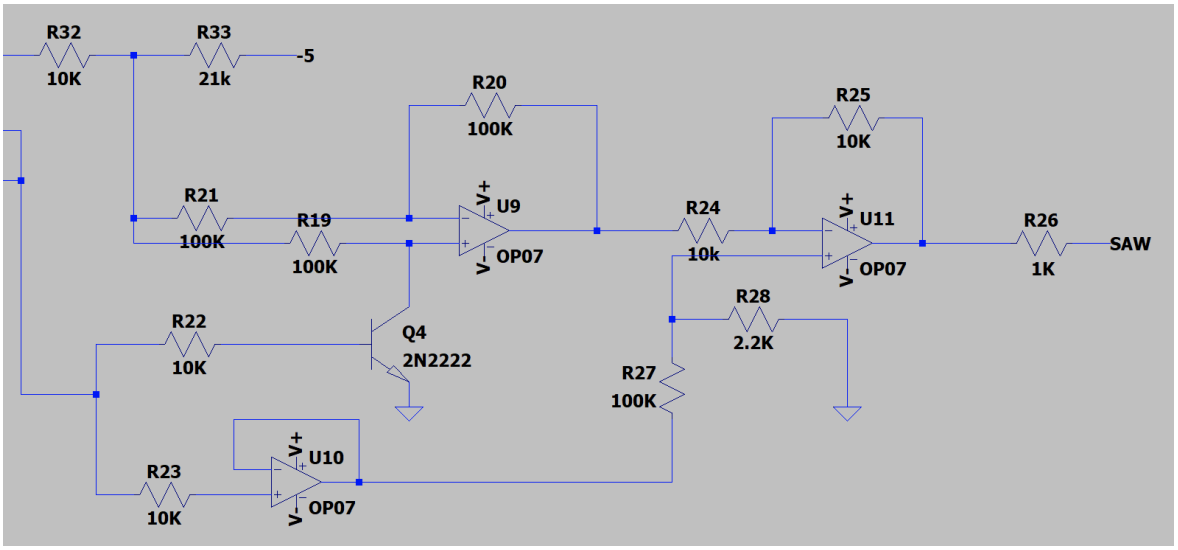
Given that $i(t)$ flowing through the 100k resistor is constant, its integral will be a linear function of time. We also know that $i(t)$ is the current through R1, and therefore should equal $\frac{V(R1)}{R1}$. Because of negative feedback at U1, $V_+ = V_- = \frac{V_{in}}{2}$, so $V_{R1} = \frac{V_{in}}{2}$. Therefore, the current charging the capacitor is $I_{C1} = \frac{V_{in}}{200k}$. A doubling in V_{in} will cause a doubling in I_{C1}, hence a doubling in the rate of charging of the capacitor, and also in the frequency of the output wave.

The time constant of the capacitor during this stage is $\tau = RC = 100k \times 1.8n = 180\mu$. Therefore, $v(t) = -\frac{1}{C}\int i(t)dt = \frac{1}{-2RC}\int V_{in}dt = -\frac{1}{360\mu}\int V_{in}dt$. Finally, to find the frequency of the wave, we just have to solve for the time needed for $v(t)$ to reach $1.701V$, which will give the time during which the triangle wave decreases. We can also find the time when the V_C reaches $1.701V$ using the capacitor charging equation, $V_C = V_{in}(1 - e^{-t/RC})$.

When the square wave is at 15V, for U2, $V_+ = (V_{REF} - 15V) \times \frac{100k}{147k} + 15V = -12.5 \times \frac{100k}{147k} + 15V = 6.4966V$. Therefore, the output of U2 will increase until it reaches $6.4966V$. During this state, the BJT will be turned on, and will have roughly 0.7V on its base, and a base current of 143µA. Considering the transistor as a switch, during this state, the capacitor will discharge through Q1, again based on the equation $v(t) = \frac{1}{C}\int i(t)dt$. We can also find the time when V_C reaches $6.4966V$ using the capacitor discharging equation, $V_C = V_{in}e^{-t/RC} \therefore t = -\tau \ln(\frac{V_C}{V_{in}})$

Sawtooth Generator Design

The idea behind the final sawtooth design relied on the generation of the triangle and square waves from the previous part of the circuit. This design is based on inverting the decreasing part of the triangle wave, and shifting up the increasing part [11]. Therefore, for the sawtooth generation, we require both the triangle wave, as well as the square wave, which indicates when we should invert the triangle, and when not. We will also be using a BJT as a switch.



Schematic 5: Sawtooth generator

This sawtooth design has two phases: during the first one, the triangle wave decreases, and the square wave is low, and therefore V_B of Q4 is low, turning the BJT off. Therefore, we can represent it as an open circuit, and hence U9 is now a simple differential amplifier, and again we can approximate $V_+ = V_- = 0V$. Given that there is

close to zero input current into the amplifier's terminals, $V_+ = V_- =$ the shifted triangle wave from the potential divider.

Calling the voltage from the potential divider X, we can perform nodal analysis on the negative input terminal of U9. We know that V_+ has to be equal to X, since there is no current through R19. This means $V_- = X$, and so the voltage at the op amp's output equals X too. Hence, U9 simply buffers the triangle. We will name its output Y. U10 also buffers 0V at its output, and sets $V_+ = 0V$ for U11. Finally, U11 inverts Y, and passes it into the SAW output. Overall, during the low phase of the square wave, the triangle wave just gets inverted.

During the high phase of the square wave, we expect the voltage on the base of Q4 to be 0.7V, and the input current to the base to be 143μA, and the BJT should be conducting. This pulls the V_+ of U9 to ground, making U9 an inverting amplifier with unity gain. U10 will also now buffer a voltage of 15V to its output, which means that for U11, $V_+ = 15 \times \frac{2.2k}{102.2k} = 0.323$. Performing nodal analysis at V_- of U11, where its output is Z:

$$\frac{0.323 - Y}{10k} + \frac{0.323 - Z}{10k} = 0 \therefore Z = 0.646 - Y$$

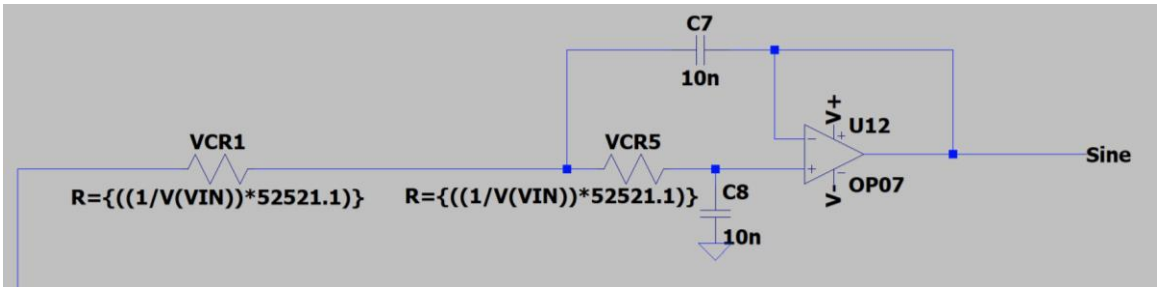
From the output of U9, we had that $Y = -X$, which we can substitute into the above equation: $Z = 0.646 + X$. Therefore, during the low stage of the square wave, we invert the triangle wave, and during the high stage, we shift it upwards.

One limitation of this sawtooth generation design is the fact that there is a discontinuity and distortion at the point where the triangle wave's gradient changes. This makes the final wave less clean than it would be if it had been generated with another method.

Sine Generator Design

The main idea behind the generation of the sine wave was obtained by considering the representation of the other waves in the frequency domain. Since all waves contain the fundamental frequency of a note as well as higher harmonics, we

can obtain the pure sine wave with only the fundamental frequency by filtering all higher harmonics, at the right corner frequency to attenuate them enough, similar to what M. Stitt does in [12]. For this purpose, we fed a triangle wave into a Low-Pass Sallen-Key filter:



Schematic 6: Sine generator

$$\frac{V_{sine}}{V_{in}} = \frac{1}{(j\omega\, RC)^2 + 2j\omega\, RC + 1} \qquad f_c = \frac{1}{2\pi RC}$$

After the exponential converter we know that:

$$f_c \propto k\, V(Vin)$$

Where: k can be found to be $k \cong 0.0033$

This gives the following relationship between control-voltage and required resistance:

$$R = \frac{1}{2\pi \frac{V}{k} 10^{-8}} = \frac{52{,}521.1}{V(Vin)}$$

The resistance is controlled by a function of VIN, the voltage at the output of the exponential converter into the oscillator core, and it determines the cutoff point.

Testing the VCO design

To confirm the VCO is working, we tested it for different keyboard voltage inputs, and looked at the different wave shapes generated. We investigated also their frequency-domain representation, to check that the fundamental frequency was at the frequency we expected. Plots 1-4 in the Appendix show the wave shapes for E3 and E4 in the time and frequency domain. The waveforms generated have different

amplitudes and are centered around different values. However, they can all be amplified, and they are all audible. The shapes of the triangle, square and sine waves are almost ideal. The sawtooth does not look as good as the rest, however it still follows the expected shape in an acceptable way.

The figures shown testing for the notes E3 and E4, which are one octave apart, therefore we expect the frequency to double. We expect frequencies at 164.81Hz, and 329.63Hz. From our test, we see spikes at 165Hz and 333Hz. The small offset from the actual value is expected, since the exponential converter does not exactly double frequencies, but instead multiplies by e. It will also not be significantly perceptible, and can be easily fixed by appropriate coarse and fine-tuning inputs.

Filtering stages and Voltage Controlled Filtering

Overview of VCF function

Every soundwaves that is generated in the voltage-controlled oscillator can be decomposed using Fourier Transform analysis into a weighted sum of sinusoidal soundwaves of different frequencies. Together, these waves superpose to create the frequency spectrum of the soundwave. When using a synthesizer, it might be desirable to change the waveshape or frequency of generated soundwaves which translates to changes in timbre, amplitude and possibly the pitch of the sound we are hearing. This is done by passing soundwaves through different filters which change the frequency composition of the wave by allowing certain frequency ranges to pass while attenuating others. Common filtering types include: High-Pass (HP)-, Low-Pass (LP)-, Band-Pass (BP)- and Notch filters. Their general working principle is illustrated in Figure 4, below.

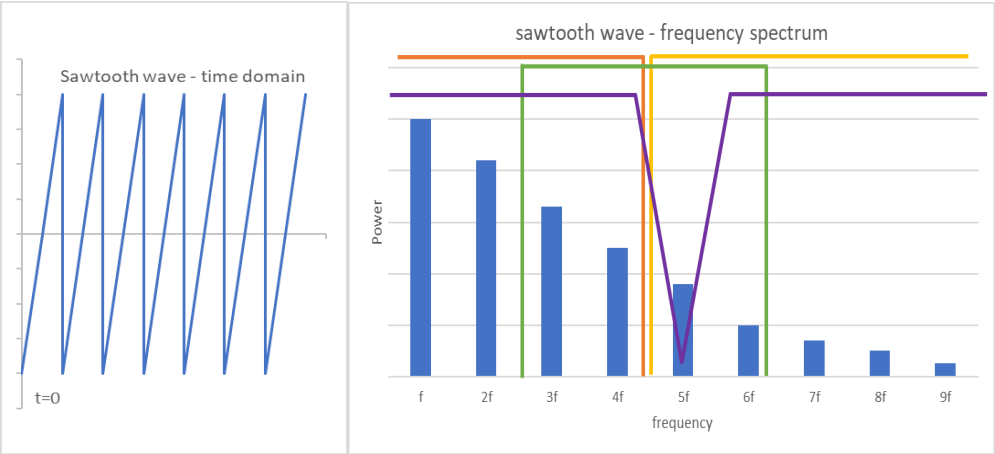
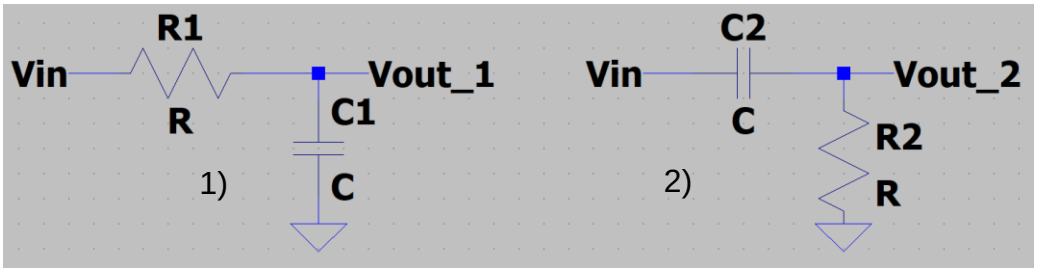


Figure 4: time and frequency representation of a soundwave combined run through different filtering types. HP – yellow, LP – orange, BP – green, Notch - purple

Design Process

Passive filters

The fundamental building blocks of every filter are resistors and capacitors. When working with alternating currents created by alternating voltage waves such as our generated soundwaves, certain arrangements can give us desired frequency responses. The most basic arrangements of these are the first order passive Low-Pass (LP)- and High-Pass (HP) filters.



Schematic 4: 1) passive LP filter and 2) passive HP filter

These filters are governed by the following transfer functions respectively:

$$LP: \frac{V_{out\_1}}{V_{in}} = \frac{1}{RC\,j\omega + 1} \quad HP: \frac{RC\,j\omega}{RC\,j\omega + 1}$$

With corner frequencies f_c given by the following equation:

$$f_c = \frac{1}{2\pi\, RC}$$

Frequencies higher than this corner frequency are attenuated at a rate of $-20\ \frac{dB}{decade}$. For a sharper frequency roll off, *i.e.* a better filtering result, filtering stages can be cascaded to create filters with higher order transfer functions.

Figure 5: Cascaded LP filters creating a higher order freq. response

For instance, the 3rd order filter shown in Figure 5, constructed from the LP filter shown in Schematic 4 has transfer function and corner frequency:

$$\frac{Output}{Input} = \frac{1}{(RC\ j\omega + 1)^3} \qquad f_c = \frac{1}{2\pi\, RC}$$

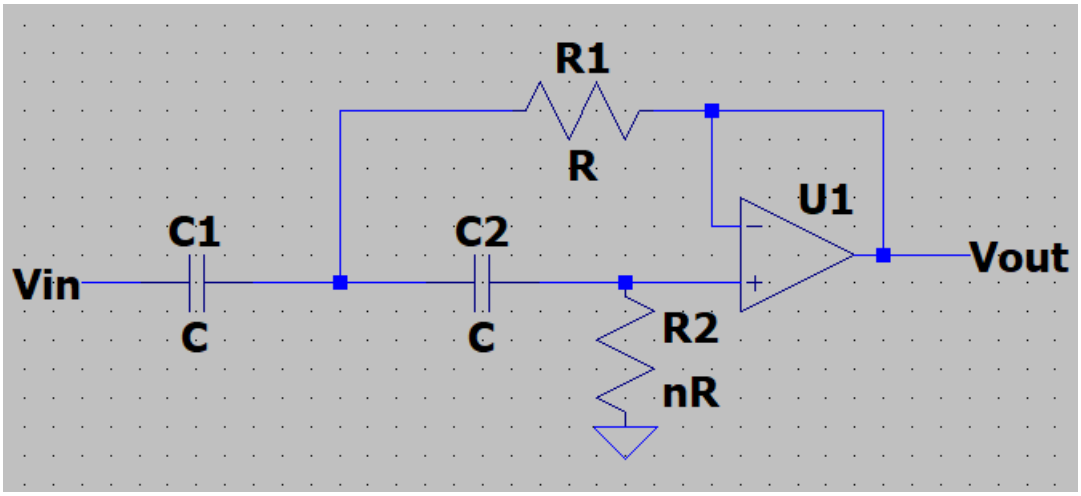
Thus, the same corner frequency is maintained while the frequency roll-off increases to $-60\ \frac{dB}{octave}$, attenuating frequencies higher then f_c 3 times as much as a single stage.

Active Filters

An alternative to passive filtering, *i.e.* filtering using passive components only, are active filters. Active filters combine passive components with amplifying elements such as operational amplifiers (op-amps) to achieve the same filtering results but with certain advantages. Just like passive filters, active filters can be cascaded to create desired frequency responses. Moreover, their high input impedances and low output impedances make their frequency response practically independent of source and load impedances [13, p. 7]. Combined with a small size, and easy gain control, they are ideal for the implementation of the filtering stage [13, p. 7].

The use of active filters also brings certain limitations such as a Power rails (omitted from schematics for simplicity), and limitations arising from the op-amp used, perhaps limiting the size of the input signal as well as the sensitivity of the design to changes in temperature [13, p. 7].

Filters such as the Sallen-Key filter (see Schematic 5) manage to create frequency responses that closely match linear approximations of filtering stages and make adjusting the filtering properties straightforward.



Schematic 5: Sallen-Key HP filter

This high-pass filter has a transfer function and corner frequency of:

$$\frac{V_{out}}{V_{in}} = \frac{n(j\omega\, RC)^2}{n(j\omega\, RC)^2 + 2j\omega\, RC + 1} \qquad f_c = \frac{1}{2\pi\sqrt{n}RC}$$

Thus, second order filter attenuates at a rate of $-40\ \frac{dB}{decade}$.

To compare the performance of our filters frequency response we refer to its quality factor (Q). The quality factor of a filter is defined as the “ratio of its bandwidth to its centre frequency” [13, p. 9] and helps us determine to find the roll-off, damping factor of a filter. The quality factor of our Sallen-Key filter shown in Schematic 5 is found using the following equations:

$$Q = \frac{1}{2\zeta} \qquad \zeta = 2\pi f_c\, RC$$

Where ζ is the damping factor of our filter and lets us gain insight on the resonance of our filter. Typically, we will look for either underdamped or critically damped systems, with high quality factors. We can change the type of the filter from HP to LP by changing the arrangement of Resistors and Capacitors.

Band-Pass filters

Another type of filtering is a band-pass filter. This filter attenuates frequencies attenuates both, frequencies higher and lower than frequencies outside of a desired frequency range. Cascading a High-Pass and a Low-Pass filter can achieve a result like this.

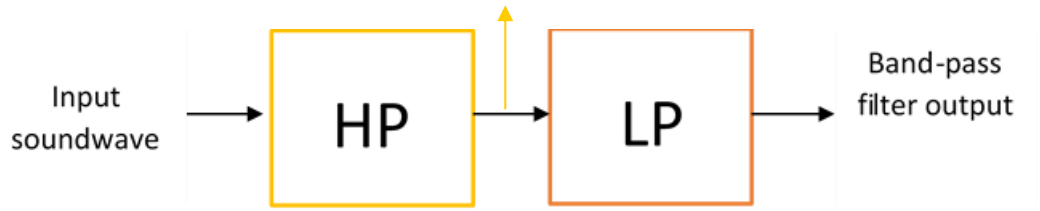


Figure 7: Cascading HP and LP filters to create BP filters

A design like in Figure 7 would be able to supply a Band-Pass as well as a High-Pass filtered soundwave. However, a second Low-Pass filter would be needed to obtain an LP filtered waveform. Therefore, another design that combines all three filtering types in one would be desirable. Thus, a second order Band-Pass filter would have a transfer function of:

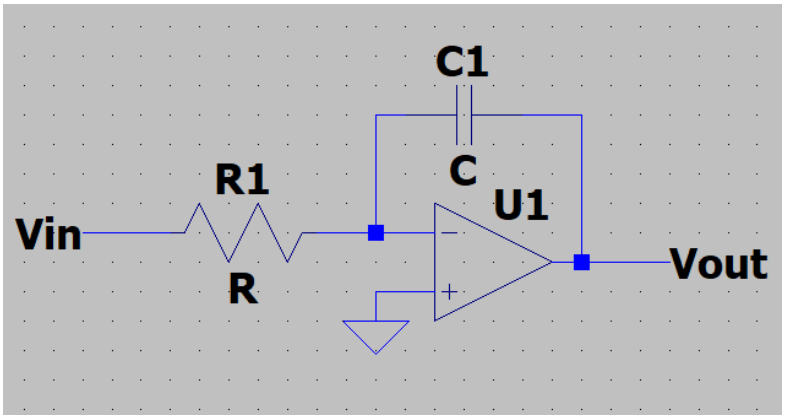
$$\frac{V_{out}}{V_{in}} = \frac{j\omega\, RC}{(j\omega\, RC)^2 + 2j\omega\, RC + 1}$$

The two-integrator-loop biquadratic ("biquad") circuit

The biquad filtering circuit makes use of two integrators to achieve a design which can potentially output HP, BP and LP filtered waveforms. To understand the general working principle of the filtering circuit, one has to get a better understanding of the integrator circuit first.

The integrator circuit

The integrator circuit is an active first order filtering circuit. Consisting of capacitor, resistor and operational amplifier.



Schematic 6: integrator circuit

It has a transfer function which can be represented in the following way:

$$\frac{V_{out}}{V_{in}} = -\frac{1}{j\omega\, RC}$$

Thus, passing a wave through an integrating circuit is equivalent to multiplying the input phasor V_{in} with the factor $-\frac{1}{j\omega\, RC}$. This will be useful when cascading integrators to achieve certain transfer functions.

General working principle of the filter

Every Filter output (HP, BP, LP, Notch) has its corresponding transfer function. When trying to achieve a certain type of filtering want to recreate this

transfer function by passing the input wave through different stages. To understand the general working principle of the biquad filter, we first consider the transfer function of a generic second order High-Pass filter (see Sallen-Key filter) [14, p. 1143]:

$$\frac{V_{hp}}{V_{in}} = \frac{Ks^2}{s^2 + s\left(\frac{\omega_c}{Q}\right) + {\omega_c}^2}$$

Where: $s = j\omega RC,\ \omega_c = 2\pi f_c$

We have established that passing a waveform through an integrator introduces a factor of $-\frac{1}{j\omega RC}$. Thus, when passing the HP-filter output waveform through integrators we can achieve the transfer functions of our filtering stages [14, p. 1117]: Passing it through one integrator stage, we obtain the transfer function as the transfer function of a Band-Pass filter (See BP–filter) [14, p. 1117].

$$\frac{(\frac{\omega_c}{s})V_{hp}}{V_{in}} = -\frac{\omega_c Ks}{s^2 + s\left(\frac{\omega_c}{Q}\right) + {\omega_c}^2} = \frac{V_{BP}}{V_{in}}$$

Integrating the resulting output again, we are left with the transfer function for a Low-Pass filtering stage (See LP-filter) [14, p. 1117].

$$\frac{(\frac{{\omega_c}^2}{s^2})V_{hp}}{V_{in}} = \frac{(\frac{\omega_c}{s})V_{BP}}{V_{in}} = \frac{{\omega_c}^2 Ks}{s^2 + s\left(\frac{\omega_c}{Q}\right) + {\omega_c}^2} = \frac{V_{LP}}{V_{in}}$$

When rearranging the equation for our High-Pass filter (multiplying both sides by $\frac{1}{s^2}$) we can obtain the following equation to relate HP-output to input voltage [14, p. 1117].

$$V_{hp} = KV_{in} - \frac{1}{Q}\left(\frac{\omega_c}{s}\right)V_{hp} - (\frac{{\omega_c}^2}{s^2})V_{hp}$$

This suggests that a High-Pass output can be obtained by summing input voltage, Band-Pass- and Low-Pass filter responses [14, p. 1117]. The general design can thus be represented in the following way:

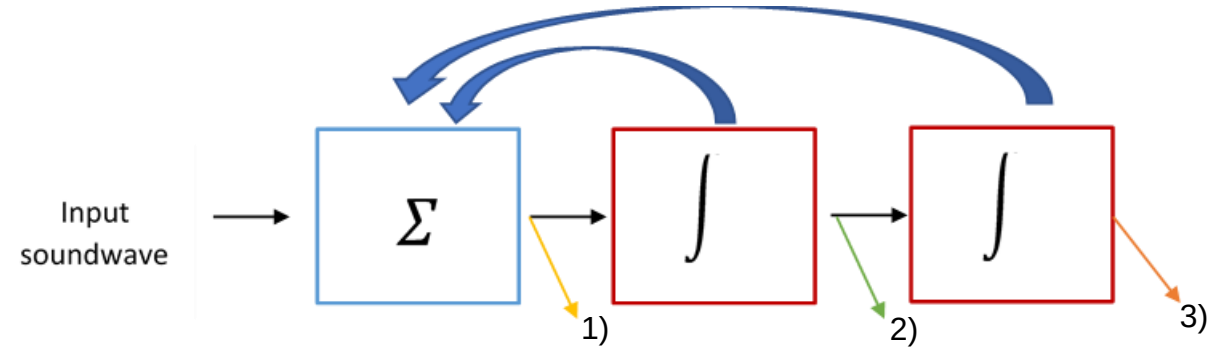
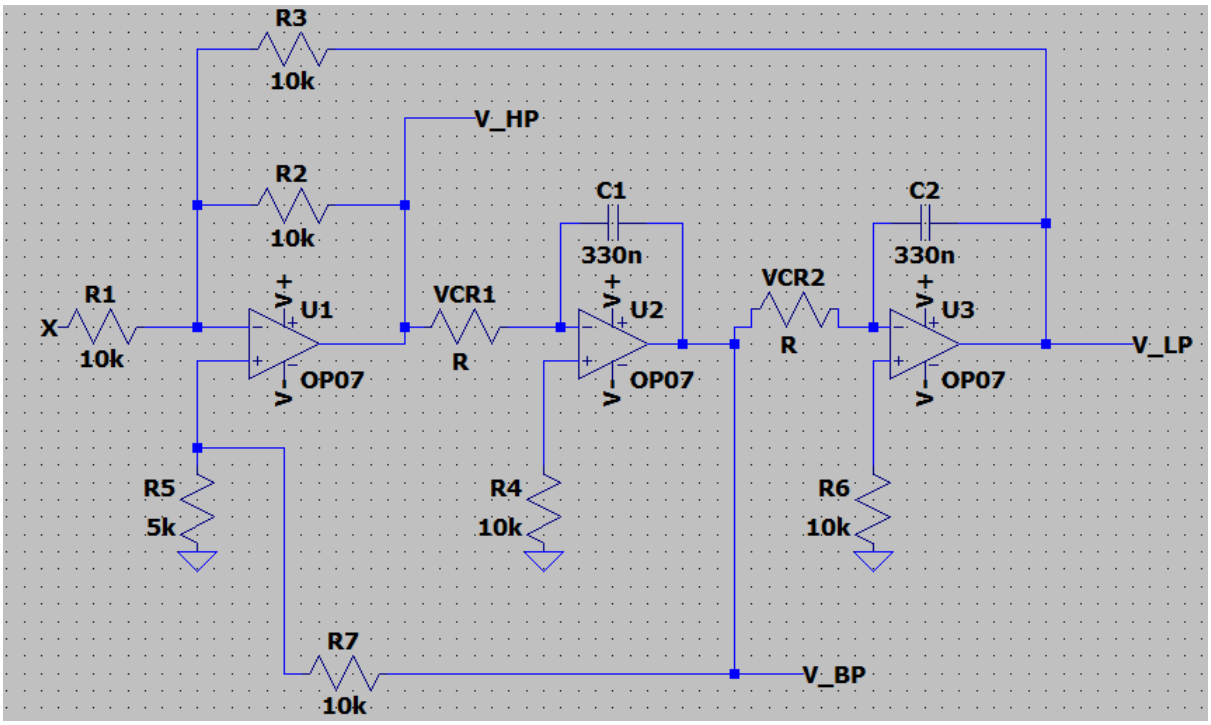


Figure 8: Block diagram of biquad filter, showing 1) HP, 2) BP and 3) LP outputs

This design was used for the final design of the filter.



Schematic 7: Final biquad filter design

The filter can be damped in different ways to create resonance effects and outputs attenuate unwanted frequencies with a roll-off of $-40\ \frac{dB}{decade}$. All Filtering types are centred around the same corner frequency f_c. This is shown below, in Figure 11.

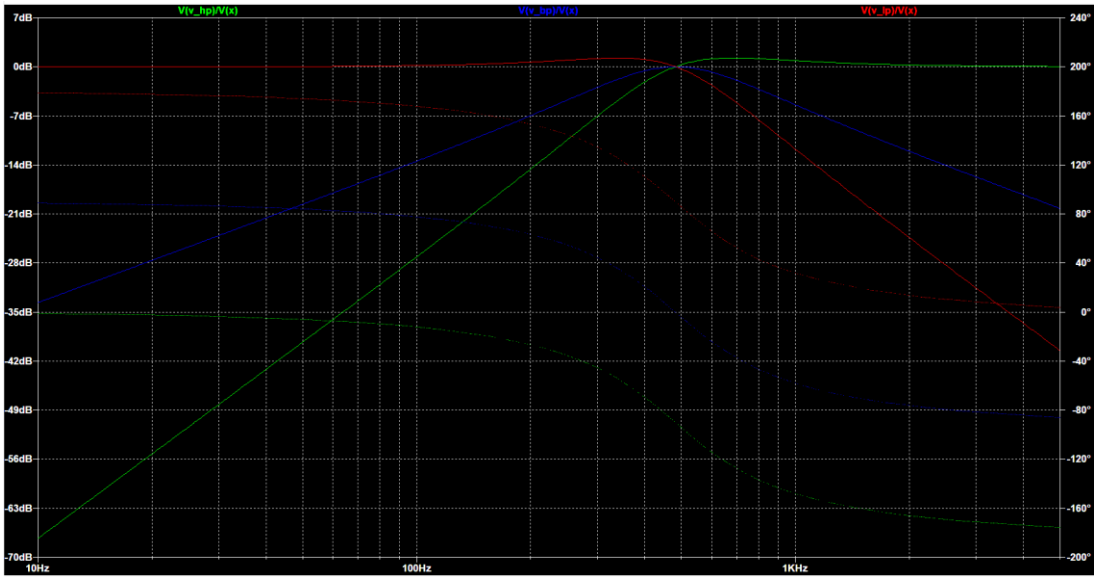


Figure 9: Example of biquad frequency response

The cut-off frequency of the HP, LP filter and the centre of the BP filter are determined by the integrator stages, and can therefore be found by the following equation:

$$f_c = \frac{1}{2\pi\, R\, C}$$

Where: $R = R(VCR1); R(VCR2),\ \ C\ = C(C1); C(C2)$

To ensure that the transfer-function results in only one corner frequency, their values need to be matched. This can easily be done using a stereo potentiometer.

The resonance (damping factor) of the circuit close to the cut-off frequency can be changed by adjusting the values of R7 and R5 respectively [13, p. 180]. A desired damping factor of ζ can be achieved by matching the pair in the following way:

$$R7 = R5\frac{3-\zeta}{\zeta}$$

All other resistor values are chosen to give a gain of -1 [13, p. 180]. Filters like these can reach quality factors (Q) of more than 500 are easily obtained, making it a better fit for our filtering design [13, p. 15].

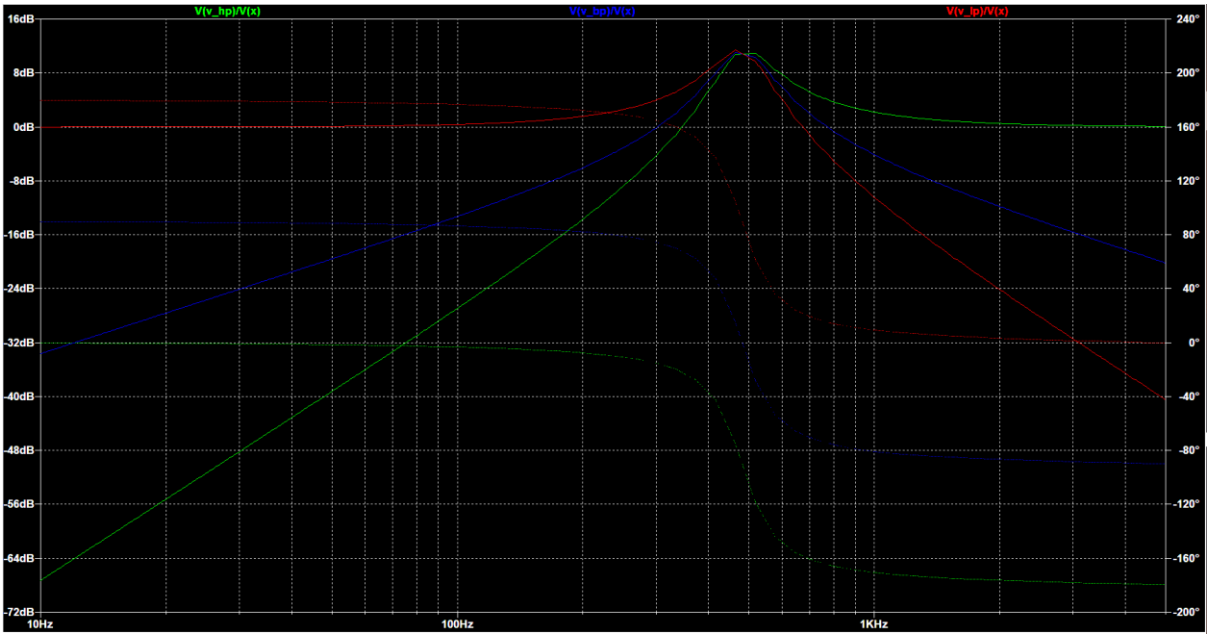
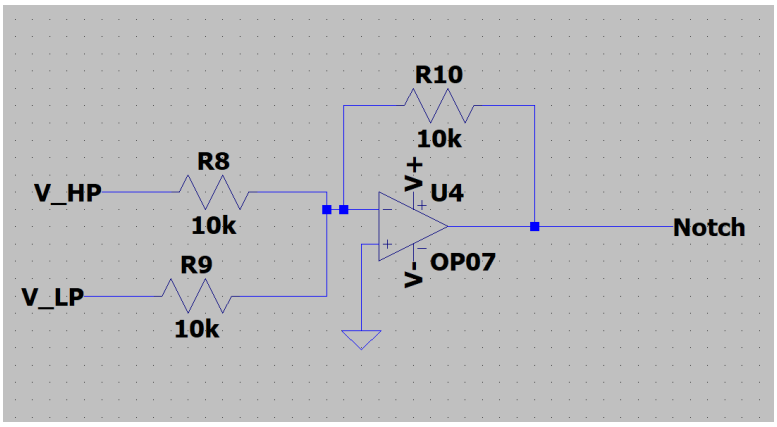


Figure 10: Resonant filter response with $\zeta = \frac{3}{11}$ (underdamped system)

Notch filter

Sometimes we might want to attenuate only a given frequency range, while allowing components of all other frequencies to pass. In these cases, a Notch filter is used. A notch Filter combines High-Pass and Low-Pass frequencies to achieve this effect, illustrated in Figure 3.



Schematic 8: Notch Filter

The second order Notch filter is governed by the following general equation [13, p. 206]:

$$\frac{V_{Notch}}{V_{in}} = \frac{s^2 + 1}{s^2 + s\left(\frac{\omega_c}{Q}\right) + {\omega_c}^2}$$

We recognise this as the non-weighted sum of High-Pass and Low-Pass filter responses. Therefore, a summing amplifier (illustrated in Figure X54574) can be used to create this type of filter. The resulting frequency response will also be centred around f_c.

Overview of frequency responses

The resulting frequency response of the filtering stage is shown in the Appendix (see Figure 15).

Voltage controlled filtering

When trying to achieve certain sound effects with a synthesizer such as tremolo, “wah” or vibrato, we want to control certain synthesizer stages with a control voltage instead of just a user command. From previous sections we know that the cut-off frequency is related to the Resistance and Capacitance of our components in the integrator circuit.

$$f_c = \frac{1}{2\pi\, RC}$$

Although variable capacitors exist, they cannot usually be voltage controlled. This leaves the resistance as the only other parameter of our integrator which we can voltage control. Ideally, we would want a building block that gives us a certain output current for a given control voltage to replace the stereo potentiometers. Their relationship should be consistent and it should respond equally well to positive and negative voltages [13, p. 199]. This “voltage-controlled resistor” (VCR) can be achieved by different designs. MOSFETs, JFETs operating in their triode/ohmic region can be for such a purpose, however, they usually are used as a grounded resistance and come with limitations when it comes to dealing with larger voltage signals [14, p. 333 et sqq].

Transconductance amplifiers

Transconductance amplifiers can be used to make resistor networks voltage controlled. Their linear relationship between voltage and frequency-controlled gain enables us to proportionally raise the gain of the device by increasing the supply of a voltage-controlled input current [13, p. 203]. Thus, we manage to obtain a “variable and controlled output current” for a controlled input current. Common devices used for such purposes are the CA3080 or the LM13700.

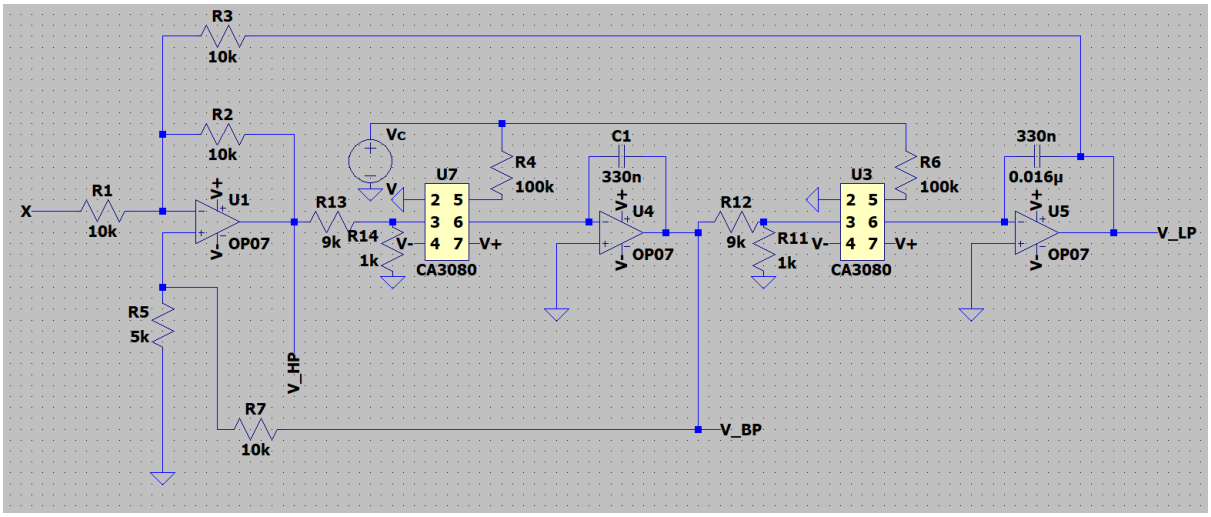
The CA 3080

The CA3080 is limited to an input voltage of 100mV due to its NPN BJT circuitry [15]. Input waveforms from the VCO therefore have to be stepped down by an amplifier stage with gain of 1:100. Furthermore, the current into the voltage control pin has to be limited as it is directly incident on the Base of another Transistor [15]. This gives us a linear relationship between the output resistor and the voltage

gain of the amplifier [13, p. 203]. Using capacitor values of $C = 330nF$ this means to filter between $10Hz - 5kHz$ we need an output resistance between approximately:

$$f_c = \frac{482.287{,}70}{R} \therefore R_{max} = 48.2k\Omega;\ R_{min} = 96\Omega$$

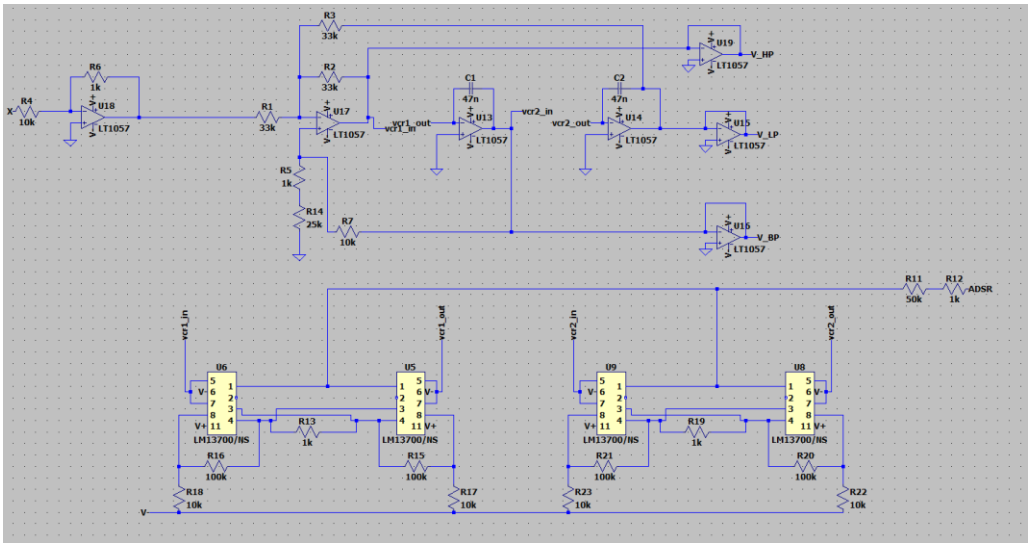
These voltage-controlled resistance should therefore be able to filter values within these bounds.



Schematic 9: Voltage-controlled filter using the CA3080

The LM13700

One alternative to the CA3080 is the LM13700 Dual Operational Transconductance amplifier chip. It combines a pair of transconductance amplifiers with two buffer stages which can be set up to connect the desired voltage-controlled resistor effect.



Schematic 10: VCF using the LM13700 IC

The transconductance amplifiers and buffers used in the design in Figure X1354 are interconnected in the following way [16]:

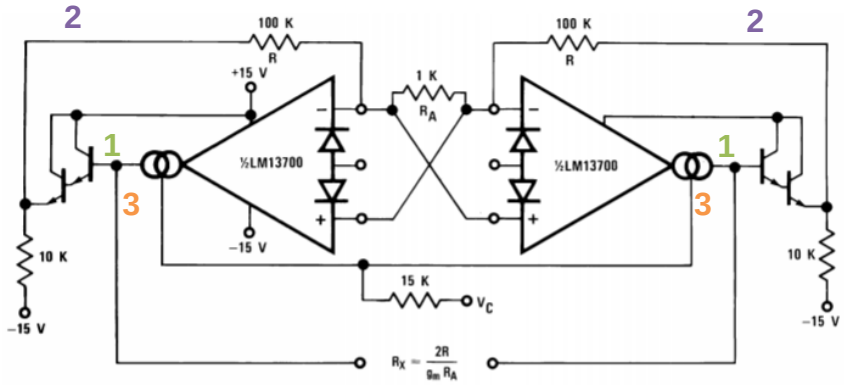
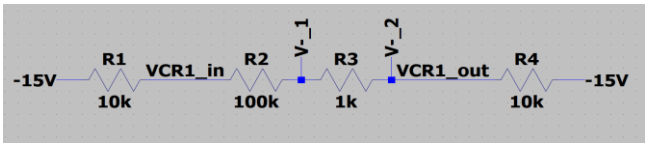


Figure 28. Floating Voltage-Controlled Resistor

Figure 11: floating voltage-controlled resistor using the LM13700 [16]

When connecting the floating voltage-controlled resistor to the network, the voltages at $VCR1\_in$ and $VCR1\_out$ (see Figure 16) are applied to the base of the BJT amplifier pair, set as a buffer stage. This buffers the input voltage which is now incident on a potential divider:



Schematic 11: potential divider stage (2)

Giving a voltage difference between the negative terminals of the amplifiers (ΔV) and the input voltages (ΔV_{in}) of:

$$\Delta V = \Delta V_{in} \frac{1k\Omega}{1k\Omega + 2 * 100k\Omega}$$

From this an output current, I_{out} (3), out of the amplifiers of [14, p. 838]:

$$I_{out} = \pm g_m \Delta V = \pm g_m \Delta V_{in} \frac{1k\Omega}{1k\Omega + 2 * 100k\Omega}$$

is generated, resulting in an equivalent resistance of:

$$\frac{V_{in}}{I_{out}} = \frac{1}{g_m} \frac{1k\Omega + 2 * 100k\Omega}{1k\Omega} = R_{eqv} = \frac{1}{g_m} 201$$

The transconductance parameter of the Amplifier can then be changed using the control voltage supplied by either an input potentiometer or functional input voltages, created by the Low Frequency Oscillator (LFO) or Envelope generator (ADSR) stages. This enables us to use the circuit with a variable cut-off point.

Amplification stage and Voltage Controlled Amplification

Overview of the VCA's function

The VCA is the final stage of the Analogue synthesizer. It is responsible for taking the signal from the output of the VCF and controlling its amplitude with regards to the control voltage signal. The inputs into the VCA are the carrier signal (the signal that undergoes alterations) and the modulating signal (the control voltage which could be the modulating signal from the ADSR, from the LFO or simply from a

potentiometer controlled externally). The VCA only consists of one output: the output of the altered carrier signal.

Seeing as the VCA effects the amplitude of the signal, the VCA not only controls how loud the signal sounds from the speaker but also achieves the musical effect called Tremolo which is a “modulation effect that rhythmically changes the volume of the signal” [17]. The Tremolo effects usually comes from the modulating signal from the ADSR. For instance, a sine wave would produce a mellow smooth sound whilst a triangle wave from the ADSR, with its sharp straight lines and edges, would produce more discrete cut-through sound [17]. It is the VCA that produces the rate at which the sound changes in addition to the ‘depth’ which determines the extent to which a signal is deafened. It is the VCA which quiets down at the end of a note as well as preventing the output from continuously sounding like the VCO signal.

For the purposes of our synthesizer, we will use a ‘two quadrant’ VCA; A VCA that produces no output if the control voltage is equal to or below 0V [18].

Design Process

The block diagram of a VCA looks like Figure 12 below:

Figure 12: Block Diagram of VCA

Conceptual Design Stage

We created a macro-block diagram of the sub-sections consisted within the VCA as shown in Figure 13 below. There were four key main areas as shown below.

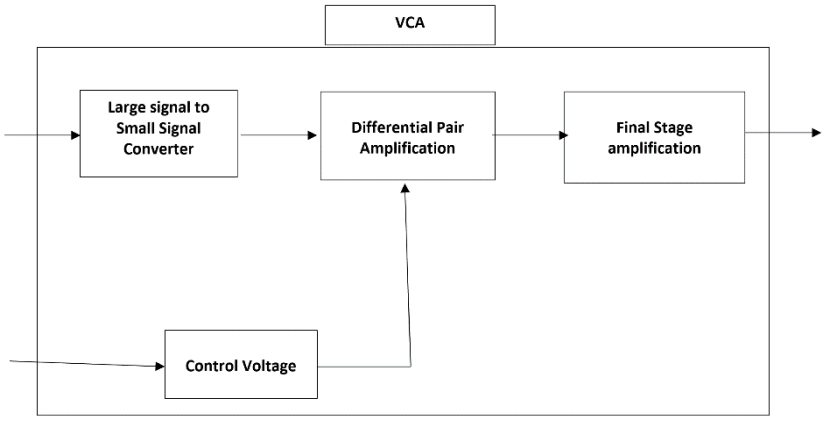
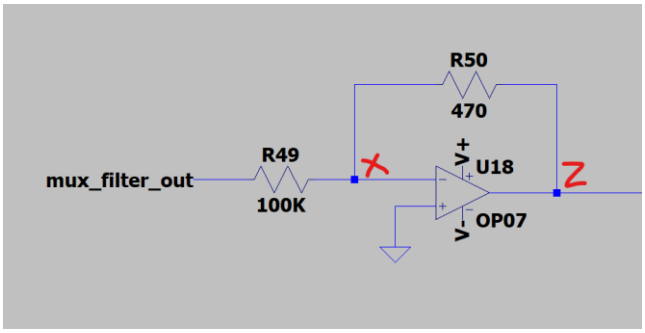


Figure 13: Sub-sections of VCA

Large Signal to Small signal Converter



Schematic 12: Input amplifier of VCA stage

This converts the input signal from a large signal to a small signal through an inverting opamp. Nodal analysis gives us:

$$\frac{X - v_{in}}{100k} + \frac{X - Z}{470} = 0$$

Due to negative feedback, $v_+ = v_-$ and thus node X being a virtual ground, we get:

$$-\frac{v_{in}}{100k} = \frac{Z}{470} \rightarrow \frac{Z}{v_{in}} = -\frac{47}{10k}$$

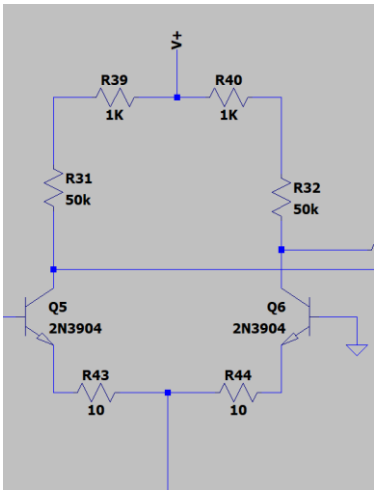
Hence, the inverting amplifier attenuates the signal by a factor of 0.0047.

The choice of 100kΩ resistor value was chosen not just for the gain factor but also because the output impedance between the previous stage was a maximum of

1kΩ. To ensure all the signal comes to the inputs of the VCA, the input resistance of the VCA was set to be very high.

Long-Tail Differential Pair

This configuration amplifies the difference between two inputs into the matched transistors by a factor of A_d (Differential Gain).



Schematic 13: Long-tail Differential Pair

It consists of two matched transistors that have their emitters coupled to the same node that is being supplied by a relatively constant current source, which in our case will be dependent on the control voltage block. As a result, one of the transistors can be thought of as operating in a common-emitter configuration whilst the other one as a emitter-follower configuration [19]. As a result of a relative constant current (I), the summation of the collector currents in transistors Q5 and Q6 will follow: $I_{Q5} + I_{Q6} = I_{tail}$.

For the synth, the input into Q5 will be the small signal outputted from the 'Large Signal to Small Signal Converter' whilst input to Q6 transistor will be grounded.

To be able to analyse this circuit with small signals, we need to know the biased conditions. The differential pair has 0V at both the inputs (V_{in1} and V_{in2}) into the transistor in addition to having $R_{31} = R_{32}$. Hence, under pure bias operating conditions, $I_{Q5} = I_{Q6}$ and since $I_{Q5} + I_{Q6} = I_{tail}$, $I_{Q5} = I_{Q6} = \frac{I_{tail}}{2}$. This will define the small-signal parameters. Hence, V_{OUT+} and V_{OUT-} (the two outputs from the differential pair) will be equivalent.

To calculate the gain, we need to find quiescent I_{Q5} and I_{Q6}.

Since $I_{Q5} = I_s \exp(\frac{V_{BE1}}{V_T})$ and $I_{Q6} = I_s \exp\left(\frac{V_{BE2}}{V_T}\right)$. dividing the two collector currents by each other gives:

$$\frac{I_{Q5}}{I_{Q6}} = \frac{\mathrm{I_s} \exp\left(\frac{V_{BE1}}{V_T}\right)}{I_s \exp\left(\frac{V_{BE2}}{V_T}\right)} = \exp(\frac{V_{BE1} - V_{BE2}}{V_T})$$

Since $I_{Q5} + I_{Q6} = I_{tail}$, $\frac{I_{Q5}}{I_{tail} - I_{Q5}} = \exp(\frac{V_{BE1} - V_{BE2}}{V_T})$. Let $V_D = V_{BE1} - V_{BE2}$, then $I_{Q5} \exp\left(-\frac{V_D}{V_T}\right) = I_{tail} - I_{Q5}$. Hence, $I_{Q5} = \frac{I_{tail}}{1+\exp\left(-\frac{V_D}{V_T}\right)}$. Similarly, $I_{Q6} = \frac{I_{tail}}{1+\exp\left(\frac{V_D}{V_T}\right)}$.

The double-ended differential gain is:

$$\frac{v_{out1} - v_{out2}}{v_d} = -g_m/(r_o//R_c)$$

Since both transistors are matched, they have the same g_m and thus: $g_m = \frac{I_{Q5}}{V_T}$. Using $I_{Q5} = \frac{I_{tail}}{1+\exp\left(-\frac{V_D}{V_T}\right)}$, the gain becomes: $A_d = -\frac{I_{tail}}{V_T\left(1+\exp\left(-\frac{V_D}{V_T}\right)\right)}/(r_o//R_c)$, implying that changing the tail current allows us to control the gain. This is significant because this allows the Control Block to vary the current based on the voltage, creating a voltage-controlled gain. Furthermore, to be able to manually control the volume of the synth, we need to be able to change the power of the output signal.

Since, $P = VI$, increasing the voltage by shifting the wave up will increase power and thus, volume. Hence, one of the R_C resistors is a potentiometer which changes its resistance based on an external knob thereby, controlling the gain as based on the formula above.

Small Signal Analysis

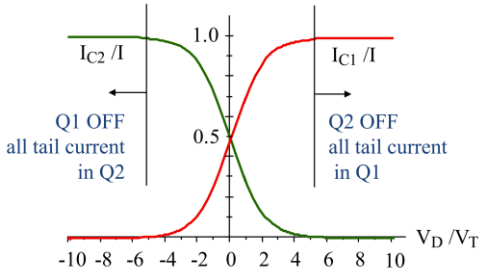
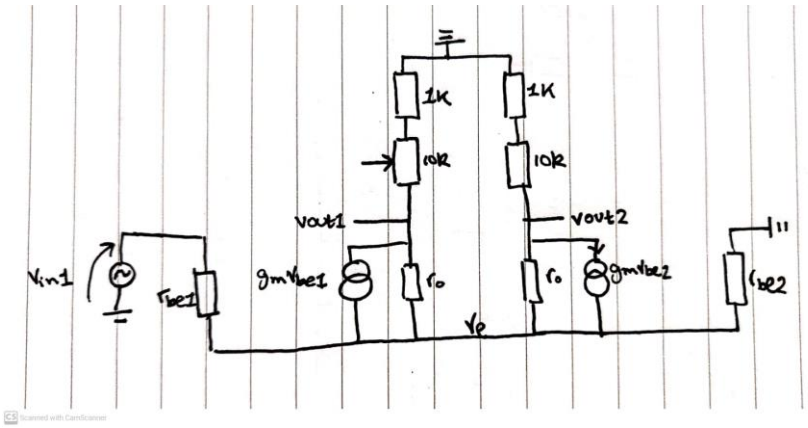


Figure 14: Collector Current vs $\frac{Input}{Thermal\ Voltage}$ [30]

A key condition for the differential pair to act properly as a differential amplifier is for the input signals to be $|v_{in}| \ll V_T$ (typically between ±50mV). Figure 14 shows that if $|v_{in}| \gg V_T$, we exit the linear region of increasing current proportionally with respect to $\frac{V_D}{V_T}$ and eventually saturate at a particular I_C current level. Note: $I_{C1} + I_{C2} = I$ condition still maintains. Hence, the 'Large Signal to Small Signal converter' was very important.

To be able to see how gain is controlled, we need to do the small-signal analysis as the input signal will be small-signal.



Schematic 14: Small-Signal Equivalent model of Differential Pair

All DC voltages, such as the V+ voltage that was above R_C and the 1kΩ resistors, have become short-circuited to ground and the BJT's have been replaced by their respective small-signal equivalent model. We can assume that the V_E is 0 based on symmetry and the fact that common-mode voltages are approximately zero and that the input voltage is a differential.

From Schematic 14, the input and output impedance of the differential pair is:

$r_{ind} = 2r_{be}$ and $R_o = R_c r_o$ [20] where $r_{be} = \frac{\beta}{g_m}$ [21] and $r_o = \frac{V_A}{I_C}$.

The input impedance for a base current of 10mA is:

$$r_{ind} = 2\left(\frac{0.025}{0.01}\right) = 5\Omega$$

Although this input resistance is very low, it played little significance because the input into the BJT was from the output of an opamp which has very low impedance.

Common-Mode Voltages and Rejection Ratio

One advantage of utilizing the differential pair is the ability to reject common-mode voltages. An ideal differential amplifier would exhibit zero common-modes.

Common-mode voltage is the average signal that is applied to both input terminals and thus is given by the formula:

$$v_{cm} = \frac{v_+ + v_-}{2}$$

The purpose of rejecting common-mode voltages is because they provide no information, they are unwanted signals for our musical purpose and are often a result of noises present within the system [22].

Since common-mode voltage is when $V_{IN1} = V_{IN2}$ (i.e. both inputs have the same potential present), the current that flows during common-mode voltage in the differential pair is symmetric ($i_{c1} = ic_2$) assuming R_C on both sides are the same. Hence, we obtain:

$i_e = \frac{V_{cm}}{2r_e}$ *where* r_e *is the output resistance of the current source* and $i_c = \propto \frac{V_{cm}}{2r_e}$

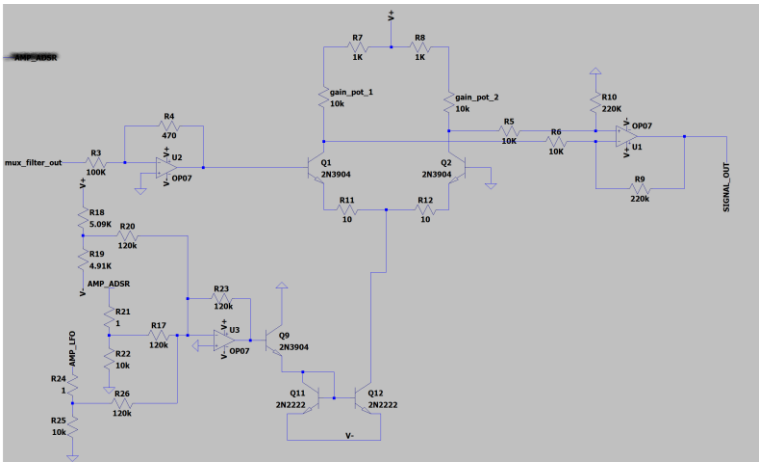
where $\propto = \frac{\beta}{\beta+1}$ [20], resulting in the common-mode gain to be: $A_{cm} = \frac{V_{out}}{V_{cm}} \approx -\propto \frac{R_C}{2r_e}$ if we neglect r_o. To reduce the common-mode gain, we could reduce the R_C value. However, this isn't feasible as not only does it reduce the gain but also, the R_C will also be manually controlled by the user in our scenario.

Instead, we could increase r_e by utilizing Wilson current mirror in place of the 33kΩ resistor in the tail. This is because the output of the Wilson mirror has the same current as the input into the Wilson mirror, but the output impedance is significantly larger. This would drastically improve the Common-mode rejection ratio (CMMR) which is the ratio between the differential voltage gain with respect to common-mode gain. CMRR has the formula:

$CMRR = \frac{A_d}{A_{cm}} = g_m R_E = \left(\frac{I}{2V_T}\right) R_E$ where $I = tail\ current$ and $R_E = tail\ resistance$.

With a tail current of 800mA which is the limit of 2N2222 transistor [23], CMRR $= \frac{0.8}{0.05} * 48{,}000 = 768{,}000$ which is high.

A high CMRR ratio drastically improves the signal-to-noise-ratio, making the output signal much less distorted. However, unfortunately, this modification into the differential pair led to problems with voltage drops and resistances which effected the overall amplification process.

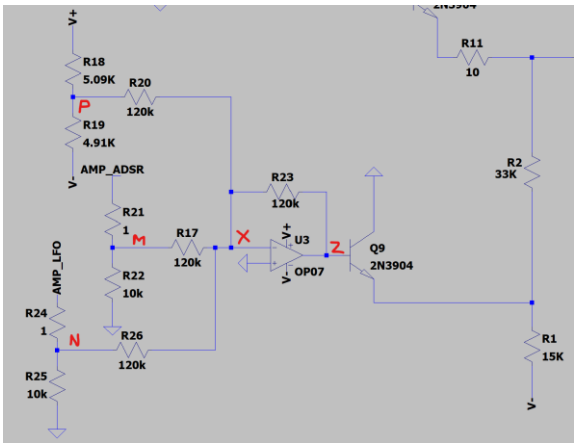


Schematic 15: Failed Design of VCA

Although replacing the R_C resistors with an active current source, such as a current mirror, can improve the gain massively, this is unneeded for our operation as the maximum gain for most synthesizers is 1 [24]. Hence, placing a current mirror at the collector ends was not used as a method to improve the CMRR.

Control Voltage

The Control Voltage Block is responsible for producing a current that's dependent on the voltage. The inputs into the control voltage block are the ADSR and the LFO. In order to be able to use both ADSR and the LFO simultaneously, we used a inverting summing voltage amplifier circuit in order to keep the gain unchanged whilst adding the inputs together. Using simply resistors wouldn't have kept the gain of the summation as 1.



Schematic 16: Control Voltage Block

From nodal analysis, we can deduce that (assuming op-amp has high input impedance and thus draws zero current):

$$\frac{X-M}{120k}+\frac{X-P}{120k}+\frac{X-N}{120k}+\frac{X-Z}{120k}=0 \rightarrow 4X-M-P-N-Z=0$$

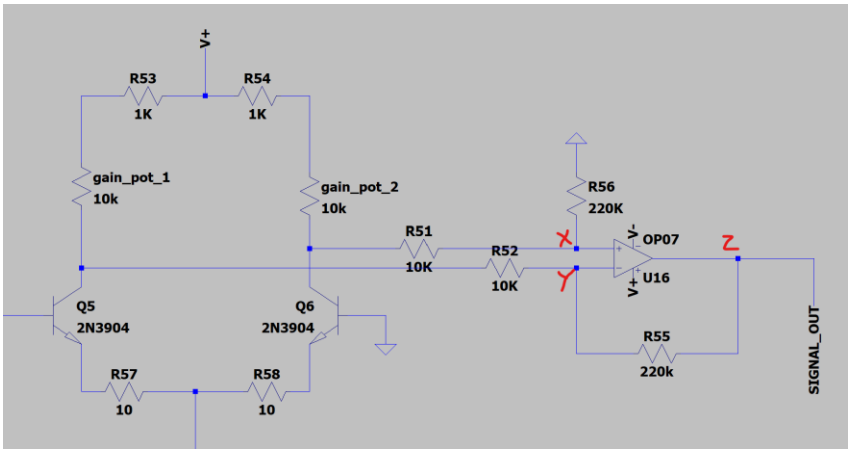
Due to negative feedback, $v_+ = v_- = 0$ and hence, $X = 0V$.

Substituting this into the previous equation gives us: $0-M-P-N-Z=0 \rightarrow Z=-(M+P+N)$, proving that this sums up all the input signals with gain of -1 as the output signal is inverted.

This causes a particular voltage into the base of the transistor and setting the voltage of the emitter of Q_9 transistor as 0.7V less compared to the base potential, almost like a follower. However, there is current amplification as $I_E = (\beta + 1)I_B$ and this current influences the tail current which results in a different gain [25].

Final Amplification Stage

This stage takes the two outputs V_{out1} and V_{out2} from the differential pair and inputs it into a op-amp to amplify the difference between V_{out1} and V_{out2} and convert it into a single output.



Schematic 17: Final Amplification Stage

The negative feedback helps control the gain of the op-amp. From nodal analysis, $\frac{X-v_{out2}}{10k}+\left(\frac{X}{220k}\right)=0$ and $\frac{Y-v_{out1}}{10k}+\frac{Y-Z}{220k}=0$. Hence, we can say:

$$\frac{X-v_{out2}}{10k}+\left(\frac{X}{220k}\right)=\frac{Y-v_{out1}}{10k}+\frac{Y-Z}{220k}$$

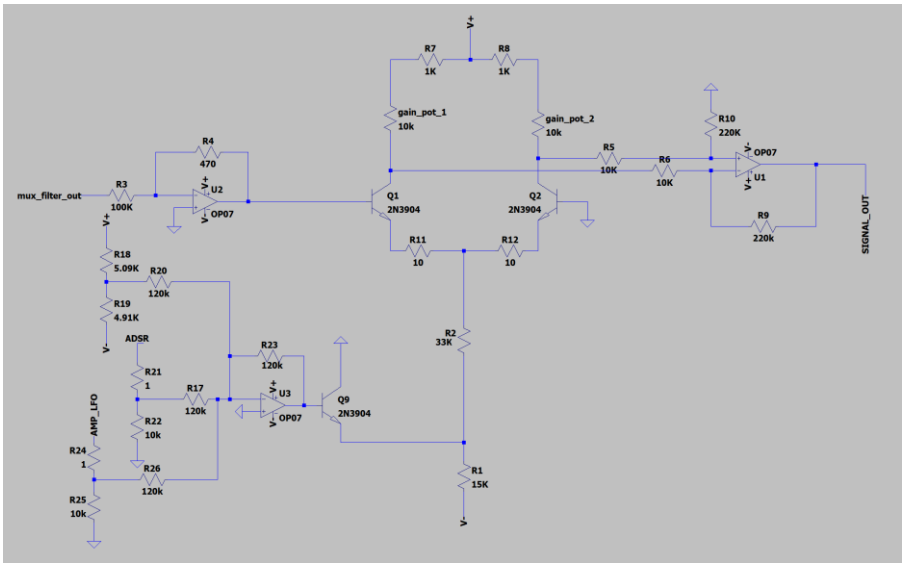
Due to negative feedback: $v_+ = v_-$ and thus:

$$\frac{X-v_{out2}}{10k}+\left(\frac{X}{220k}\right)=\frac{X-v_{out1}}{10k}+\frac{X-Z}{220k}$$

$$\frac{v_{out1}-v_{out2}}{10k}=-\frac{Z}{220k}\rightarrow\frac{Z}{v_{ou1}-v_{out2}}=-22$$

This forms the gain of the amplifier output. This can be adjusted based on the needs of the type of synth manufactured.

For the v_- input, all the input current goes through the feedback loop as opamp has high input impedance.



Schematic 18: Final VCA design [25]

To test the VCA, we first used a simple rectangular pulse from the ADSR and a sine wave input signal of 3V amplitude and frequency of 1kHz. We tested the output to see if the result was the sinewave of a particular amplitude only present when the rectangular pulse was high. The discontinuities were clear and sharp with virtually no decay curve form. Seeing as the control voltage block worked properly, we tested the entire VCA just with different ADSR inputs, then with just different LFO inputs and finally tested it with both ADSR and LFO inputs simultaneously to see if the output signal was the effect of the superposition of LFO an ADSR. The results of the are shown in the appendix (Figure 27/28).

Envelope Generator / ADSR

Similar to the Low Frequency Oscillator, the ADSR is a building block that serves as a functional input to the basic building blocks of filter and amplifier. The generated envelope can be used as a reference for how the sound of the output will change over time. A common example for a natural occurring envelope is the mechanical generation of a note on a piano. Just like a common ADSR envelope the piano initially produces sharp rise in amplitude (Attack) which is followed by a Decay in amplitude until a Sustained level is reached. This level is maintained for as long as the key is being pressed down. As soon as key is Released, the amplitude of the sound will fade out. These phase are illustrated in the Figure below:

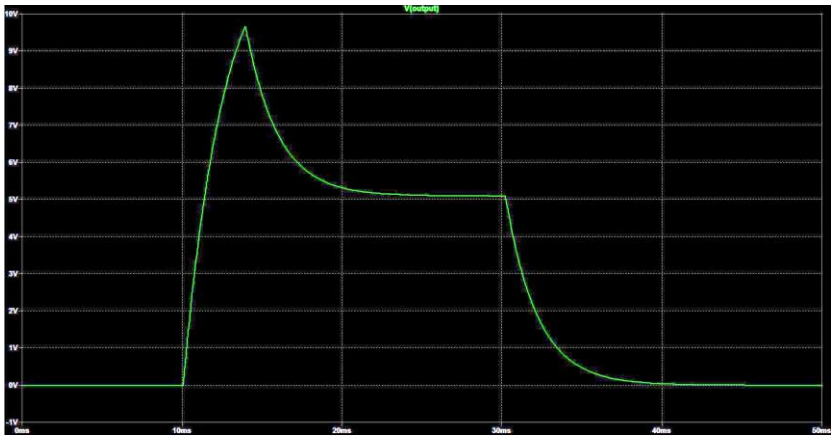
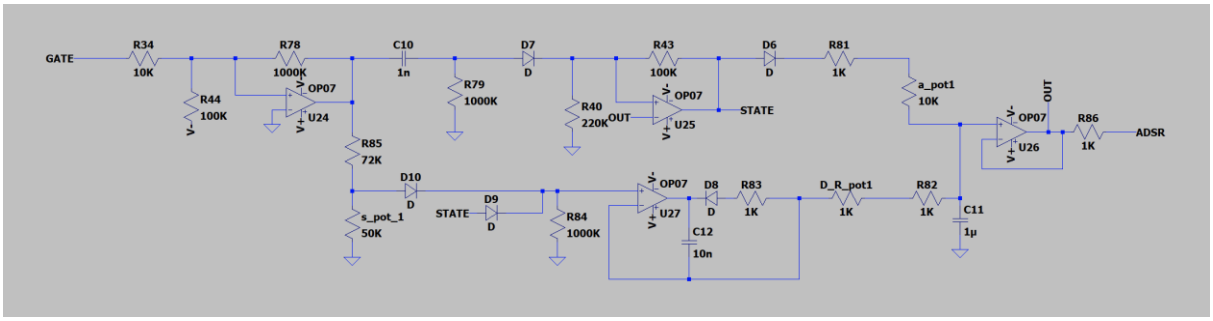


Figure 15: Typical ADSR envelope

Each parameter should be adjustable by the user to achieve the desired effect on the output soundwave. Other configurations are shown in the Appendix (Figure 29/30). For as long as a key is pressed on the keyboard, the corresponding Gate signal going into the ADSR will be high. Usually, this is a binary input, changing between Low ($0V$) and High ($5V$).

The design of the Envelope generator is based on a design by Ockeloen-Korppi [26]. This design merges control of Decay and Release to create a Variable ASR stage whose Decay and Release can only be adjusted simultaneously.



Schematic 19: ADSR envelope generator

When a Gate signal is fed into the circuit, the circuit will enter the attack stage at the rising edge of the gate signal. Opamp U24 is configured as a Schmitt trigger with a stable output of $\pm 15V$. Input voltages at its input terminal V_+ are compared to ground, *i.e.* 0V. Thus, the rising edge will cause the output of the Schmitt trigger to jump from $-15V$ to $+15V$.

U25 is connected to emulate a flip flop, which toggles the state output as soon as $OUT = V_+$. At the leading edge of the gate, the state is set to +15V. This will cause capacitor C11 to charge through the Attack potentiometer, until V_out reaches the toggling voltage of:

$$15V \times \frac{220k\Omega}{320k\Omega} = 10.3V$$

The charging of the capacitor is modelled by the following equation:

$$V_C = V_{in}(1 - e^{-t/\tau})$$

Where the time constant, $\tau = RC$, can be determined by adjusting the attack potentiometer (a_pot1). This is due to the feedback diode, D8, in the precision amplifier setup, which blocks, and effectively creates an open circuit at the Release/Decay control section.

As soon as V_{out} reaches 10.3V, STATE toggles. This causes the output of U25 to switch to -15V, reverse-biasing D6. Thus, C11 discharges through the Decay/Release potentiometer, forward-biasing D8. The capacitor will discharge according to the equation

$$V_C = V_{in}e^{-t/\tau}$$

Where τ is set by the Decay/Release potentiometer and the capacitance of C11. The discharging process will continue until V_-, and consequently V_+ of U27 (negative feedback) is equal to approximately the voltage set by the Sustain potentiometer minus $0.7V$. In this case, $V_{sustain} = 15V \times \frac{50k\Omega}{122k\Omega} = 6.15V$, therefore V_+ is smaller than or equal to $5.45V$. Only then will the diode D10 enter forward-bias, stopping the discharging process and entering the sustain phase, where it remains, until the binary gate signal switches from high to low.

At that point, the voltage at the Sustain potentiometer is set at $-6.15V$, and D10 is reverse-biased. V_+ U27 is 0V, consequently D8 is forward-biased. This allows C11 to again discharge through the Decay/Release potentiometer. It will discharge at the same rate as the Decay state.

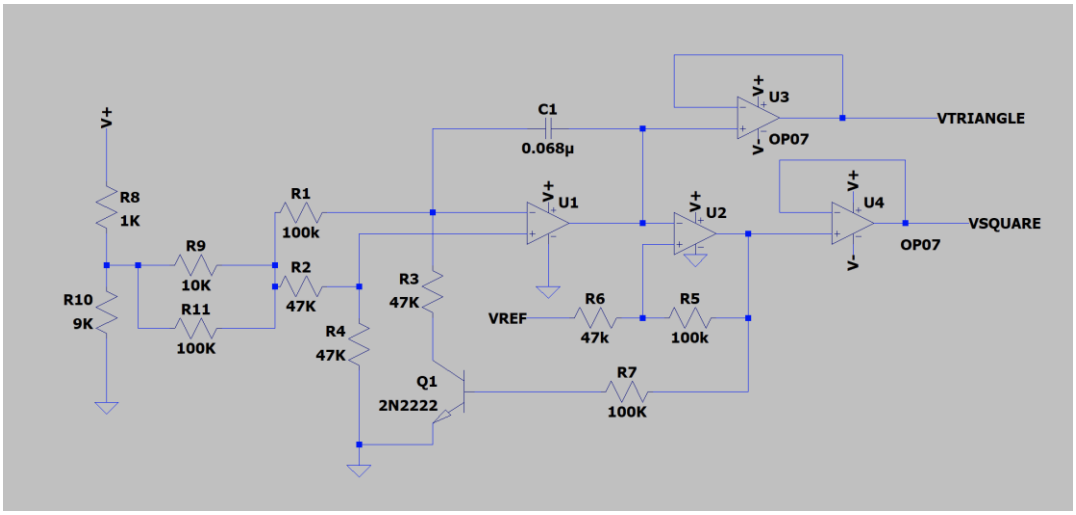
Diode	*Attack*	*Decay*	*Sustain*	*Release*
D6	Conducts	Blocks	Blocks	Blocks
D7	Leading edge of gate	Blocks	Blocks	Blocks
D8	Blocks	Conducts	Blocks	Conducts
D9	Conducts	Blocks	Blocks	Blocks
D10	Blocks	Conducts	Conducts	Blocks

Table 2: Overview of Diodes and their biases during ADSR stages

The Low Frequency Oscillator (LFO)

The Low Frequency Oscillator (LFO) offers one of the extra functionalities of the synthesizer, which can make the output wave more interesting. It is inputted both into the VCF and the VCA to modulate the waveform in terms of frequency and amplitude.

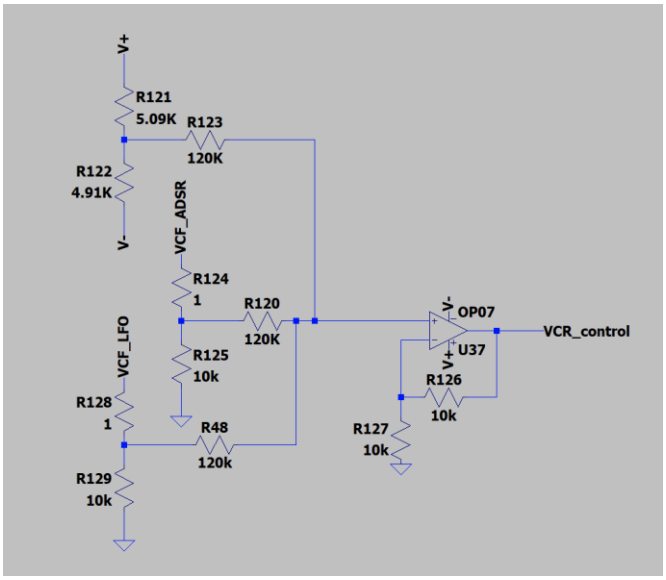
The LFO design was the same as that of the VCO, only a bit simpler. It does not require an exponential converter, and is independent of the keyboard input. Its only control voltage comes from a potentiometer (resistors R8 and R10), which is controlled by the user, and this sets the frequency between 1.5 and 34Hz. It also only generates triangle and square waves, using the feedback loop that was implemented in the VCO. We did not implement the other two to keep a simpler design, however they could be added to the design in the future.



Schematic 20: The Low Frequency Oscillator

In the VCF, the LFO is one of the inputs to the summing amplifier of Schematic 21, which generates an output controlling the resistance of the filter, which in turn controls the cutoff point, according to the equation:

$$R = \frac{827.3}{0.01 + VCR\_control}$$



Schematic 21: VCR control circuit

An increase in $VCR\_control$ causes the resistance to decrease, and therefore the cutoff point to increase. The inverse happens for a decrease in $VCR\_control$. Therefore, the voltage input of the LFO causes a slight periodic shift in the cutoff frequency of the waveform.

$$\frac{VCR_{control}}{2} = V_{-} = V_{+}$$

And:

$$\frac{V_{+} - VCF_{ADSR}}{120k} + \frac{V_{+} - 0}{120k} + \frac{V_{+} - VCF_{LFO}}{120k} = 0 \;\; \therefore V_{+} - VCF_{ADSR} + V_{+} + V_{+} - VCF_{LFO} = 0$$

$$\therefore 3V_{+} = VCF_{ADSR} + VCF_{LFO} \;\; \therefore V_{+} = \frac{VCF_{ADSR} + VCF_{LFO}}{3}$$

Substituting back:

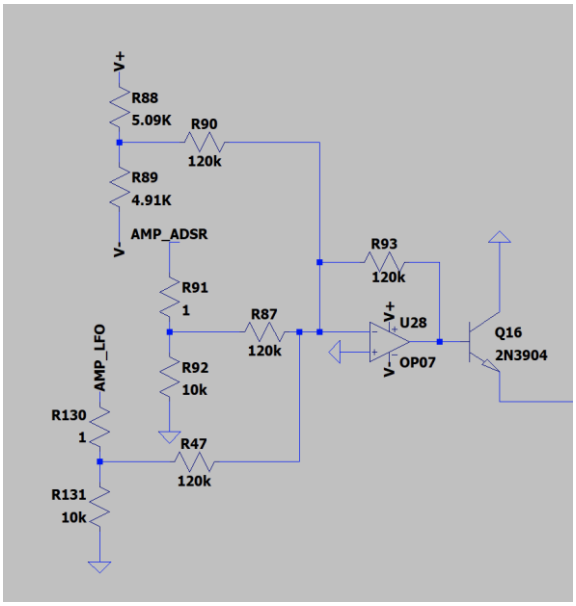
$$\frac{VCR_{control}}{2} = \frac{VCF_{ADSR} + VCF_{LFO}}{3} \;\; \therefore VCR_{control} = \frac{2(VCF_{ADSR} + VCF_{LFO})}{3}$$

And back into the equation giving the resistance:

$$R = \frac{827.3}{0.01 + \frac{2(VCF_{ADSR} + VCF_{LFO})}{3}} = \frac{2481.9}{0.03 + 2(VCF_{ADSR} + VCF_{LFO})}$$

In the VCA, the LFO is again inputted to a summing amplifier, which controls the current drawn from the differential pair. An increase in the LFO input voltage will cause the voltage at the base of Q9 to increase, and therefore the emitter current to increase, which in turn increases the gain of the differential pair and the amplitude of

the output signal. The opposite happens for negative LFO voltage. Thus we can have amplitude modulation, which is tremolo.



Schematic 22: VCA control voltage circuit

$$V_+ = V_- = 0 \ \therefore \frac{V_-}{120k} + \frac{V_- - AMP_{ADSR}}{120k} + \frac{V_- - AMP_{LFO}}{120k} + \frac{V_- - Vout}{120k} = 0$$

$$\therefore V_- + V_- - AMP_{ADSR} + V_- - AMP_{LFO} + V_- - Vout \ = 0 \ \therefore$$

$$Vout = \ -AMP_{ADSR} - AMP_{LFO}$$

Hence, the LFO can be used to affect the instantaneous cutoff frequency and amplitude of our output wave.

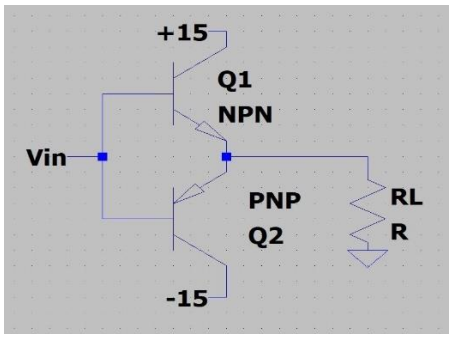
Power Amplifier

The synthesizer should be able to adequately drive a loudspeaker with an input impedance of 8Ω. A consistent power output to the loudspeaker can be achieved by running our output waveform through a power amplifier. To achieve the desired power output, the amplifying stage should have high input impedance and sufficiently low output impedance to drive the load. Furthermore, the use of transistors in our design makes our design vulnerable to high currents flowing to our

design. High currents can cause damage to these components, possibly breaking the circuit and requiring the user to replace parts or to hand it in for maintenance. In accordance to our formulated PDS, this should be kept to a minimum. Consequently, a current limit should be introduced for the design, effectively decoupling synthesizer and load.

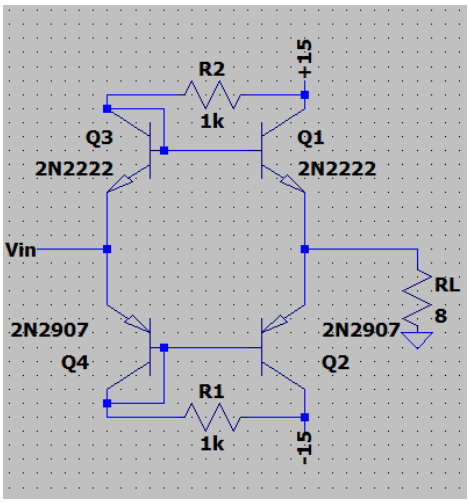
Design Process

The power amplifier is based on a common push-pull common-collector amplifier. In this class B amplifier, the NPN transistor pushes current into the load for positive voltages during a cycle while the PNP transistor pulls a current from the load during the negative part of the cycle [27].



Schematic 23: B push-pull power amplifier

Although this setup achieves Power amplification, it is limited by significant ‘cross-over distortion’ [27] as changes in the polarity of the input signal will not affect the state transistors until a threshold voltage of approximately $0.6V$ across the base-emitter junction is achieved. To reduce this distortion a DC bias current is supplied to the transistors to ensure operation in the active mode [28]. This can be achieved by connecting a current limiting resistor and diodes or diode like transistors to the base of Q1 and Q2. This creates a AB push-power amplifying circuit [27].

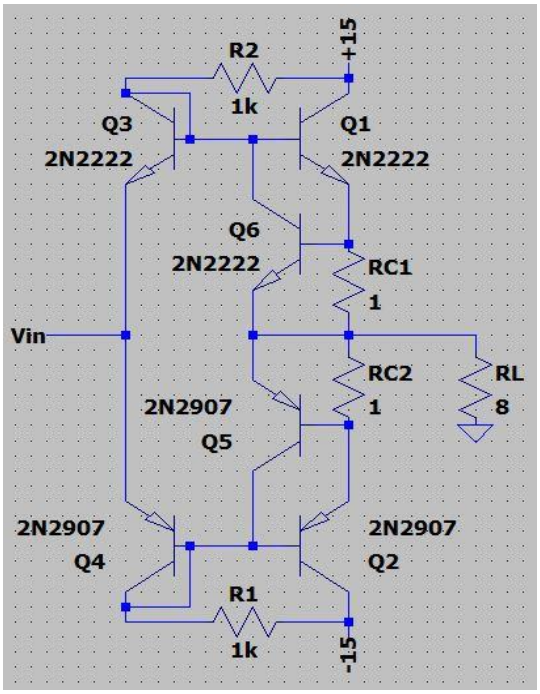


Schematic 24: AB push-pull power amplifying circuit

This arrangement of transistors will allow a current flow through the R2,Q3,Q4 and R1 circuit, causing symmetrical voltage drops of $0.7V$ (assuming the transistors are matched) across the diode like transistors either side of the input [27].

Thus, the total voltage difference of $1.4V$ between both bases biases transistors Q1 and Q2 (see Schematic 24) to constantly operate in active mode, preventing larger effects of cross-over distortion [28]. The close distance between the matched transistors also has a positive effect on the temperature stability of the circuit. The arrangement of the transistors in a current mirror ensures that variations in the output behavior are compensated in the transistor pairs (Q1, Q3 and Q2, Q4). To achieve the current limiting behavior, another pair of transistors and current limiting resistors is included in the circuit.

Current limiting Power amplifier



Schematic 25: current limiting AB push-pull power amplifier

The newly introduced transistors Q5 and Q6 will remain off, until a voltage drop of about $0.6V$ is registered across their base emitter junctions, limiting the current through RC1 and RC2 to [28]:

$$\frac{0.6V}{R_c} = \frac{0.6V}{1\Omega} = 0.6A$$

With an average voltage output of about 3.6V supplied to our speaker, we expect to drive the speaker with a maximum average power of 1.6W.

For AC currents higher than 600mA, voltages larger than $0.6V$ will be dropped across the current limiting resistors (RC1, RC2) causing the transistors Q5 and Q6 to be in forward bias. The conducting transistors will then "'rob' current" [28] from the base of the transistor in the current mirror, limiting the current flow in the circuit.

We expect the power amplifier to be the leading power consumer of our synthesizer design. Therefore, its essential to operate it with high power efficiency. The following equation can be used to investigate the maximum efficiency of our design [29]:

$$\eta = \frac{\pi}{4} * \frac{V_{AC}}{V_{SUPPLY}}$$

For a design with unity voltage gain ($\frac{V_{AC}}{V_{SUPPLY}} = 1$) , this gives us a maximum efficiency of $\eta = 78.5\%$. Moreover, the use of the bias current determining resistors R1 and R2 significantly lowers the input impedance of the circuit. With the power amplifier following up on an amplifier stage with low output impedance, this is not necessarily a major issue. However, he low input impedance can have a negative effect on the maximum peak output voltage our amplifier can supply. High voltage drops across the bias resistors (R1 and R2, combined as) can limit our maximum “swing voltage” [28] to [28]:

$$V_{swing_{max}} \approx V_{supply} - V_{R_B} - V_B$$

For high currents through these bias resistors, the quantity V_{R_B} becomes non trivial, reducing the peak output voltage and thus the power supplied to the speaker. Thus, the components have to be chose with care and adjusted to the rest of the circuit.

In conclusion the design successfully manages to amplify the power of an input signal to adequately drive an 8Ω speaker. The current limiting characteristics also make it a good way to protect other synthesizer building block from high input currents, preventing failure of components.

Functionality and Testing

Testing outputs

Some of the testing outputs when testing the Synthesizer are illustrated below:

VCO outputs:

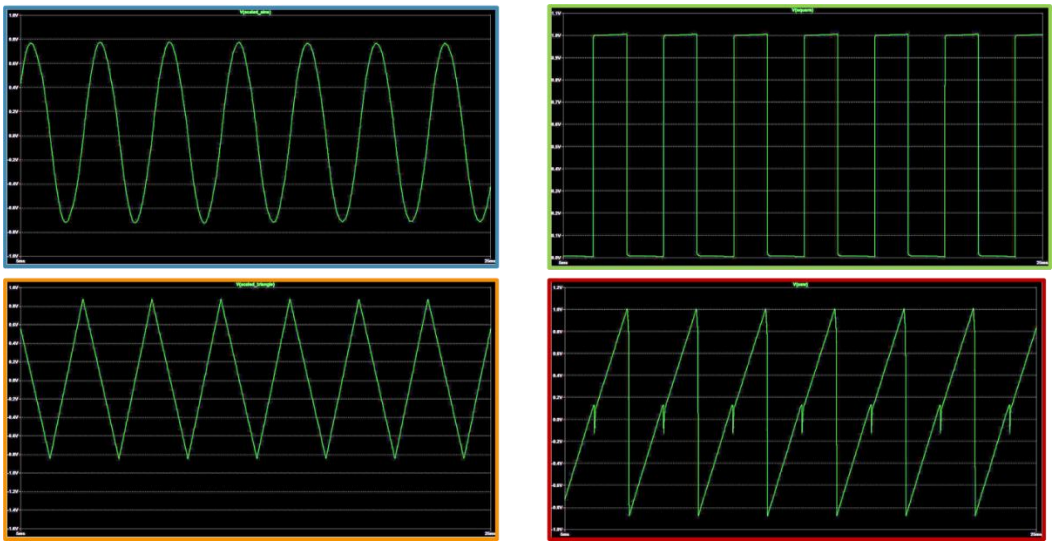


Figure 16: VCO outputting: Sine, triangle, square and sawtooth waves of note E4

Filtering outputs:

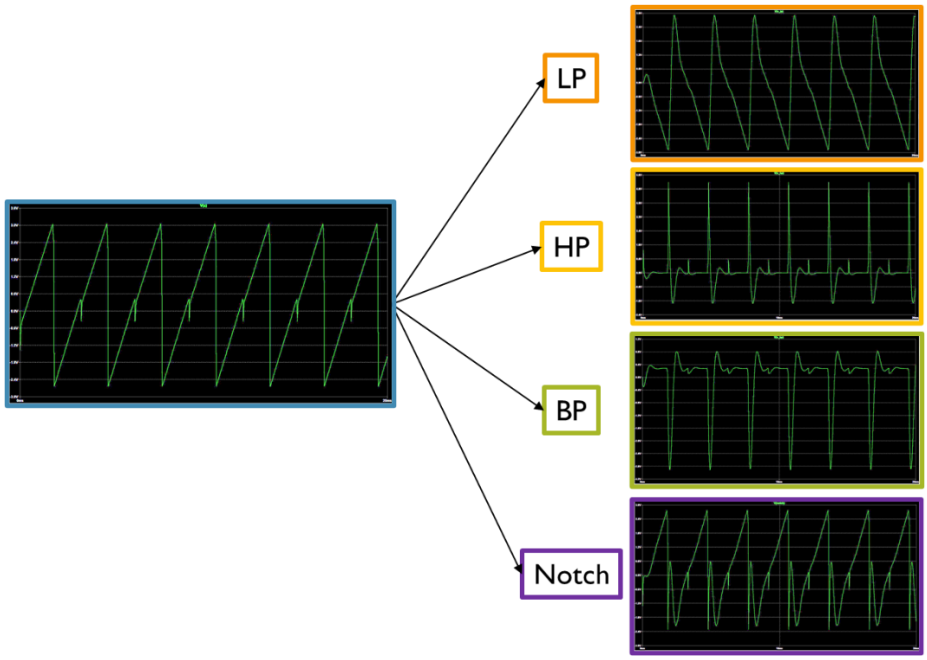


Figure 17: VCF filtering an E4 sawtooth at a corner frequency of 1760Hz

VCA outputs:

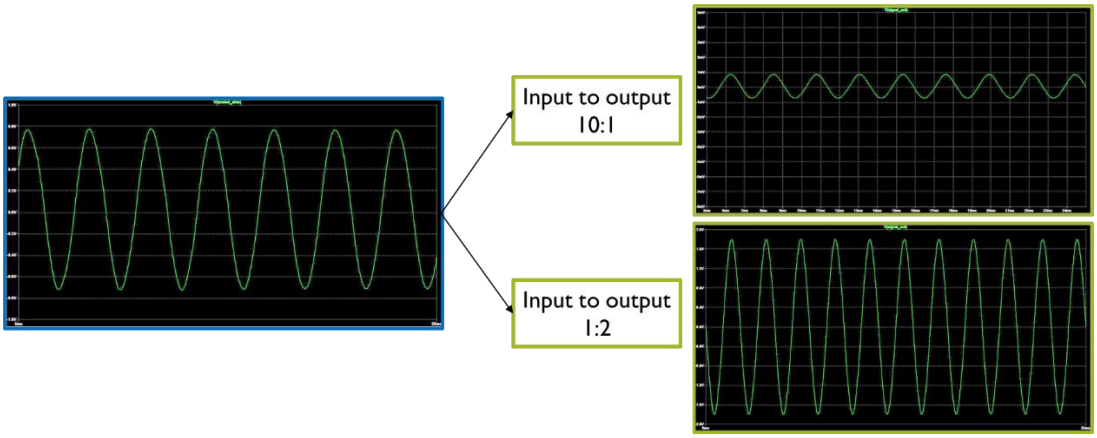


Figure 18: VCA amplifying a 400Hz sinewave

ADSR outputs:

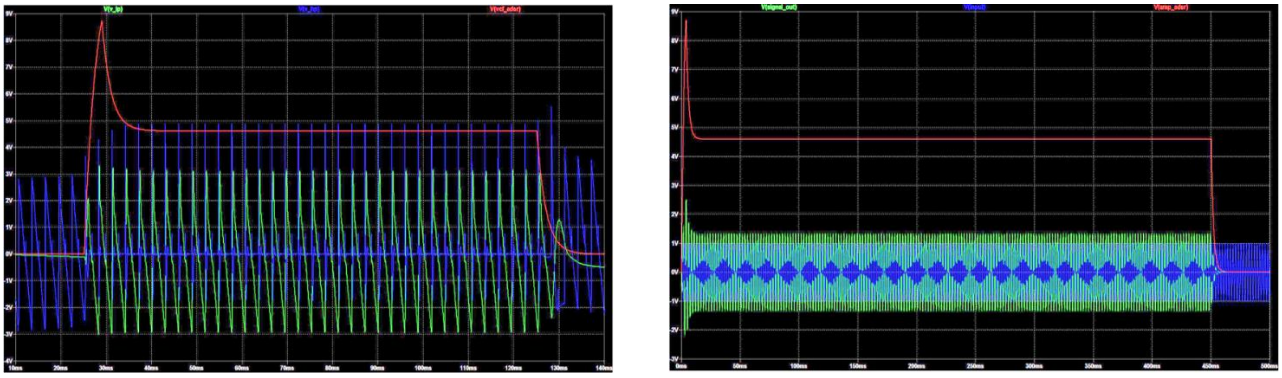


Figure 19: ADSR effects on VCF (left) and VCA (right)

LFO outputs:

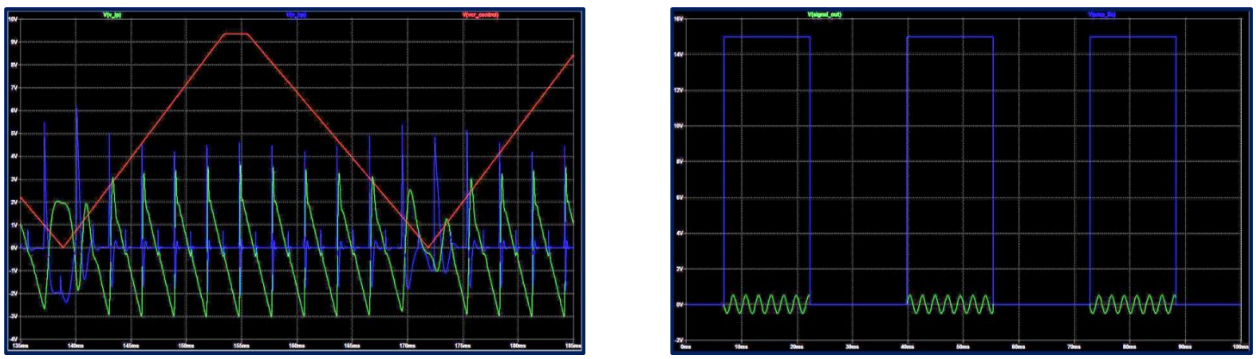


Figure 20: LFO effects on VCF (left) and VCA (right)

Power Consumption

As stated in the PDS, our Synthesizer should have minimal power consumption. Just by inspection of the block diagram, we expect the bulk of the Power to be consumed in the Power Amplifying stage. This is confirmed in the table below:

Block	Power consumed (W)	%
VCO	0.70558	6.92
VCF	0.87669	8.60
VCA	0.74853	7.34
ADSR	0.27254	2.67
LFO	0.17010	1.67
Power Amp	7.8671	77.13
Total Power	10.2	100

Temperature [°C]	**% Normal power consumption**
5	105.3
40	106.3

Table 3: Power consumption

We expect the average power to be higher at higher temperatures, due to the heating up of components. Specifically, with BJTs, increases in temperature cause increases in their collector currents, and therefore this increases power consumption and leakage currents. Changes in temperature will also affect the overall resistance of a circuit, contributing to the increase in power consumption, given by the equation:

$$P = I^2R$$

This allows to power the synthesizer with a power supply of approximately $10W$ at a voltage of 15 Volts. Power supplies like this are commonly available.
As found in previous sections our Power amplifier operates at a maximum efficiency of $\eta = 78.5\%$. Thus, from the required input power of $10.2W$ of which only $7.86W$ are fed

into the Power Amplifier, only $6.17W$ are converted into a useful Power output. Resulting in a power loss of approximately $1.6W$ in the Power Amplifier alone. This corresponds to the Power supply of the synthesizer to the speaker. Hence the overall efficiency of the synthesizer is $\eta_{total} = 60.4\%$.

In future designs this number should be significantly increased.

Conclusion and future work

Future work

Voltage controlled oscillator

There are many different solutions on implementing a VCO, as well as different types of waveforms that could be implemented. Another future design of a VCO core could include a NE555 timer, a very popular component in synthesizer design, instead of just passive components, BJTs and operational amplifiers. This could generate a cleaner sawtooth wave. We could also implement pulse-width modulation, to not only generate a square wave, but rather a pulse wave with variable duty cycle, while we could also find a way to implement a ramp wave, the inverse of the sawtooth wave. Finally, we could implement vibrato, meaning a modulation in frequency based on the LFO, the same way we implemented the ‘wah’ in the VCF and the tremolo in the VCA.

Filtering stage

Instead of simulating component responses with equivalent resistors in the schematic, a representative LT-Spice component could be created.

Voltage controlled amplifier

If we had more time, we would have tried to implement the current mirror in the tail and solve what exactly the problem was. In addition, we could have

implemented a VCA that varied the amplification based on LED/LDR to create special musical effects. Moreover, combining the VCA's together in different ways could have enabled us to achieve more sophisticated musical effects. For instance, Figure 21 below shows ways to achieve crossfading and panning musical effects. Note that the need for multiple speakers for the following diagram to work is not necessary.

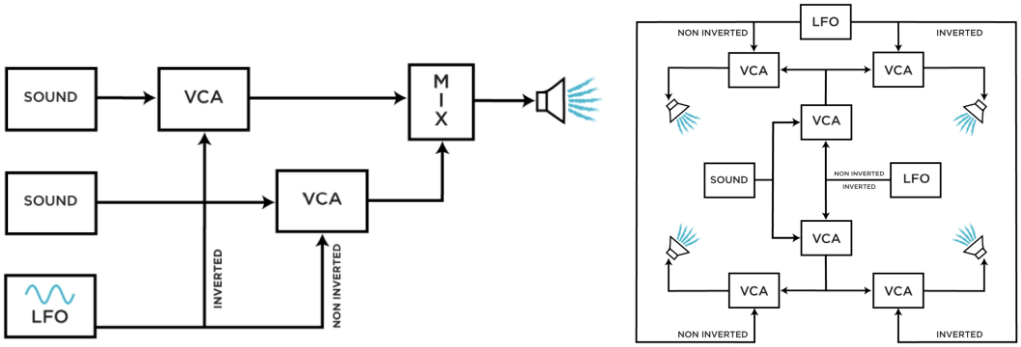


Figure 21: Examples of VCA configurations for special effects [31]

Power Amplifier

To improve the performance of the Power Amplifier, active loads instead of bias current limiting Resistors could be used boost the performance. This would decrease losses in maximum swing voltage and thus ensure a higher efficiency of the design. Furthermore, including active loads would significantly increase the input resistance of the building block, ensuring that all of the output voltage of the voltage-controlled amplifier is actually fed into the power amplifier [28].

Bill of Materials

Ref.	Mfg.	Part No.	Description	Quantity	Price [£]
Capacitors	-	-	capacitor, 100pF	1	0.86
	-	-	capacitor, 1nF	2	0.84
	-	-	capacitor, 1.8nF	1	0.107
	-	-	capacitor, 10nF	4	0.364
	-	-	capacitor, 68nF	2	0.256
	-	-	capacitor, 330nF	2	1.66
	-	-	capacitor, 1µF	2	1.046
Diodes	OnSemi	1N4148	diode	10	0.49
Transistors	NXP	2N2222	bipolar transistor	7	2.961
	NXP	2N2907	bipolar transistor	5	2.045
	NXP	2N3904	bipolar transistor	3	0.033
Operational Amplifiers	Analog Devices	OP07	integrated circuit	36	11.88
SPST switches	RSPRO	734-7154	switches	12	27.36
Potentiometers	Alps Alpine	RK09K/RK09D	pot. 10kΩ	8	5.44
	Alps Alpine	RK11K1140A72	pot. 100kΩ	6	4.212
			pot. 2x100kΩ	2	3.74
Resistors	-	-	resistor, 1Ω	2	0.028
	-	-	resistor, 10Ω	3	0.147
	-	-	resistor, 180Ω	2	0.0792
	-	-	resistor, 470Ω	1	0.0587
	-	-	resistor, 1kΩ	16	1.9136
	-	-	resistor, 2.2kΩ	1	0.12
	-	-	resistor, 5kΩ	1	0.0595
	-	-	resistor, 10kΩ	34	6.732
	-	-	resistor, 15kΩ	1	0.0548
	-	-	resistor, 22kΩ	2	0.2592
	-	-	resistor, 33kΩ	1	0.0605
	-	-	resistor, 47kΩ	12	0.4344
	-	-	resistor, 50kΩ	2	1.058
	-	-	resistor, 100kΩ	22	1.2804
	-	-	resistor, 120kΩ	4	0.2304
	-	-	resistor, 220kΩ	4	0.2348
	-	-	resistor, 1MΩ	6	0.3444
	-	-	resistor, 3.3MΩ	2	1.14
Power Supply	Mean Well	IRM-10	P, 10W @ 15V	1	8.26
				Total	£85.79

Project planning and Management

We have tried to divide the workload among the three group members as equitable as possible. For each of the essential building blocks of the synthesizer (oscillator, filter and amplifier), a person in charge of the overall progress was named (Eleftheria, Robert and Ash, respectively). Their task was it to be the main driver of the progress of the building block, ensuring that deadlines were met, coordinating input from other group members while also sharing potential problems met during all phases of the design process. Having had members that were operating on different timetables and being forced to work remotely for the first week meant communication between team members as well as establishing a platform on which we could collaborate and share files and ideas was essential. For this purpose, a Team on MS Teams as well as a Team Notebook was set up. This helped us to have daily catch-up meetings during which shared our progress to coordinate our next steps ahead. Essential Milestones and Goals as well as a general itinerary were summed up in a Gantt Chart (See Appendix Chart 1).

Having had the opportunity to meet up in person later on in the project, the daily meetups on MS Teams were replaced by team meeting in working spaces on campus. This aided our collaboration process as work and progress could be shared more easily and problems could immediately be tackled as a group.

Reflections

Ashcharya

I was able to utilise my strength of my understanding on transistor operations to understand the operation of my section in the entire synthesizer.

This project helped me identify the importance of communication in terms of updating your progress to your teammates regularly to be on the same page, discussing problems you may be encountering and being open-minded in hearing possible solutions they might be offering. Communication was vital in combining different parts into one synth in addition to writing the report. Finally, in the future, I would try to be more resourceful with my time. Despite using Teams and One-note as our organisation tool, I found myself falling behind because I wanted to create a unique Voltage-Controlled-Amplifier. This would prevent my team from reaching the testing and write-up stages at a much later date.

Eleftheria

Working on this project was a unique experience, that was really instructive in multiple ways. Firstly, it introduced me to the process of an engineering design project, and how to translate the desired specifications of a product into feasible, practical design steps. It helped me understand the implementations of the theoretical background we were taught during the year into the real world. The project was also valuable in practicing time management and group work. The use of deadlines for designing parts of the final product was really useful in terms of planning and making sure work was completed on time. It was also very important that we collaborated effectively as a group, we were in constant contact about our progress. Overall, I believe the project supplied me with many valuable skills.

Robert

I have thoroughly enjoyed the design process of our synthesizer. The project proved to be the ideal opportunity to apply theoretical concepts, learned in lectures to a real design project which helped me to better understand and appreciate contents such as FET and BJT transistors together with their limitations.

Working in a group meant that ideas and comments to designs could be shared immediately which helped me consider certain problems from a different perspective. Working together as a group has also highlighted the importance of communication as some time in the building process could have been saved if we had collaborated on certain problems earlier instead of trying to fix them on our own first.

Appendix

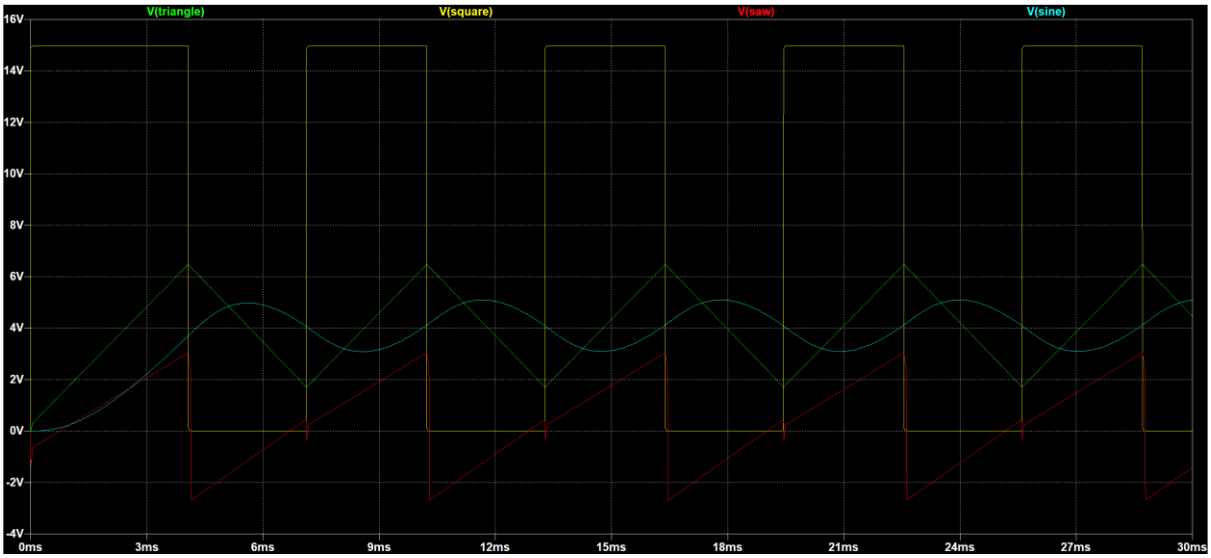


Figure 22: generated triangle-, square-, sawtooth-, and sinewaves

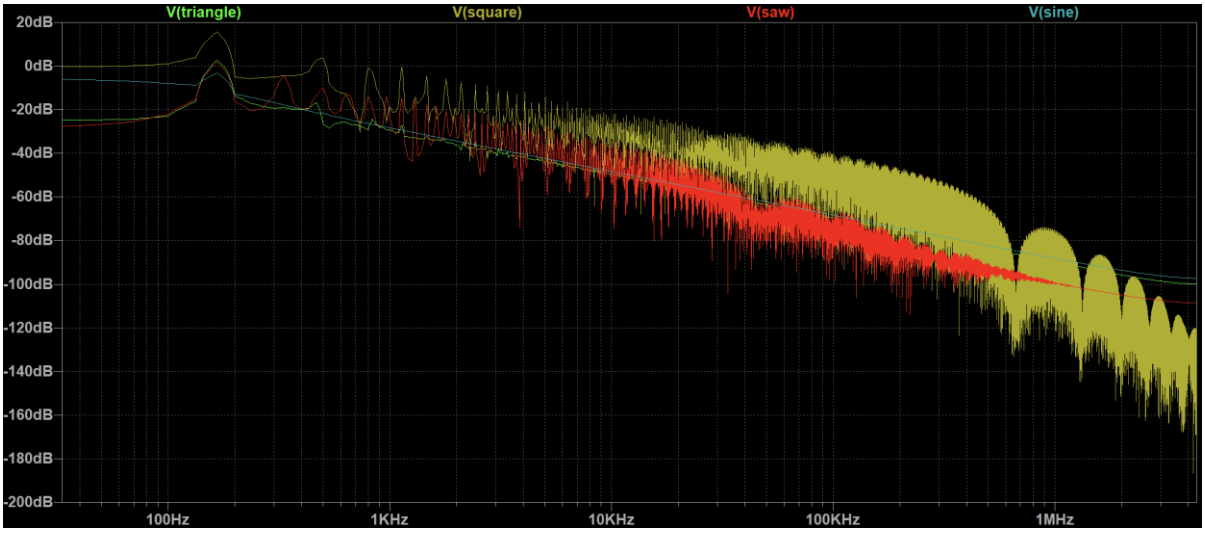


Figure 23: Fourier representation of waveforms at note E4 with peak at 165 Hz

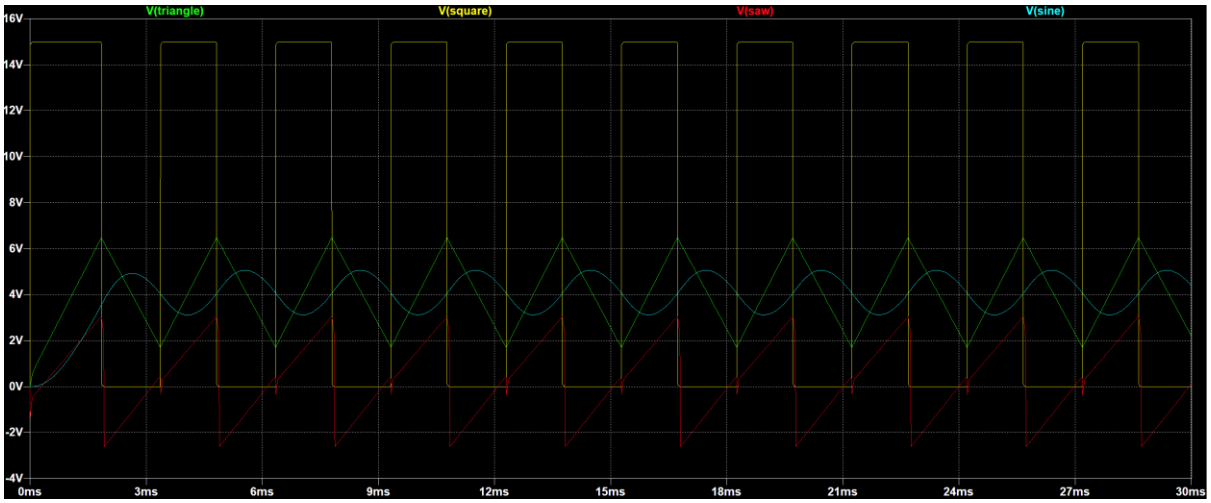


Figure 24: triangle-, square-, sawtooth-, and sinewaves for note E3

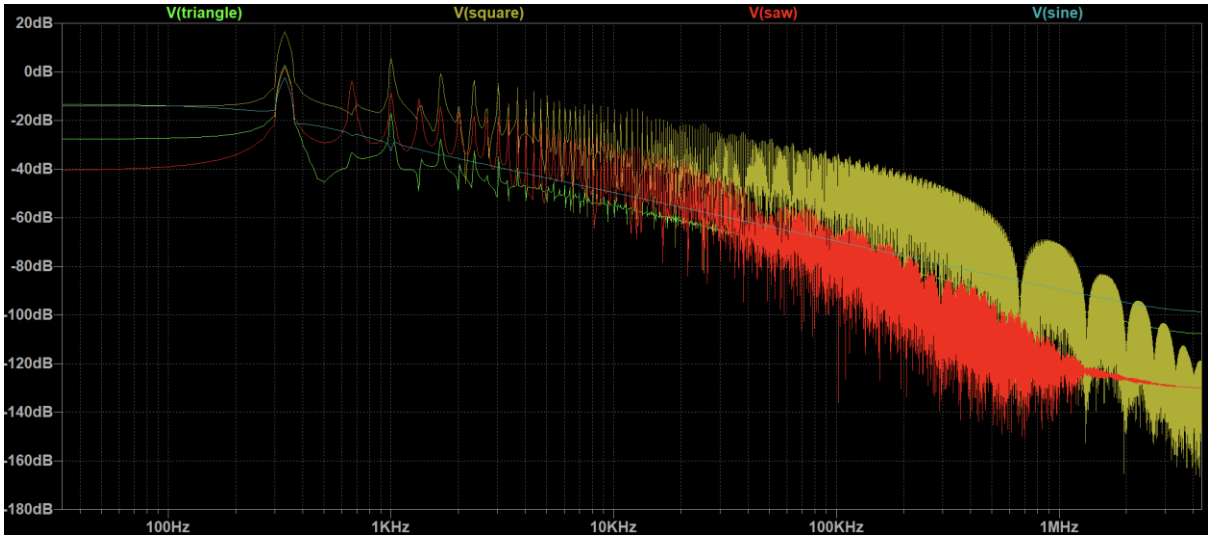


Figure 25: Fourier representation of waveforms at note E3 with peak at 333Hz

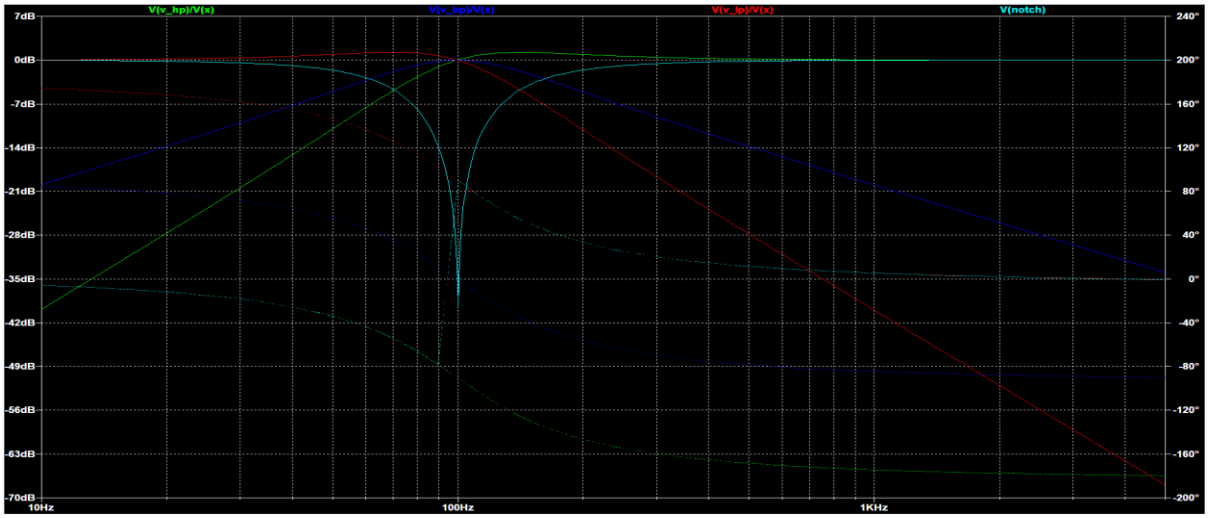


Figure 26: Filtering Stage Frequency response

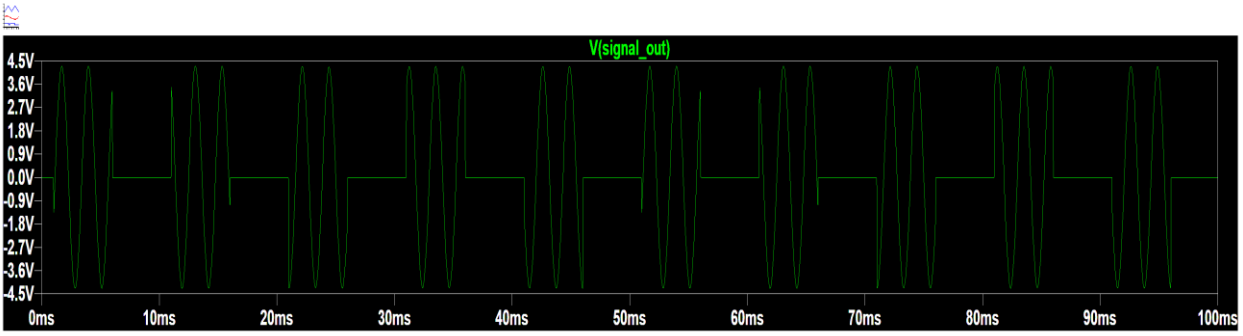


Figure 27: Output of VCA with sine-wave input and ADSR as a rectangular pulse

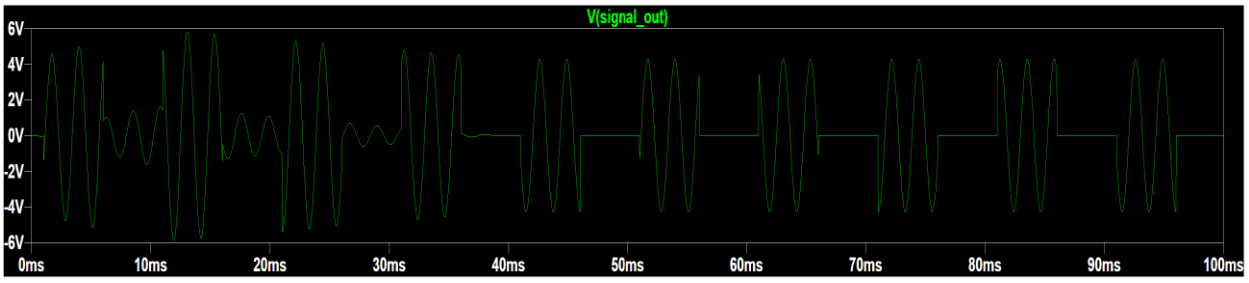


Figure 28: Output of VCA with ADSR as rectangular pusle and the LFO

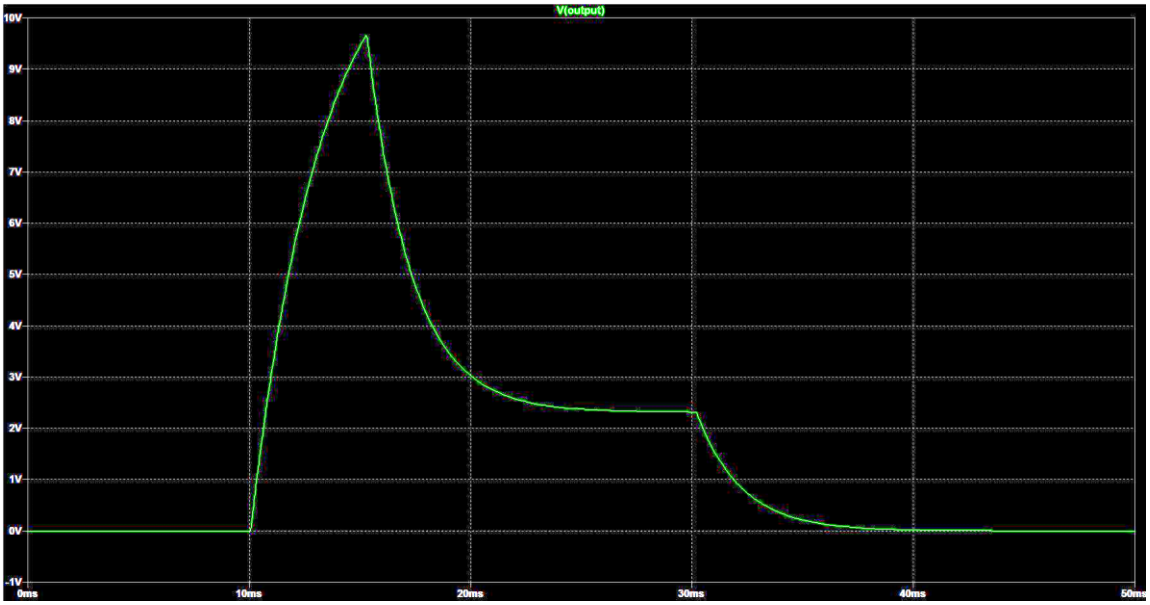


Figure 29: ADSR envelope, increase attack time, decreased sustain level

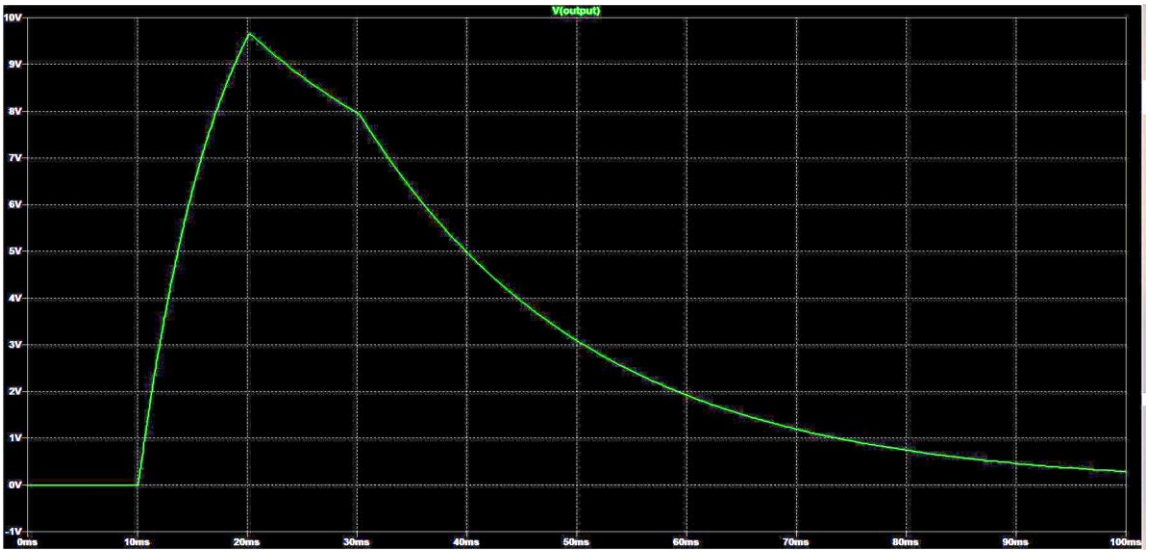


Figure 30: ADSR envelope, long attack followed by near maximum decay and release

Design of Analogue Synthesizer

Legende: Research | Building stage | Testing | Writing

Team Ash, Eleftheria, Robert

Start of the Projekt: 10.05.2021

Description	Category	Assigned to	Progress	Start	Days
Research stage					
Find general working principle of synthesizer	Milestone	ALL		10.05.2021	1
working principle of VCO	Research	Eleftheria	100%	11.05.2021	2
working principle of VCF	Research	Robert	100%	11.05.2021	2
working principle of VCA	Research	Ash	100%	11.05.2021	2
working principle of ADSR and LFO	Research	ALL	100%	12.05.2021	1
PSD finalisation and pinpoint technical problem	Milestone	ALL		12.05.2021	1
Circuit					
Splitting up building blocks	Milestone	ALL		13.05.2021	1
Research of potential designs and potential solutions for individual stages	Research	ALL	100%	13.05.2021	7
Discussion of findings and exchange of ideas	Milestone	ALL		17.05.2021	1
Transfer Design to LTSpice and start of Testing	Building	ALL	100%	17.05.2021	11
Testing of Designs	Testing	ALL	100%	24.05.2021	8
Combining Designs into final design	Building	ALL	100%	31.05.2021	2
Testing combined circuit	Testing	ALL	100%	02.06.2021	6
Fully working and combined ciruit	Milestone			07.06.2021	1
Deliverables					
Handing in Deliverables	Goal			13.06.2021	1
write up the report	Writing			07.06.2021	7
finished video and report	Milestone			12.06.2021	1

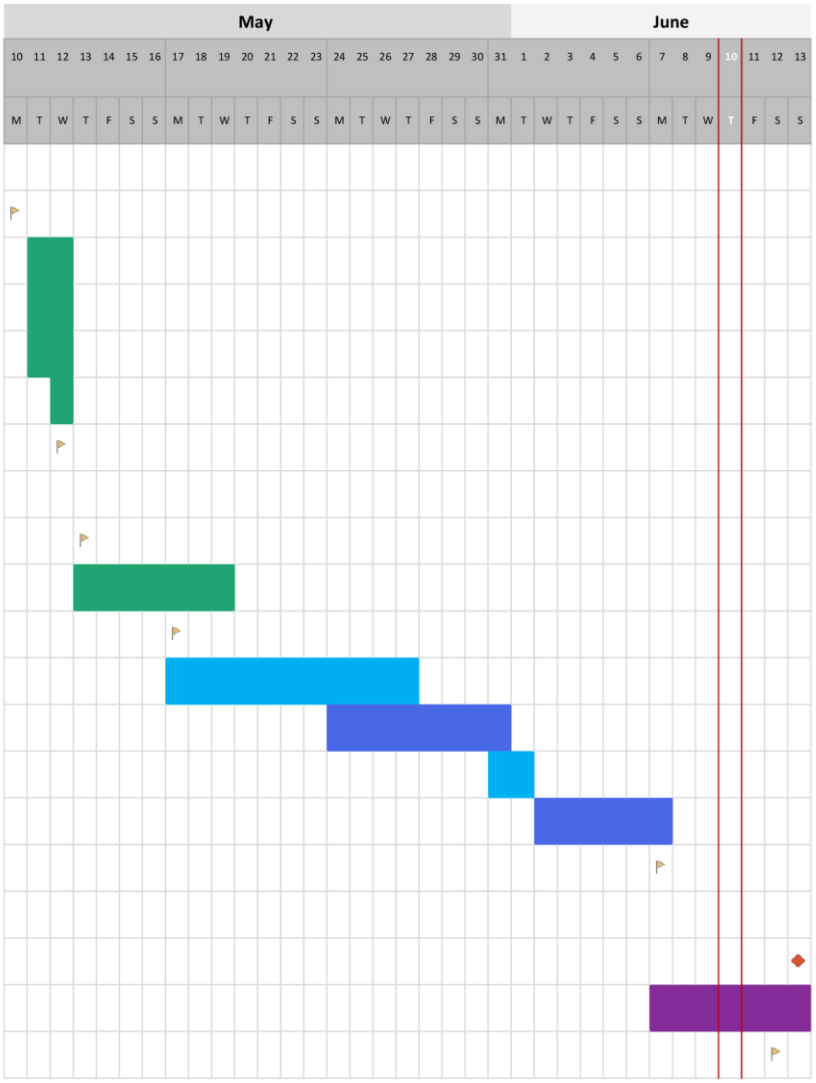


Chart 1: Gantt Chart outlining the project timeline

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