DESIGN OF 3 BIT DIGITAL TO ANALOG CONVERTER USING 180 NM CMOS TECHNOLOGY

PROJECT REPORT

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF BACHELOR OF TECHNOLOGY IN ELECTRONICS AND COMMUNICATION ENGINEERING UNDER TRIGUNA SEN SCHOOL OF TECHNOLOGY, ASSAM UNIVERSITY, SILCHAR

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Chapter 1

Introduction

1.1 Digital to Analog Converter

One of the most important functions in signal processing is the conversion between analog and digital signals. Consequently, it is necessary to be able to convert back and forth between the two types of signals. Therefore, analog-to-digital and digital-to-analog converters are an important part of any signal-processing system. The input to a DAC is a digital word consisting of parallel binary signals that are generated from a digital signal-processing system. These parallel binary signals are converted to an equivalent analog signal by scaling a reference.

A DAC with a voltage output can be characterized by the block diagram in Fig. 1.1. We see that it consists of a digital word of N-bits (b_0, b_1, b_2, ……., b_{n-2}, b_{n-1}) and a reference voltage V_{ref}. b_0 is called the most significant bit, MSB, and $b_{N-1}$is called the least significant bit, LSB.

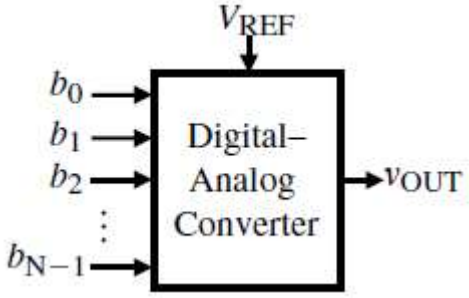

Figure 1.1 Block Diagram of DAC

1.1.1 Binary Weighted Resistor DAC

A binary weighted resistor network is a type of digital-to-analog converter (DAC) that uses a set of resistors with values weighted in powers of two to convert a binary input into an analog voltage. It is one of the simplest and most intuitive methods of implementing a DAC.

Working Principle:

Each bit of a binary number controls a switch that connects either a reference voltage (V_{ref}) or ground to one end of a resistor.The other ends of all resistors are connected together and then to an op-amp configured as a summing amplifier.

The resistors are weighted: for an *n*-bit DAC, the most significant bit (MSB) connects through a resistor **R**, the next bit through **2R**, then **4R**, and so on up to $\mathbf{2^{n-1}R}$ for the least significant bit (LSB). For example:-

If V_{ref}= 5V and the binary input is 101, only the first and third resistors will have current fromV_{ref}, resulting in an output analog voltage that corresponds to the binary value 5 (out of maximum 7 for 3-bit input).

1.2 Common Source Amplifier

A common source amplifier is one of the basic configurations used in analog electronics to amplify voltage signals using a MOSFET (or a JFET). It is called "common source" because the source terminal is common to both the input and output—usually connected to ground. This amplifier is widely used due to its good voltage gain, inverting output, and relatively simple design.

1.3 Current Mirror

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading. The current being "copied" can be, and sometimes is, a varying signal current. Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well, or it could consist of a current-controlled current source (CCCS).

1.4 Differential Amplifier

The differential amplifier can be implemented with BJTs or MOSFETs. A differential amplifier multiplies the voltage difference between two inputs (V_{in}^{+}-V_{in}^{-}) by some constant factor A_d, the differential gain. It may have either one output or a pair of outputs where the signal of interest is the voltage difference between the two outputs. A differential amplifier also tends to reject the part of the input signals that are common to both inputs (V_{in}^{+}- V_{in}^{-}) /2 . This is referred to as the common mode signal.

1.5 Op-Amp

An operational amplifier is an integrated circuit that can amplify weak electric signals. An operational amplifier has two input pins and one output pin. Its basic role is to amplify and its output voltage is proportional to the voltage difference between the input pins. Op-amps are designed to be used with feedback components like capacitors and resistors to determine the operation of the amplifier.

1.6 Summing Amplifier

A summing amplifier is an operational amplifier circuit that combines several input signals and produces an output that is the weighted sum of these inputs. The weights are determined by the resistances in the circuit. The basic configuration typically uses inverting inputs to sum the signals, but non-inverting summing amplifiers can also be constructed.

1.7 Subtractor

The subtractor is a differential amplifier circuit which produces an output voltage proportional to the voltage difference of two input signals applied to the inputs of the inverting and non-inverting terminals of an operational amplifier. By connecting one voltage signal onto one input terminal and another voltage signal onto the other input terminal the resultant output voltage will be proportional to the "difference" between the two input voltage signals of V_1 and V_2.

1.8 Differentiator

An operational amplifier (op-amp) can be configured as a differentiator, a circuit that produces an output voltage proportional to the rate of change of the input voltage. This is achieved by using a capacitor in the feedback loop and connecting the input to the inverting input of the op-amp. The output voltage is essentially the time derivative of the input voltage, but inverted.

1.9 Integrator

An integrator is an electronic circuit that generates an output voltage proportional to the time integral of its input voltage. In an ideal integrator, the output is the continuous summation of the input signal over time, effectively calculating the area under the curve of the input signal.

Chapter 2

Design, Analysis and Simulation

This chapter describes the design, analysis and simulation results of various analog circuits such as current mirror, differential amplifier, Opamp, DAC etc. Cadence Virtuoso software was used for the designing the schematic of the circuits and performing their simulation.

2.1 NMOS Transistor

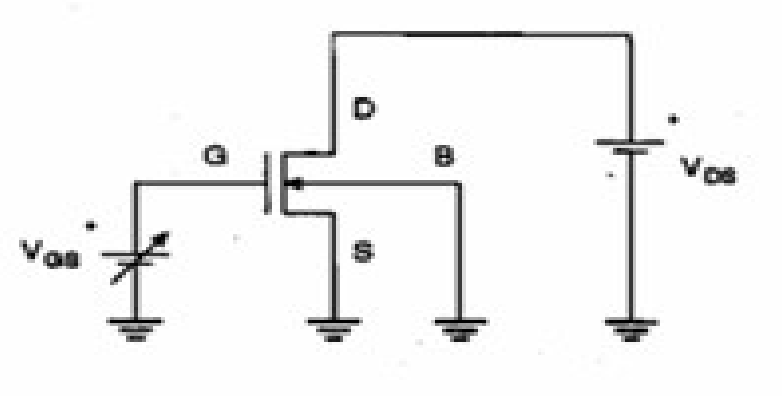

Figure 2.1 NMOS Transistor

The minimum gate to source voltage required to on the NMOS transistor is called the threshold voltage. Therefore we require a certain V_{gs} to on the transistor and then current I_d increases with increasing V_{ds}. After a certain V_{ds} called pinchoff voltage output become saturated.

If the length of NMOS is decreased to a very small value we encounter the phenomenon of channel length modulation due to which current increases even after saturation.

2.1.1 Designing and Calculation of NMOS Transistor

Schematic:

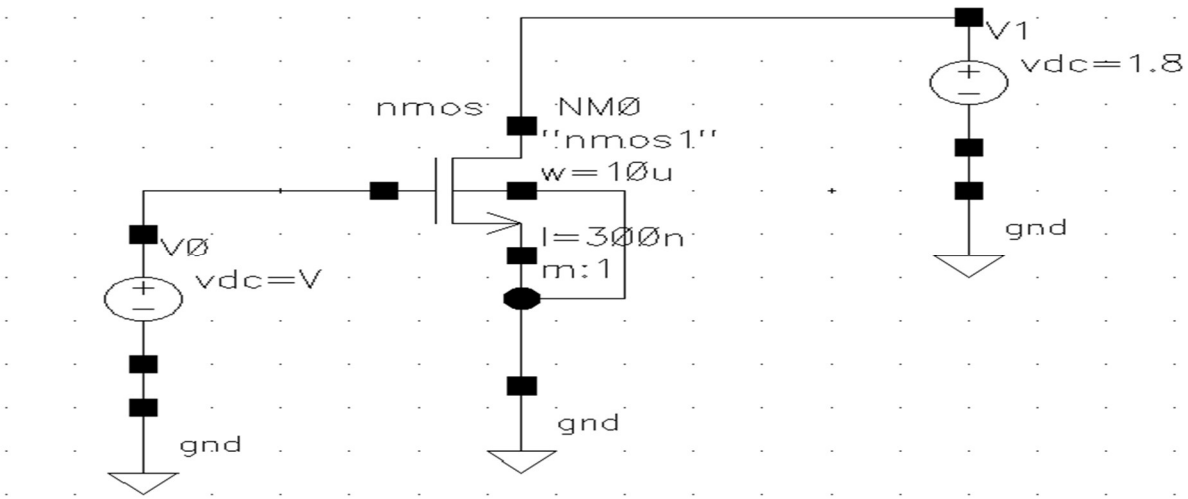

Figure 2.2 Schematic of NMOS Transistor

Simulation output:

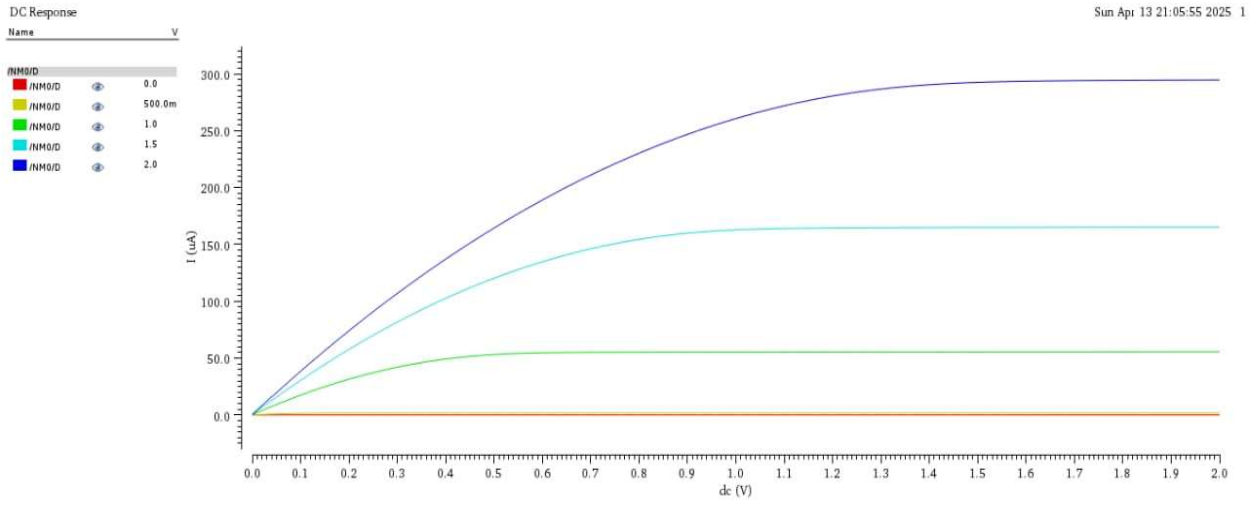

Figure 2.3 Simulation result of NMOS transistor ($\frac{W}{L} = \frac{10\mu}{9\mu}$)

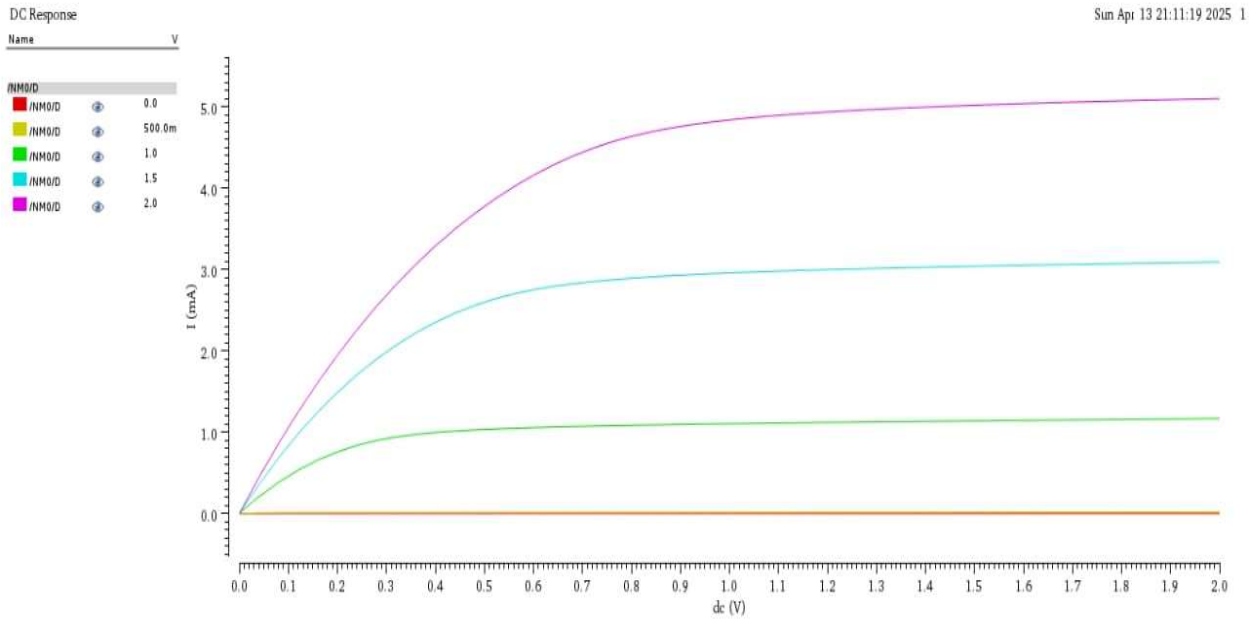

Figure 2.4 Channel Length Modulation effect ($\frac{W}{L} = \frac{10\mu}{0.5\mu}$)

2.2 Common Source Amplifier

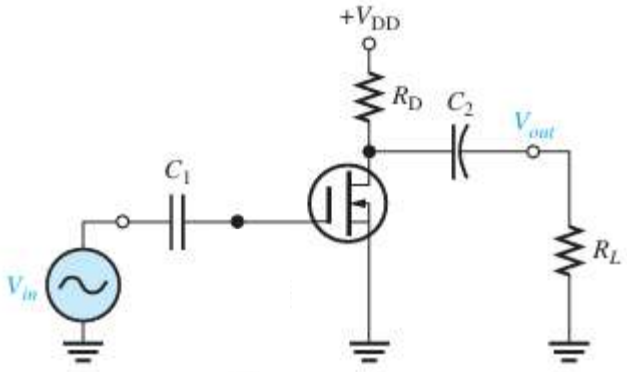

Figure 2.6 Common source amplifier

When the input signal is applied at the gate terminal and source terminal, then the output voltage is amplified and obtained across the resistor at the load in the drain terminal. This is called a common source amplifier. Here source acts as a common terminal between the input and output. It is also known as a voltage amplifier or a transconductance amplifier. It produces current gain and voltage gain according to the input impedance and output impedance.

2.2.1 Designing and Calculation of Common Source Amplifier

Schematic:

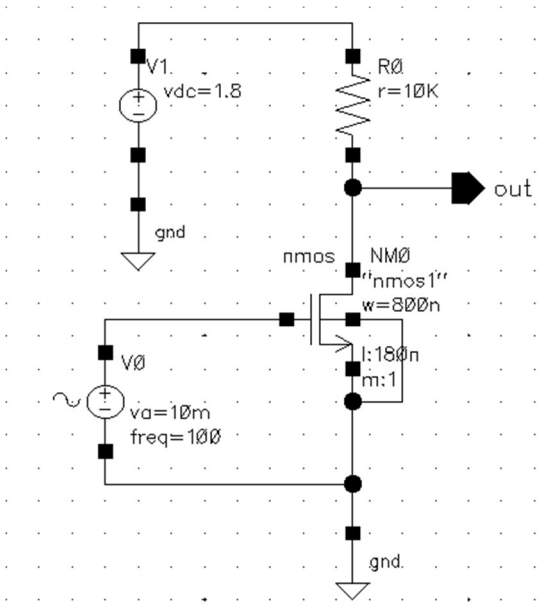

Figure 2.7 Schematic of Common source amplifier without capacitor

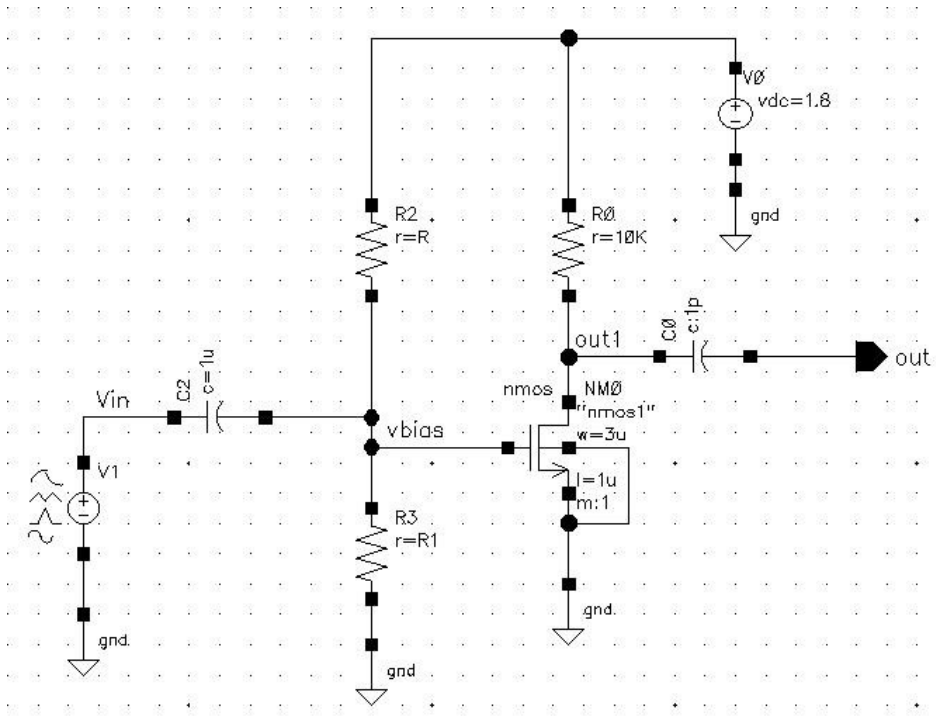

Figure 2.8 Schematic of Common source amplifier with capacitor

Simulation Output:

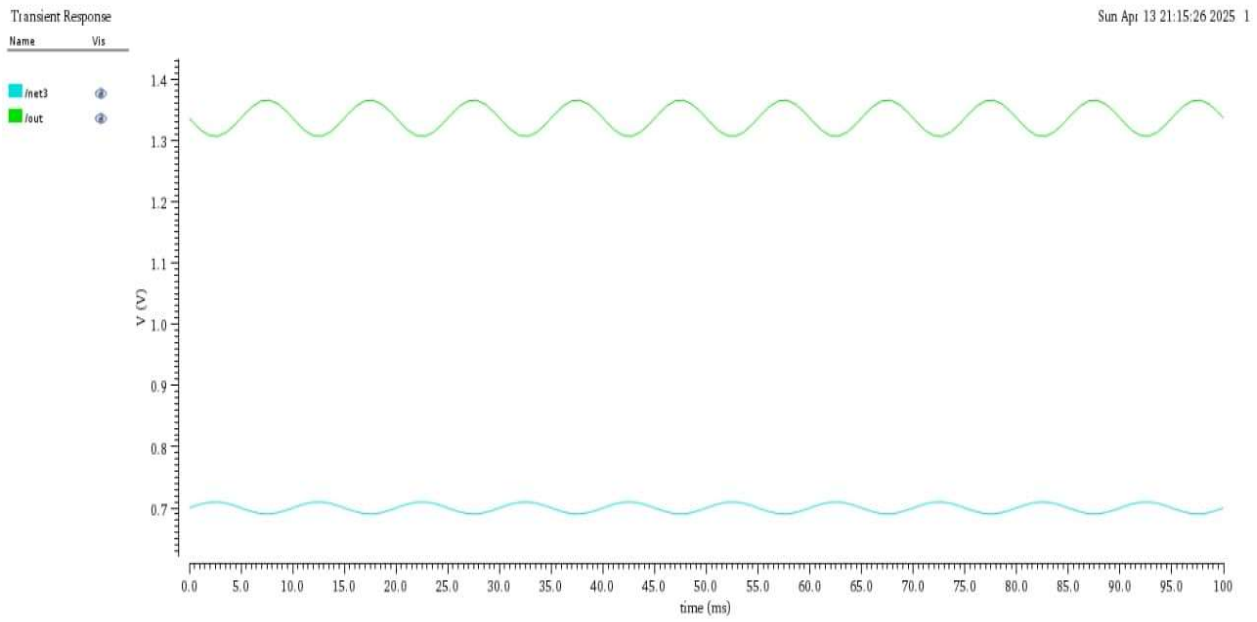

Figure 2.9 Simulation of Common source amplifier without capacitor

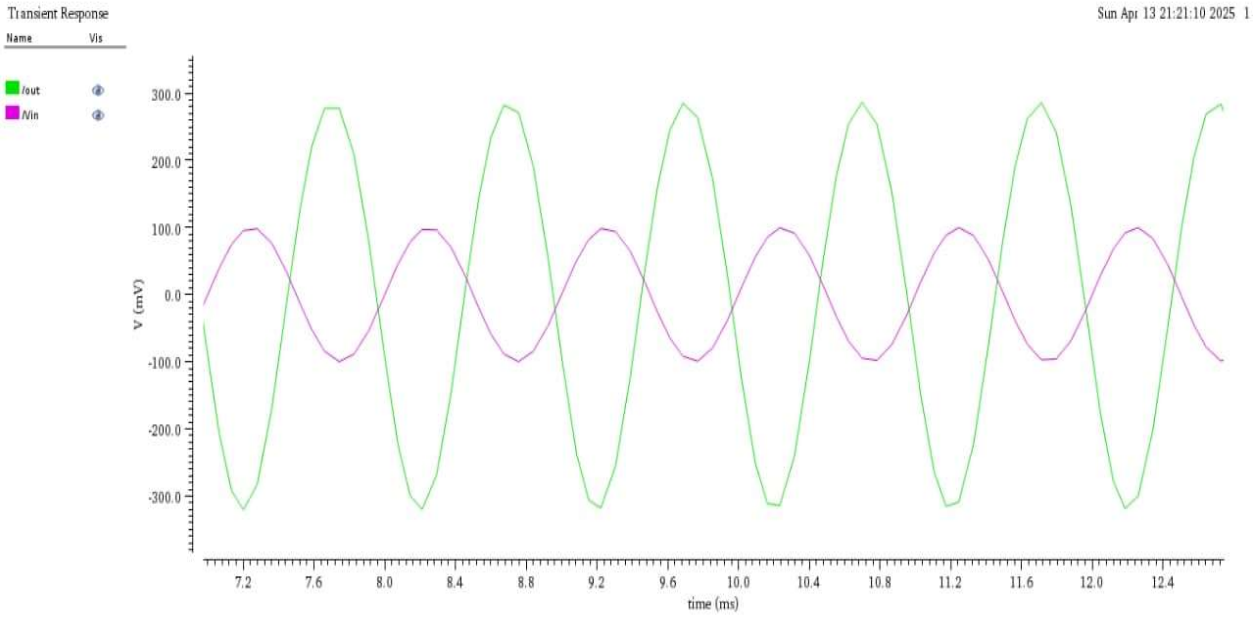

Figure 2.10 Simulation of Common source amplifier with capacitor

2.3 Current Mirror

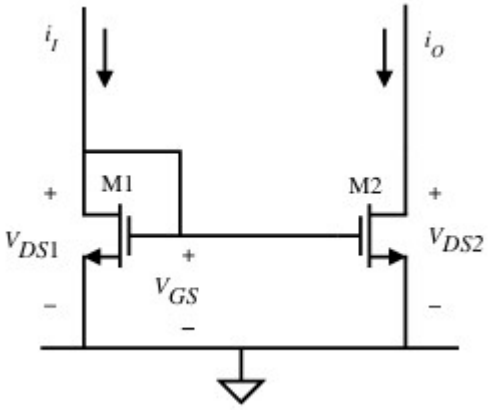

Figure 2.11 Current Mirror

The circuit is used to copy the flow of current in one active device and controlling the flow of current in another device by maintaining the output current stable instead of loading is known as a current mirror. Theoretically, a perfect current mirror is an inverting current amplifier. The main function of this amplifier is to reverse the direction of the flow of current. The main function of the current mirror is to provide active loads as well as bias currents to circuits and also used to form a more practical current source.

2.3.1 Designing and Calculation of Current Mirror

Schematic:

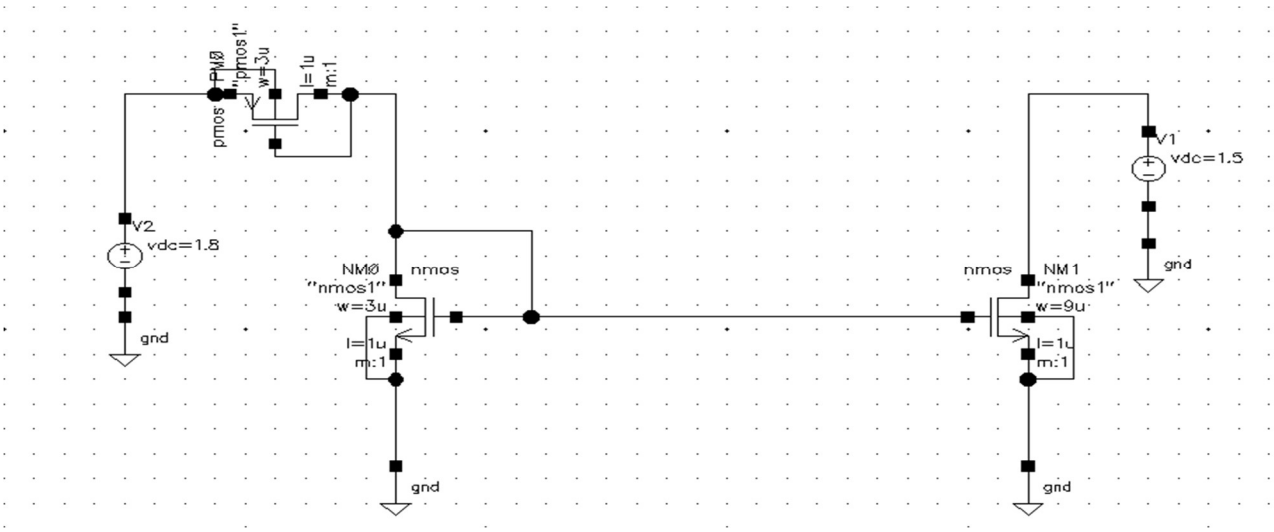

Figure 2.12 Schematic of current mirror

Simulation Output:

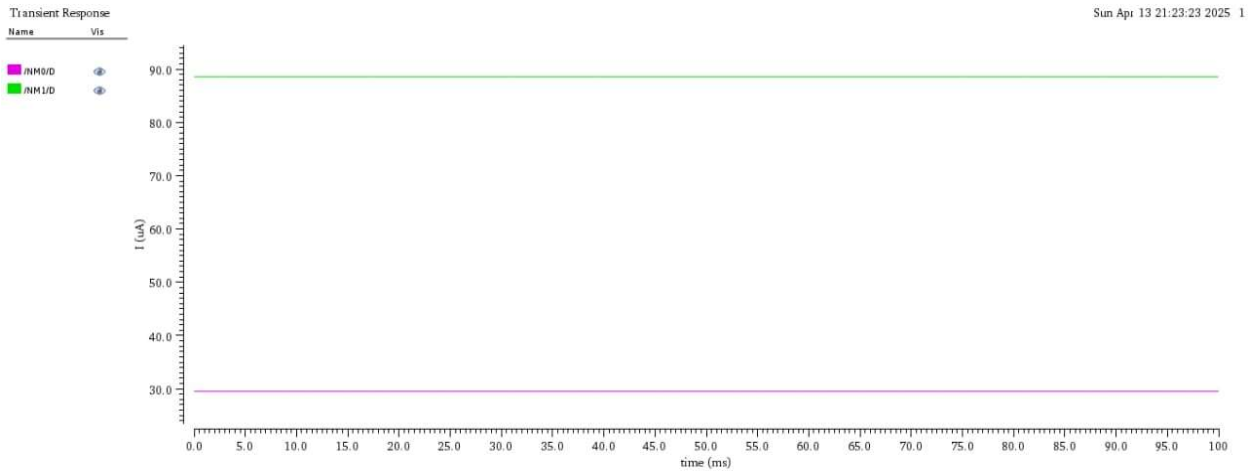

Figure 2.13 Simulation of current mirror

2.4 Differential Amplifier

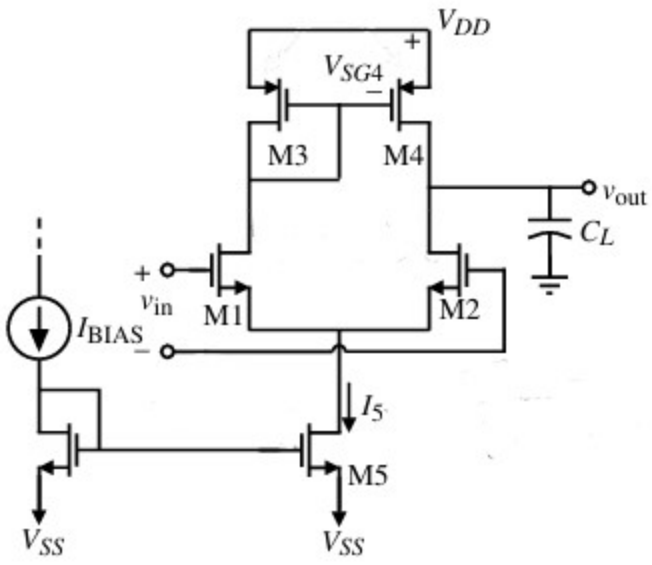

Figure 2.14 Differential amplifier

A differential amplifier is an amplifier that amplifies the difference between two voltages and rejects the average or common mode value of the two voltages. V_1 and V_2 are called single-ended voltages. They are the voltages referenced to AC ground. The differential-

mode input voltage,V_{id}, is the voltage difference between V_1 and V_2. The common-mode input voltage,V_{ic}, is the average value of V_1 and V_2 .

$$\therefore V_{id} = V_1 - V_2 \quad \text{and} \quad V_{ic} = \frac{V_1 + V_2}{2} \qquad \ldots\ldots\ldots\ldots \text{eq (2.4.1)}$$

$$\Longrightarrow V_1 = V_{ic} + 0.5\, V_{id} \quad \text{and} \quad V_2 = V_{ic} - 0.5 V_{id} \qquad \ldots\ldots\ldots\ldots \text{eq (2.4.2)}$$

Then,

$$V_{out} = A_{id} V_{id} \pm A_{ic} V_{ic}$$
$$= A_{id}\,(V_1 - V_2) \pm A_{ic}\left(\frac{V_1 + V_2}{2}\right) \qquad \ldots\ldots\ldots\ldots \text{eq (2.4.3)}$$

Where,

A_{id} = Differential-mode voltage gain

A_{ic} = Common-mode voltage gain

V_{id} = Differential voltage

V_{ic} = Common mode voltage

2.4.1 Designing and Simulation of Differential Amplifier

Schematic:

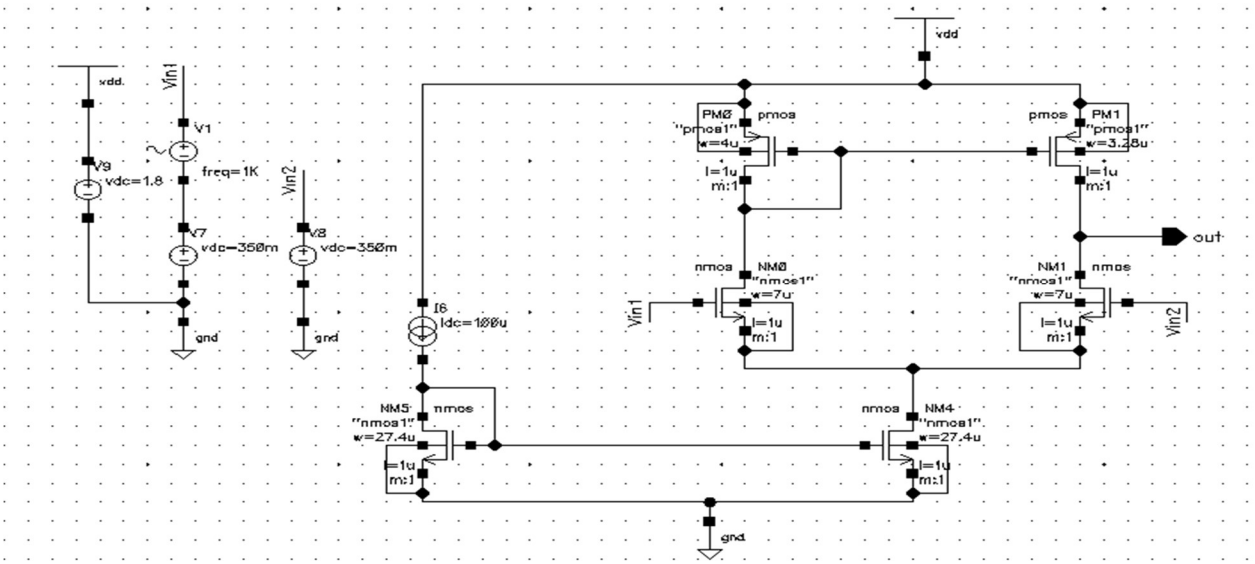

Figure 2.15 Schematic of Differential Amplifier

Simulation Output:

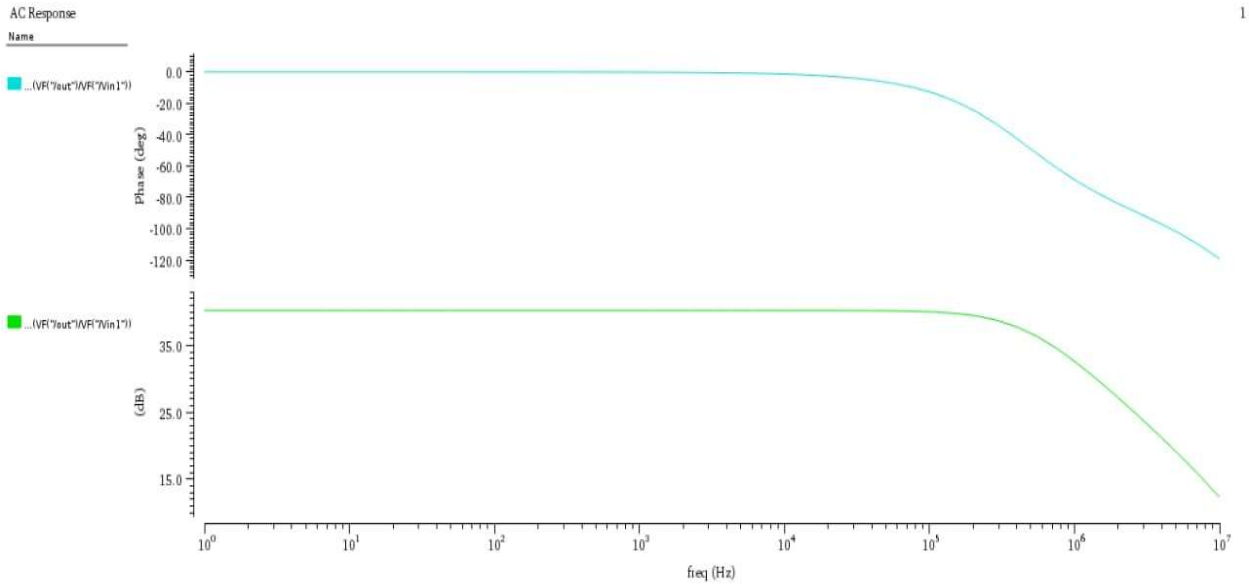

Figure 2.16 Gain and Phase plots of Differential Amplifier

2.5 Two Stage Operational Amplifier

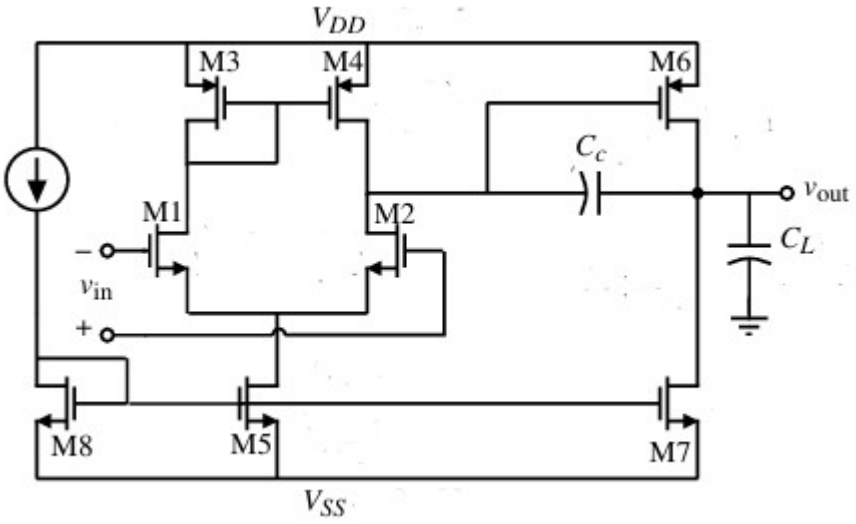

Figure 2.17 2-Stage Operational Amplifier

One of the most commonly used devices in the analog world is the operational amplifier (Op-Amp). It is a device whose output can be easily related to input in terms of some known mathematical equations and operations. Basically an Op-Amp mainly consists of four different functional blocks likely, the differential gain stage, the single ended conversion stage, the level shifting stage and finally the buffer stage. In The first stage that is the differential gain stage, amplifies independently there average and common mode signals. It is one of the most critical and important stages of an Op-Amp, it decides some of the most important parameters like Common mode rejection ratio (CMRR), common mode input range (ICMR) and the input noise. The second stage is the single ended conversion stage which is present after the differential stage is responsible for giving a single ended output which is referred to with the ground. The next is the level shifter stage which is introduced after the single ended conversion stage and finally the buffer or the second gain stage which provides the necessary gain to the amplifier. Fig 2.17 shows diagram of a 2 stage Operational Amplifier. Some of the basic principles behind the operation of Op-Amp is, a differential pair of p-MOS transistors (M1, M2) is used to implement the input differential amplifier stage. Where their sources are tied together. It is biased with a current mirror which acts as a load circuit. In Order to increase the common mode rejection ratio (CMRR) of the Op-Amp two current mirror circuits (M7, M8) which is p-MOS circuit and (M3, M4) n-MOS circuit are used instead of only one.

2.5.1 Designing and Calculation of Two Stage Op-amp

A step by step approach is adopted here to design the circuit of two stage op-amp. The design of circuit starts with the specifications and precise calculations of MOSFETs. The circuit consists of 8 MOS transistors and one miller capacitor. With precise and accurate calculations we are able to design the perfect two stage OpAmp according to our specifications.

Parameters	Values
DC Gain	80 dB
Gain Bandwidth	15 MHz
Phase Margin	60 º
Slew Rate	20 V/μs
ICMR (+)	1.6 V
ICMR (-)	0.7 V
V_{dd}	1.8 V
Power Dissipation	500 μW

Table 2.1 Circuit Specification

Transistor	W/L ratios
M1, M2	7.6μ / 4μ
M3, M4	7μ / 1μ
M5, M8	4.15μ / 1μ
M6	70μ / 1μ
M7	16μ / 1μ

Table 2.2 Transistor Dimensions and W/L Ratios

Schematic:

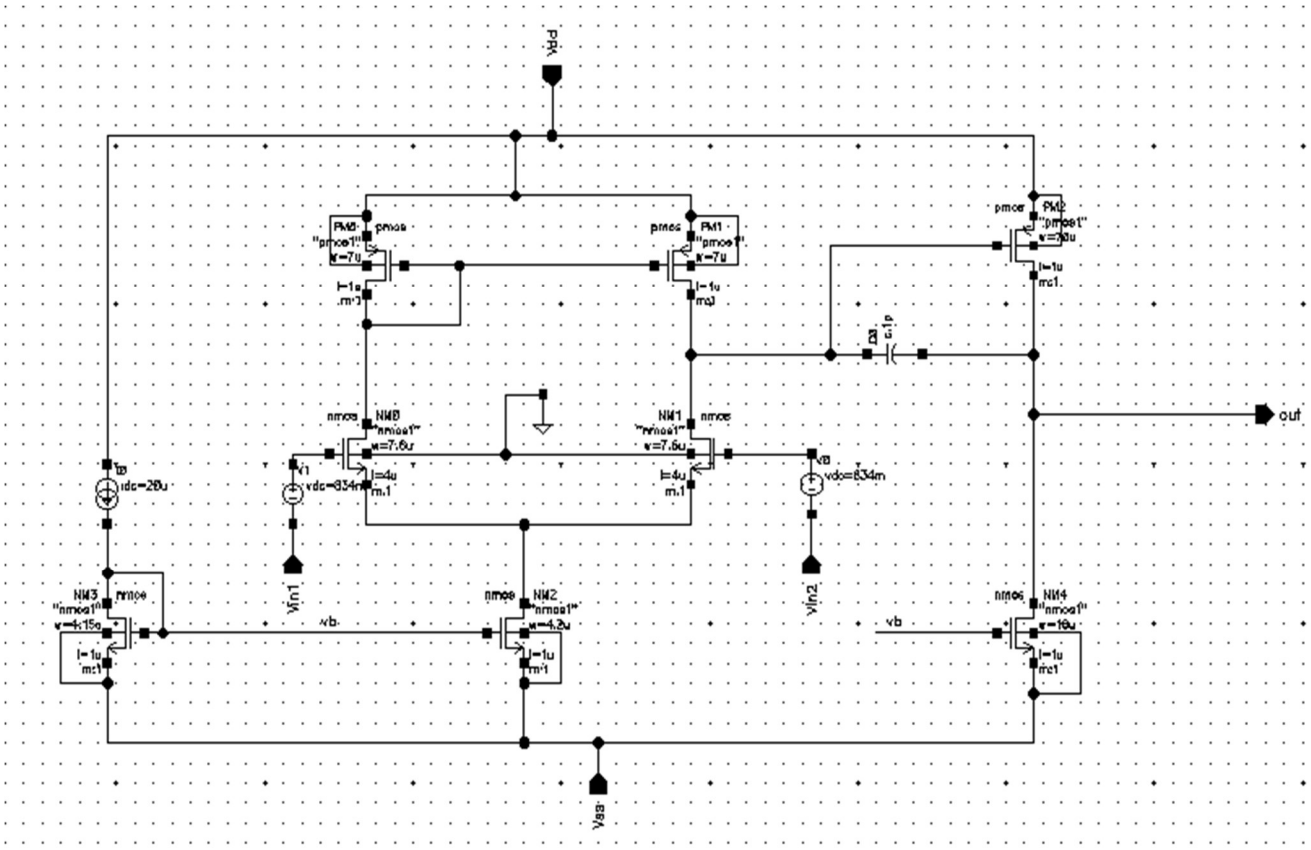

Figure 2.17 Schematic of 2-Stage Operational Amplifier

Symbol:

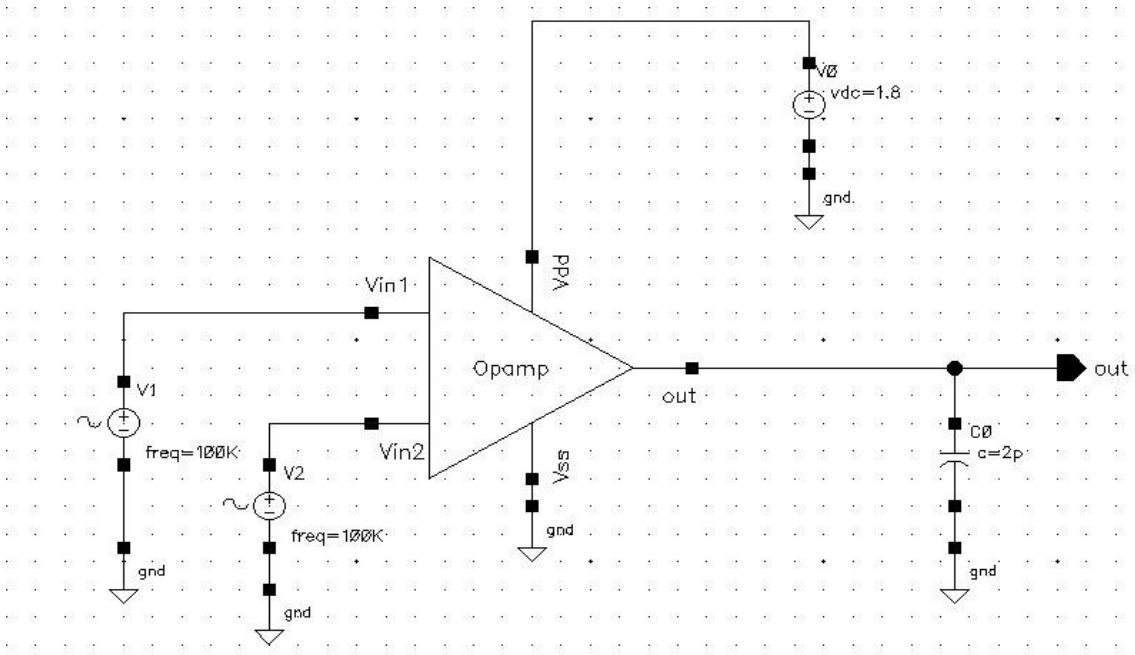

Figure 2.18 Symbol of 2-Stage Operational Amplifier

Simulation Output:

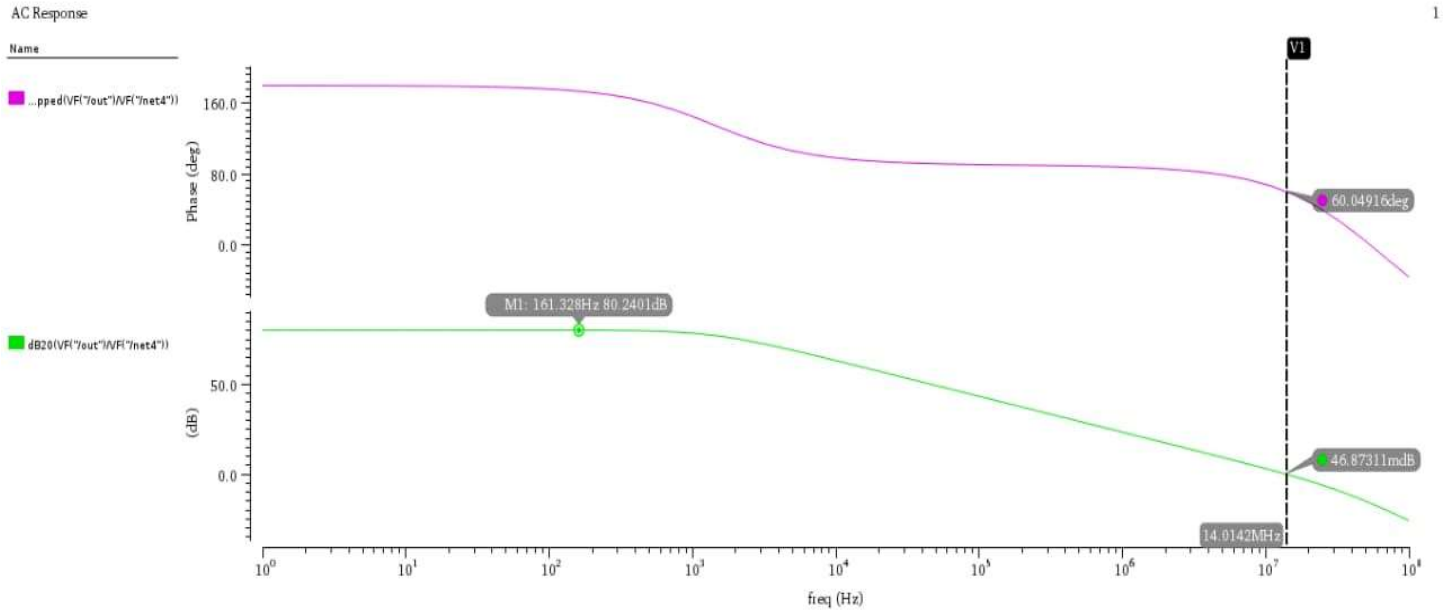

Figure 2.19 Gain and Phase of 2-Stage Operational Amplifier

Results:

Parameters	Values
DC Gain	80.2 dB
Phase Margin	60 º
Gain Margin	16.2 dB
CMRR	64.8 dB

Table 2.3 Obtained specs of Operational Amplifier

2.6 Designing of a Summing Amplifier

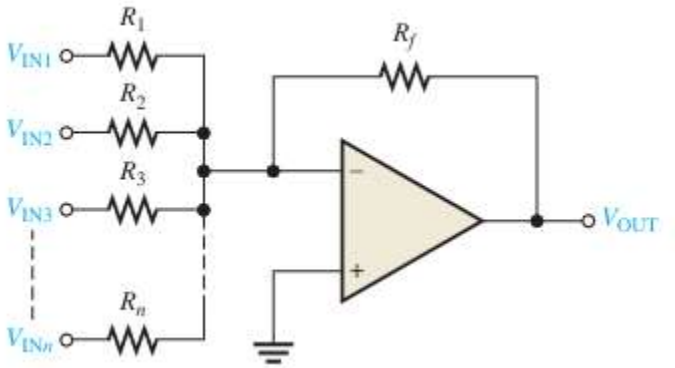

Figure 2.20 Summing Amplifier

The Summing Amplifier is another type of operational amplifier circuit configuration that is used to combine the voltages present on two or more inputs into a single output voltage Summing amplifier or an adder is used to sum two signal voltages. Voltage adder circuit is a simple circuit that enables you to add several signals together. It has wide variety of applications in electronic circuits. For example, on a precision amplifier, you may need to add a small voltage to cancel the offset error of the op amp itself.

The output voltage (V_{out}) for an inverting summing amplifier is given by the weighted sum of the input voltages i.e,

$$V_{out} = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \ldots\ldots\ldots + \frac{R_f}{R_n}V_n\right] \quad \ldots\ldots\ldots\ldots \text{ eq (2.6.1)}$$

$$\Rightarrow V_{out} = -R_f\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \ldots\ldots\ldots\ldots + \frac{V_n}{R_n}\right] \quad \ldots\ldots\ldots\ldots \text{ eq (2.6.2)}$$

2.6.1 Designing and Calculations of Summing Amplifier

Schematic:

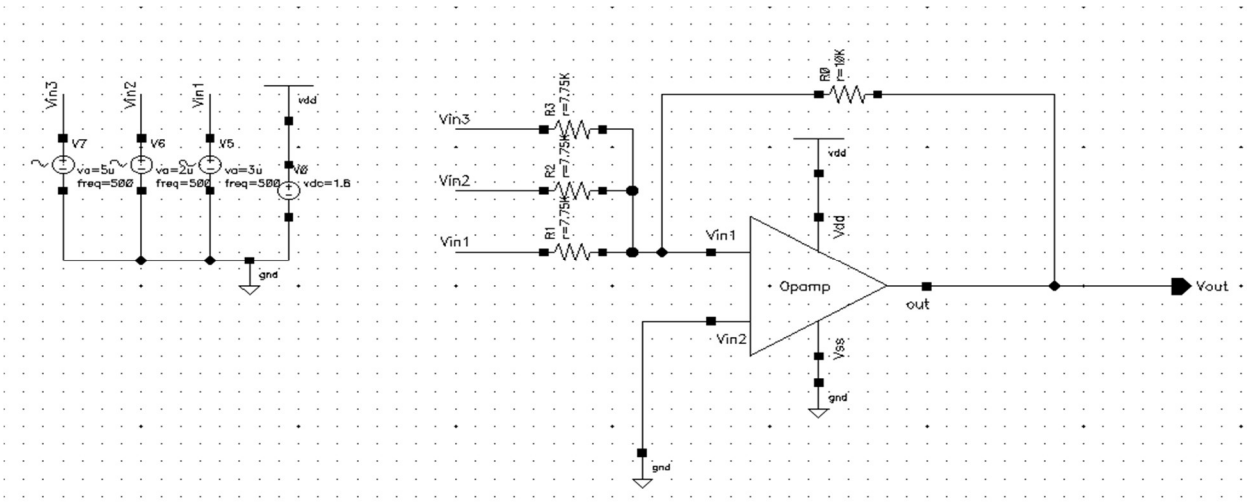

Figure 2.21 Schematic of a Summing Amplifier

Simulation Output :

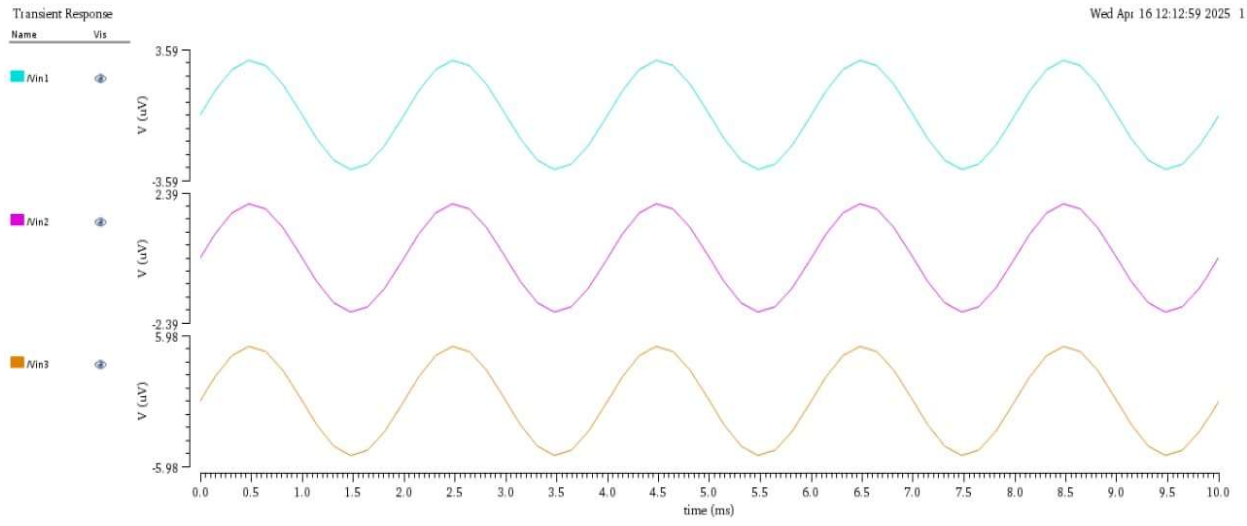

Figure 2.22 Simulation of Input for Summing Amplifier
V_{in1}= 3μV, V_{in2}= 2μV, V_{in3}= 5μV

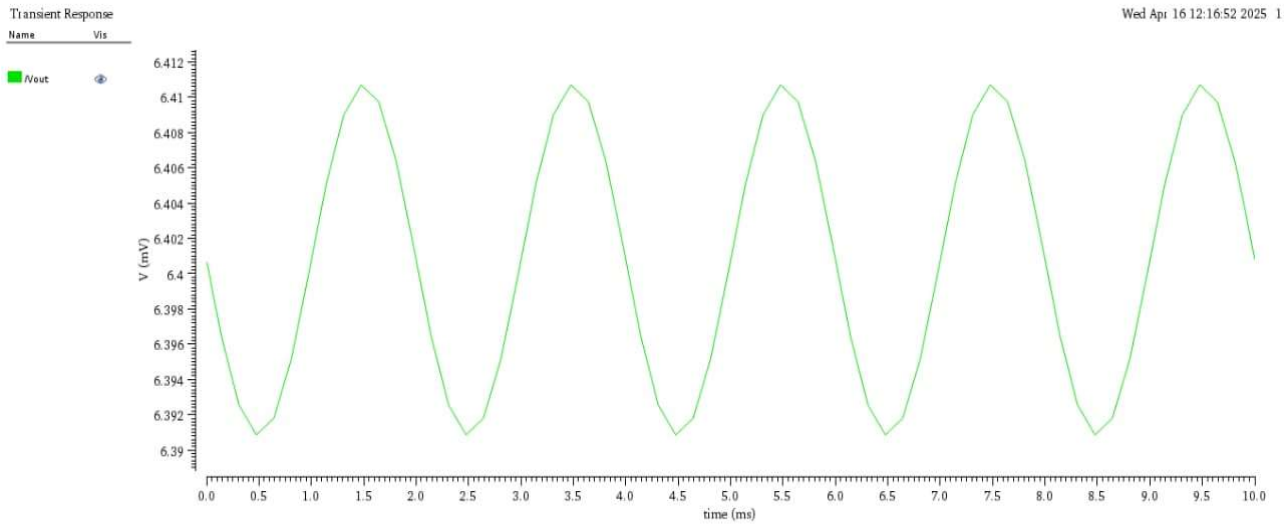

Figure 2.23 Simulation of output in Summing Amplifier. V_{out} = 9.9μV

2.7 Designing of Subtractor

An op-amp based subtractor produces an output equal to the difference of the input voltages applied at its inverting and non-inverting terminals. It is also called as a differential amplifier, since the output is an amplified one.

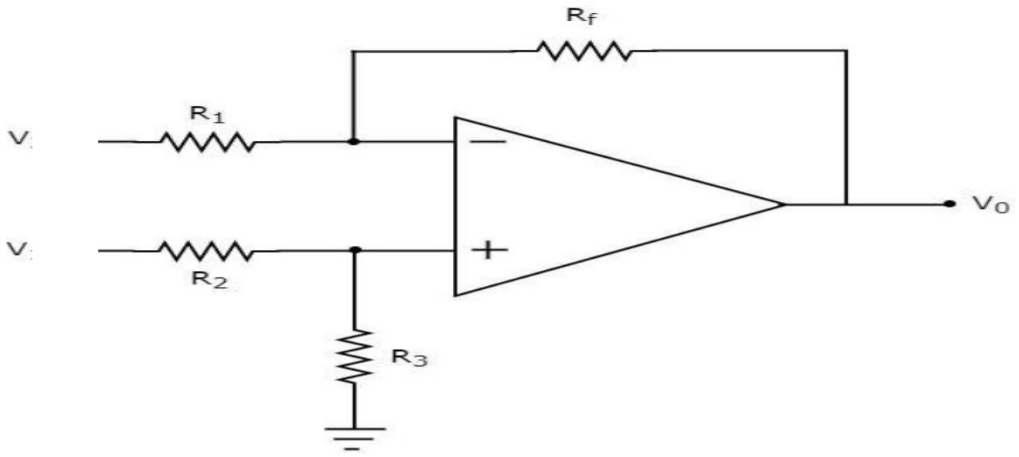

Figure 2.24 Subtractor

$$V_{out} = V_1\left(\frac{R_3}{R_2+R_3}\right)\left(1+\frac{R_f}{R_1}\right) + \left(-\frac{R_f}{R_1}\right)V_2 \qquad \text{. . . . . eq (2.7.1)}$$

$$\Rightarrow V_{out} = V_1\left(\frac{R_3}{R_2+R_3}\right)\left(1+\frac{R_f}{R_1}\right) - \left(\frac{R_f}{R_1}\right) V_2 \qquad \text{..... eq (2.7.2)}$$

2.7.1 Designing and Calculations of Subtractor

Since, the Op-amp is not ideal, so virtual ground concept does not apply here. Therefore to get unity gain, ratio of R_f/ R cannot be equal to 1 and hence are adjusted as shown in schematic.

Schematic:

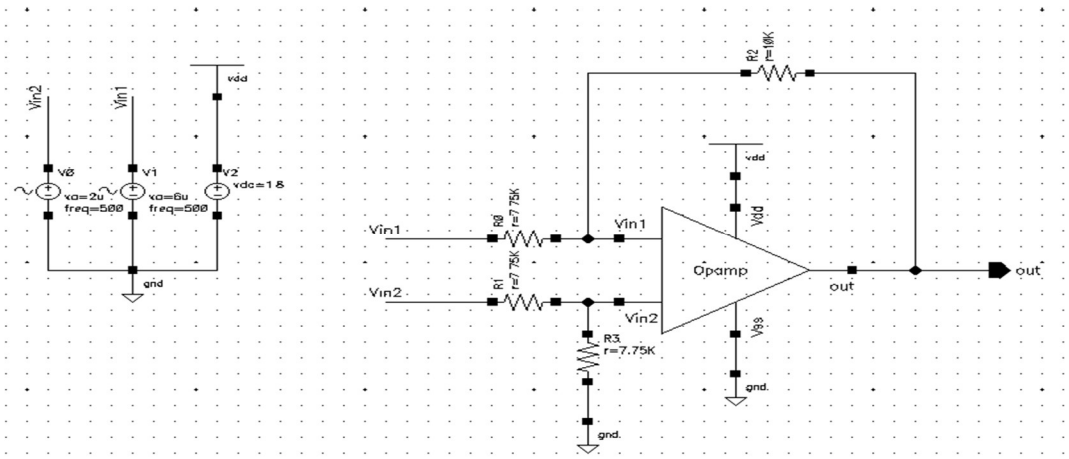

Figure 2.25 Schematic of Subtractor

Simulation Output:

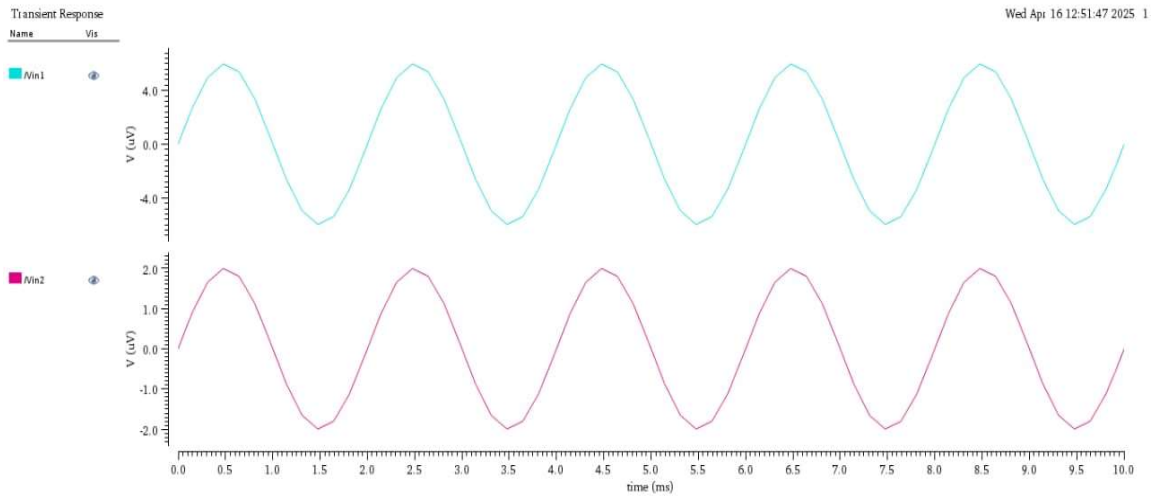

Figure 2.26 Simulation of inputs for Subtractor. V_{in1}= 6μV, V_{in2}= 2μV

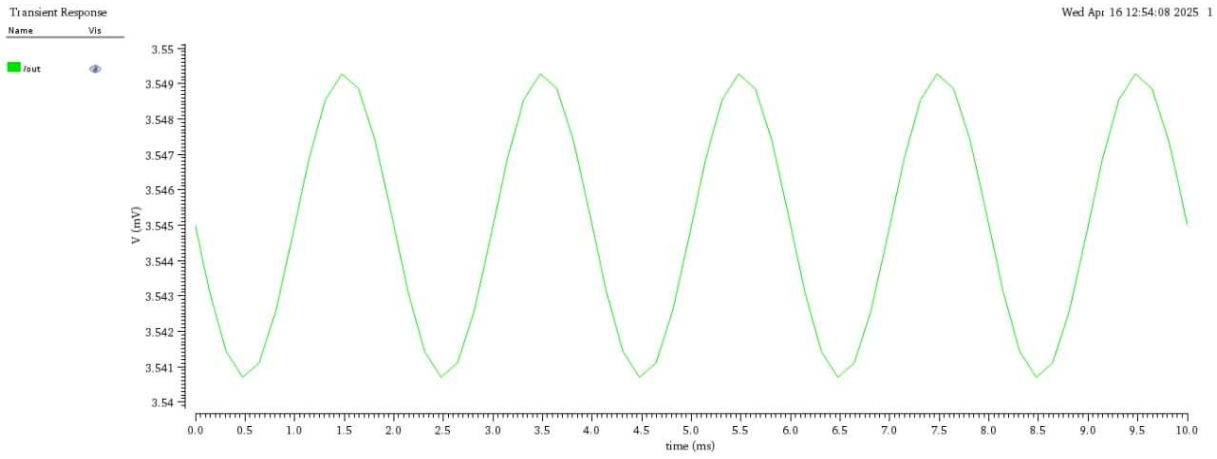

Figure 2.27 Simulation of output for Subtractor. V_{out}= 4μV

2.8 Design of a Differentiator Circuit

An op-amp based differentiator produces an output, which is equal to the differential of input voltage that is applied to its inverting terminal. The circuit diagram of an op-amp based differentiator is shown in the following figure –

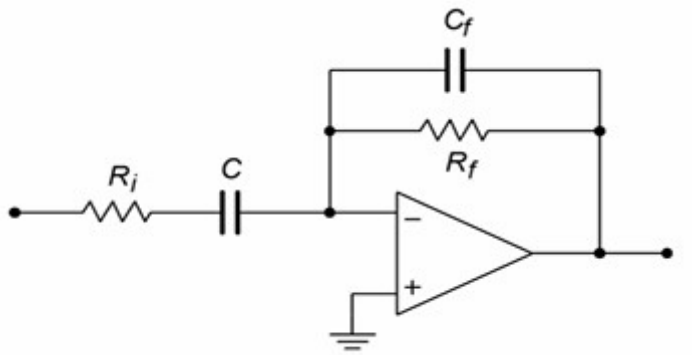

Figure 2.28 Differentiator circuit

The nodal equation at the inverting input terminal's node is –

$$-C\frac{dV_i}{dt} + \frac{0 - V_o}{R} = 0$$

$$\Rightarrow -C\frac{dV_i}{dt} = \frac{V_o}{R}$$

$$\Rightarrow V_o = -RC\frac{dV_i}{dt} \qquad \text{. . . . . eq (2.8.1)}$$

If RC=1s, then the output voltage V_o will be –

$$V_o = -\frac{dV_i}{dt} \qquad \text{. . . . . eq (2.8.2)}$$

2.8.1 Designing and Calculations of Differentiator

The values of capacitors and resistors are so chosen to allow proper time for charging and discharging of the output signal and provide the required gain. The capacitor on feedback network reduces harmonic distortion in the output signal. Two different signals, sinusoidal and square wave are given to the circuit and its output are plotted as given below-

Schematic:

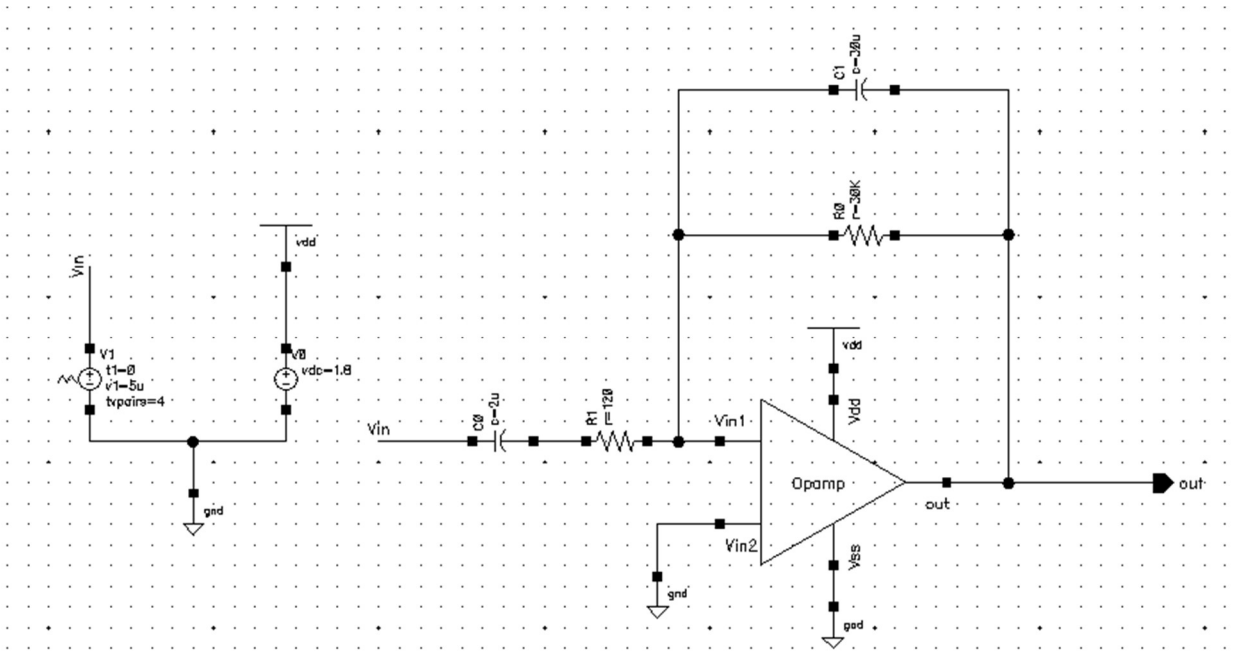

Figure 2.29 Schematic of Differentiator

Simulation Output:

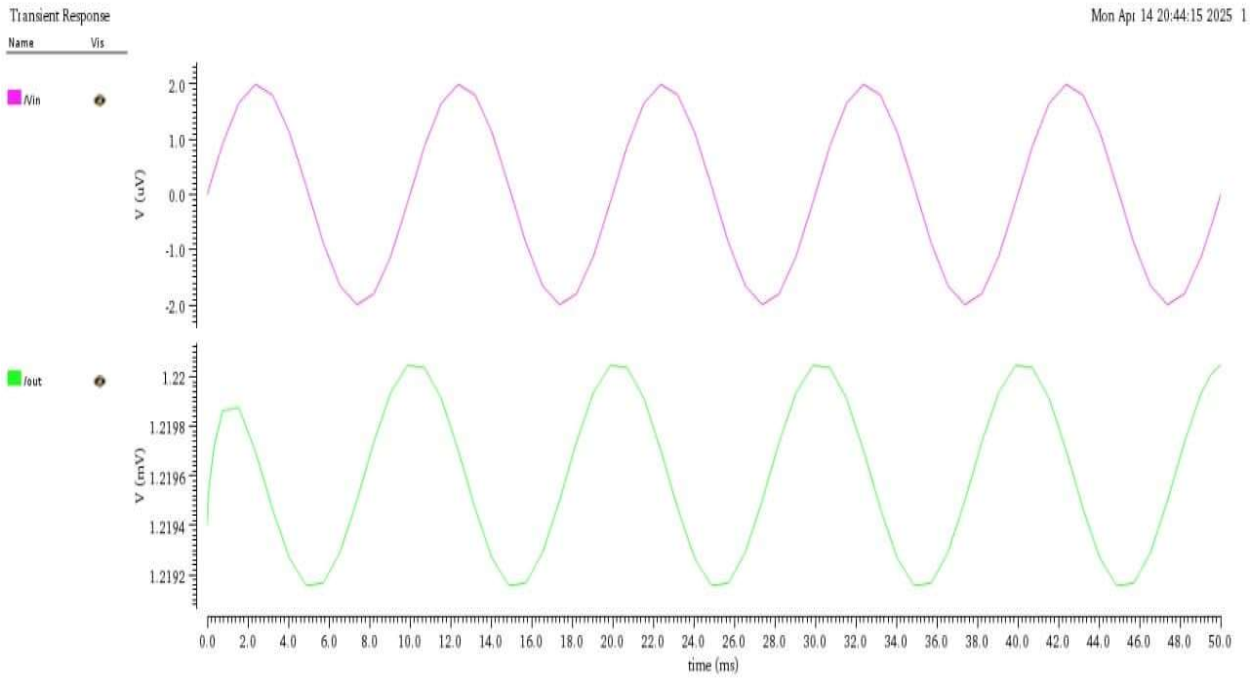

Figure 2.30(a) Simulation result for Sinusuidal input

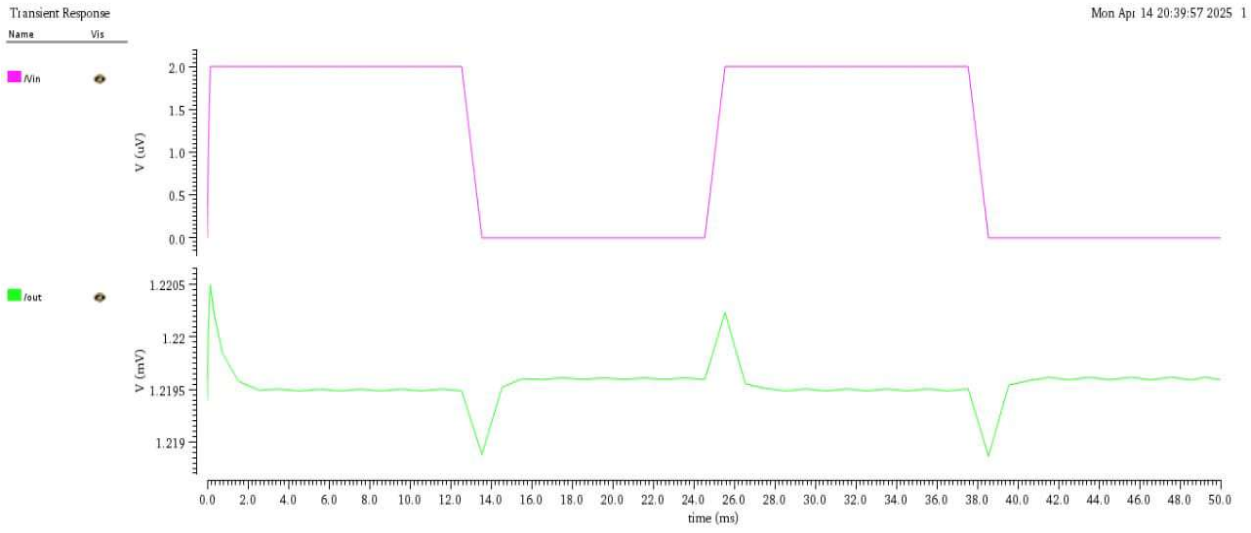

Figure 2.30(b) Simulation result for Square input

2.9 Design of Integrator Circuit

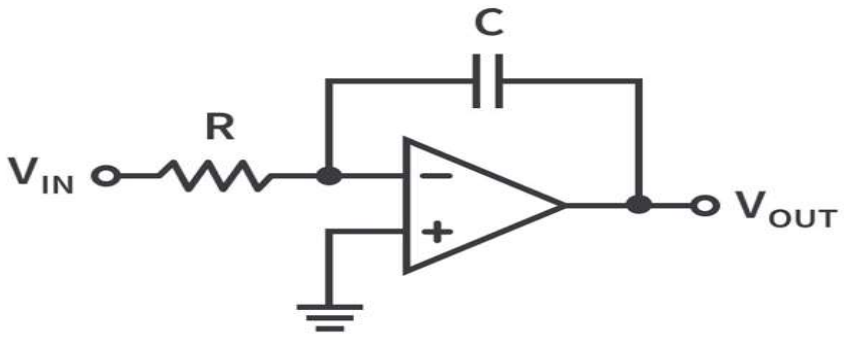

Figure 2.31 Ideal Op-Amp Integrator circuit

As the name implies, the Op-Amp Integrator is an operational amplifier circuit which performs the mathematical operation of integration. The basic op-amp integrator circuit consists of an operational amplifier with a resistor R connected to its inverting input and a capacitor C connected between the output and the inverting input.

$$V_{out} = - \frac{1}{R_1 C_1} \int_0^t V_{in}\, dt$$

$$= - \int_0^t \frac{V_{in}}{R_1 C_1} dt \qquad \text{. . . . . eq (2.9.1)}$$

2.9.1 Designing and Calculation of Op-amp Integrator

The values of capacitors and resistors are so chosen to allow proper time for charging and discharging of the output signal and provide the required gain. The capacitor on feedback network reduces harmonic distortion in the output signal. Two different signals, sinusoidal and square wave are given to the circuit and its output are plotted as given below -

Schematic:

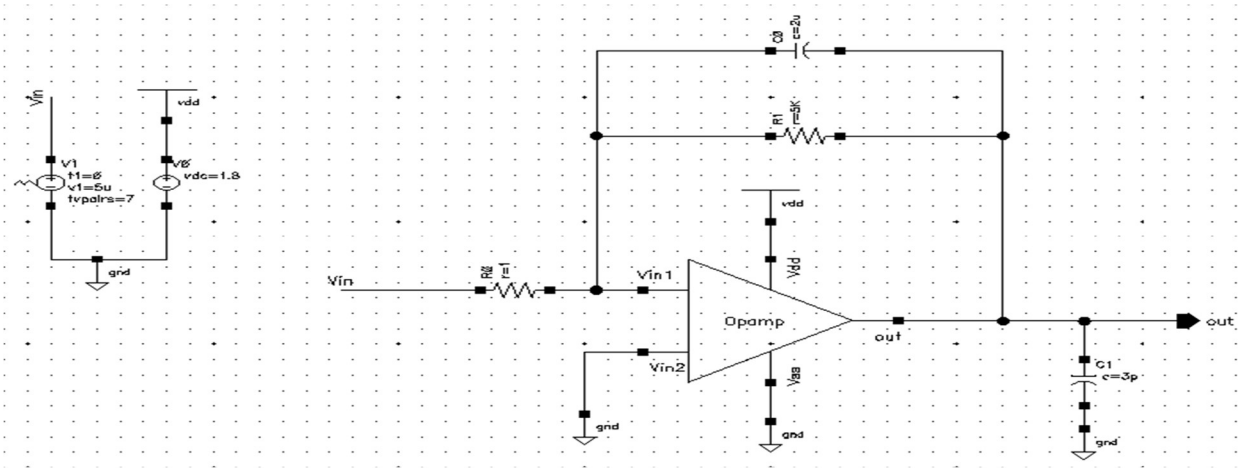

Figure 2.32 Schematic of Op-Amp Integrator

Simulation Output:

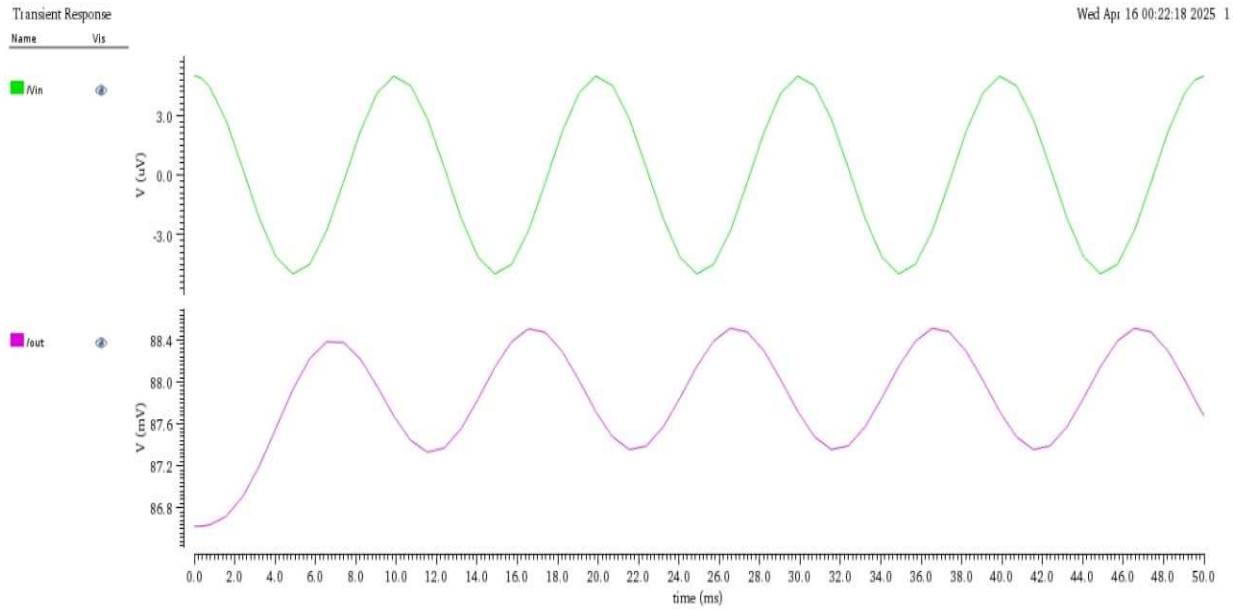

Figure 2.33(a) Simulation result for Sinusoidal input

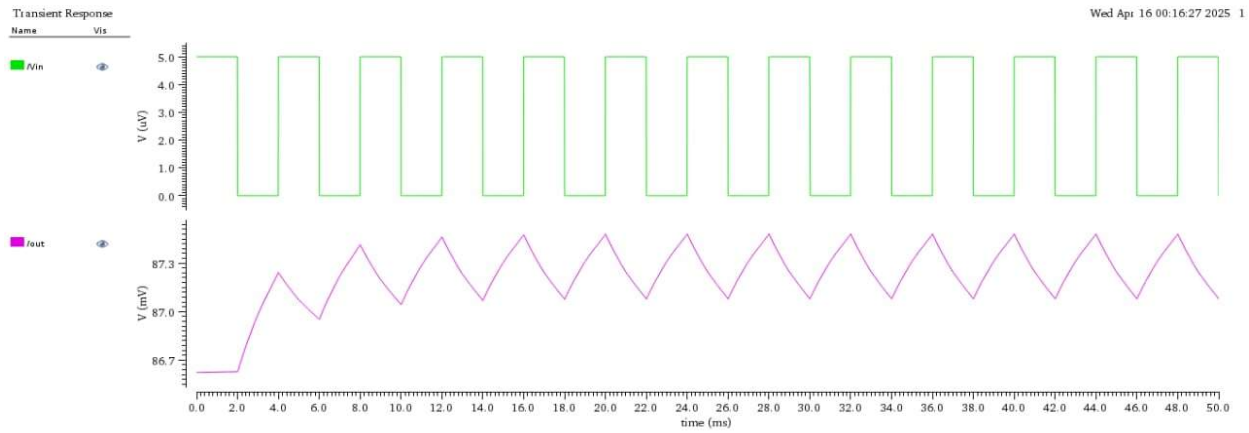

Figure 2.33(b) Simulation result for Square input

2.10 Designing Of 3-bit DAC Circuit

General Circuit:

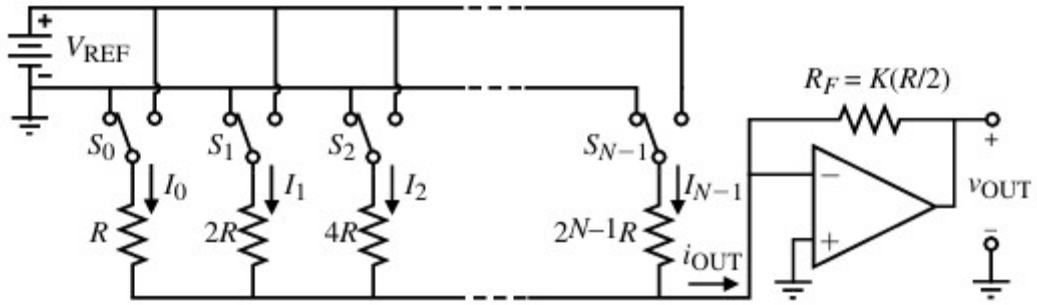

Figure 2.34 General Circuit for DAC

3-bit DAC:

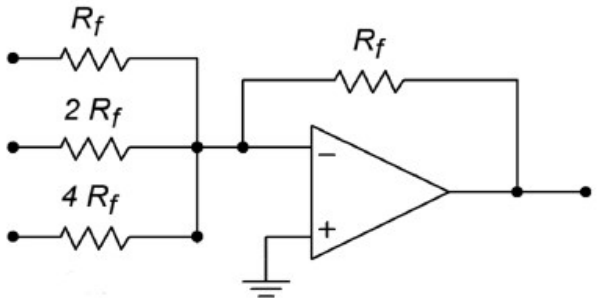

Figure 2.35 3-bit DAC Circuit

2.10.1 Designing and Calculation of 3-bit DAC Circuit

Schematic:

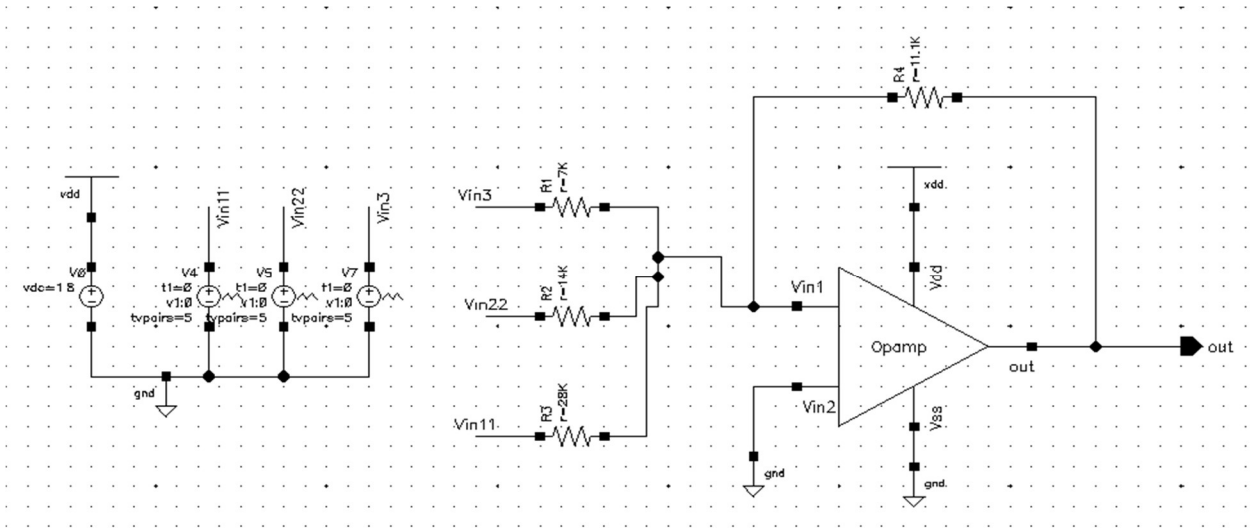

Figure 2.36 Schematic of 3-bit DAC Circuit

Simulation Output:

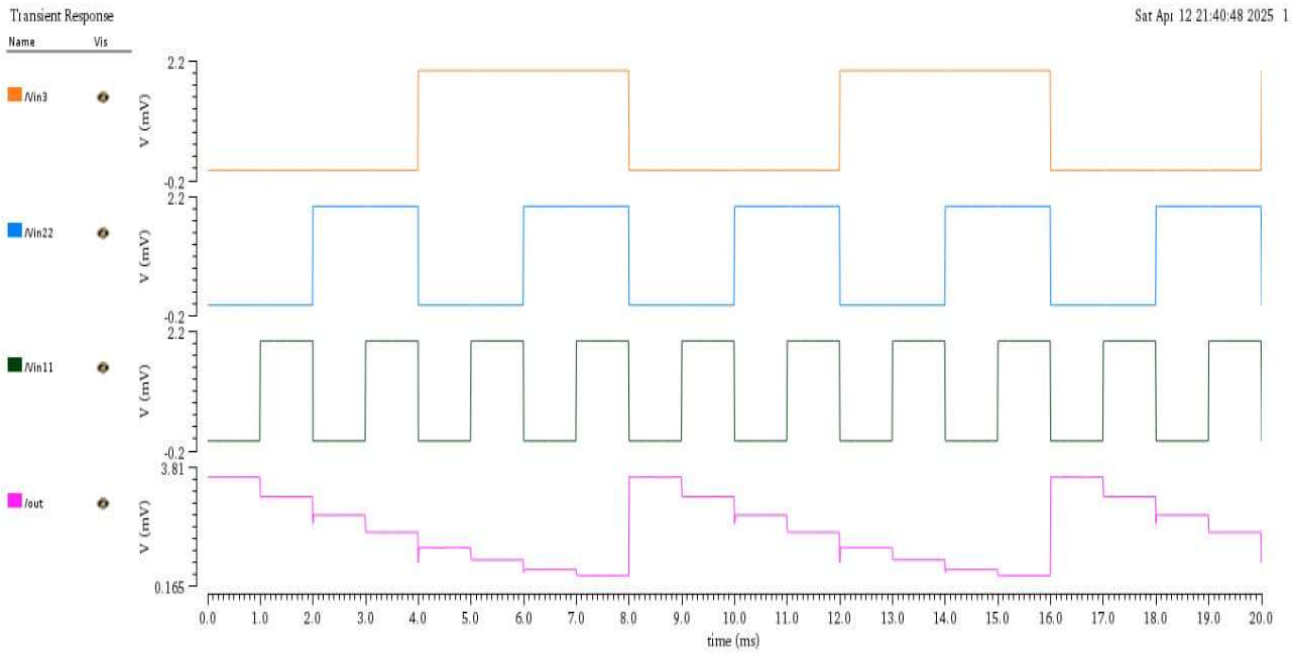

Figure 2.37 Simulation output of 3-bit DAC Circuit

Chapter 3

Conclusion and Future Scope

3.1 Future Scope and Modifications:-

The Binary Weighted Resistor DAC designed here can be implemented to design an ADC. Moreover, R-2R ladder DAC provides more accuracy.

The CMRR of the Opamp can be improved & flicker and thermal noise can be reduced by adjusting the W/L ratios of the transistors. Currently the Opamp gives a gain of 80dB. More gain can be obtained by using a different configuration of the transistors to design the OpAmp.

Instead of using a direct current source, a PMOS current source could be used to implement the whole circuit using only transistors. Moreover a little different configuration can be used to increase the Power Supply Rejection Ratio of the Op-amp.

3.2 Conclusion:-

A 3 bit Binary Weighted Resistor DAC was designed with considerable accuracy and precision. An Op-amp with a gain of 80dB, PM of 60° and CMRR of 64dB was designed to implement the DAC.

DC, AC, Transient, Stability and Noise analysis were studied during the designing and implementation of the circuits.

A comprehensive mathematical analysis was also performed during the designing of Common Source Amplifier, Differential amplifier, Opamp and DAC

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