Computer Architecture – Final Exam 2021

True or false questions. Each is 5 points.

a. Dependency existing among instructions is the lower bound of instruction level parallelism (ILP).

b. Issuing multiple instructions per cycle can reduce ideal CPI.

c. Each processor in an MIMD (Multiple Instruction Multiple Data) operates independently.

d. Shared memory multiprocessors can be global shared memory and distributed shared mmemory.

e. The number of bits in the (0,2) branch predictor with 8K entries is 4K bits.

f. Corelating branch predictors use local predictor and global predictor to predict branches.

g. For vector architectures, registers are controlled by compiler to hide memory latency and leverage memory bandwidth.

h. A group is a set of 32 threads that execute in parallel on GPU.

i. Amdahl's Law can be applied to SMTs.

j. Vector architectures are supersets of the multimedia SIMD instructions, including a better model for compilation.

K. The following loop has no loop-carried dependency.

```
for (i=0;i<100;i++) {
    A[i] = B[4*i+4];
    B[8*i+5] = A[i];
}
```

L. In the following loop, there are true dependences, output dependences, and antidependences.

```
for (i=0;i<100;i++) {
    A[i] = A[i] * B[i]; /* S1 */
    B[i] = A[i] + c; /* S2 */
    A[i] = C[i] * c; /* S3 */
    C[i] = D[i] * A[i]; /* S4 */
 }
```

M. That instructions are of the same length in a processor will make pipelining easy.

N. For performance, the datapath with CPI = 1 is better than the datapath with CPI = 2.

O. Vector architectures and compilers are easier than scalar architectures for multimedia applications.

P. Simultaneous multithreading (SMT) is not suitable for dynamic scheduling.

R. In a dynamic scheduling processor, the instructions of the same type (e. g. add) will be executed following the execution order.

S. Consider a branch-target buffer that has penalties of 0, 2, and 2 clock cycles for correct

conditional branch prediction, incorrect prediction, and a buffer miss, respectively. Consider a branch-target buffer design that distinguishes conditional and unconditional branches, storing the largest address for a conditional branch and the target instruction for an unconditional branch. The penalty is 1 cycle when an unconditional branch is found in the buffer.

T. Snoopy cache coherence protocol can be used without a centralized bus.

U.On average, the misprediction rate for the integer programs is higher than that for the floating-point programs.