PAA5101: Optical Tracking Miniature Chip

General Description

The PAA5101 is a high performance and high accurate optical tracking chip using PixArt LASER/LED hybrid optical navigation technology. It integrates an optical chip with a LASER light source in a single miniature package. When working with an external infrared LED and a PixArt designed companion lens LST0-217, the chip can track on a wide range of material surfaces from white glossy tiles to shag carpets. Besides, the sensor also provides a high DOF range to accommodate to uneven surfaces when tracking.

Key Features

- Reflowable SMT package with built-in VCSEL LASER light source in a single package
- LASER/LED hybrid optical navigation technology
- Compliance to IEC/EN 60825-1:2014 Eye Safety with Class 1 LASER power output level
- Tracking on glossy surfaces (metal, tiles) by LASER and rough surface (cloth, carpets) by LED with a lens
- Wide DOF range of tracking
- High accuracy of tracking
- Tracking speed is up to 45 ips on glossy metal surfaces
- Support 3-wire SPI interface
- Programmable resolution

Applications

- Devices that requires tracking on surfaces with wide DOF working range
- Devices that requires tracking on surfaces with wide range of material surfaces
- Devices that requires detecting the speed and distance of moving surfaces

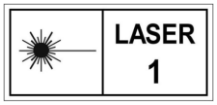
Key Parameters

Parameter	Value
Supply Voltage	VDD : 2.7 ~ 3.6V
Control Interface	3-wire SPI
Companion lens	LST0-217
Light Source	Infrared 850nm LED Infrared 850nm LASER
Max .Tracking Speed	45ips (LASER mode) 100ips (LED mode)
Operating current (@ VDD = 3.3V)	Run mode : 10mA (LASER mode) 44mA (LED mode) Power down : 15uA
Distance from chip top to tracking surface	5 cm (TBD)
Package Size L x W x H	4.4 x 4.6 x 1.0 mm

Ordering Information

Part Number	Package Type
PAA5101	LGA 10-pin

RoHS compliant



For any additional inquiries, please contact us at
http://www.pixart.com/contact.asp

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1.0 Introduction

1.1 Overview

PAA5101 is a high performance CMOS-processed optical image chip with integrated digital image process circuits. It is based on PixArt LASER/LED hybrid optical navigation technology which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the speed, the direction and the magnitude of motion. The displacement X and Y information are available in registers. A host controller can read and translate the displacement X and Y information from the SPI serial interface.

Since LASER and LED are not allowed to turn on at the same time, the host controller should also keep reading the Image Quality registers to determine whether if LASER or LED should be chosen to illuminate the surfaces. In general, when LASER is chosen for illumination, the Image Quality value is high when tracking on tiles and is low when tracking on carpets. On the contrary, when LED is chosen for illumination, the Image Quality is high when tracking on carpets and is low when tracking on tiles.

Note: Throughout this document PAA5101 is referred to as the chip.

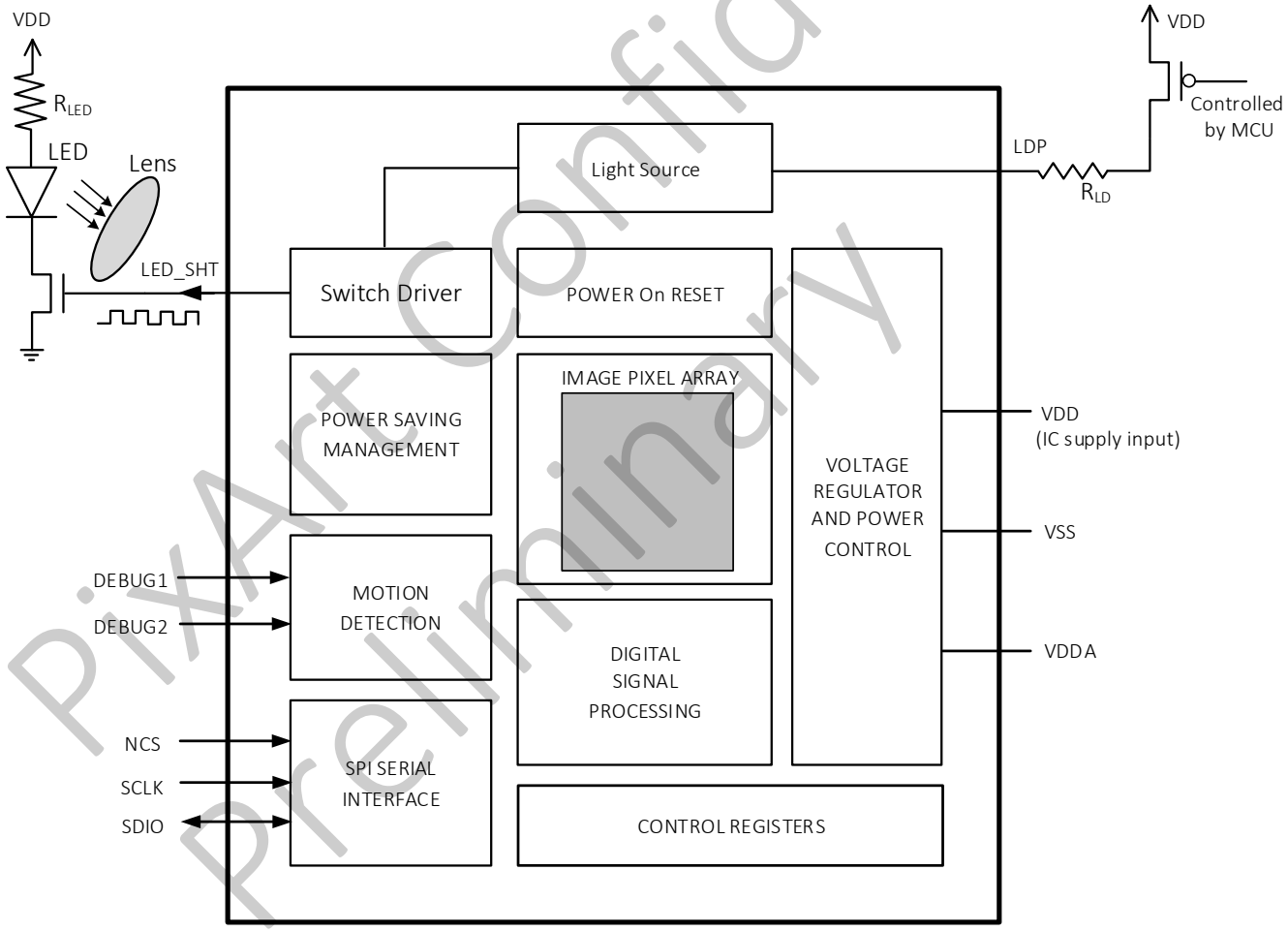
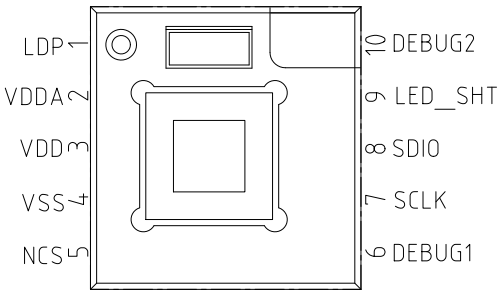


Figure 1. Chip Architecture Functional Block Diagram

1.2 Signal Description



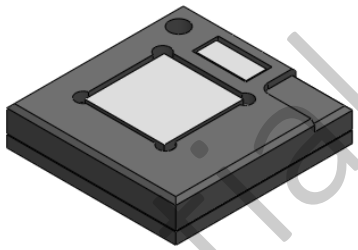


Figure 2. Pinout Configuration

Table 1. Signal Pins Description

Pin No.	Signal Name	Type	Description
1	LDP	PWR	Anode of the VCSEL LASER. This pin should be connected to VDD (2.7V - 3.6V) through a resistor (R_{LD}).
2	VDDA	PWR	Internal 1.8V regulator output
3	VDD	PWR	Power supply for I/O and LASER, voltage range : 2.7V ~ 3.6V
4	VSS	GND	Chip ground
5	NCS	IN	Chip select for 3-wire SPI interface (active low)
6	DEBUG1	IN	This pin is for debug purpose and is only for PixArt internal use. In normal operation, this pin should connect a 100k ohm resistor to GND.
7	SCLK	IN	Clock input for SPI interface
8	SDIO	I/O	Bi-directional I/O for SPI interface
9	LED_SHT	OUT	LED Shutter. The shutter control for the external LED light source
10	DEBUG2	NC	This pin is for debug purpose and is only for PixArt internal use. In normal operation, this pin should connect a 100k ohm resistor to GND.

2.0 Mechanical Specifications

2.1 Package Mechanical Dimension

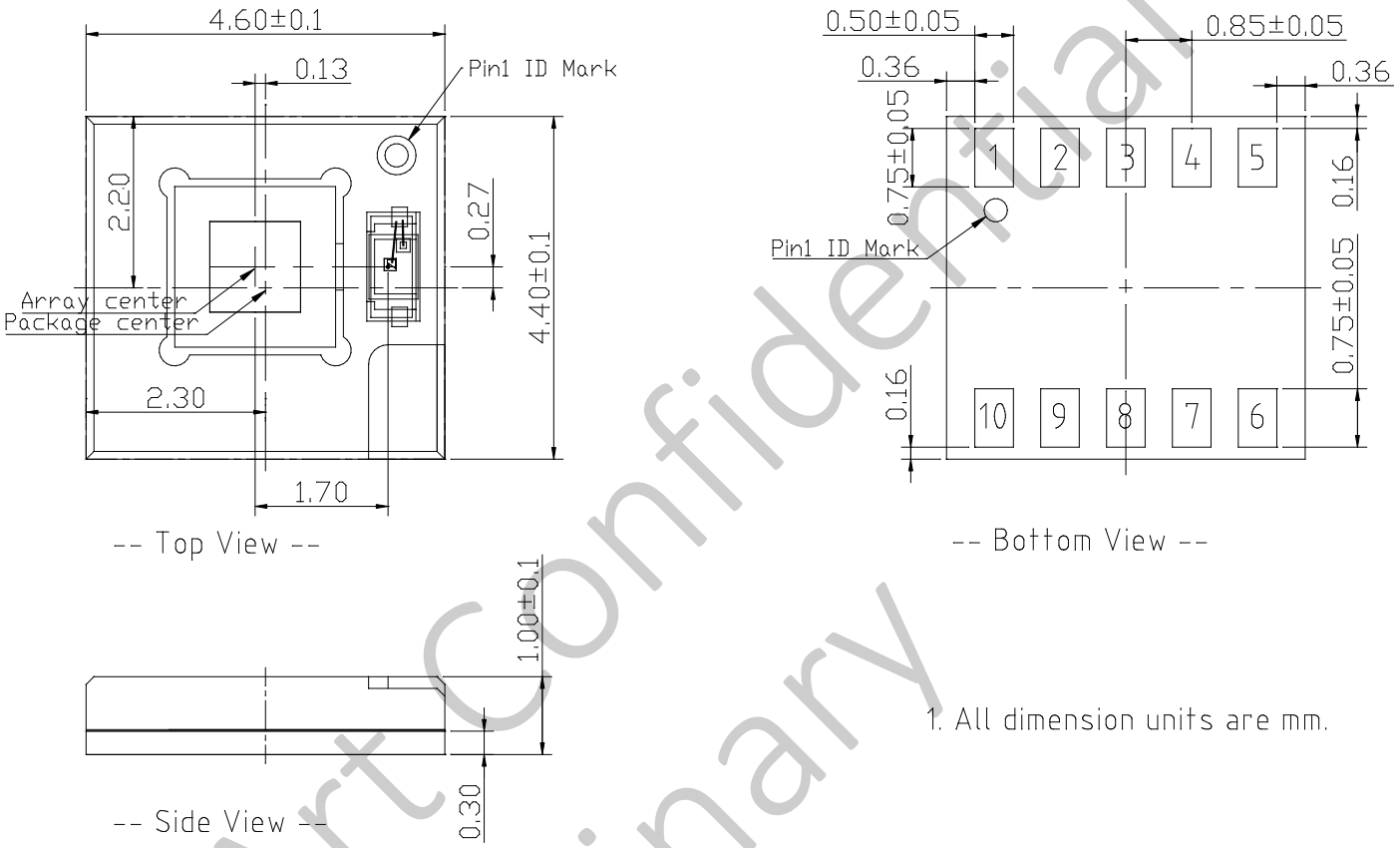


Figure 3. Chip Package Outline Diagram

2.2 Lens Mechanical Dimension

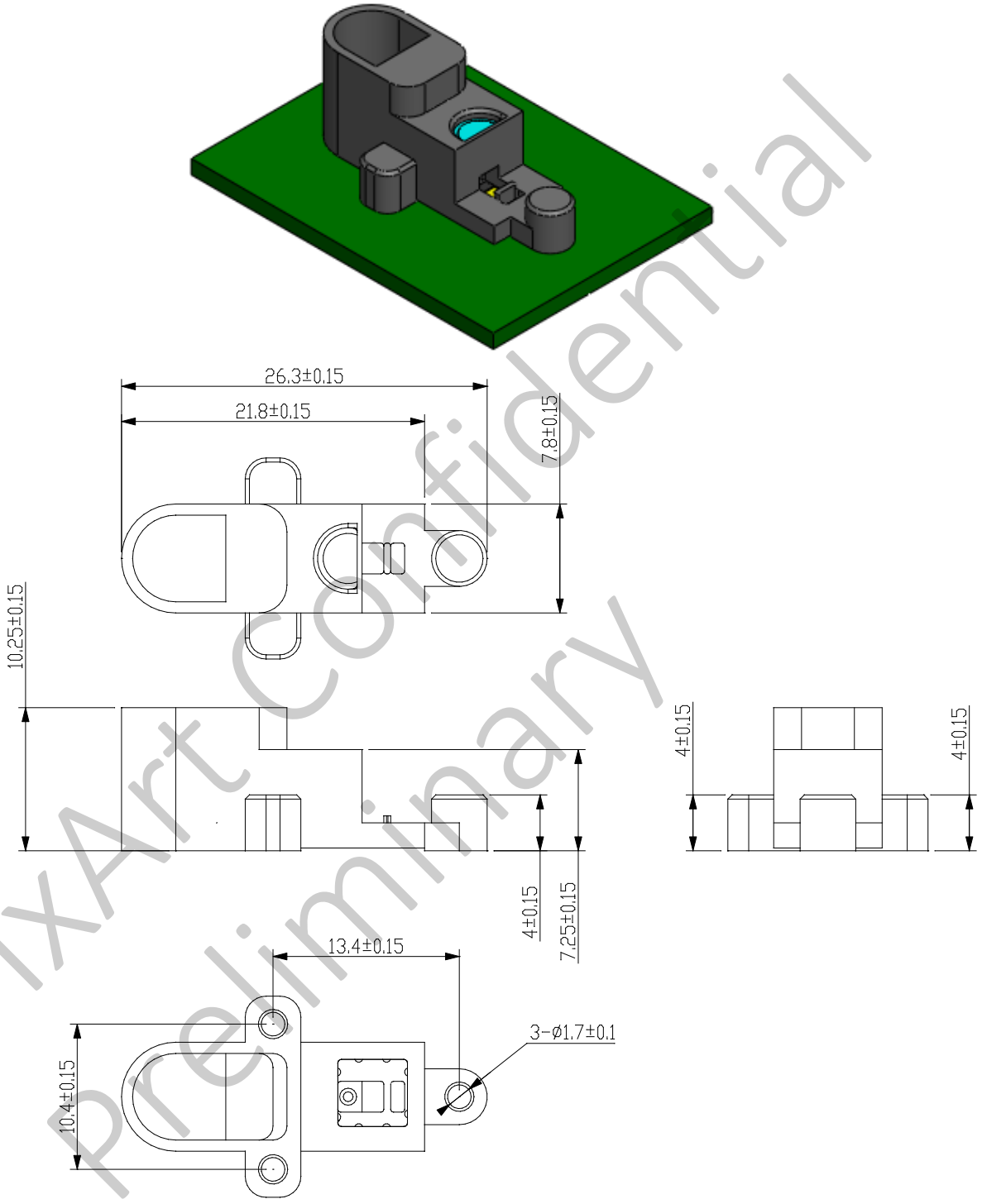


Figure 4. Lens Mechanical Dimensions

2.3 PCB Layout Guides

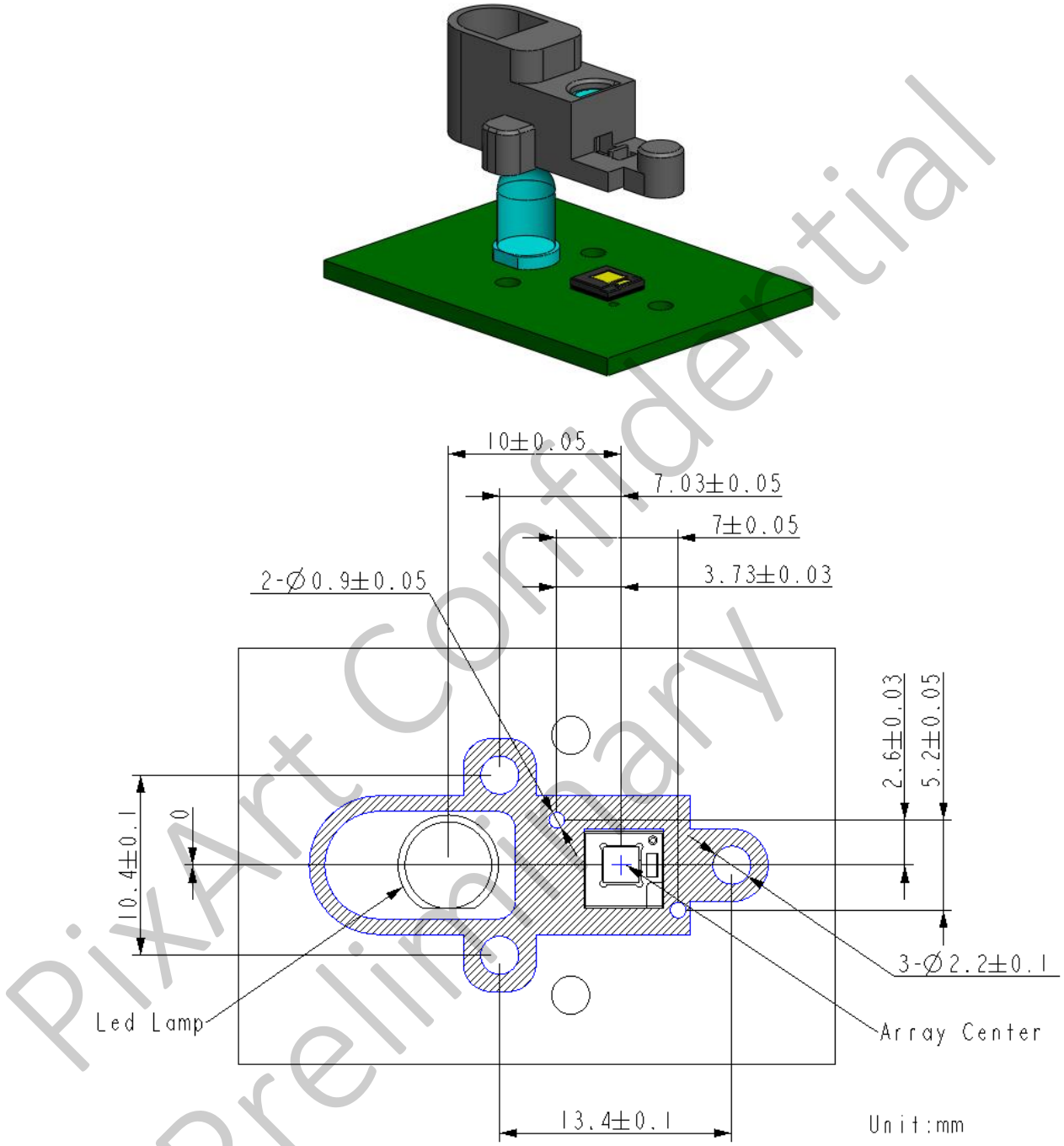


Figure 5. PCB Layout Guides

3.0 Operating Specifications

3.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
Supply Voltage	VDD	-0.3	3.9	V	I/O and LASER power
	VDDA	-0.2	2.3	V	Core circuitry power
ESD	ESD_{HBM}		2	kV	Class 2 on all pins, as per human body model. JESD22-A114E with 15 sec zap interval.

Notes:
1. At room temperature.
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.

3.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_{STG}	-40	-	85	°C	
Operating Temperature	T_A	-20	25	60	°C	
Power Supply Voltage	VDD	2.7	3.3	3.6	V	I/O and LASER power supply
Supply Noise (peak to peak)	V_{pp}	-	-	100	mV	Peak to peak voltage within 100KHz – 80MHz
SPI Clock Frequency	SCLK	-	-	2	MHz	
Tracking Speed	SP	-	-	45	IPS	on glossy metal surfaces
				100		on white copy paper
Laser Drive Current (DC)	I_{LD}	5.0	7.0	8.0	mA	Configured via LD_SRC register

Note: PixArt does not guarantee the performance if the operating temperature is beyond the specified limit.

3.3 DC Characteristics

Table 4. DC Electrical Specifications

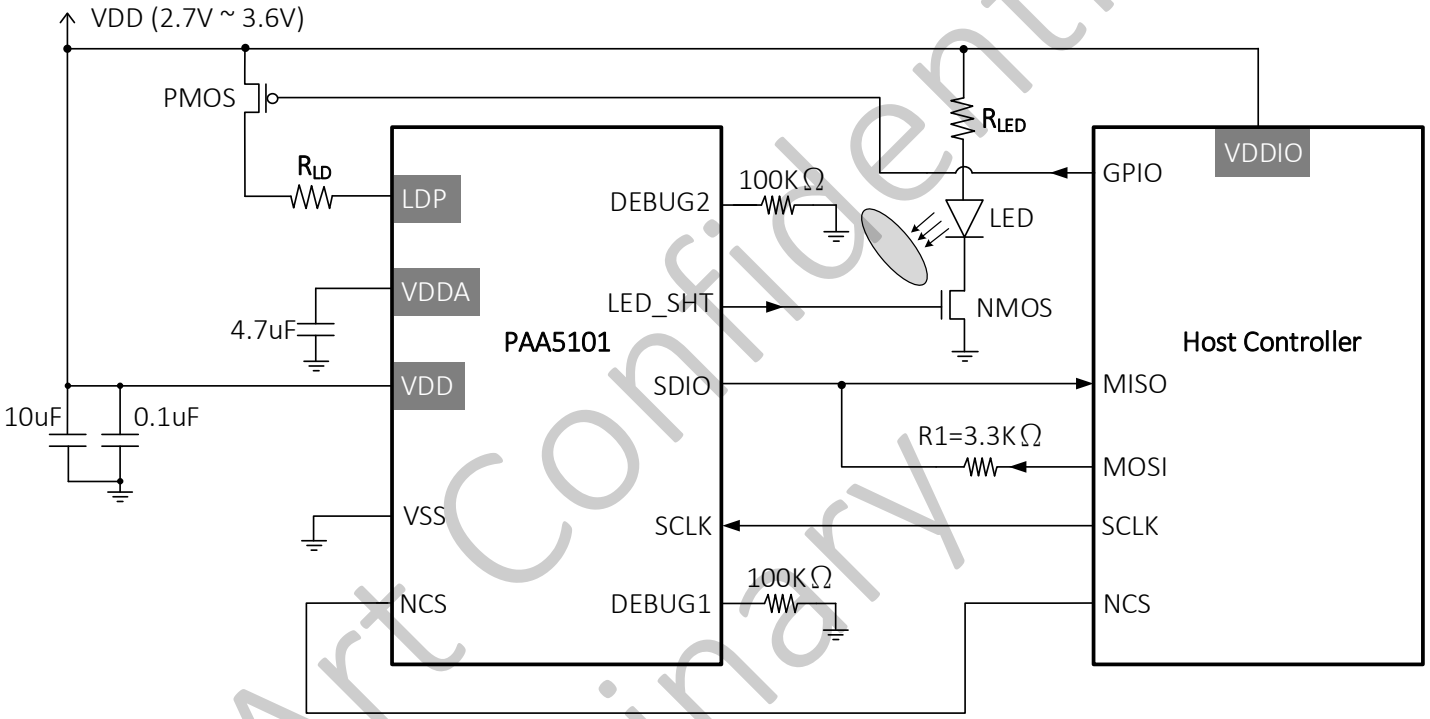
Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Consumption	I_{VDDRN}	-		-	mA	VDD current @ run mode
	I_{VDDPD}				mA	VDD current @power down
I/O Input High Voltage	V_{IH}	0.7* V_{DD}	-	-	V	
I/O Input Low Voltage	V_{IL}	-	-	0.3* V_{DD}	V	
I/O Output High Voltage	V_{OH}	V_{DD} -0.4	-	-	V	@I_{OH} = 2mA
I/O Output Low Voltage	V_{OL}	-	-	0.4	V	@I_{OL} = 2mA

Notes: All the parameters are tested under operating conditions: V_{DD} = 3.3V (including LASER current), T_A = 25°C

4.0 Design Reference

4.1 Reference Application Schematics

The chip only supports simplified 3-wire SPI slave mode, while some host controllers may only support standard 4-wire SPI master mode. In this case, users can connect the host controller to the chip using the method shown below to communicate with each other. Take note that the 3.3K ohm resistor (R1) is for reference only and the resistance may have to be modified according to different I/O capability as per the specification of the host controllers. The resistor R_{LD} and R_{LED} are to restrict the current flowing through the LASER and LED. In order not to overdrive the LASER and LED, please adopt the resistance specified on the table.



VDD (Volt)	R_{LD}(ohm) +/-3%	R_{LED}(ohm) +/-3%
3.6	177	19
3.5	165	18
3.4	152	17
3.3	140	15
3.2	128	14
3.1	115	13
3.0	102	12
2.9	90	11
2.8	78	10
2.7	65	9

Figure 6. Reference Application Schematics

5.0 3-Wire SPI Serial Interface

The chip supports 3-wire Serial Peripheral Interface (SPI). The host controller can use the SPI to write and read registers in the chip, and to read out the motion information. The host controller always initiates communication; the chip never initiates data transfers. NCS, SCLK and SDIO may be driven directly by the host controller. SDIO may also be driven by the chip when data is read out from chip registers.

- NCS: Chip select input (active low). NCS needs to be low to activate the SPI; otherwise, SDIO will be at high-Z state and SCLK will be ignored. NCS can also be used to reset the SPI in case a communicational error happens.
- SCLK: Clock input. It is always generated by the host controller.
- SDIO: Bi-directional input/output data

5.1 Transmission Protocol

The transmission protocol is a 3-wire link, half duplex protocol between the host controller and the chip. All data changes on SDIO are initiated by the falling edge on SCLK. The host controller always initiates communication; the chip never initiates data transfers. The transmission protocol consists of the following two operation modes.

- Write Operation
- Read Operation

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has a bit-7 as its MSB to indicate data direction. The second byte contains the data.

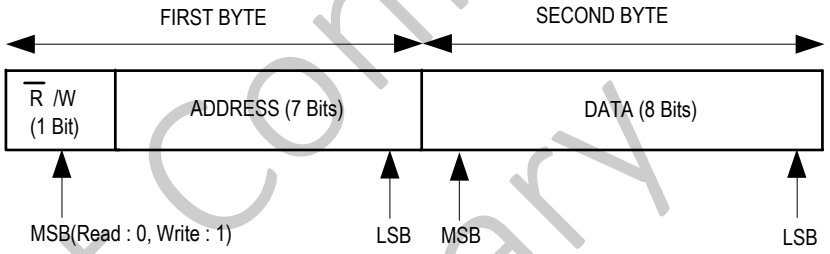


Figure 7. Transmission Protocol

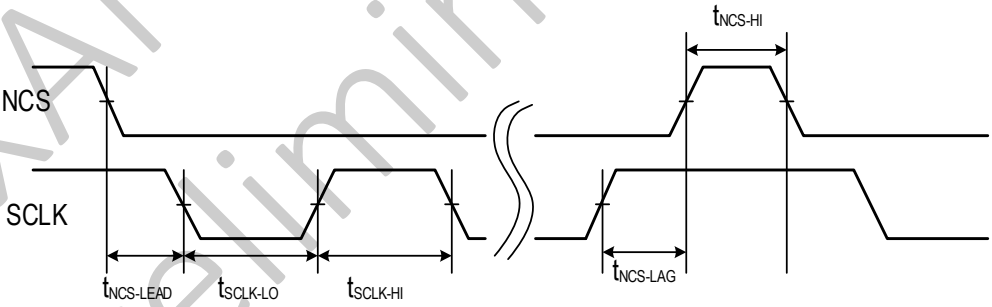


Figure 8. NCS vs SCLK Timing Requirement

5.1.1 Write Operation

A write operation, defined as data is going from the host controller to the chip, is always initiated by the host controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The communication is synchronized by SCLK. The host controller changes SDIO on the falling edges of SCLK and the chip reads SDIO on the rising edges of SCLK.

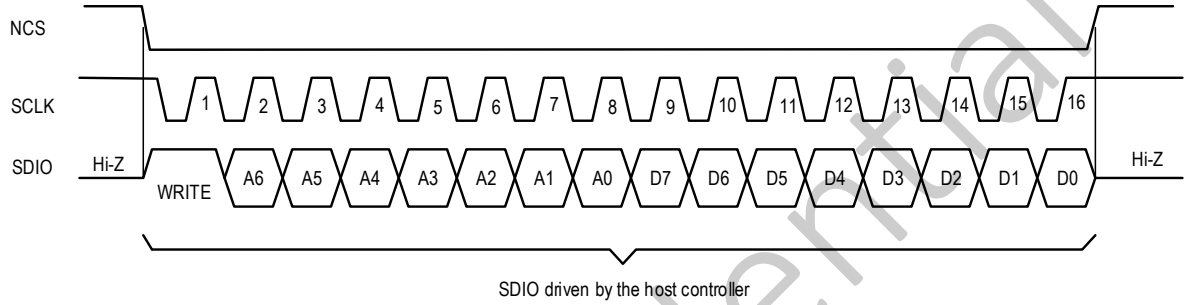


Figure 9. Write Operation

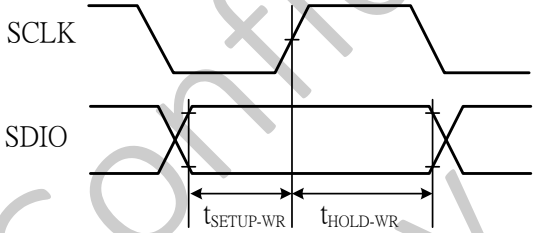


Figure 10. SDIO setup and hold time during write operation

5.1.2 Read Operation

A read operation is initiated by the host controller and consists of two bytes. The first byte contains the address specified by the host controller and has a "0" as its MSB to indicate data direction. The second byte contains the data which is outputted by the chip. The communication is synchronized by SCLK. SDIO is changed on the falling edges of SCLK and is read on every rising edge of SCLK. The host controller must release SDIO bus and handover the control of SDIO bus to the chip on the falling edge of last address bit.

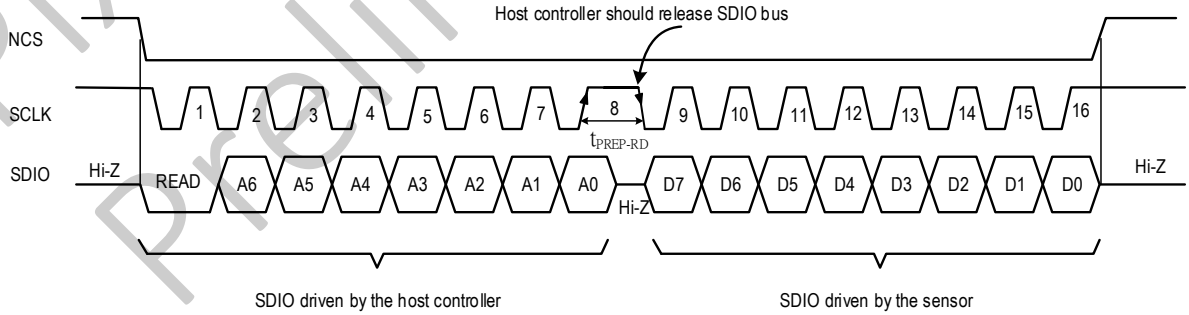


Figure 11. Read Operation

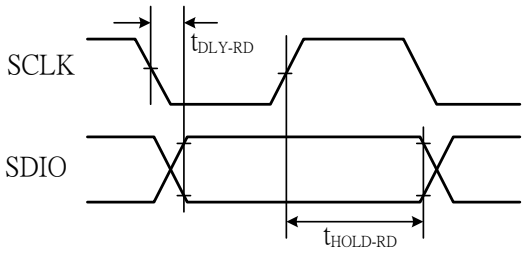


Figure 12. SDIO delay and hold time during read operation

5.2 SPI Timing

Table 5. SPI Timing Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCLK frequency	F_{SCLK}	-	-	2	MHz	SPI max. operation frequency
SCLK High Time	$t_{SCLK-HI}$	250	-	-	ns	SCLK min. high time
SCLK Low Time	$t_{SCLK-LO}$	250	-	-	ns	SCLK min. low time
NCS Enable Lead Time	$t_{NCS-LEAD}$	1	-	-	us	From NCS falling to first SCLK falling
NCS Enable Lag Time	$t_{NCS-LAG}$	1	-	-	us	From Last SCLK rising to NCS rising
NCS min. High Time	t_{NCS-HI}	2	-	-	us	From previous NCS rising to next NCS falling
SDIO Write Setup Time	$t_{SETUP-WR}$	250	-	-	ns	SDIO data valid before SCLK rising
SDIO Write Hold Time	$t_{HOLD-WR}$	250	-	-	ns	SDIO data valid after SCLK rising
SDIO delay after SCLK	t_{DLY-RD}	-	-	50	ns	From SCLK falling to SDIO data valid, no load conditions
SCLK delay for Data Preparation	$T_{PREP-RD}$	250	-	-	ns	The min. time between the falling of 8th SCLK and the rising of 9th SCLK
SDIO Read Hold Time	$t_{HOLD-RD}$	250	-	-	ns	SDIO data valid after SCLK rising
SDIO Rise Time	t_{SDIO-R}	-	30	-	ns	@C_L = 30 pF
SDIO Fall Time	t_{SDIO-F}	-	30	-	ns	@C_L = 30 pF

6.0 Read Motion Data

Whenever the chip detects the occurrence of motion, the detected motion data (X-movement and Y-movement) is accumulated and stored in chip's internal buffer. The host controller can read out this motion data through register Delta_X (address 0x03 and 0x011) and Delta_Y(address 0x04 and 0x12). Before reading the motion data through these registers, be sure to read register Motion_Status (address 0x02) first to check if the MOTION bit (bit 7) is 1. If the MOTION bit is 1, the data in register Delta_X and Delta_Y is valid, otherwise it is invalid. By reading and checking register MOTION Status (address 0x02) periodically, the host controller can get the motion data in a simple way through the SPI interface. Be noticed that the 8ms shown in the flowchart below is just for reference. The delay time might depend on the capability of the host controller and the need for different applications.

Besides, in order to track on a wide range of surface material, the light source for illumination has to be switched between LASER and LED. The host controller should monitor the IQ value of the surface and if the IQ value is too low (lower than a predefined value, IQ_THD, stored in the host controller), the host controller has to switch the existing light source to another one and change other related register settings as well.

Note: the flowchart below just shows one of the methods to switch between LED mode and LASER mode. Different applications might need different methods to implement this switch function.

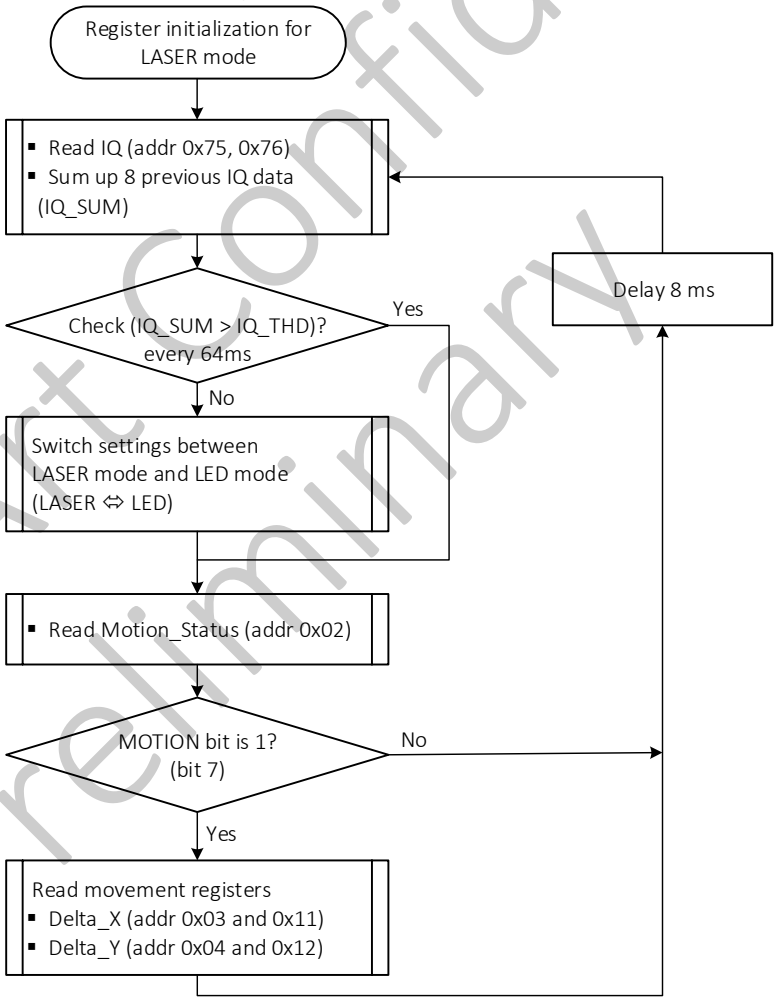


Figure 13. Read Motion Data with Polling Mode

7.0 Software Control Functions

7.1 Software Power-Down

The chip can also be put into the lowest power state in power-down mode by setting PD_EnH bit (bit 3) in the Configuration register (address 0x06) through SPI interface. In power-down mode, all the chip register settings are retained and can be accessed through SPI interface as well. Reset PD_EnH bit will get the chip out of the power-down mode. To obtain correct motion data, it is recommended that the host controller should wait at least 3ms before reading the motion data after resetting the PD_EnH bit.

7.2 Software Reset

During power-up, the chip does not need an external power-on reset as there is an internal circuitry that performs power-on reset function in the chip. However the chip can also be reset by setting the RESET bit (bit 7) of Configuration register (address 0x06). Upon a software reset being executed, all the register values will be reset to the power-up default values and all the recommended register settings must be reloaded in order to keep the chip working correctly.

8.0 LASER Drive

8.1 LASER Drive Control

Under normal operating condition, the chip internally generates the drive current for the integrated LASER diode in pulsed mode. The LASER drive current source is configurable via LD_SRC register (address 0x51) with power-up default setting of LD_SRC[4:0] = 0x0E which is equivalent to ~17mA when in continuous mode; while the maximum drive current could be up to ~37mA when LD_SRC[4:0] = 0x1F. However, the software setting MUST limit any value beyond LD_SRC[3:0] = 0x06 that drive >8mA current as the LASER output may degrade in long run or could be damaged in the worst scenario. The recommended setting for common surface tracking application is LD_SRC[4:0] = 0x06 (~7.2mA drive current).

As shown in Section 4.1 Reference Schematics, an external current limiting resistor, Rext is mandatory to be included in any design application to limit the overcurrent condition during the system power-up stage as prevention on overdriving the LASER. The VDD power supplies for the chip should be well regulated and filtered to prevent spurious voltage conditions at all time.

8.2 LASER Power

The LASER eye safety limit of the sensor is at LASER output power within the 716µW when the LASER drive current is not exceeding 8mA in continuous mode. Since the LASER drive is always pulsed during any sensor operational modes, the average LASER power will never exceed the LASER eye safety limit. As the connection of LASER drive control pin to the LASER's Cathode pin is bonded internally in the module package, the risk of any external means for the LASER could be driven in continuous mode is relatively low. Thus, the system design of PAA5101 is claimed to be compliant to LASER Eye Safety Class 1 (IEC/EN 60825-1:2014).

The manufacturer of the end product is responsible to ensure the end system design is taking the following precaution steps:

1. The software setting of the LASER drive control register does not exceed the maximum allowable LASER drive current specification as listed in Table 3. Recommended Operating Conditions.
2. The external current limiting resistor, Rext, is well connecting in between LDP pin to VDD. Please refer to chapter 4.1.

Users must be aware and take steps to avoid being exposed to the LASER light at all times.

Precautions:

1. All users who will be working with an active (powered) sensor component should consider taking LASER eye safety training.
2. LASER eye safety responsibility resides at the system level, not at the component level, thus the system is responsible to ensure the user's eye safety by clearly instructing and labeling the potential danger to the unprotected eyes.
3. The LASER light is in the infrared spectrum of 850 nm. It is not intended to be viewed so users should not try to look at the sensor's aperture directly. Appropriate instrument for indirect viewing is recommended.

9.0 Registers

9.1 Registers Summary

Table 6. Registers List

Address	Register Name	Access	Reset	Brief Description
0x00	Product_ID1	R	0x31	Product Identifier [11:4]
0x01	Product_ID2	R	0x61	Upper 4 bits for Product Identifier, PID [3:0] Lower 4 bits for Product Version, VID [3:0]
0x02	Motion_Status	R	-	Motion Status information
0x03	Delta_XL	R	-	Low Byte of X-movement for 16-bit 2's complement data Delta_X[15:0] = {Delta_XH[7:0], Delta_XL[7:0]}
0x04	Delta_YL	R	-	Low Byte of Y-movement for 16-bit 2's complement data Delta_Y[15:0] = {Delta_YH[7:0], Delta_YL[7:0]}
0x06	Configuration	R/W	0x10	Software power down and reset
0x09	Write_Protect	R/W	0x00	Write Protect to avoid missed-writing registers
0x0D	RES_X	R/W	0x27	CPI resolution setting for X-direction
0x0E	RES_Y	R/W	0x2B	CPI resolution setting for Y-direction
0x11	Delta_XH	R	-	High Byte of X-movement for 16-bit 2's complement data Delta_X[15:0] = {Delta_XH[7:0], Delta_XL[7:0]}
0x12	Delta_YH	R	-	High Byte of Y-movement for 16-bit 2's complement data Delta_Y[15:0] = {Delta_YH[7:0], Delta_YL[7:0]}
0x15	Shutter	R	-	Shutter value[7:0]
0x17	Frame_Avg	R	-	Average brightness of a frame
0x51	LD_SRC	R/W	0x0E	Programmable current source for LASER
0x75	IQH	R	-	High byte of IQ (Image Quality) [15:8]
0x76	IQL	R	-	Low byte of IQ (Image Quality) [7:0]

9.2 Register Functional Description

Register Name	Product_ID1							
Bank	0			Address		0x00		
Access	Read-Only			Reset Value		0x31		
Bit Field	7	6	5	4	3	2	1	0
	PID[11:4]							
Description	This value is a unique identification assigned to this chip only. The value in this register does not change; it can be used to verify that the serial communications link is functional. PID[11:4] = Product Identifier[11:4]							

Register Name	Product_ID2							
Bank	0			Address		0x01		
Access	Read-Only			Reset Value		0x61		
Bit Field	7	6	5	4	3	2	1	0
	PID[3:0]				VID[3:0]			
Description	This value is a unique identification assigned to this chip only. The value in this register does not change; it can be used to verify that the serial communications link is functional. PID[3:0] = Product Identifier[3:0] VID[3:0] = Product Version[3:0]							

Register Name	Motion_Status							
Bank	0			Address		0x02		
Access	Read-Only			Reset Value		NA		
Bit Field	7	6	5	4	3	2	1	0
	MOTION	Reserved	DYOVF	DXOVF	Reserved	Reserved	Reserved	Reserved
Description	Typically in the motion detection routine, the host controller will poll the chip for valid motion data by checking the MOTION bit. If the MOTION bit is set, the motion data in Delta_XL, Delta_YL, Delta_XH and Delta_YH registers are valid and available to be read. Be sure to read MOTION bit first before reading out Delta_XL, Delta_YL, Delta_XH and Delta_YH registers. DXOVF bit and DYOVF bit show whether if the motion report buffers have overflowed since last read out.							

Field	Reset	Description
MOTION	0	Motion detected since last report 0 = No motion 1 = Motion detected, data in register Delta_XL, Delta_XH, Delta_YL and Delta_YH is valid and ready to be read out.
DYOVF	0	Internal buffer for Y-movement has overflowed since last read out 0 = No overflowed 1 = Overflowed
DXOVF	0	Internal buffer for X-movement has overflowed since last read out 0 = No overflowed 1 = Overflowed

Register Name	Delta_XL							
Bank	0			Address		0x03		
Access	Read-Only			Reset Value		NA		
Bit Field	7	6	5	4	3	2	1	0
	Delta_X[7:0]							
Description	Delta_XL is the low byte of a 2's complement value of 16-bit X-movement data. Delta_X[15:0] = {Delta_XH[7:0], Delta_XL[7:0]} Register Delta_XL is valid only if register Motion_Status (address 0x02) is read and MOTION bit (bit 7) is 1.							

Register Name	Delta_YL							
Bank	0			Address		0x04		
Access	Read-Only			Reset Value		NA		
Bit Field	7	6	5	4	3	2	1	0
	Delta_Y[7:0]							
Description	Delta_YL is the low byte of a 2's complement value of 16-bit Y-movement data. Delta_Y[15:0] = {Delta_YH[7:0], Delta_YL[7:0]} Register Delta_YL is valid only if register Motion_Status (address 0x02) is read and MOTION bit (bit 7) is 1.							

Register Name	Configuration							
Bank	0			Address		0x06		
Access	R/W			Reset Value		0x10		
Bit Field	7	6	5	4	3	2	1	0
	RESET	Reserved	Reserved	Reserved	PD_EnH	Reserved	Reserved	Reserved
Description	Configuration register allows users to change the configuration of the chip.							

Field	Reset	Description
RESET	0	Full chip reset. This bit will be de-asserted automatically. 0 = Normal operation mode 1 = Full chip reset (to reset all the chip's internal registers and states)
PD_EnH	0	Power down mode for lowest power consumption 0 = Normal operation 1 = Power down mode (but retain the chip register settings)

Register Name	Write_Protect							
Bank	0			Address		0x09		
Access	R/W			Reset Value		0x00		
Bit Field	7	6	5	4	3	2	1	0
	WP[7:0]							
Description	Write Protect register is used to avoid host controller miss-writing to the registers after address 0x09 onwards. 0x00 = Enable (Default), registers after address 0x09 are read only 0x5A = Disable, registers after address 0x09 can be read/write							

Register Name	RES_X							
Bank	0			Address		0x0D		
Access	R/W			Reset Value		0x27		
Bit Field	7	6	5	4	3	2	1	0
	Reserved	RES_X[6:0]						
Description	CPI resolution setting of X-direction movement. Estimated CPI resolution of X-direction = 50 * RES_X Note: the resolution of a step of RES_X (i.e. 50) might slightly change across different types of surface, curvature of the surface and distances between chip and surface.							

Register Name	RES_Y							
Bank	0			Address		0x0E		
Access	R/W			Reset Value		0x2B		
Bit Field	7	6	5	4	3	2	1	0
	Reserved	RES_Y[6:0]						
Description	CPI resolution setting of Y-direction movement. Estimated CPI resolution of Y-direction = 50 * RES_Y Note: the resolution of a step of RES_Y (i.e. 50) might slightly change across different types of surface, curvature of the surface and distances between chip and surface.							

Register Name	Delta_XH							
Bank	0			Address		0x11		
Access	Read-Only			Reset Value		NA		
Bit Field	7	6	5	4	3	2	1	0
	Delta_X[15:8]							
Description	Delta_XH is the high byte of a 2's complement value in 16-bit X-movement data. Delta_X[15:0] = {Delta_XH[7:0], Delta_XL[7:0]} Register Delta_XH is valid only if register Motion_Status (address 0x02) is read and MOTION bit (bit 7) is 1.							

Register Name	Delta_YH							
Bank	0			Address		0x12		
Access	Read-Only			Reset Value		NA		
Bit Field	7	6	5	4	3	2	1	0
	Delta_Y[15:8]							
Description	Delta_YH is the high byte of a 2's complement value in 16-bit Y-movement data. Delta_Y[15:0] = {Delta_YH[7:0], Delta_YL[7:0]} Register Delta_YH is valid only if register Motion_Status (address 0x02) is read and MOTION bit (bit 7) is 1.							

Register Name	Shutter							
Bank	0			Address		0x15		
Access	Read-Only			Reset Value		NA		
Bit Field	7	6	5	4	3	2	1	0
	Shutter[7:0]							
Description	Shutter register is an index of LASER shutter time. It is automatically adjusted by the chip's internal auto-exposure algorithm to keep the average pixel values within normal operating ranges. The higher the Shutter index is, the lower the surface reflectiveness is.							

Register Name	LD_SRC							
Bank	0			Address		0x51		
Access	R/W			Reset Value		0x0E		
Bit Field	7	6	5	4	3	2	1	0
	Reserved	Reserved	Reserved	LD_SRC[4:0]				
Description	To program the current source for LASER							

Field	Reset	Description
LD_SRC[4:0]	14	This register is to set the LASER drive current (in the DC current) in the LASER driver to adjust the light intensity to accommodate for different tracking surfaces. Note that the max. rating of operating LASER drive current is 8mA as shown in Table 3. Recommended Operating Conditions, the host controller **MUST** limit any value beyond LD_SRC[4:0] = 0x06 that may drive >8mA current in the software setting as the LASER output may degrade in long run or could be damaged in the worst scenario. The power-up value of LD_SRC is 14 and the recommended value is 6. I_{LD} = LD_SRC[4:0] x 1.2mA

Register Name	Frame_Avg							
Bank	0			Address		0x17		
Access	Read-Only			Reset Value		NA		
Bit Field	7	6	5	4	3	2	1	0
	FA[7:0]							
Description	Frame_Avg register represents the average brightness of all pixels within a frame (35x35 = 1225 pixels). The larger the value is, the brighter the image will be. The value of Frame_Avg ranges from 0 ~ 255.							

Register Name	LD_SRC							
Bank	0			Address		0x51		
Access	R/W			Reset Value		0x0E		
Bit Field	7	6	5	4	3	2	1	0
	Reserved	Reserved	Reserved	LD_SRC[4:0]				
Description	To program the current source for LASER							

Field	Reset	Description
LD_SRC[4:0]	14	This register is to set the LASER drive current (in the DC current) in the LASER driver to adjust the light intensity to accommodate for different tracking surfaces. Note that the max. rating of operating LASER drive current is 8mA as shown in Table 3. Recommended Operating Conditions, the host controller **MUST** limit any value beyond LD_SRC[4:0] = 0x06 that may drive >8mA current in the software setting as the LASER output may degrade in long run or could be damaged in the worst scenario. The power-up value of LD_SRC is 14 and the recommended value is 6. I_{LD} = LD_SRC[4:0] x 1.2mA

Register Name	IQH							
Bank	0			Address		0x75		
Access	Read-Only			Reset Value		NA		
Bit Field	7	6	5	4	3	2	1	0
	IQH[7:0]							
Description	IQH is the high byte of IQ (Image Quality). IQ (Image Quality) is a measure of the number of valid features visible by the chip in the current frame. The theoretical max/min IQ value is 65,535/0. Since small changes in the current frame can result in changes in IQ value, variations in IQ when looking at a surface are expected. The higher the IQ is, the easier for the chip to have a good tracking on the navigation surfaces.							

Register Name	IQL							
Bank	0			Address		0x76		
Access	Read-Only			Reset Value		NA		
Bit Field	7	6	5	4	3	2	1	0
	IQL[7:0]							
Description	IQL is the low byte of IQ (Image Quality).							

Document Revision History

Revision Number	Date	Description
0.1	08 Dec. 2017	New creation, preliminary version.
0.2	03 Apr. 2018	Modify typos and add the dimension of PCB layout guide.