Enterprise-Ready 2S Efficient Performance Intel Motherboard Specification

Intel® Xeon® processor E5-2600 product family

Revision 0.5

April 2012

Revision History

Date	Revision Number	Modifications
April 2012	0.5	First Draft

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1. Introduction

This Technical Product Specification (TPS) provides board-specific information detailing the features, functionality, and high-level architecture of the Enterprise-ready 2S Efficient Performance Intel® Motherboard based on the Intel® Xeon® processor E5-2600 product family and the Intel® C602 (-A) chipset.

The Intel® Xeon® processor E5-2600 product family and the Intel® C602 (-A) chipset provide a platform capable of supporting features and functions attractive to a number of market segments. The purpose of this document is to define a dual socket server board that is capable of deployment in scale out data centers as well as traditional data centers with 19” rack enclosures. Intel’s intent is to provide a platform that enables server vendors to leverage a single design across multiple market segments via multiple board SKUs.

2. Product Overview

Table 1 shows the requirements that a design must meet in order to be considered a compliant Intel® dual socket server board.

Table 1. Intel® Server Board Feature Set

Feature	Description
Processor Support	▪ Two LGA2011 (Socket R) processor sockets ▪ Support for one or two Intel® Xeon® processors E5-2600 product family ▪ Support for the full range of processors offered, although a board may be optimized for a particular processor TDP level (i.e. VR phases removed to optimize for lower power processors)
Memory	▪ 8 – 24 DIMM slots ▪ Unbuffered DDR3 (UDIMM), registered DDR3 (RDIMM), Load Reduced DDR3 (LRDIMM) ▪ Memory DDR3 data transfer rates of 800, 1066, 1333 MT/s, and 1600 MT/s ▪ DDR3 standard I/O voltage of 1.5V and DDR3 Low Voltage of 1.35V
Chipset	Intel® C602 (-A) chipset with support for optional Storage Option Select keys
External I/O connections	▪ May support DB-15 Video connector ▪ Shall support at least two RJ-45 Network Interface Connectors supporting 10/100/1000Mb ▪ Shall support at least two USB 2.0 connectors
I/O Module Options	The following I/O module options may be supported. Installed I/O modules shall be supported in addition to standard on-board features and any add-in expansion cards. ▪ Quad port 1 GbE module ▪ Dual port 10GBase-T Ethernet module ▪ Dual SFP+ port 10GbE module ▪ Single Port FDR speed InfiniBand module with QSFP connector
System Fans	▪ Managed system fan headers
PCIe* Adapter Card Support	▪ Two half-length x8 PCIe* adapter cards for 1U chassis ▪ Three x8 PCIe* Adapter cards for 2u chassis with at least one full length
Video	▪ May contain a 2D Video Controller ▪ 16 MB DDR3 Memory
Storage	▪ Two single port AHCI SATA connectors capable of supporting up to 6 Gb/sec ▪ Two SCU 4-port mini-SAS connectors capable of supporting up to 3 Gb/sec SATA/SAS ▪ RAID 0/1/10/5
Security	▪ May Intel® Trusted Platform Module (TPM)
Server Management	▪ Integrated Baseboard Management Controller, IPMI 2.0 compliant ▪ Support for DCMI 1.5

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2.1 Server Board Dimensional Mechanical Drawing

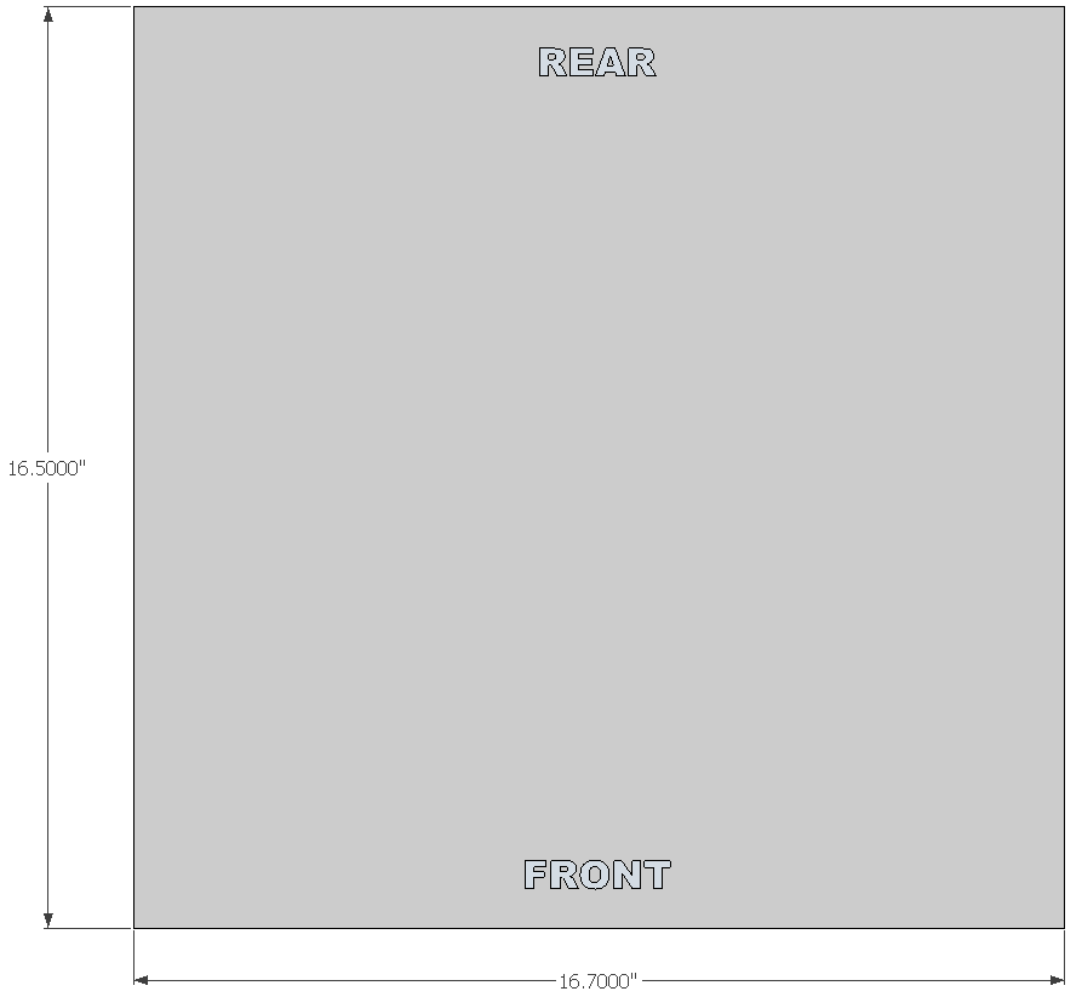


Figure 1. Motherboard maximum dimensions

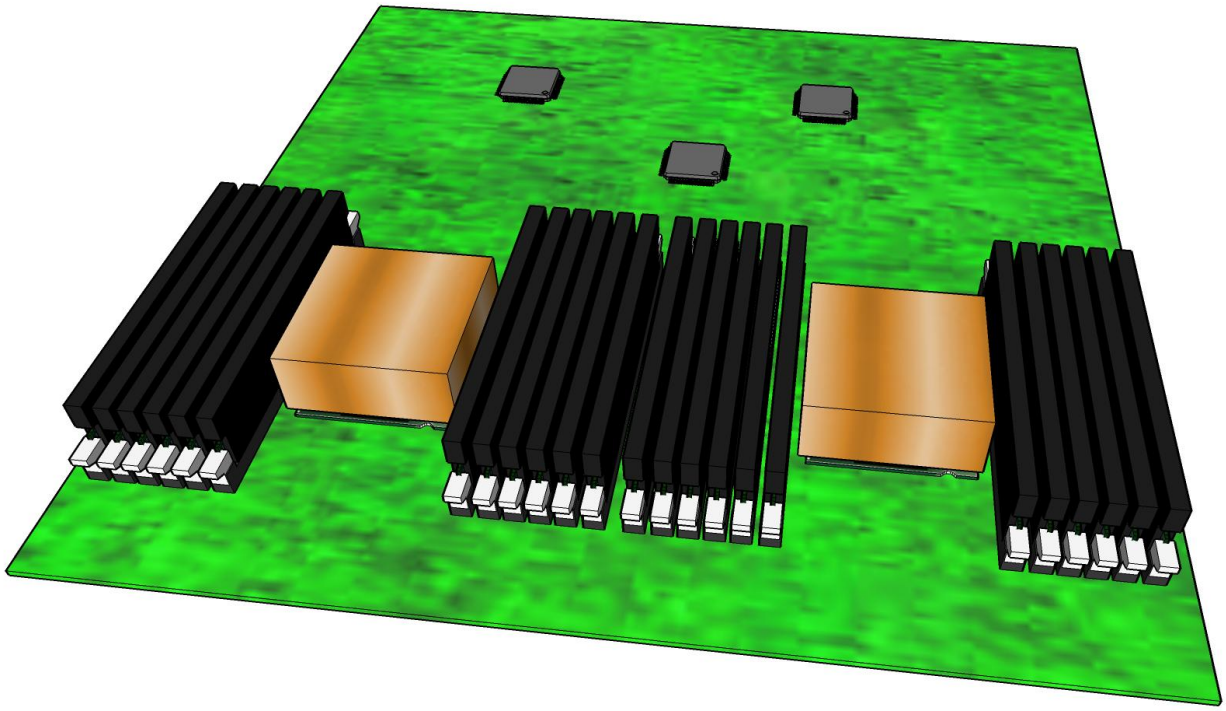


Figure 2. 24 DIMM Motherboard Concept

3. Product Architecture Overview

The following diagram provides an overview of the server board architecture, showing the features and interconnects of each of the major sub-system components of the Intel® Xeon® processor E5-2600 product family and the Intel® C602 (-A) chipset.

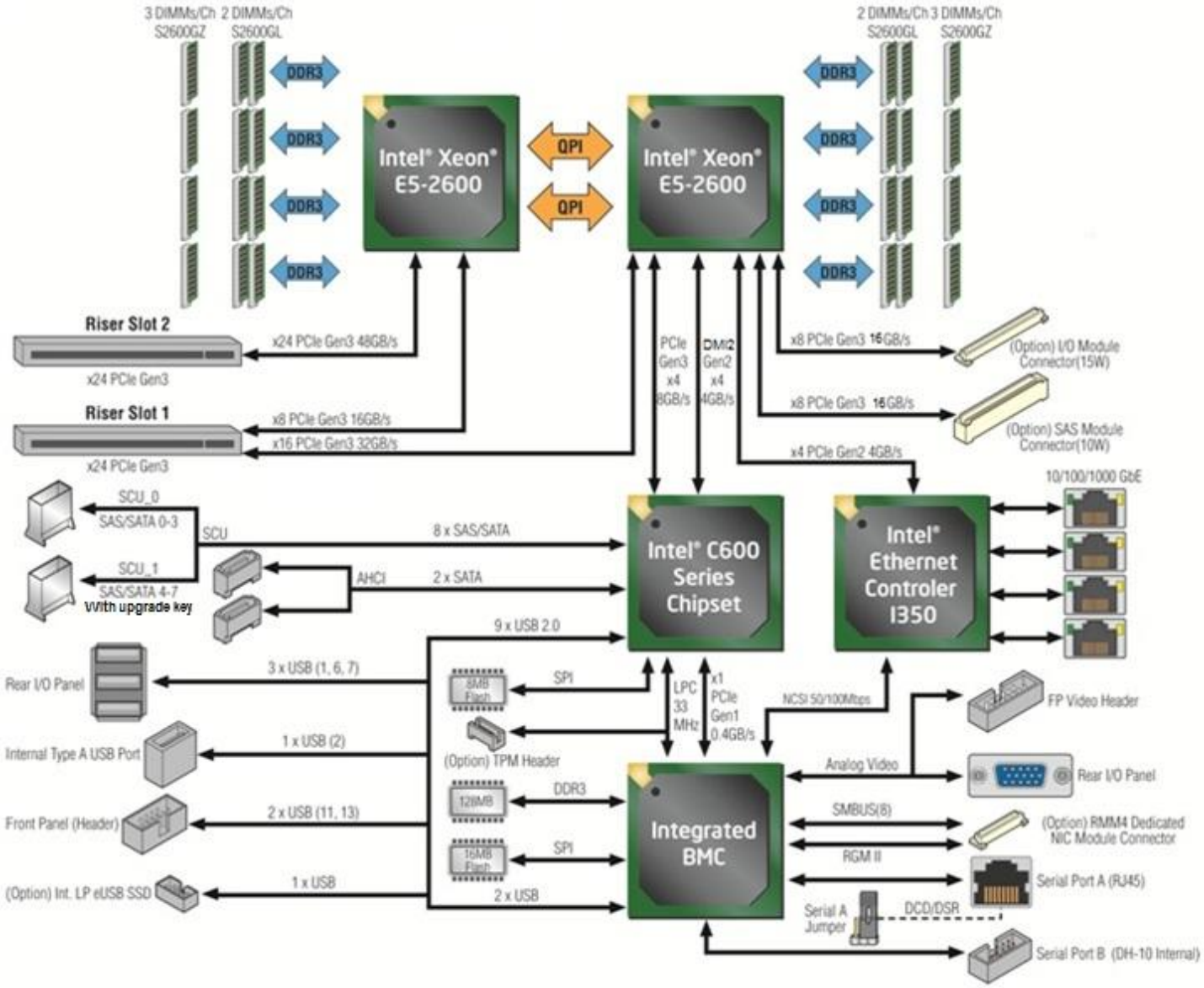


Figure 3. Intel® Xeon® processor E5-2600 product family Functional Block Diagram

3.1 Processor Support

The server board shall support two Socket-R (LGA2011) processor sockets and the full range of the Intel® Xeon® processor E5-2600 product family.

Note: Previous generation Intel® Xeon® processors are not supported on the Intel server boards described in this document.

Visit the Intel web site for a complete list of supported processors.

3.2 Supported Memory

Table 2. UDIMM Support Guidelines

Ranks Per DIMM & Data Width	Memory Capacity Per DIMM[1]			Speed (MT/s) and Voltage Validated by Slot per Channel (SPC) and DIMM Per Channel (DPC)							
				2 Slots per Channel Intel® Server Board S2600GL				3 Slots per Channel Intel® Sever Board S2600GZ			
				1DPC		2DPC		1DPC		2DPC	
				1.35V	1.5V	1.35V	1.5V	1.35V	1.5V	1.35V	1.5
SRx8 ECC	1GB	2GB	4GB	1066, 1333	1066, 1333	1066	1066, 1333	1066	1066, 1333	1066	1066, 1333
DRx8 ECC	2GB	4GB	8GB	1066, 1333	1066, 1333	1066	1066, 1333	1066	1066, 1333	1066	1066, 1333

Table 3. RDIMM Support Guidelines

Ranks Per DIMM & Data Width	Memory Capacity Per DIMM[1]			Speed (MT/s) and Voltage Validated by Slot per Channel (SPC) and DIMM Per Channel (DPC)									
				2 Slots per Channel Intel® Server Board S2600GL				3 Slots per Channel Intel® Sever Board S2600GZ					
				1DPC		2DPC		1DPC		2DPC		3DPC	
				1.35V	1.5V	1.35V	1.5V	1.35V	1.5V	1.35V	1.5V	1.35V	1.5
SRx8	1GB	2GB	4GB	1066 1333	1066 1333 1600	1066, 1333	1066 1333 1600	1066, 1333	1066 1333 1600	1066, 1333	1066 1333 1600	n/a	800, 1066
DRx8	2GB	4GB	8GB	1066 1333	1066 1333 1600	1066 1333	1066 1333 1600	1066, 1333	1066 1333 1600	1066, 1333	1066 1333 1600	n/a	800, 1066
SRx4	2GB	4GB	8GB	1066 1333	1066 1333 1600	1066 1333	1066 1333 1600	1066, 1333	1066 1333 1600	1066, 1333	1066 1333 1600	n/a	800, 1066
DRx4	4GB	8GB	16GB	1066 1333	1066 1333 1600	1066 1333	1066 1333 1600	1066, 1333	1066 1333 1600	1066, 1333	1066 1333 1600	n/a	800, 1066
QRx4	8GB	16GB	32GB	800	1066	800	800	800	1066	800	800	n/a	n/a
QRx8	4GB	8GB	16GB	800	1066	800	800	800	1066	800	800	n/a	n/a

Table 4. LRDIMM Support Guidelines

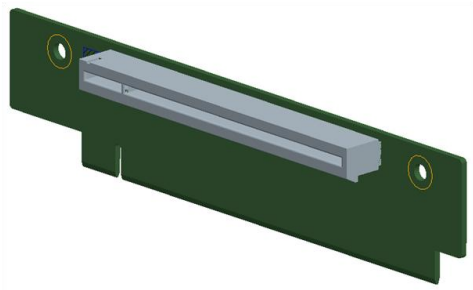
Ranks Per DIMM & Data Width[1]	Memory Capacity Per DIMM[2]		Speed (MT/s) and Voltage Validated by Slot per Channel (SPC) and DIMM Per Channel (DPC)[3,4,5]					
			2 Slots per Channel Intel® Sever Board S2600GL		3 Slots per Channel Intel® Sever Board S2600GZ			
			1DPC and 2DPC		1DPC and 2DPC		3DPC	
			1.35V	1.5V	1.35V	1.5V	1.35V	1.5V
QRx4 (DDP)[6]	16GB	32GB	1066	1066, 1333	1066	1066, 1333	1066	1066
QRx8 (P)[6]	8GB	16GB	1066	1066, 1333	1066	1066	1066	1066

3.3 Riser Card Support

The server board shall provide two riser cards, and the riser card slots can be configured to meet a range of usage models. Exact PCIe* lane assignments to the slots is determined by the board vendor.

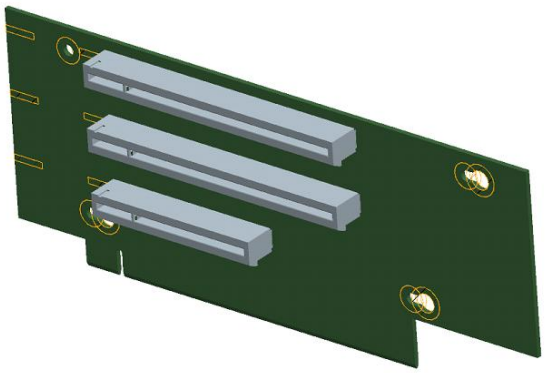
The following section shows examples of 1U and 2U riser cards:

- 1U – One add-in card slot – PCIe* x16, x16 mechanical



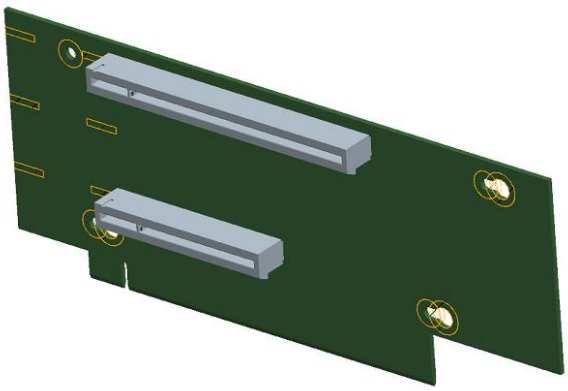
- 2U – Three add-in card slots –

Slot #	Description
Slot-1 (Top)	PCIe* x8, x16 mechanical
Slot-2 (Middle)	PCIe* x8, x16 mechanical
Slot-3 (Bottom)	PCIe* x8, x8 mechanical



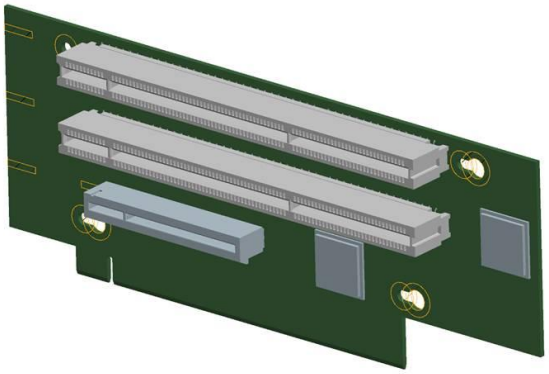
- 2U – Two add-in card slots –

Slot #	Description
Slot-1 (Top)	PCIe* x16, x16 mechanical
Slot-2 (Bottom)	PCIe* x8, x8 mechanical



- 2U – Three add-in card slots –

Slot #	Description
Slot-1 (Top)	PCIx 133MHz
Slot-2 (Middle)	PCIx 133 MHz
Slot-3 (Bottom)	PCIe* x8, x8 mechanical



3.4 Network Interface

Each Ethernet port shall drive two LEDs located on each network interface connector. The LED at the right of the connector is the link/activity LED and indicates network connection when on, and transmit/receive activity when blinking. The LED at the left of the connector indicates link speed as defined in the following table.

Table 5. External RJ45 NIC Port LED Definition

LED	Color	LED State	NIC State
Left	Green	Off	LAN link not established
		On	LAN link is established
		Blinking	LAN activity is occurring
Right		Off	10 Mb/sec data rate
	Green	On	100 Mb/sec data rate
	Yellow	On	1000 Mb /sec data rate

3.5 I/O Module Support

To broaden the standard on-board feature set, the server board may provide support for additional I/O Module options. The I/O module shall attach to a vendor defined connector supporting x8 PCIe* Gen3 signals from the CPU 1 processor.

4. Technology Support

4.1 Intel® Trusted Execution Technology

The Intel® Xeon® Processor E5 2600 Product Family supports Intel® Trusted Execution Technology (Intel® TXT), which is a robust security environment designed to help protect against software-based attacks. Intel® Trusted Execution Technology integrates new security features and capabilities into the processor, chipset and other platform components. When used in conjunction with Intel® Virtualization Technology and Intel® VT for Directed IO, with an active TPM, Intel® Trusted Execution Technology provides hardware-rooted trust for your virtual applications.

4.2 Intel® Virtualization Technology – Intel® VT-x/VT-d/VT-c

Intel® Virtualization Technology consists of three components which are integrated and interrelated, but which address different areas of Virtualization.

- Intel® Virtualization Technology ***(VT-x)*** is processor-related and provides capabilities needed to provide a hardware assist to a Virtual Machine Monitor (VMM).
- Intel® Virtualization Technology for Directed I/O (***VT-d)*** is primarily concerned with virtualizing I/O efficiently in a VMM environment. This would generally be a chipset I/O feature, but in the Second Generation Intel® Core™ Processor Family there is an Integrated I/O unit embedded in the processor, and the IIO is also enabled for VT-d.
- Intel® Virtualization Technology for Connectivity (***VT-c)*** is primarily concerned I/O hardware assist features, complementary to but independent of VT-d.

4.3 Trusted Platform Module (TPM) Support

The server board shall support TPM 1.2.

5. Platform Management Functional Overview

This section describes the management features supported by the server board.

5.1 Management Controller Firmware Feature Support

The following sections outline features that the integrated management controller firmware can support. Support and utilization for some features is dependent on the server platform in which the server board is integrated and any additional system level components and options that may be installed.

5.1.1 IPMI Features

- IPMI 2.0 Features Shall support OCP remote management
- May support Baseboard management controller (BMC)
- Shall support IPMI Watchdog timer
- Shall support Chassis device functionality, including power/reset control and BIOS boot flags support
- Shall support Field Replaceable Unit (FRU) inventory device functionality
- Shall support System Event Log (SEL) device functionality Shall support Sensor Data Record (SDR) repository device functionality
- Shall support Sensor device and sensor scanning/monitoring Shall support Serial-over-LAN (SOL)

5.1.2 Non IPMI Features

The management controller supports the following non-IPMI features.

- Shall support In-circuit management firmware update
- Shall support Chassis intrusion detection
- Shall support Fan speed control
- Shall support Fan redundancy monitoring and support
- Shall support Hot-swap fans
- Shall support Power Supply Fan Sensors
- May support System Airflow Monitoring
- Shall support Exit Air Temperature Monitoring
- May support Ethernet Controller Thermal Monitoring
- Shall support Platform environment control interface (PECI) thermal management support
- Shall support DIMM temperature monitoring
- Shall support Power supply redundancy monitoring and support
- May support power management (e.g. power capping at node level)
- May support diagnostic beep codes for fault conditions.
- Shall support System status LED and chassis ID LED.
- May support secure lockout of certain front panel functionality
- Shall support Power state retention
- May support Integrated KVM
- Shall support DCMI 1.1 compliance (product-specific).
- May support management of PMBus rev1.2 compliant power supplies
- May support Smart Ride Through (SmaRT) / Closed Loop System Throttling (CLST)
- Shall support Power Supply FW Update
- May support Power Supply Compatibility Check

5.2 Remote BIOS Update

The BIOS can be updated remotely under these scenarios:

- Scenario 1: Sample/Audit BIOS settings
  - Return current BIOS settings, or
  - Save/export BIOS settings in a human-readable form that can be restored/imported (as in scenario 2)
- Scenario 2: Update BIOS with pre-configured set of BIOS settings
  - Update/change multiple BIOS settings
  - Reboot
- Scenario 3: BIOS/firmware update with a new revision
  - Load new BIOS/firmware on machine and update, retaining current BIOS settings
  - Reboot

Additionally, the update tools have the following capabilities:

- Update from the operating system over the LAN – the OS standard is CentOS v5.2
- Can complete BIOS update or setup change with a single reboot (no PXE boot, no multiple reboots)
- No user interaction (like prompts)
- BIOS updates and option changes do not take longer than five minutes to complete

- Can be scripted and propagated to multiple machines

5.3 Firmware Update

The board vendor must provide tool(s) to update the management engine firmware remotely, which does not require any physical input at the system. Remote update means either through out-of-band by the management controller (or PCH ME) or through logging into the local OS (CentOS 5.2) over the network. A remote firmware update may take a maximum of 5 minutes to complete and requires no more than one reset cycle to the system. The tool must support CentOS 5.2, should support updating the FW and BIOS together or separately, and must also provide an option to update only the operational FW region or the entire FW region.

5.4 Advanced Configuration and Power Interface (ACPI)

The server board has support for the following ACPI states:

Table 6. ACPI Power States

State	Supported	Description
S1	Yes	Sleeping: Context is maintained; equate to processor and chipset clocks being stopped. • The front panel power LED blinks at a rate of 1Hz with a 50% duty cycle • The watchdog timer is stopped • The front panel buttons are unprotected • Fan speed control is determined by available SDRs. Fans may be set to a fixed state, or basic fan management may be applied
S2	No	Not Supported
S3	No	Normally supported only on workstation platforms
S4	No	Not Supported
S5	Yes	Soft Off • The front panel buttons are not locked • The fans are stopped • The power-up process goes through the normal boot process

5.5 Power Control Sources

The server board supports several power control sources which can initiate a power-up or power-down activity.

Table 7. Power Control Initiators

Source	External Signal Name or Internal Subsystem	Capabilities
Power button	Front panel power button	Turns power on or off
management controller watchdog timer	Internal management controller timer	Turns power off, or power cycle
Command	Routed through command processor	Turns power on or off, or power cycle
Power state retention	Implemented by means of management controller internal logic	Turns power on when AC power returns
Chipset	Sleep S4/S5 signal (same as POWER_ON)	Turns power on or off
CPU Thermal	CPU Thermtrip	Turns power off
WOL(Wake On LAN)	LAN	Turns power on

5.6 Fan Speed Control

Shall support intelligent fan speed control based on thermal sensors. Placement of thermal sensors to be determined by board vendor.

5.7 Power and Thermal Monitoring

The server board shall support platform power monitoring. The board shall support thermal monitoring, including processor, memory, chipset, and inlet and outlet temperatures.

5.8 Serial-Over-LAN (SOL)

The server board shall support serial-over-LAN through a single shared network interface available on the motherboard. The shared network interface can be integrated on the motherboard or provided through a come from LOM (82574 or I350) and NIC on the mezzanine card or the PCIe* card.

5.9 Remote Power Control

The server board shall support remote system power on/off and reboot over LAN.

5.10 Error Threshold Settings

An error threshold setting must be enabled for both correctable and uncorrectable errors. Once the programmed threshold is reached, an event should be triggered and logged.

- **Memory Correctable ECC:** The threshold value is 1000. When the threshold is reached, the BIOS should log the event including DIMM location information and output DIMM location code through the debug card.
- **QPI errors:** Follow the Intel® C602 (-A) chipset product specification.
- **PCIe* errors:** Follow the Intel® C602 (-A) chipset product specification.

5.11 System Event Log (SEL)

The server board shall support the DCMI 1.5 SEL information.

5.12 Dedicated Management Channel

Shall support two management NICs

5.13 Data Center Management Interface (DCMI) 1.5

DCMI is an IPMI-based standard that builds upon a set of required IPMI standard commands by adding a set of DCMI-specific IPMI OEM commands. The motherboard shall support DCMI 1.5.

6. On-board Connector/Header Overview

This section identifies the location and pin-out for on-board connectors and headers of the server board that provide an interface to system options/features, on-board platform management, or other user accessible options/features.

6.1 Power Connectors

The server board includes several power connectors that are used to provide DC power to various devices.

6.1.1 Main Power

TBD: This main power connector may need to be consistent between the various board vendors in order to insure interoperability between power distribution boards (i.e. one power cable harness, if a PDB and cable harness is included in the design, can be leveraged between all designs)

7. Power / Sleep Button and LED Support

Pressing the Power button will toggle the system power on and off. This button also functions as a sleep button if enabled by an ACPI compliant operating system. Pressing this button will send a signal to the integrated management controller, which will power on or power off the system. The power LED is a single color and is capable of supporting different indicator states as defined in the following table.

Table 8. Power/Sleep LED Functional States

State	Power Mode	LED	Description
Power-off	Non-ACPI	Off	System power is off, and the BIOS has not initialized the chipset.
Power-on	Non-ACPI	On	System power is on
S5	ACPI	Off	Mechanical is off, and the operating system has not saved any context to the hard disk.
S4	ACPI	Off	Mechanical is off. The operating system has saved context to the hard disk.
S3-S1	ACPI	Slow blink1	DC power is still on. The operating system has saved context and gone into a level of low-power state.
S0	ACPI	Steady on	System and the operating system are up and running.

7.1.1 System ID Button and LED Support

Pressing the System ID Button will toggle both the ID LED on the front panel and the Blue ID LED on the server board on and off. The System ID LED is used to identify the system for maintenance when installed in a rack of similar server systems. The System ID LED can also be toggled on and off remotely using the IPMI "Chassis Identify" command which will cause the LED to blink for 15 seconds.

7.1.2 System Reset Button Support

When pressed, this button will reboot and re-initialize the system

7.1.3 NMI Button Support

When the NMI button is pressed, it puts the server in a halt state and causes the management controller to issue a non-maskable interrupt (NMI). This can be useful when performing diagnostics for a given issue where a memory download is necessary to help determine the cause of the problem. Once an NMI has been generated by the management controller, the management controller does not generate another NMI until the system has been reset or powered down.

The following actions cause the management controller to generate an NMI pulse:

- Receiving a *Chassis Control* command to pulse the diagnostic interrupt. This command does not cause an event to be logged in the SEL.
- Watchdog timer pre-timeout expiration with NMI/diagnostic interrupt pre-timeout action enabled.

The following table describes behavior regarding NMI signal generation and event logging by the management controller.

Table 9. NMI Signal Generation and Event Logging

Causal Event	NMI	
	Signal Generation	Front Panel Diag Interrupt Sensor Event Logging Support
Chassis Control command (pulse diagnostic interrupt)	X	–
Front panel diagnostic interrupt button pressed	X	X
Watchdog Timer pre-timeout expiration with NMI/diagnostic interrupt action	X	X

7.1.4 NIC Activity LED Support

The Front Control Panel includes an activity LED indicator for each on-board Network Interface Controller (NIC). When a network link is detected, the LED will turn on solid. The LED will blink once network activity occurs at a rate that is consistent with the amount of network activity that is occurring.

7.1.5 Hard Drive Activity LED Support

The drive activity LED on the front panel indicates drive activity from the on-board hard disk controllers. The server board also provides a header giving access to this LED for add-in controllers.

7.1.6 System Status LED Support

The System Status LED is a bi-color (Green/Amber) indicator that shows the current health of the server system. The system provides two locations for this feature; one is located on the Front Control Panel, the other is located on the back edge of the server board, viewable from the back of the system. Both LEDs are tied together and will show the same state. The System Status LED states are driven by the on-board platform management sub-system. The following table provides a description of each supported LED state.

Table 10. System Status LED State Definitions

Color	State	Criticality	Description
Off	System is not operating	Not ready	1. System is powered off (AC and/or DC). 2. System is in EuP Lot6 Off Mode. 3. System is in S5 Soft-Off State. 4. System is in S4 Hibernate Sleep State.
Green	Solid on	Ok	Indicates that the System is running (in S0 State) and its status is 'Healthy'. The system is not exhibiting any errors. AC power is present and management controller has booted and manageability functionality is up and running.
Green	~1 Hz blink	Degraded - system is operating in a degraded state although still functional, or system is operating in a redundant state but with an impending failure warning	System degraded: Redundancy loss, such as power-supply or fan. Applies only if the associated platform sub-system has redundancy capabilities. Fan warning or failure when the number of fully operational fans is more than minimum number needed to cool the system. Non-critical threshold crossed – Temperature (including HSBP temp), voltage, input power to power supply, output current for main power rail from power supply and Processor Thermal Control (Therm Ctrl) sensors. Power supply predictive failure occurred while redundant power supply configuration was present. Unable to use all of the installed memory (one or more DIMMs failed/disabled but functional memory remains available) Correctable Errors over a threshold and migrating to a spare DIMM (memory sparing). This indicates that the user no longer has spared DIMMs indicating a redundancy lost condition. Corresponding DIMM LED lit. Uncorrectable memory error has occurred in memory Mirroring Mode, causing Loss of Redundancy. Correctable memory error threshold has been reached for a failing DDR3 DIMM when the system is operating in fully redundant RAS Mirroring Mode. Battery failure. Management controller executing in uBoot. (Indicated by Chassis ID blinking at Blinking at 3Hz). System in degraded state (no manageability). Management controller uBoot is running but has not transferred control to management controller Linux. Server will be in this state 6-8 seconds after management controller reset while it pulls the Linux image into flash Management controller booting Linux. (Indicated by Chassis ID solid ON). System in degraded state (no manageability). Control has been passed from management controller uBoot to management controller Linux itself. It will be in this state for ~10-~20 seconds. Management controller Watchdog has reset the management controller. Power Unit sensor offset for configuration error is asserted. HDD HSC is off-line or degraded.

Amber	~1 Hz blink	Non-critical - System is operating in a degraded state with an impending failure warning, although still functioning	Non-fatal alarm – system is likely to fail: Critical threshold crossed – Voltage, temperature (including HSBP temp), input power to power supply, output current for main power rail from power supply and PROCHOT (Therm Ctrl) sensors. VRD Hot asserted. Minimum number of fans to cool the system not present or failed Hard drive fault Power Unit Redundancy sensor – Insufficient resources offset (indicates not enough power supplies present) In non-sparing and non-mirroring mode if the threshold of correctable errors is crossed within the window Correctable memory error threshold has been reached for a failing DDR3 DIMM when the system is operating in a non-redundant mode
Amber	Solid on	Critical, non-recoverable – System is halted	Fatal alarm – system has failed or shutdown: CPU CATERR signal asserted MSID mismatch detected (CATERR also asserts for this case). CPU 1 is missing CPU Thermal Trip No power good – power fault DIMM failure when there is only 1 DIMM present and hence no good memory present1. Runtime memory uncorrectable error in non-redundant mode. DIMM Thermal Trip or equivalent SSB Thermal Trip or equivalent CPU ERR2 signal asserted Management controller\Video memory test failed. (Chassis ID shows blue/solid-on for this condition) Both uBoot management controller FW images are bad. (Chassis ID shows blue/solid-on for this condition) 240VA fault Fatal Error in processor initialization: Processor family not identical Processor model not identical Processor core/thread counts not identical Processor cache size not identical Unable to synchronize processor frequency Unable to synchronize QPI link frequency

8. Power System

Power must be distributed from the rack power bus bars to the server board. The server enclosure may contain a power distribution board (PDB) that connects directly to the power bus bars and connects to the server board via a cable harness. The PDB, or motherboard if the motherboard connects directly to the power bus bar, shall contain logic to enable reporting of system input power to the server board. The ADI ADM1276 hot swap controller component may be used to provide this functionality.

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8.1 CPU VRM Optimizations

The CPU VRM shall be optimized to reduce cost and increase the efficiency of the power conversion system. The board vendor should use only the minimum number of required phases to support the maximum CPU power. A PSI (power state indicator) allows the shedding of unused phases, letting the VRM operate at its peak efficiency.

8.2 CPU VRM Efficiency

The minimum efficiency for the CPU VRM shall be 90%.

9. Environmental Requirements

The motherboard meets the following environmental requirements:

- Gaseous Contamination: Severity Level G1 per ANSI/ISA 71.04-1985
- Ambient operating temperature range: -5°C to +45°C
- Operating and storage relative humidity: 10% to 90% (non-condensing)
- Storage temperature range: -40°C to +70°C
- Transportation temperature range: -55°C to +85°C (short-term storage)

9.1 Vibration and Shock

The motherboard meets shock and vibration requirements according to the following IEC specifications: IEC78-2-(*) and IEC721-3-(*) Standard & Levels.

Table 11. Vibration and Shock Requirements

	Operating	Non-Operating
Vibration	0.5g acceleration, 1.5mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave / minute for each of the three axes (one sweep is 5 to 500 to 5 Hz)	1g acceleration, 3mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave / minute for each of the three axes (one sweep is 5 to 500 to 5 Hz)
Shock	6g, half-sine 11mS, 5 shocks for each of the three axes	12g, half-sine 11mS, 10 shocks for each of the three axes

10. Prescribed Materials

10.1 Disallowed Components

The following components are not used in the design of the motherboard:
Components disallowed by the European Union's Restriction of Hazardous Substances Directive (RoHS 6)

- Trimmers and/or potentiometers
- Dip switches

10.2 Capacitors and Inductors

The following limitations apply to the use of capacitors:

- Only aluminum organic polymer capacitors made by high quality manufacturers are used; they must be rated 105°C
- All capacitors have a predicted life of at least 50,000 hours at 45°C inlet air temperature, under worst conditions
- Tantalum capacitors using manganese dioxide cathodes are forbidden
- SMT ceramic capacitors with case size > 1206 are forbidden (size 1206 are still allowed when installed far from the PCB edge and with a correct orientation that minimizes risks of cracks)
- Ceramic material for SMT capacitors must be X7R or better material (COG or NP0 type should be used in critical portions of the design)

Only SMT inductors may be used. The use of through hole inductors is disallowed.

10.3 Component De-rating

For inductors, capacitors, and FETs, de-rating analysis should be based on at least 20% de-rating.

11. Reference Documents

- *Advanced Configuration and Power Interface Specification*, Revision 3.0, http://www.acpi.info/.
- *Intelligent Platform Management Bus Communications Protocol Specification*, Version 1.0. 1998. Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation.
- *Intelligent Platform Management Interface Specification*, Version 2.0. 2004. Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation.
- *Platform Support for Serial-over-LAN (SOL), TMode, and Terminal Mode External Architecture Specification*, Version 1.1, 02/01/02, Intel Corporation.