

CPU Model with Dual Issue Instruction Pipeline

Design and Evaluation

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1. Introduction

This report presents the design, instruction set, and test results for the SPU-lite pipeline model. Additionally all SystemC source code and supporting MATLAB code are included in the appendices.

2. Design

The design procedure for the SPU-Lite model was to incrementally construct/add each block after verifying the previous design was operating correctly. This began with constructing the even/odd pipes as described in the project milestone report. Subsequently the Register-File, Write-Back, Issue, Instruction-Decode, Instruction-Fetch, and Instruction-Cache were added incrementally. The SPU-Lite model was written in SystemC and is run externally using text based test programs in conjunction with special compiler written in MATLAB. A high level overview of the model execution process is shown below in Figure 1. A high level block diagram of the SPU-Lite SystemC model is shown in Figure 2. The remainder of this section describes the modules within SPU-Lite program in more detail. This mainly includes their I/O as well as any pertinent design decisions made along the way.

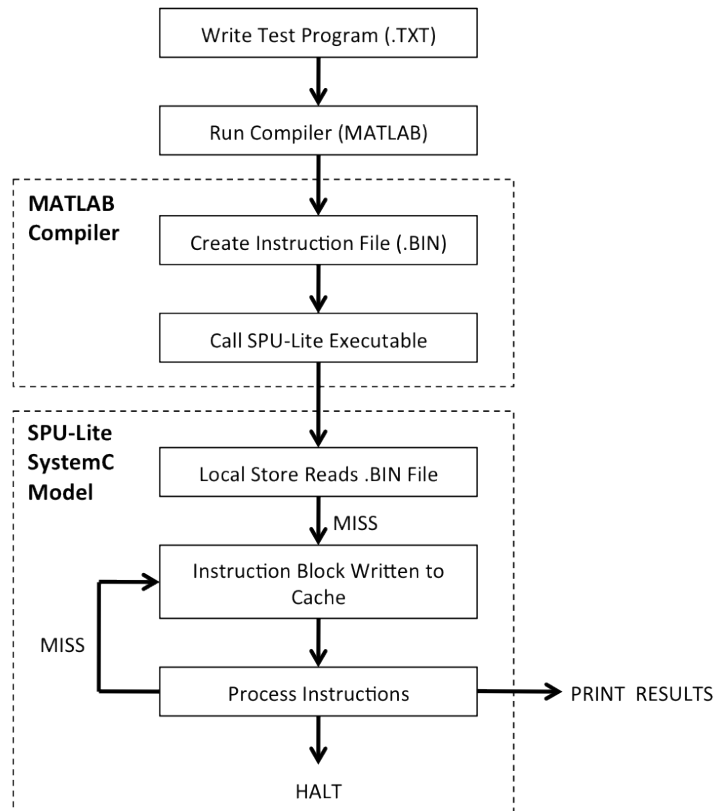


Figure 1: Model Execution Diagram

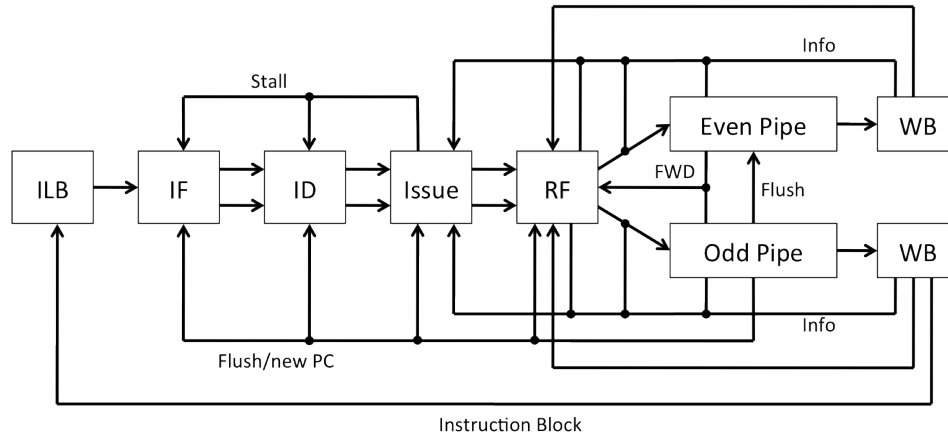


Figure 2: SPU-Lite SystemC Model High Level Block Diagram

2.1 Instruction Cache

The instruction cache is a 256B direct mapped cache with 128B blocks (i.e. 32 instructions each). The hit time is 1 clock, the miss penalty is 13 clocks, and the misses per instruction is approximately 0.03125 making the average instruction access time roughly 1.4 clocks. The cache is indexed by partitioning the program counter as follows:

Tag <7>	Index <1>	Offset <5>	Bit Mask <2> = 00
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The behavioral SystemC module has the following basic structure structure:

```
SC_MODULE(ILB) {
    //Inputs
    sc_in<bool> clock;
    sc_in<sc_uint<32> > Miss_Instrutions[1][33]; //Extra entry for cache indexing information

    //Outputs
    sc_out <bool> cache_valid[2];
    sc_out <sc_uint<32> > cache_tags[2];
    sc_out <sc_uint<32> > cache_inst[2][32];

    //Methods
    void update();

    //Constructor
    SC_CTOR(ILB){
        SC_METHOD(update);
        sensitive << clock.pos();
    }
};
```

2.2 Instruction Fetch

Instructions are fetched two at a time from the instruction cache. The behavioral SystemC module has the following basic structure:

```
SC_MODULE(IF) {
```

```

//Inputs
sc_in<bool> clock, stall;
sc_in<sc_int<32>> > new_pc;      //New PC used for branches/flush
sc_in <bool> cache_valid[2];
sc_in <sc_uint<32>> > cache_tags[2];
sc_in <sc_uint<32>> > cache_inst[2][32];

//Outputs
sc_out<sc_uint<32>> > I1, I2, PC1, PC2;

//Methods
void fetch();

//Constructor
SC_CTOR(IF){
    SC_METHOD(fetch);
    sensitive << clock.pos();
}
};

```

2.3 Instruction Decode

The behavioral SystemC module for the instruction decoder has the following basic structure:

```

SC_MODULE(ID) {
    //Inputs
    sc_in<bool> clock, stall;
    sc_in<sc_uint<32>> > PCin, I;
    sc_in<sc_int<32>> > new_pc;      //new_pc used for flush signal

    //Outputs
    sc_out<sc_uint<32>> > info[4]; //info = [PC,opcode,rt,value];
    sc_out<int> rabc[3];          //rabc = [ra,rb,rc]; register indices

    //Methods
    void decode();

    //Constructor
    SC_CTOR(ID){
        SC_METHOD(decode);
        sensitive << clock.pos();
    }
};

```

The SPU-Lite model uses 2 instantiations of the above decode module to accommodate each pipeline channel.

2.4 Issue

The “Issue” stage monitors all potential hazards and controls the flow of instructions to the pipeline. Branches are assumed not taken and all instructions are issued for in order. The behavioral SystemC module has the following basic structure:

```

SC_MODULE(Issue) {
    //Inputs
    sc_in<bool> clock;
    sc_in<sc_uint<32>> > info1_in[4],info2_in[4];    //info = [PC,opcode,rt,value];
    sc_in<int> rabc1_in[3], rabc2_in[3];            //rabc = [ra,rb,rc]; register indices
    sc_in<sc_int<32>> > new_pc;
    sc_in<sc_biguint<128>> > Result1[8], Result2[8];
}

```

```

sc_in<sc_uint<8> > Result_Destination1[8], Result_Destination2[8]; //Even=1, Odd=2
sc_in<bool> Reg_Write1[8], Reg_Write2[8];
sc_in<sc_uint<32> > info1_RF[4], info2_RF[4]; //Pre RF Info
sc_in<sc_uint<32> > info1_RFa[4], info2_RFa[4]; //Post RF Info
sc_in<sc_uint<8> > Stage_When_Ready1[8], Stage_When_Ready2[8];

//Output
sc_out<bool> stall;
sc_out<sc_uint<32> > info1_out[4], info2_out[4]; //info = [PC,opcode,rt,value];
sc_out<int> rabc1_out[3], rabc2_out[3]; //rabc = [ra,rb,rc]; register indices

//Methods
void route(){

//Constructor
SC_CTOR(Issue){
    SC_METHOD(route);
    sensitive << clock.pos();
}
};

```

2.5 Register File

The behavioral SystemC module has the following basic structure:

```

SC_MODULE(RF) {

    //Inputs
    sc_in<bool> clock;
    sc_in<sc_uint<32> > info1_in[4], info2_in[4]; //info = [PC,opcode,rt,value];
    sc_in<int> rabc1[3], rabc2[3]; //rabc = [ra,rb,rc];
    sc_in<sc_int<32> > new_pc;
    sc_in<sc_biguint<128> > Result1[8], Result2[8];
    sc_in<sc_uint<8> > Result_Destination1[8], Result_Destination2[8];
    sc_in<bool> Reg_Write1[8], Reg_Write2[8];

    //Outputs
    sc_out<sc_biguint<128> > A1, B1, C1, T1;
    sc_out<sc_biguint<128> > A2, B2, C2, T2;
    sc_out<sc_uint<32> > info1_out[4], info2_out[4];

    //Methods
    void read();
    void write();

    //Constructor
    SC_CTOR(RF){
        SC_METHOD(read);
        sensitive << clock.pos();
        SC_METHOD(write);
        sensitive << clock.pos();
    }
};

```

2.6 Even Pipe

The behavioral SystemC module has the following basic structure:

```

SC_MODULE(EvenPipe) {

    //Inputs
    sc_in<bool> clock;
    sc_in<sc_uint<32> > info[4]; //info = [PC,opcode,rt,value];
    sc_in<sc_biguint<128> > A, B, C, T;
    sc_in<sc_uint<3> > flush;

```

```

//Outputs
sc_out<sc_biguint<128>> > Result[8];
sc_out<sc_uint<8>> > Result_Destination[8];
sc_out<sc_uint<8>> > Stage_When_Ready[8];
sc_out<bool> Reg_Write[8];
sc_out<sc_uint<8>> > Unit_Id[8];

//Methods
void update();

//Constructor
SC_CTOR(EvenPipe){
    SC_METHOD(update);
    sensitive << clock.pos();
}
};

```

2.7 Odd Pipe

The behavioral SystemC module has the following basic structure:

```

SC_MODULE(OddPipe) {

    //Inputs
    sc_in<bool> clock;
    sc_in<sc_uint<32>> > info[4]; //info = [PC,opcode,rt,value];
    sc_in<sc_biguint<128>> > A, B, C, T;

    //Outputs
    sc_out<sc_biguint<128>> > Result[8];
    sc_out<sc_uint<8>> > Result_Destination[8];
    sc_out<sc_uint<8>> > Stage_When_Ready[8];
    sc_out<bool> Reg_Write[8];
    sc_out<sc_uint<8>> > Unit_Id[8];
    sc_out<sc_uint<32>> > Miss_Instructions[8][33];
    sc_out<sc_int<32>> > pc_plus_offset[8];
    sc_out<sc_uint<3>> > flush;

    //Methods
    void update();

    //Constructor
    SC_CTOR(OddPipe){
        SC_METHOD(update);
        sensitive << clock.pos();
    }
};

```


3. Instructions

Inst	Opcode	Syntax	Unit	UnitId	Pipe	Latency
Add Word	00011000000	a rt,ra,rb	Simple Fixed 1	1	even	2
	$RT^{0:3} \leftarrow RA^{0:3} + RB^{0:3}$ $RT^{4:7} \leftarrow RA^{4:7} + RB^{4:7}$ $RT^{8:11} \leftarrow RA^{8:11} + RB^{8:11}$ $RT^{12:15} \leftarrow RA^{12:15} + RB^{12:15}$					
Add Word Immediate	00011100	ai rt,ra,value	Simple Fixed 1	1	even	2
	$t \leftarrow \text{RepLeftBit}(I10,32)$ $RT^{0:3} \leftarrow RA^{0:3} + t$ $RT^{4:7} \leftarrow RA^{4:7} + t$ $RT^{8:11} \leftarrow RA^{8:11} + t$ $RT^{12:15} \leftarrow RA^{12:15} + t$					
Subtract from Word	00001000000	sf rt,ra,rb	Simple Fixed 1	1	even	2
	$RT^{0:3} \leftarrow RB^{0:3} + (\neg RA^{0:3}) + 1$ $RT^{4:7} \leftarrow RB^{4:7} + (\neg RA^{4:7}) + 1$ $RT^{8:11} \leftarrow RB^{8:11} + (\neg RA^{8:11}) + 1$ $RT^{12:15} \leftarrow RB^{12:15} + (\neg RA^{12:15}) + 1$					
Subtract from Word Immediate	00001101	sfi rt,ra,value	Simple Fixed 1	1	even	2
	$t \leftarrow \text{RepLeftBit}(I10,32)$ $RT^{0:3} \leftarrow t + (\neg RA^{0:3}) + 1$ $RT^{4:7} \leftarrow t + (\neg RA^{4:7}) + 1$ $RT^{8:11} \leftarrow t + (\neg RA^{8:11}) + 1$ $RT^{12:15} \leftarrow t + (\neg RA^{12:15}) + 1$					
Count Leading Zeros	01010100101	clz rt,ra	Simple Fixed 1	1	even	2

	<pre> for j = 0 to 15 by 4 t ← 0 u ← RA^{j:4} For m = 0 to 31 If u_m = 1 then leave t ← t + 1 end RT^{j:4} ← t end </pre>					
And	00011000001	and rt,ra,rb	Simple Fixed 1	1	even	2
	$RT^{0:3} \leftarrow RA^{0:3} \& RB^{0:3}$ $RT^{4:7} \leftarrow RA^{4:7} \& RB^{4:7}$ $RT^{8:11} \leftarrow RA^{8:11} \& RB^{8:11}$ $RT^{12:15} \leftarrow RA^{12:15} \& RB^{12:15}$					
And Word Immediate	00010100	andi rt,ra,value	Simple Fixed 1	1	even	2
	$t \leftarrow \text{RepLeftBit}(I10,32)$ $RT^{0:3} \leftarrow RA^{0:3} \& t$ $RT^{4:7} \leftarrow RA^{4:7} \& t$ $RT^{8:11} \leftarrow RA^{8:11} \& t$ $RT^{12:15} \leftarrow RA^{12:15} \& t$					
Or	00001000001	or rt,ra,rb	Simple Fixed 1	1	even	2
	$RT^{0:3} \leftarrow RA^{0:3} RB^{0:3}$ $RT^{4:7} \leftarrow RA^{4:7} RB^{4:7}$ $RT^{8:11} \leftarrow RA^{8:11} RB^{8:11}$ $RT^{12:15} \leftarrow RA^{12:15} RB^{12:15}$					
Or Word Immediate	00000100	ori rt,ra,value	Simple Fixed 1	1	even	2
	$t \leftarrow \text{RepLeftBit}(I10,32)$ $RT^{0:3} \leftarrow RA^{0:3} t$ $RT^{4:7} \leftarrow RA^{4:7} t$ $RT^{8:11} \leftarrow RA^{8:11} t$ $RT^{12:15} \leftarrow RA^{12:15} t$					
Exclusive Or	01001000001	xor rt,ra,rb	Simple Fixed 1	1	even	2

	$RT^{0:3} \leftarrow RA^{0:3} \oplus RB^{0:3}$ $RT^{4:7} \leftarrow RA^{4:7} \oplus RB^{4:7}$ $RT^{8:11} \leftarrow RA^{8:11} \oplus RB^{8:11}$ $RT^{12:15} \leftarrow RA^{12:15} \oplus RB^{12:15}$					
Exclusive Or Word Immediate	01000100	xori rt,ra,value	Simple Fixed 1	1	even	2
	$t \leftarrow \text{RepLeftBit}(l10,32)$ $RT^{0:3} \leftarrow RA^{0:3} \oplus t$ $RT^{4:7} \leftarrow RA^{4:7} \oplus t$ $RT^{8:11} \leftarrow RA^{8:11} \oplus t$ $RT^{12:15} \leftarrow RA^{12:15} \oplus t$					
Nand	00011001001	nand rt,ra,rb	Simple Fixed 1	1	even	2
	$RT^{0:3} \leftarrow \neg(RA^{0:3} \& RB^{0:3})$ $RT^{4:7} \leftarrow \neg(RA^{4:7} \& RB^{4:7})$ $RT^{8:11} \leftarrow \neg(RA^{8:11} \& RB^{8:11})$ $RT^{12:15} \leftarrow \neg(RA^{12:15} \& RB^{12:15})$					
Nor	00001001001	nor rt,ra,rb	Simple Fixed 1	1	even	2
	$RT^{0:3} \leftarrow \neg(RA^{0:3} RB^{0:3})$ $RT^{4:7} \leftarrow \neg(RA^{4:7} RB^{4:7})$ $RT^{8:11} \leftarrow \neg(RA^{8:11} RB^{8:11})$ $RT^{12:15} \leftarrow \neg(RA^{12:15} RB^{12:15})$					
Compare Equal Word	01111000000	ceq rt,ra,rb	Simple Fixed 1	1	even	2
	<pre> for i = 0 to 15 by 4 If RA^{i:4} = RB^{i:4} then RT^{i:4} ← 0xFFFFFFFF else RT^{i:4} ← 0x00000000 end </pre>					
Compare Equal Word Immediate	01111100	ceqi rt,ra,value	Simple Fixed 1	1	even	2
	<pre> for i = 0 to 15 by 4 If RA^{i:4} = RepLeftBit(l10,32) then RT^{i:4} ← 0xFFFFFFFF else RT^{i:4} ← 0x00000000 end </pre>					

Compare Greater Than Word	01001000000	cgt rt,ra,rb	Simple Fixed 1	1	even	2
	<pre> for i = 0 to 15 by 4 If RA_{i:4} > RB_{i:4} then RT_{i:4} ← 0xFFFFFFFF else RT_{i:4} ← 0x00000000 end </pre>					
Compare Greater Than Word Immediate	01001100	cgti rt,ra,value	Simple Fixed 1	1	even	2
	<pre> for i = 0 to 15 by 4 If RA_{i:4} > RepLeftBit(110,32) then RT_{i:4} ← 0xFFFFFFFF else RT_{i:4} ← 0x00000000 end </pre>					
Double Floating Compare Equal	01111000011	dfceq rt,ra,rb	Simple Fixed 1	1	even	2
	<ul style="list-style-type: none"> The double-precision floating-point value from register RA is compared with the double-precision floating-point value from register RB. If the values are equal, a result of all ones (true) is produced in register RT. Otherwise, a result of zero (false) is produced in register RT. 					
Double Floating Compare Greater Than	01011000011	dfcgt rt,ra,rb	Simple Fixed 1	1	even	2
	<ul style="list-style-type: none"> The double-precision floating-point value in register RA is compared with the double-precision floating-point value in register RB. If the value in RA is greater than the value in RB, a result of all ones (true) is produced in register RT. Otherwise, a result of zero (false) is produced in register RT. 					
Floating Compare Equal	01111000010	fceq rt,ra,rb	Simple Fixed 1	1	even	2
	<p>For each of four word slots:</p> <ul style="list-style-type: none"> The floating-point value from register RA is compared with the floating-point value from register RB. If the values are equal, a result of all ones (true) is produced in register RT. Otherwise, a result of zero (false) is produced in register RT. Two zeros always compare equal independent of their fractions and signs. 					
Floating Compare Greater Than	01011000010	fcgt rt,ra,rb	Simple Fixed 1	1	even	2
	<p>For each of four word slots:</p> <ul style="list-style-type: none"> The floating-point value in register RA is compared with the floating-point value in register RB. If the value in RA is greater than the value in RB, a result of all ones (true) is produced in register RT. Otherwise, a result of zero (false) is produced in register RT. Two zeros never compare greater than independent of their sign bits and fractions. 					
And Byte Immediate	00010110	andbi rt,ra,value	Simple Fixed 1	1	even	2

	$b \leftarrow I10 \& 0x00FF$ $bbbb \leftarrow b \parallel b \parallel b \parallel b$ $RT^{0:3} \leftarrow RA^{0:3} \& bbbb$ $RT^{4:7} \leftarrow RA^{4:7} \& bbbb$ $RT^{8:11} \leftarrow RA^{8:11} \& bbbb$ $RT^{12:15} \leftarrow RA^{12:15} \& bbbb$					
Or Byte Immediate	00000110	orbi rt,ra,value	Simple Fixed 1	1	even	2
	$b \leftarrow I10 \& 0x00FF$ $bbbb \leftarrow b \parallel b \parallel b \parallel b$ $RT^{0:3} \leftarrow RA^{0:3} bbbb$ $RT^{4:7} \leftarrow RA^{4:7} bbbb$ $RT^{8:11} \leftarrow RA^{8:11} bbbb$ $RT^{12:15} \leftarrow RA^{12:15} bbbb$					
Exclusive Or Byte Immediate	01000110	xorbi rt,ra,value	Simple Fixed 1	1	even	2
	$b \leftarrow I10 \& 0x00FF$ $bbbb \leftarrow b \parallel b \parallel b \parallel b$ $RT^{0:3} \leftarrow RA^{0:3} \oplus bbbb$ $RT^{4:7} \leftarrow RA^{4:7} \oplus bbbb$ $RT^{8:11} \leftarrow RA^{8:11} \oplus bbbb$ $RT^{12:15} \leftarrow RA^{12:15} \oplus bbbb$					
Compare Equal Byte	01111010000	ceqb rt,ra,rb	Simple Fixed 1	1	even	2
	<pre> for i = 0 to 15 If RAⁱ = RBⁱ then RTⁱ ← 0xFF else RTⁱ ← 0x00 end </pre>					
Compare Equal Byte Immediate	01111110	ceqbi rt,ra,value	Simple Fixed 1	1	even	2
	<pre> for i = 0 to 15 If RAⁱ = I10_{2:3} then RTⁱ ← 0xFF else RTⁱ ← 0x00 end </pre>					

Compare Greater Than Byte	01001010000	cgtb rt,ra,rb	Simple Fixed 1	1	even	2
	<pre> for i = 0 to 15 If $RA^i > RB^i$ then $RT^i \leftarrow 0xFF$ else $RT^i \leftarrow 0x00$ end </pre>					
Compare Greater Than Byte Immediate	01001110	cgtbi rt,ra,value	Simple Fixed 1	1	even	2
	<pre> for i = 0 to 15 If $RA^i > I10_{2:9}$ then $RT^i \leftarrow 0xFF$ else $RT^i \leftarrow 0x00$ end </pre>					
Shift Left Word	00001011011	shl rt,ra,rb	Simple Fixed 2	2	even	4
	<pre> for j = 0 to 15 by 4 s $\leftarrow RB^{j:4} \& 0x0000003F$ t $\leftarrow RA^{j:4}$ for b = 0 to 31 if $b + s < 32$ then $r_b \leftarrow t_{b+s}$ else $r_b \leftarrow 0$ end $RT^{j:4} \leftarrow r$ end </pre>					
Rotate Word	00001011000	rot rt,ra,rb	Simple Fixed 2	2	even	4
	<pre> for j = 0 to 15 by 4 s $\leftarrow RB^{j:4} \& 0x0000001F$ t $\leftarrow RA^{j:4}$ for b = 0 to 31 if $b + s < 32$ then $r_b \leftarrow t_{b+s}$ else $r_b \leftarrow t_{b+s-32}$ end $RT^{j:4} \leftarrow r$ end </pre>					
Multiply	01111000100	mpy rt,ra,rb	Single Prec 1	3	even	7

	$RT^{0:3} \leftarrow RA^{2:3} * RB^{2:3}$ $RT^{4:7} \leftarrow RA^{6:7} * RB^{6:7}$ $RT^{8:11} \leftarrow RA^{10:11} * RB^{10:11}$ $RT^{12:15} \leftarrow RA^{14:15} * RB^{14:15}$					
Multiply Immediate	01110100	mpyi rt,ra,value	Single Prec 1	3	even	7
	$t \leftarrow \text{RepLeftBit}(I(10,16))$ $RT^{0:3} \leftarrow RA^{2:3} * t$ $RT^{4:7} \leftarrow RA^{6:7} * t$ $RT^{8:11} \leftarrow RA^{10:11} * t$ $RT^{12:15} \leftarrow RA^{14:15} * t$					
Integer Multiply and Add	1100	mpya rt,ra,rb,rc	Single Prec 1	3	even	7
	$t0 \leftarrow RA^{2:3} * RB^{2:3}$ $t1 \leftarrow RA^{6:7} * RB^{6:7}$ $t2 \leftarrow RA^{10:11} * RB^{10:11}$ $t3 \leftarrow RA^{14:15} * RB^{14:15}$ $RT^{0:3} \leftarrow t0 + RC^{0:3}$ $RT^{4:7} \leftarrow t1 + RC^{4:7}$ $RT^{8:11} \leftarrow t2 + RC^{8:11}$ $RT^{12:15} \leftarrow t3 + RC^{12:15}$					
Floating Add	01011000100	fa rt,ra,rb	Single Prec 2	4	even	6
	<p>For each of the four word slots:</p> <ul style="list-style-type: none"> The operand from register RA is added to the operand from register RB. The result is placed in register RT. 					
Double Floating Add	01011001100	dfa rt,ra,rb	Single Prec 2	4	even	6
	<p>For each of two doubleword slots:</p> <ul style="list-style-type: none"> The operand from register RA is added to the operand from register RB. The result is placed in register RT. 					
Floating Subtract	01011000101	fs rt,ra,rb	Single Prec 2	4	even	6
	<p>For each of the four word slots:</p> <ul style="list-style-type: none"> The operand from register RB is subtracted from the operand from register RA. The result is placed in register RT. 					

Double Floating Subtract	01011001101	dfs rt,ra,rb	Single Prec 2	4	even	6
	For each of two doubleword slots: <ul style="list-style-type: none"> The operand from register RB is subtracted from the operand from register RA. The result is placed in register RT. 					
Floating Multiply	01011000110	fm rt,ra,rb	Single Prec 2	4	even	6
	For each of the four word slots: <ul style="list-style-type: none"> The operand from register RA is multiplied by the operand from register RB. The result is placed in register RT. 					
Double Floating Multiply	01011001110	dfm rt,ra,rb	Single Prec 2	4	even	6
	For each of two doubleword slots: <ul style="list-style-type: none"> The operand from register RA is multiplied by the operand from register RB. The result is placed in register RT. 					
Floating Multiply and Add	1110	fma rt,ra,rb,rc	Single Prec 2	4	even	6
	For each of the four word slots: <ul style="list-style-type: none"> The operand from register RA is multiplied by the operand from register RB and added to the operand from register RC. The multiplication is exact and not subject to limits on its range. The result is placed in register RT. 					
Double Floating Multiply and Add	01101011100	dfma rt,ra,rb	Single Prec 2	4	even	6
	For each of two doubleword slots: <ul style="list-style-type: none"> The operand from register RA is multiplied by the operand from register RB and added to the operand from register RT. The multiplication is exact and not subject to limits on its range. The result is placed in register RT. 					
Floating Multiply and Subtract	1111	fms rt,ra,rb,rc	Single Prec 2	4	even	6
	For each of the four word slots: <ul style="list-style-type: none"> The operand from register RA is multiplied by the operand from register RB. The result of the multiplication is exact and not subject to limits on its range. The operand from register RC is subtracted from the product. The result is placed in register RT. 					
Double Floating Multiply and Subtract	01101011101	dfms rt,ra,rb	Single Prec 2	4	even	6
	For each of two doubleword slots: <ul style="list-style-type: none"> The operand from register RA is multiplied by the operand from register RB. The multiplication is exact and not subject to limits on its range. The operand from register RT is subtracted from the product. The result is placed in register RT. 					
Count Ones in Bytes	01010110100	cntb rt,ra	Byte	5	even	4

	<pre>for j = 0 to 15 c = 0 b ← RA^j For m = 0 to 7 If b_m = 1 then c ← c + 1 end RT^j ← c end</pre>																					
Average Bytes	00011010011	avgb rt,ra,rb	Byte	5	even	4																
	<pre>for j = 0 to 15 RT^j ← ((0x00 RA^j) + (0x00 RB^j) + 1)_{7:14} end</pre>																					
Absoute Differences of Bytes	00001010011	absdb rt,ra,rb	Byte	5	even	4																
	<pre>for j = 0 to 15 if (RB^j >^u RA^j) then RT^j ← RB^j - RA^j else RT^j ← RA^j - RB^j end</pre>																					
Sum Bytes into Halfwords	01001010011	sumb rt,ra,rb	Byte	5	even	4																
	<table><tr><td>RT^{0:1}</td><td>← RB⁰ + RB¹ + RB² + RB³</td></tr><tr><td>RT^{2:3}</td><td>← RA⁰ + RA¹ + RA² + RA³</td></tr><tr><td>RT^{4:5}</td><td>← RB⁴ + RB⁵ + RB⁶ + RB⁷</td></tr><tr><td>RT^{6:7}</td><td>← RA⁴ + RA⁵ + RA⁶ + RA⁷</td></tr><tr><td>RT^{8:9}</td><td>← RB⁸ + RB⁹ + RB¹⁰ + RB¹¹</td></tr><tr><td>RT^{10:11}</td><td>← RA⁸ + RA⁹ + RA¹⁰ + RA¹¹</td></tr><tr><td>RT^{12:13}</td><td>← RB¹² + RB¹³ + RB¹⁴ + RB¹⁵</td></tr><tr><td>RT^{14:15}</td><td>← RA¹² + RA¹³ + RA¹⁴ + RA¹⁵</td></tr></table>						RT ^{0:1}	← RB ⁰ + RB ¹ + RB ² + RB ³	RT ^{2:3}	← RA ⁰ + RA ¹ + RA ² + RA ³	RT ^{4:5}	← RB ⁴ + RB ⁵ + RB ⁶ + RB ⁷	RT ^{6:7}	← RA ⁴ + RA ⁵ + RA ⁶ + RA ⁷	RT ^{8:9}	← RB ⁸ + RB ⁹ + RB ¹⁰ + RB ¹¹	RT ^{10:11}	← RA ⁸ + RA ⁹ + RA ¹⁰ + RA ¹¹	RT ^{12:13}	← RB ¹² + RB ¹³ + RB ¹⁴ + RB ¹⁵	RT ^{14:15}	← RA ¹² + RA ¹³ + RA ¹⁴ + RA ¹⁵
RT ^{0:1}	← RB ⁰ + RB ¹ + RB ² + RB ³																					
RT ^{2:3}	← RA ⁰ + RA ¹ + RA ² + RA ³																					
RT ^{4:5}	← RB ⁴ + RB ⁵ + RB ⁶ + RB ⁷																					
RT ^{6:7}	← RA ⁴ + RA ⁵ + RA ⁶ + RA ⁷																					
RT ^{8:9}	← RB ⁸ + RB ⁹ + RB ¹⁰ + RB ¹¹																					
RT ^{10:11}	← RA ⁸ + RA ⁹ + RA ¹⁰ + RA ¹¹																					
RT ^{12:13}	← RB ¹² + RB ¹³ + RB ¹⁴ + RB ¹⁵																					
RT ^{14:15}	← RA ¹² + RA ¹³ + RA ¹⁴ + RA ¹⁵																					
Shift Left Quadword by Bytes	00111011111	shlqby rt,ra,rb	Perm	6	odd	4																
	<pre>s ← RB_{27:31} for b = 0 to 15 if b + s < 16 then r^b ← RA^{b+s} else r^b ← 0 end RT ← r</pre>																					

Rotate Quadword by Bytes	00111011100	rotqby rt,ra,rb	Perm	6	odd	4
	<pre> s ← (0 - RB_{27:31}) & 0x1F for b = 0 to 15 if b ≥ s then r^b ← t^{b-s} else r^b ← 0x00 end RT ← r </pre>					
Load Quadword (x-form)	00111000100	lqx rt,ra,rb	Local Store	7	odd	6
	<pre> LSA ← (RA^{0:3} + RB^{0:3}) & LSLR & 0xFFFFFFFF0 RT ← LocStor(LSA,16) </pre>					
Load Quadword (a-form)	001100001	lqa rt,symbol	Local Store	7	odd	6
	<pre> LSA ← RepLeftBit(116 0b00,32) & LSLR & 0xFFFFFFFF0 RT ← LocStor(LSA,16) </pre>					
Store Quadword (x-form)	00101000100	stqx rt,ra,rb	Local Store	7	odd	6
	<pre> LSA ← (RA^{0:3} + RB^{0:3}) & LSLR & 0xFFFFFFFF0 LocStor(LSA,16) ← RT </pre>					
Store Quadword (a-form)	001000101	stqa rt,symbol	Local Store	7	odd	6
	<pre> LSA ← RepLeftBit(116 0b00,32) & LSLR & 0xFFFFFFFF0 LocStor(LSA,16) ← RT </pre>					
Miss	10000000000	miss	Local Store	7	odd	6
	Load instructions from local store into instruction cache					
Branch Relative	001100100	br symbol	Branch	8	odd	3
	<pre> PC ← (PC + RepLeftBit(116 0b00,32)) & LSLR </pre>					
Branch Absolute	001100000	bra symbol	Branch	8	odd	3
	<pre> PC ← RepLeftBit(116 0b00,32) & LSLR </pre>					
Branch If Not Zero Word	001000010	brnz rt,symbol	Branch	8	odd	3

	<p>If $RT^{0:3} \neq 0$ then $PC \leftarrow (PC + \text{RepLeftBit}(I16 \parallel 0b00)) \& \text{LSLR} \& 0xFFFFFFFFC$ else $PC \leftarrow (PC+4) \& \text{LSLR}$</p>					
Branch If Zero Word	001000111	brz rt,symbol	Branch	8	odd	3
	<p>If $RT^{0:3} = 0$ then $PC \leftarrow (PC + \text{RepLeftBit}(I16 \parallel 0b00)) \& \text{LSLR} \& 0xFFFFFFFFC$ else $PC \leftarrow (PC + 4) \& \text{LSLR}$</p>					
Halt	01111011000	halt	NA	9	N/A	0
No Operation (Execute)	01000000001	nop	NA	9	even	0
No Operation (Load)	00000000001	lnop	NA	9	odd	0

4. Testing

4.1 Preloaded Register Data

Prior to running the design verification tests, the following data was preloaded into the registers:

Reg.	Word 0	Word 1	Word 2	Word 3
0	0 <uint32>	0 <uint32>	0 <uint32>	0 <uint32>
1	1 <uint32>	0 <uint32>	0 <uint32>	0 <uint32>
2	2 <uint32>	0 <uint32>	0 <uint32>	0 <uint32>
3	7 <uint32>	0 <uint32>	0 <uint32>	0 <uint32>
4	10 <uint32>	0 <uint32>	0 <uint32>	0 <uint32>
5	-1 <int32>	0 <uint32>	0 <uint32>	0 <uint32>
6	299792458 <uint32>	0 <uint32>	0 <uint32>	0 <uint32>
7	3.14 <float>	0 <uint32>	0 <uint32>	0 <uint32>
8	-0.5 <float>	0 <uint32>	0 <uint32>	0 <uint32>
9	2.71 <double>		0 <uint32>	0 <uint32>
10	-0.25 <double>		0 <uint32>	0 <uint32>
11	1.41 <double>		0 <uint32>	0 <uint32>
12	-1.22e-09 <float>	0 <uint32>	0 <uint32>	0 <uint32>
13	1 <uint32>	0 <uint32>	0 <uint32>	0 <uint32>
14	0 <uint32>	0 <uint32>	0 <uint32>	1 <uint32>
15:127	0 <uint32>	0 <uint32>	0 <uint32>	0 <uint32>

4.2 Test Case 1: No Hazards

Objectives

- Verify the model can process independent instructions simultaneously in both pipes.
- Verify instruction miss works for multiple instruction blocks.

Test Program

```

a 15,2,3
shlqby 16,13,1
ai 17,1,-400
rotqby 18,14,3
sf 19,3,2
shlqby 20,13,1
sfi 21,1,-100
rotqby 22,14,3
clz 23,1
shlqby 24,13,1
and 25,3,4
rotqby 26,14,3
andi 27,3,1023
shlqby 28,13,1
or 29,3,4
rotqby 30,14,3
ori 31,3,1022
shlqby 32,13,1
xor 33,3,4
rotqby 34,14,3
xori 35,2,11
shlqby 36,13,1
nand 37,3,3
rotqby 38,14,3
nor 39,3,4
shlqby 40,13,1
ceq 41,6,6
rotqby 42,14,3
ceqi 43,6,5
shlqby 44,13,1
cgt 45,6,1
rotqby 46,14,3
cgti 47,6,-8
shlqby 48,13,1
dfceq 49,9,9
rotqby 50,14,3
dfcgt 51,11,10
shlqby 52,13,1
fceq 53,8,8
rotqby 54,14,3
fcgt 55,7,8
shlqby 56,13,1
andbi 57,3,10
rotqby 58,14,3
orbi 59,3,10
shlqby 60,13,1

```

```

xorbi 61,3,10
rotqby 62,14,3
ceqb 63,3,3
shlqby 64,13,1
ceqbi 65,4,0
rotqby 66,14,3
cgtb 67,4,3
shlqby 68,13,1
cgtbi 69,4,9
rotqby 70,14,3
shl 71,1,6
shlqby 72,13,1
rot 73,6,4
rotqby 74,14,3
halt

```

Expected Calculation Results (Even Pipe)

```

Reg[15] = Reg[2]+Reg[3] = 9 //EVEN
Reg[17] = Reg[1]-400 = 1-400 = -399 //EVEN
Reg[19] = Reg[3]-Reg[2] = 5 //EVEN
Reg[21] = -100-Reg[1] = -100-1 = -101 //EVEN
Reg[23] = countLeadingZeros(Reg[1]) = 31 //EVEN
Reg[25] = Reg[3] & Reg[4] = 2 //EVEN
Reg[27] = Reg[3] & signExt(1023) = 7 //EVEN
Reg[29] = Reg[3] | Reg[4] = 15 //EVEN
Reg[31] = Reg[3] | signExt(1022) = -1 //EVEN
Reg[33] = Reg[3]^Reg[4] = 13 //EVEN
Reg[35] = Reg[3]^signExt(11) = 9 //EVEN
Reg[37] = !(Reg[3] & Reg[3]) = -8 //EVEN
Reg[39] = !(Reg[3] | Reg[4]) = -16 //EVEN
Reg[41] = chk(Reg[6]==Reg[6]) = -1 //EVEN
Reg[43] = chk(Reg[6]==repLeftBit(5)) = 0 //EVEN
Reg[45] = chk(Reg[6]>Reg[1]) = -1 //EVEN
Reg[47] = chk(Reg[6]>-8) = -1 //EVEN
Reg[49] = chk(Reg[9]==Reg[9]) = -1 //EVEN
Reg[51] = chk(Reg[11]>Reg[10]) = 0 //EVEN
Reg[53] = chk(Reg[8]==Reg[8]) = -1 //EVEN
Reg[55] = chk(Reg[7]>Reg[8]) = -1 //EVEN
Reg[57] = andBytes(Reg[3],168430090) = 2 //EVEN
Reg[59] = orBytes(Reg[3],168430090) = 168430095 //EVEN
Reg[61] = xorBytes(Reg[3],168430090) = 168430093 //EVEN
Reg[63] = chkBytes(Reg[3]==Reg[3]) = -1 //EVEN
Reg[65] = chkBytes(Reg[4]==0) = -256 //EVEN
Reg[67] = chkBytes(Reg[4]>Reg[3]) = 255 //EVEN
Reg[69] = chkBytes(Reg[4]>9) = 255 //EVEN
Reg[71] = shiftLeftBits(Reg[1],10) = 1024 //EVEN
Reg[73] = rotBits(Reg[6],10) = 2044799047 //EVEN

```

Expected Calculation Results (Odd Pipe)

```

Reg[16] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[18] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
Reg[20] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[22] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
Reg[24] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[26] = rotLeftBytes(Reg[14],3) = 16777216 //ODD

```

```

Reg[28] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[30] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
Reg[32] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[34] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
Reg[36] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[38] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
Reg[40] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[42] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
Reg[44] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[46] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
Reg[48] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[50] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
Reg[52] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[54] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
Reg[56] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[58] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
Reg[60] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[62] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
Reg[64] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[66] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
Reg[68] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[70] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
Reg[72] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[74] = rotLeftBytes(Reg[14],3) = 16777216 //ODD

```

Expected Timing Results

```

[clock 01] Instruction Miss
[clock 14] First Instruction Pair Fetch (Instruction Block 0)
[clock 15] First Instruction Pair Decode (Instruction Block 0)
[clock 16] First Instruction Pair Issue (Instruction Block 0)
[clock 17] First Instruction Pair RF (Instruction Block 0)
[clock 18] First Instruction Pair Pipe Input (Instruction Block 0)
[clock 19] First Instruction Pair Appear at Pipe Stage 1 (Instruction Block 0)
[clock 30] Instruction Miss
[clock 43] First Instruction Pair Fetch (Instruction Block 1)
[clock 44] First Instruction Pair Decode (Instruction Block 1)
[clock 45] First Instruction Pair Issue (Instruction Block 1)
[clock 46] First Instruction Pair RF (Instruction Block 1)
[clock 47] First Instruction Pair Pipe Input (Instruction Block 1)
[clock 48] First Instruction Pair Appear at Pipe Stage 1 (Instruction Block 1)

```

Model Output (Even Pipe)

```

*****
TEST CASE 1: NO HAZARDS (EVEN PIPE)
*****

```

```

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```

EVEN PIPE PRINTOUT:

Clk	Unit Id	Stage Ready	Register Write	Result Destination	Fl	Result
<INSTRUCTION MISS>						
1	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0, 0, 0, 0, 0, 0, 0,	0	0,0,0,0,0,0,0,
2	9,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0, 0, 0, 0, 0, 0, 0,	0	0,0,0,0,0,0,0,
3	9,9,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0, 0, 0, 0, 0, 0, 0,	0	0,0,0,0,0,0,0,
4	9,9,9,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0, 0, 0, 0, 0, 0, 0,	0	0,0,0,0,0,0,0,
5	9,9,9,9,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0, 0, 0, 0, 0, 0, 0,	0	0,0,0,0,0,0,0,

4.3 Test Case 2: Structural Hazards

Objectives

- Verify model can handle the following structural hazards:
 - 2 sequential even pipe instructions.
 - 2 sequential odd pipe instructions.
 - Even/odd instruction pipe swap.
 - 2 sequential instructions with the same register file destination.

Test Program

```
a 16,2,3
ai 17,1,-400
shlqby 18,13,1
rotqby 19,14,3
shlqby 20,13,1
sf 21,3,2
sfi 22,1,-100
rotqby 22,14,3
halt
```

Expected Calculation Results

```
Reg[16] = Reg[2]+Reg[3] = 2+7 = 9           //EVEN
Reg[17] = Reg[1]-400 = 1-400 = -399        //EVEN
Reg[18] = shiftLeftBytes(Reg[13],1) = 256   //ODD
Reg[19] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
Reg[20] = shiftLeftBytes(Reg[13],1) = 256   //ODD
Reg[21] = Reg[3]-Reg[2] = 5                 //EVEN
Reg[22] = -100-Reg[1] = -100-1 = -101       //EVEN
Reg[22] = rotLeftBytes(Reg[14],3) = 16777216 //ODD
```

Expected Timing Results (Even Pipe)

```
[clock 01] Instruction Miss
[clock 14] First Instruction Pair Fetch
[clock 15] First Instruction Pair Decode
[clock 16] "A" Instruction Issue (Appears in EvenPipe on clock 19)
[clock 17] "AI" Instruction Issue (Appears in EvenPipe on clock 20)
[clock 21] "SF" Instruction Issue (Appears in EvenPipe on clock 24)
[clock 22] "SFI" Instruction Issue
[clock 23] "SFI" Instruction RF
[clock 24] "SFI" Instruction Pipe Input
[clock 25] "SFI" Instruction Appears in EvenPipe
```

Expected Timing Results (Odd Pipe)

```
[clock 01] Instruction Miss
[clock 14] First Instruction Pair Fetch
[clock 18] "SHLQBY" Instruction Issue (Appears in OddPipe on clock 21)
[clock 19] "ROTQBY" Instruction Issue (Appears in OddPipe on clock 22)
```

[clock 20] "SHLQBY" Instruction Issue (Appears in OddPipe on clock 23)
[clock 26] "ROTBQBY" Instruction Issue (Appears in OddPipe on clock 29)

Model Output (Even Pipe)

TEST CASE 2: STRUCTURAL HAZARDS (EVEN PIPE)

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EVEN PIPE PRINTOUT:

Clk	Unit Id	Stage Ready	Register Write	Result Destination	Fl	Result
<INSTRUCTION MISS>						
1	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
2	9,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
3	9,9,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
4	9,9,9,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
5	9,9,9,9,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
6	9,9,9,9,9,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
7	9,9,9,9,9,9,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
8	9,9,9,9,9,9,9,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
9	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
10	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
11	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
12	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
13	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
<INSTRUCTION BLOCK WRITTEN TO CACHE>						
14	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
15	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
16	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
17	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
18	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
19	1,9,9,9,9,9,9,9	2,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	16, 0, 0, 0, 0, 0, 0, 0	0	9,0,0,0,0,0,0,0
20	1,1,9,9,9,9,9,9	2,2,0,0,0,0,0,0	0,1,0,0,0,0,0,0	17,16, 0, 0, 0, 0, 0, 0	0	-399,9,0,0,0,0,0,0
21	9,1,1,9,9,9,9,9	0,2,2,0,0,0,0,0	0,1,1,0,0,0,0,0	0,17,16, 0, 0, 0, 0, 0, 0	0	0,-399,9,0,0,0,0,0,0
22	9,9,1,1,9,9,9,9	0,0,2,2,0,0,0,0	0,0,1,1,0,0,0,0	0, 0,17,16, 0, 0, 0, 0, 0, 0	0	0,0,-399,9,0,0,0,0,0
23	9,9,9,1,1,9,9,9	0,0,0,2,2,0,0,0	0,0,0,1,1,0,0,0	0, 0, 0,17,16, 0, 0, 0, 0, 0, 0	0	0,0,0,-399,9,0,0,0
24	1,9,9,9,1,1,9,9	2,0,0,0,2,2,0,0	0,0,0,0,1,1,0,0	21, 0, 0, 0,17,16, 0, 0, 0, 0, 0, 0	0	5,0,0,0,-399,9,0,0
25	1,1,9,9,9,1,1,1	2,2,0,0,0,0,2,2	0,1,0,0,0,1,1,1	22,21, 0, 0, 0,17,16, 0, 0, 0, 0, 0, 0	0	-101,5,0,0,0,-399,9,0
26	9,1,1,9,9,9,1,1	0,2,2,0,0,0,0,2	0,1,1,0,0,0,0,1	0,22,21, 0, 0, 0,17, 0, 0, 0, 0, 0, 0	0	0,-101,5,0,0,0,-399,9,0
27	9,9,1,1,9,9,9,9	0,0,2,2,0,0,0,0	0,0,1,1,0,0,0,0	0, 0,22,21, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0	0	0,0,-101,5,0,0,0,0
28	9,9,9,1,1,9,9,9	0,0,0,2,2,0,0,0	0,0,0,1,1,0,0,0	0, 0, 0,22,21, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,-101,5,0,0,0
29	9,9,9,9,1,1,9,9	0,0,0,0,2,2,0,0	0,0,0,0,1,1,0,0	0, 0, 0, 0,22,21, 0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,-101,5,0,0
30	9,9,9,9,9,1,1,1	0,0,0,0,0,0,2,2	0,0,0,0,0,1,1,1	0, 0, 0, 0, 0,22,21, 0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,-101,5,0
31	9,9,9,9,9,9,1,1	0,0,0,0,0,0,0,2	0,0,0,0,0,0,0,1	0, 0, 0, 0, 0, 0,0,22, 0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,-101,5

Model Output (Odd Pipe)

TEST CASE 2: STRUCTURAL HAZARDS (ODD PIPE)

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ODD PIPE PRINTOUT:

Clk	Unit Id	Stage Ready	Register Write	Result Destination	PC	Result
<INSTRUCTION MISS>						
1	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
2	9,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
3	9,9,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
4	9,9,9,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	0	0,0,0,0,0,0,0,0
5	9,9,9,9,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	-1	0,0,0,0,0,0,0,0
6	9,9,9,9,9,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	-1	0,0,0,0,0,0,0,0
7	9,9,9,9,9,9,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	-1	0,0,0,0,0,0,0,0
8	9,9,9,9,9,9,9,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	-1	0,0,0,0,0,0,0,0
9	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	-1	0,0,0,0,0,0,0,0
10	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0, 0, 0, 0, 0, 0, 0, 0	-1	0,0,0,0,0,0,0,0

11	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0
12	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0
13	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0
<INSTRUCTION BLOCK WRITTEN TO CACHE>						
14	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0
15	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0
16	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0
17	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0
18	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0
19	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0
20	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0
21	6,9,9,9,9,9,9	4,0,0,0,0,0,0	0,0,0,0,0,0,0	18,0,0,0,0,0,0	-1	256,0,0,0,0,0,0
22	6,6,9,9,9,9,9	4,4,0,0,0,0,0	0,0,0,0,0,0,0	19,18,0,0,0,0,0	-1	16777216,256,0,0,0,0
23	6,6,6,9,9,9,9	4,4,4,0,0,0,0	0,0,0,0,0,0,0	20,19,18,0,0,0,0	-1	256,16777216,256,0,0,0,0
24	9,6,6,6,9,9,9	0,4,4,4,0,0,0	0,0,0,1,0,0,0	0,20,19,18,0,0,0	-1	0,256,16777216,256,0,0,0
25	9,9,6,6,6,9,9	0,0,4,4,4,0,0	0,0,0,1,1,0,0	0,0,20,19,18,0,0	-1	0,0,256,16777216,256,0,0
26	9,9,9,6,6,6,9	0,0,0,4,4,4,0	0,0,0,1,1,1,0	0,0,0,20,19,18,0	-1	0,0,0,256,16777216,256,0
27	9,9,9,9,6,6,6	0,0,0,0,4,4,4	0,0,0,0,1,1,1	0,0,0,0,20,19,18	-1	0,0,0,0,256,16777216,256
28	9,9,9,9,9,6,6	0,0,0,0,0,4,4	0,0,0,0,0,1,1	0,0,0,0,0,20,19	-1	0,0,0,0,0,256,16777216
29	6,9,9,9,9,9,6	4,0,0,0,0,0,4	0,0,0,0,0,0,1	22,0,0,0,0,0,20	-1	16777216,0,0,0,0,0,256
30	9,6,9,9,9,9,9	0,4,0,0,0,0,0	0,0,0,0,0,0,0	0,22,0,0,0,0,0	-1	0,16777216,0,0,0,0,0
31	9,9,6,9,9,9,9	0,0,4,0,0,0,0	0,0,0,0,0,0,0	0,0,22,0,0,0,0	-1	0,0,16777216,0,0,0,0
32	9,9,9,6,9,9,9	0,0,0,4,0,0,0	0,0,0,1,0,0,0	0,0,0,22,0,0,0	-1	0,0,0,16777216,0,0,0
33	9,9,9,9,6,9,9	0,0,0,0,4,0,0	0,0,0,0,1,0,0	0,0,0,0,22,0,0	-1	0,0,0,0,16777216,0,0
34	9,9,9,9,9,6,9	0,0,0,0,0,4,0	0,0,0,0,0,1,0	0,0,0,0,0,22,0	-1	0,0,0,0,0,16777216,0
35	9,9,9,9,9,9,6	0,0,0,0,0,0,4	0,0,0,0,0,0,1	0,0,0,0,0,0,22	-1	0,0,0,0,0,0,16777216

4.4 Test Case 3A: Data Hazards – No Stalls

Objectives

- Verify forwarding is functioning correctly without stalls.
- Verify blocks can be replaced in the instruction cache (test has 3 instruction blocks)

Test Program

```
cntb 15,3
lnop
nop
lnop
nop
lnop
nop
lnop
nop
lnop
nop
lnop
nop
stqa 15,99
avgb 16,3,4
lqa 17,99
nop
lnop
nop
lnop
nop
lnop
nop
lnop
nop
lnop
nop
lnop
nop
lnop
lnop
a 15,16,17
lnop
nop
lnop
nop
lnop
nop
lnop
mpy 15,15,5
lnop
nop
lnop
nop
lnop
nop
lnop
```

```

nop
lnop
nop
lnop
nop
lnop
nop
lnop
nop
lnop
nop
stqa 15,99
nop
lqa 18,99
nop
lnop
nop
lnop
nop
lnop
nop
lnop
nop
lnop
nop
lnop
nop
lnop
nop
lnop
a 19,18,5
halt

```

Expected Calculation Results

```

Reg[15] = sum(bin(7)==1) = 3           //EVEN
LS[99] = Reg[15] = 3                   //ODD
Reg[16] = avgBytes(7,10) = 9           //EVEN
Reg[17] = LS[99] = 3                   //ODD
Reg[15] = Reg[16]+Reg[17] = 9+3 = 12   //EVEN
Reg[15] = Reg[15]*Reg[5] = 12*(-1) = -12 //EVEN
LS[99] = Reg[15] = -12                 //ODD
Reg[18] = LS[99] = twosComp(-12) = 4294967284 //ODD
Reg[19] = Reg[18]+Reg[5] = -13         //EVEN

```

Expected Timing Results (Even Pipe)

```

[clock 01] Instruction Miss (Block 0)
[clock 16] "CNTB" Instruction Issue
[clock 17] "CNTB" Instruction RF
[clock 18] "CNTB" Instruction Pipe Input
[clock 19] "CNTB" Appears at EvenPipe Stage 1
[clock 23] "AVGB" Instruction Issue (Appears in EvenPipe on clock 26)
[clock 30] Instruction Miss (Block 1)
[clock 31] "A" Instruction Issue (Reg[16],Reg[17] results ready)
[clock 43] First Instruction Pair Fetch (Block 1)
[clock 48] "MPY" Instruction Issue (Appears in EvenPipe on clock 51)
[clock 59] Instruction Miss (Block 2)
[clock 72] First Instruction Pair Fetch (Block 2)

```

[clock 79] "A" Instruction Issue (Appears in EvenPipe on clock 82)

Expected Timing Results (Odd Pipe)

[clock 01] Instruction Miss (Block 0)

[clock 22] "STQA" Instruction Issue (Reg[15] results ready)

[clock 23] "LQA" Instruction Issue (Appears in OddPipe on clock 26)

[clock 30] Instruction Miss (Block 1)

[clock 57] "STQA" Instruction Issue

[clock 58] "LQA" Instruction Issue (Appears in OddPipe on clock 61)

Model Output (Even Pipe)

TEST CASE 3: DATA HAZARDS - NO STALLS (EVEN PIPE)

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EVEN PIPE PRINTOUT:

Clk	Unit Id	Stage Ready	Register Write	Result Destination	Fl	Result
<INSTRUCTION MISS>						
1	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
2	9,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
3	9,9,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
4	9,9,9,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
5	9,9,9,9,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
6	9,9,9,9,9,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
7	9,9,9,9,9,9,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
8	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
9	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
10	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
11	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
12	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
13	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
<INSTRUCTION BLOCK WRITTEN TO CACHE>						
14	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
15	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
16	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
17	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
18	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
19	5,9,9,9,9,9,9,9	4,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	15,0,0,0,0,0,0,0	0	3,0,0,0,0,0,0,0
20	9,5,9,9,9,9,9,9	0,4,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,15,0,0,0,0,0,0	0	0,3,0,0,0,0,0,0
21	9,9,5,9,9,9,9,9	0,0,4,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,15,0,0,0,0,0	0	0,0,3,0,0,0,0,0
22	9,9,9,5,9,9,9,9	0,0,0,4,0,0,0,0	0,0,0,1,0,0,0,0	0,0,0,15,0,0,0,0	0	0,0,0,3,0,0,0,0
23	9,9,9,9,5,9,9,9	0,0,0,0,4,0,0,0	0,0,0,0,1,0,0,0	0,0,0,0,15,0,0,0	0	0,0,0,0,3,0,0,0
24	9,9,9,9,9,5,9,9	0,0,0,0,0,4,0,0	0,0,0,0,0,1,0,0	0,0,0,0,0,15,0,0	0	0,0,0,0,0,3,0,0
25	9,9,9,9,9,9,5,9	0,0,0,0,0,0,4,0	0,0,0,0,0,0,0,1	0,0,0,0,0,0,15,0	0	0,0,0,0,0,0,3,0
26	5,9,9,9,9,9,9,9	4,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	16,0,0,0,0,0,0,0	0	9,0,0,0,0,0,0,0
27	9,5,9,9,9,9,9,9	0,4,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,16,0,0,0,0,0,0	0	0,9,0,0,0,0,0,0
28	9,9,5,9,9,9,9,9	0,0,4,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,16,0,0,0,0,0	0	0,0,9,0,0,0,0,0
29	9,9,9,5,9,9,9,9	0,0,0,4,0,0,0,0	0,0,0,1,0,0,0,0	0,0,0,16,0,0,0,0	0	0,0,0,9,0,0,0,0
<INSTRUCTION MISS>						
30	9,9,9,9,5,9,9,9	0,0,0,0,4,0,0,0	0,0,0,0,1,0,0,0	0,0,0,0,16,0,0,0	0	0,0,0,0,9,0,0,0
31	9,9,9,9,9,5,9,9	0,0,0,0,0,4,0,0	0,0,0,0,0,1,0,0	0,0,0,0,0,16,0,0	0	0,0,0,0,0,9,0,0
32	9,9,9,9,9,9,5,9	0,0,0,0,0,0,4,0	0,0,0,0,0,0,1,0	0,0,0,0,0,0,16,0	0	0,0,0,0,0,0,9,0
33	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
34	1,9,9,9,9,9,9,9	2,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	15,0,0,0,0,0,0,0	0	12,0,0,0,0,0,0,0
35	9,1,9,9,9,9,9,9	0,2,0,0,0,0,0,0	0,1,0,0,0,0,0,0	0,15,0,0,0,0,0,0	0	0,12,0,0,0,0,0,0
36	9,9,1,9,9,9,9,9	0,0,2,0,0,0,0,0	0,0,1,0,0,0,0,0	0,0,15,0,0,0,0,0	0	0,0,12,0,0,0,0,0
37	9,9,9,1,9,9,9,9	0,0,0,2,0,0,0,0	0,0,0,1,0,0,0,0	0,0,0,15,0,0,0,0	0	0,0,0,12,0,0,0,0
38	9,9,9,9,1,9,9,9	0,0,0,0,2,0,0,0	0,0,0,0,1,0,0,0	0,0,0,0,15,0,0,0	0	0,0,0,0,12,0,0,0
39	9,9,9,9,9,1,9,9	0,0,0,0,0,2,0,0	0,0,0,0,0,1,0,0	0,0,0,0,0,15,0,0	0	0,0,0,0,0,12,0,0
40	9,9,9,9,9,9,1,9	0,0,0,0,0,0,2,0	0,0,0,0,0,0,1,0	0,0,0,0,0,0,15,0	0	0,0,0,0,0,0,12,0
41	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
42	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
<INSTRUCTION BLOCK WRITTEN TO CACHE>						
43	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
44	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
45	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
46	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0

47	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
48	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
49	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
50	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
51	3,9,9,9,9,9,9,	7,0,0,0,0,0,0,	0,0,0,0,0,0,0,	15,0,0,0,0,0,0,	-12,0,0,0,0,0,0,
52	9,3,9,9,9,9,9,	0,7,0,0,0,0,0,	0,0,0,0,0,0,0,	0,15,0,0,0,0,0,	0,-12,0,0,0,0,0,
53	9,9,3,9,9,9,9,	0,0,7,0,0,0,0,	0,0,0,0,0,0,0,	0,0,15,0,0,0,0,	0,0,-12,0,0,0,0,
54	9,9,9,3,9,9,9,	0,0,0,7,0,0,0,	0,0,0,0,0,0,0,	0,0,0,15,0,0,0,	0,0,0,-12,0,0,0,
55	9,9,9,9,3,9,9,	0,0,0,0,7,0,0,	0,0,0,0,0,0,0,	0,0,0,0,15,0,0,	0,0,0,0,-12,0,0,
56	9,9,9,9,9,3,9,	0,0,0,0,0,7,0,	0,0,0,0,0,0,0,	0,0,0,0,0,15,0,	0,0,0,0,0,-12,0,
57	9,9,9,9,9,9,3,	0,0,0,0,0,0,7,	0,0,0,0,0,0,1,	0,0,0,0,0,0,15,	0,0,0,0,0,0,-12,
58	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
<INSTRUCTION MISS>					
59	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
60	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
61	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
62	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
63	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
64	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
65	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
66	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
67	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
68	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
69	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
70	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
71	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
<INSTRUCTION BLOCK WRITTEN TO CACHE>					
72	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
73	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
74	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
75	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
76	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
77	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
78	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
79	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
80	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
81	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,
82	1,9,9,9,9,9,9,	2,0,0,0,0,0,0,	0,0,0,0,0,0,0,	19,0,0,0,0,0,0,	-13,0,0,0,0,0,0,
83	9,1,9,9,9,9,9,	0,2,0,0,0,0,0,	0,1,0,0,0,0,0,	0,19,0,0,0,0,0,	0,-13,0,0,0,0,0,
84	9,9,1,9,9,9,9,	0,0,2,0,0,0,0,	0,0,1,0,0,0,0,	0,0,19,0,0,0,0,	0,0,-13,0,0,0,0,
85	9,9,9,1,9,9,9,	0,0,0,2,0,0,0,	0,0,0,1,0,0,0,	0,0,0,19,0,0,0,	0,0,0,-13,0,0,0,
86	9,9,9,9,1,9,9,	0,0,0,0,2,0,0,	0,0,0,0,1,0,0,	0,0,0,0,19,0,0,	0,0,0,0,-

Model Output (Odd Pipe)

TEST CASE 3: DATA HAZARDS - NO STALLS (ODD PIPE)

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ODD PIPE PRINTOUT:

Clk	Unit Id	Stage Ready	Register Write	Result Destination	PC	Result
<INSTRUCTION MISS>						
1	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
2	9,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
3	9,9,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
4	9,9,9,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
5	9,9,9,9,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
6	9,9,9,9,9,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
7	9,9,9,9,9,9,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
8	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
9	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
10	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
11	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
12	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
13	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
<INSTRUCTION BLOCK WRITTEN TO CACHE>						
14	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
15	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
16	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
17	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
18	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
19	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0

4.5 Test Case 3B: Data Hazards – With Stalls

Objectives

- Verify forwarding is functioning correctly with stalls.

Test Program

```
cntb 15,3
stqa 15,99
avgb 16,3,4
lqa 17,99
a 15,16,17
mpy 15,15,5
stqa 15,99
lqa 18,99
a 19,18,5
halt
```

Expected Calculation Results

```
Reg[15] = sum(bin(7)==1) = 3           //EVEN
LS[99] = Reg[15] = 3                   //ODD
Reg[16] = avgBytes(7,10) = 9           //EVEN
Reg[17] = LS[99] = 3                   //ODD
Reg[15] = Reg[16]+Reg[17] = 9+3 = 12    //EVEN
Reg[15] = Reg[15]*Reg[5] = 12*(-1) = -12 //EVEN
LS[99] = Reg[15] = -12                 //ODD
Reg[18] = LS[99] = -12 = 4294967284 (2s cmp) //ODD
Reg[19] = Reg[18]+Reg[5] = -13          //EVEN
halt
```

Expected Timing Results (Even Pipe)

```
[clock 01] Instruction Miss (Block 0)
[clock 16] "CNTB" Instruction Issue (Appears in EvenPipe on clock 19)
[clock 23] "AVGB" Instruction Issue (Appear in EvenPipe on clock 26)
[clock 31] "A" Instruction Issue (Appears in EvenPipe on clock 34)
[clock 35] "MPY" Instruction Issue (Appears in EvenPipe on clock 38)
[clock 53] "A" Instruction Issue (Appears in EvenPipe on clock 56)
```

Expected Timing Results (Odd Pipe)

```
[clock 01] Instruction Miss (Block 0)
[clock 22] "STQA" Instruction Issue (Appears in OddPipe on clock 25)
[clock 23] "LQA" Instruction Issue (Appears in OddPipe on clock 26)
[clock 44] "STQA" Instruction Issue (Appears in OddPipe on clock 47)
[clock 45] "LQA" Instruction Issue (Appears in OddPipe on clock 48)
```

Model Output (Even Pipe)

 TEST CASE 3: DATA HAZARDS - WITH STALLS (EVEN PIPE)

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EVEN PIPE PRINTOUT:

Clk	Unit Id	Stage Ready	Register Write	Result Destination	Fl	Result
<INSTRUCTION MISS>						
1	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
2	9,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
3	9,9,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
4	9,9,9,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
5	9,9,9,9,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
6	9,9,9,9,9,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
7	9,9,9,9,9,9,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
8	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
9	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
10	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
11	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
12	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
13	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
<INSTRUCTION BLOCK WRITTEN TO CACHE>						
14	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
15	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
16	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
17	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
18	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
19	9,9,9,9,9,9,9	4,0,0,0,0,0,0	0,0,0,0,0,0,0	15,0,0,0,0,0,0	0	3,0,0,0,0,0,0
20	9,5,9,9,9,9,9	0,4,0,0,0,0,0	0,0,0,0,0,0,0	0,15,0,0,0,0,0	0	0,3,0,0,0,0,0
21	9,9,5,9,9,9,9	0,0,4,0,0,0,0	0,0,0,0,0,0,0	0,0,15,0,0,0,0	0	0,0,3,0,0,0,0
22	9,9,9,5,9,9,9	0,0,0,4,0,0,0	0,0,0,1,0,0,0	0,0,0,15,0,0,0	0	0,0,0,3,0,0,0
23	9,9,9,9,5,9,9	0,0,0,0,4,0,0	0,0,0,0,1,0,0	0,0,0,0,15,0,0	0	0,0,0,0,3,0,0
24	9,9,9,9,9,5,9	0,0,0,0,0,4,0	0,0,0,0,0,1,0	0,0,0,0,0,15,0	0	0,0,0,0,0,3,0
25	9,9,9,9,9,9,5	0,0,0,0,0,0,4	0,0,0,0,0,0,1	0,0,0,0,0,0,15	0	0,0,0,0,0,0,3
26	5,9,9,9,9,9,9	4,0,0,0,0,0,0	0,0,0,0,0,0,0	16,0,0,0,0,0,0	0	9,0,0,0,0,0,0
27	9,5,9,9,9,9,9	0,4,0,0,0,0,0	0,0,0,0,0,0,0	0,16,0,0,0,0,0	0	0,9,0,0,0,0,0
28	9,9,5,9,9,9,9	0,0,4,0,0,0,0	0,0,0,0,0,0,0	0,0,16,0,0,0,0	0	0,0,9,0,0,0,0
29	9,9,9,5,9,9,9	0,0,0,4,0,0,0	0,0,0,1,0,0,0	0,0,0,16,0,0,0	0	0,0,0,9,0,0,0
30	9,9,9,9,5,9,9	0,0,0,0,4,0,0	0,0,0,0,1,0,0	0,0,0,0,16,0,0	0	0,0,0,0,9,0,0
31	9,9,9,9,9,5,9	0,0,0,0,0,4,0	0,0,0,0,0,1,0	0,0,0,0,0,16,0	0	0,0,0,0,0,9,0
32	9,9,9,9,9,9,5	0,0,0,0,0,0,4	0,0,0,0,0,0,1	0,0,0,0,0,0,16	0	0,0,0,0,0,0,9
33	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
34	1,9,9,9,9,9,9	2,0,0,0,0,0,0	0,0,0,0,0,0,0	15,0,0,0,0,0,0	0	12,0,0,0,0,0,0
35	9,1,9,9,9,9,9	0,2,0,0,0,0,0	0,1,0,0,0,0,0	0,15,0,0,0,0,0	0	0,12,0,0,0,0,0
36	9,9,1,9,9,9,9	0,0,2,0,0,0,0	0,0,1,0,0,0,0	0,0,15,0,0,0,0	0	0,0,12,0,0,0,0
37	9,9,9,1,9,9,9	0,0,0,2,0,0,0	0,0,0,1,0,0,0	0,0,0,15,0,0,0	0	0,0,0,12,0,0,0
38	3,9,9,9,1,9,9	7,0,0,0,2,0,0	0,0,0,0,1,0,0	15,0,0,0,15,0,0	0	-12,0,0,0,12,0,0
39	9,3,9,9,9,1,9	0,7,0,0,0,2,0	0,0,0,0,0,1,0	0,15,0,0,0,15,0	0	0,-12,0,0,0,12,0
40	9,9,3,9,9,9,1	0,0,7,0,0,0,2	0,0,0,0,0,0,1	0,0,15,0,0,0,15	0	0,0,-12,0,0,0,12
41	9,9,9,3,9,9,9	0,0,0,7,0,0,0	0,0,0,0,0,0,0	0,0,0,15,0,0,0	0	0,0,0,-12,0,0,0
42	9,9,9,9,3,9,9	0,0,0,0,7,0,0	0,0,0,0,0,0,0	0,0,0,0,15,0,0	0	0,0,0,0,-12,0,0
43	9,9,9,9,9,3,9	0,0,0,0,0,7,0	0,0,0,0,0,0,0	0,0,0,0,0,15,0	0	0,0,0,0,0,-12,0
44	9,9,9,9,9,9,3	0,0,0,0,0,0,7	0,0,0,0,0,0,1	0,0,0,0,0,0,15	0	0,0,0,0,0,0,-12
45	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
46	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
47	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
48	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
49	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
50	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
51	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
52	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
53	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
54	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
55	9,9,9,9,9,9,9	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0,0,0,0,0,0,0	0	0,0,0,0,0,0,0
56	1,9,9,9,9,9,9	2,0,0,0,0,0,0	0,0,0,0,0,0,0	19,0,0,0,0,0,0	0	-13,0,0,0,0,0,0
57	9,1,9,9,9,9,9	0,2,0,0,0,0,0	0,1,0,0,0,0,0	0,19,0,0,0,0,0	0	0,-13,0,0,0,0,0
58	9,9,1,9,9,9,9	0,0,2,0,0,0,0	0,0,1,0,0,0,0	0,0,19,0,0,0,0	0	0,0,-13,0,0,0,0
59	9,9,9,1,9,9,9	0,0,0,2,0,0,0	0,0,0,1,0,0,0	0,0,0,19,0,0,0	0	0,0,0,-13,0,0,0
60	9,9,9,9,1,9,9	0,0,0,0,2,0,0	0,0,0,0,1,0,0	0,0,0,0,19,0,0	0	0,0,0,0,-13,0,0
61	9,9,9,9,9,1,9	0,0,0,0,0,2,0	0,0,0,0,0,1,0	0,0,0,0,0,19,0	0	0,0,0,0,0,-13,0
62	9,9,9,9,9,9,1	0,0,0,0,0,0,2	0,0,0,0,0,0,1	0,0,0,0,0,0,19	0	0,0,0,0,0,0,-13

Model Output (Odd Pipe)

 TEST CASE 3: DATA HAZARDS - WITH STALLS (ODD PIPE)

SystemC 2.2.0 --- Oct 10 2009 07:49:18
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Packaged for MacOS by Logic Poet: <http://www.logicpoet.com>

ODD PIPE PRINTOUT:

Clk	Unit Id	Stage Ready	Register Write	Result Destination	PC	Result
<INSTRUCTION MISS>						
1	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
2	9,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
3	9,9,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
4	9,9,9,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
5	9,9,9,9,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
6	9,9,9,9,9,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
7	9,9,9,9,9,9,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
8	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
9	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
10	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
11	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
12	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
13	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
<INSTRUCTION BLOCK WRITTEN TO CACHE>						
14	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
15	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
16	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
17	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
18	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
19	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
20	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
21	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
22	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
23	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
24	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
25	7,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
26	7,7,9,9,9,9,9,9	6,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	17,0,0,0,0,0,0,0	-1	3,0,0,0,0,0,0,0
27	9,7,7,9,9,9,9,9	0,6,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,17,0,0,0,0,0,0	-1	0,3,0,0,0,0,0,0
28	9,9,7,7,9,9,9,9	0,0,6,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,17,0,0,0,0,0	-1	0,0,3,0,0,0,0,0
29	9,9,9,7,7,9,9,9	0,0,0,6,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,17,0,0,0,0	-1	0,0,0,3,0,0,0,0
30	9,9,9,9,7,7,9,9	0,0,0,0,6,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,17,0,0,0	-1	0,0,0,0,3,0,0,0
31	9,9,9,9,9,7,7,9	0,0,0,0,0,6,0,0	0,0,0,0,0,1,0,0	0,0,0,0,0,17,0,0	-1	0,0,0,0,0,3,0,0
32	9,9,9,9,9,9,7,9	0,0,0,0,0,0,6,0	0,0,0,0,0,0,1,0	0,0,0,0,0,0,17,0	-1	0,0,0,0,0,0,3,0
33	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
34	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
35	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
36	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
37	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
38	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
39	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
40	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
41	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
42	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
43	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
44	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
45	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
46	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
47	7,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	-1	0,0,0,0,0,0,0,0
48	7,7,9,9,9,9,9,9	6,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	18,0,0,0,0,0,0,0	-1	4294967284,0,0,0,0,0,0,0
49	9,7,7,9,9,9,9,9	0,6,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,18,0,0,0,0,0,0	-1	0,4294967284,0,0,0,0,0,0,0
50	9,9,7,7,9,9,9,9	0,0,6,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,18,0,0,0,0,0	-1	0,0,4294967284,0,0,0,0,0,0,0
51	9,9,9,7,7,9,9,9	0,0,0,6,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,18,0,0,0,0	-1	0,0,0,4294967284,0,0,0,0,0,0,0
52	9,9,9,9,7,7,9,9	0,0,0,0,6,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,18,0,0,0	-1	0,0,0,0,4294967284,0,0,0,0,0,0,0
53	9,9,9,9,9,7,7,9	0,0,0,0,0,6,0,0	0,0,0,0,0,1,0,0	0,0,0,0,0,18,0,0	-1	0,0,0,0,0,4294967284,0,0,0,0,0,0,0
54	9,9,9,9,9,9,7,9	0,0,0,0,0,0,6,0	0,0,0,0,0,0,1,0	0,0,0,0,0,0,18,0	-1	0,0,0,0,0,0,4294967284,0,0,0,0,0,0,0

4.6 Test Case 4: Control Hazards

Objectives

- Verify branch taken/untaken cases
- Verify pipe flushing

Test Program

```
shlqby 15,13,1
shlqby 16,13,1
shlqby 17,13,1
shlqby 18,13,1
a 19,4,5
stqa 19,99
brnz 19,9
a 20,1,5
stqa 20,99
a 21,0,5
shlqby 22,13,2
a 23,0,5
shlqby 24,13,2
a 25,0,5
shlqby 26,13,2
lqa 27,99
brz 27,-1
shlqby 28,13,2
a 29,6,5
a 30,6,5
shlqby 31,13,2
halt
```

Expected Calculation Results

```
Reg[15] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[16] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[17] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[18] = shiftLeftBytes(Reg[13],1) = 256 //ODD
Reg[19] = Reg[4]+Reg[5] = 10+(-1) = 9 //EVEN
LS[99] = Reg[19] = 9 //ODD
BranchIf(Reg[19]!=0) is true, PC=PC+36=60 //ODD
Reg[27] = LS[99] = 9 //ODD
BranchIf(Reg[27]==0) is false PC=PC+4=68 //ODD
Reg[28] = shiftLeftBytes(Reg[13],2) = 65536 //ODD
Reg[29] = Reg[6]+Reg[5] = 299792457 //EVEN
Reg[30] = Reg[6]+Reg[5] = 299792457 //EVEN
Reg[31] = shiftLeftBytes(Reg[13],2) = 65536 //ODD
```

Expected Timing Results (Even Pipe)

```
[clock 01] Instruction Miss (Block 0)
[clock 20] "A" Instruction Issue (Appears in EvenPipe on clock 23)
[clock 33] OddPipe broadcasts flush signal and new PC (a 20,1,5 flushed)
[clock 46] "A" Instruction Issue (Appears in EvenPipe on clock 49)
```

[clock 47] "A" Instruction Issue (Appears in EvenPipe on clock 50)

Expected Timing Results (Odd Pipe)

[clock 01] Instruction Miss (Block 0)
[clock 16] "SHLQBY" Instruction Issue (Appears in OddPipe on clock 19)
[clock 17] "SHLQBY" Instruction Issue (Appears in OddPipe on clock 20)
[clock 18] "SHLQBY" Instruction Issue (Appears in OddPipe on clock 21)
[clock 19] "SHLQBY" Instruction Issue (Appears in OddPipe on clock 22)
[clock 24] "STQA" Instruction Issue (Appears in OddPipe on clock 27)
[clock 27] "BRNZ" Instruction Issue (Condition True)
[clock 30] "BRNZ" Appears in OddPipe stage 1
[clock 33] OddPipe broadcasts flush signal and new PC
[clock 36] "LQA" Instruction Issue (Appears in OddPipe on clock 39)
[clock 44] "BRZ" Instruction Issue (Condition False)
[clock 45] "SHLQBY" Instruction Issue (Appears in OddPipe on clock 48)
[clock 47] "SHLQBY" Instruction Issue (Appears in OddPipe on clock 50)

Model Output (Even Pipe)

TEST CASE 4: CONTROL HAZARDS (EVEN PIPE)

SystemC 2.2.0 --- Oct 10 2009 07:49:18
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EVEN PIPE PRINTOUT:

Clk	Unit Id	Stage Ready	Register Write	Result Destination	Fl	Result
<INSTRUCTION MISS>						
1	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
2	9,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
3	9,9,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
4	9,9,9,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
5	9,9,9,9,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
6	9,9,9,9,9,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
7	9,9,9,9,9,9,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
8	9,9,9,9,9,9,9,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
9	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
10	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
11	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
12	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
13	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
<INSTRUCTION BLOCK WRITTEN TO CACHE>						
14	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
15	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
16	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
17	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
18	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
19	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
20	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
21	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
22	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
23	1,9,9,9,9,9,9,9	2,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	19,0,0,0,0,0,0,0	0	9,0,0,0,0,0,0,0
24	9,1,9,9,9,9,9,9	0,2,0,0,0,0,0,0	0,1,0,0,0,0,0,0	0,19,0,0,0,0,0,0	0	0,9,0,0,0,0,0,0
25	9,9,1,9,9,9,9,9	0,0,2,0,0,0,0,0	0,0,1,0,0,0,0,0	0,0,19,0,0,0,0,0	0	0,0,9,0,0,0,0,0
26	9,9,9,1,9,9,9,9	0,0,0,2,0,0,0,0	0,0,0,1,0,0,0,0	0,0,0,19,0,0,0,0	0	0,0,0,9,0,0,0,0
27	9,9,9,9,1,9,9,9	0,0,0,0,2,0,0,0	0,0,0,0,1,0,0,0	0,0,0,0,19,0,0,0	0	0,0,0,0,9,0,0,0
28	9,9,9,9,9,1,9,9	0,0,0,0,0,2,0,0	0,0,0,0,0,1,0,0	0,0,0,0,0,19,0,0	0	0,0,0,0,0,9,0,0
29	9,9,9,9,9,9,1,9	0,0,0,0,0,0,2,0	0,0,0,0,0,0,1,0	0,0,0,0,0,0,19,0	0	0,0,0,0,0,0,9,0
30	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
31	1,9,9,9,9,9,9,9	2,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	20,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
32	9,1,9,9,9,9,9,9	0,2,0,0,0,0,0,0	0,1,0,0,0,0,0,0	0,20,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
<BRANCH: PC=60>						
33	9,9,1,9,9,9,9,9	0,0,2,0,0,0,0,0	0,0,1,0,0,0,0,0	0,0,20,0,0,0,0,0	3	0,0,0,0,0,0,0,0
34	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
35	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
36	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0
37	9,9,9,9,9,9,9,9	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0,0,0,0,0,0,0,0	0	0,0,0,0,0,0,0,0

43	9,9,9,9,7,9,9,	0,0,0,0,6,0,0,	0,0,0,0,0,0,0,	0, 0, 0, 0,27, 0, 0,	-1	0,0,0,0,9,0,0,
44	9,9,9,9,9,7,9,	0,0,0,0,0,6,0,	0,0,0,0,0,1,0,	0, 0, 0, 0, 0,27, 0,	-1	0,0,0,0,0,9,0,
45	9,9,9,9,9,9,7,	0,0,0,0,0,0,6,	0,0,0,0,0,0,1,	0, 0, 0, 0, 0, 0,27,	-1	0,0,0,0,0,0,9,
46	9,9,9,9,9,9,9,	0,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0, 0, 0, 0, 0, 0, 0,	-1	0,0,0,0,0,0,0,
47	8,9,9,9,9,9,9,	3,0,0,0,0,0,0,	0,0,0,0,0,0,0,	0, 0, 0, 0, 0, 0, 0,	-1	0,0,0,0,0,0,0,
48	6,8,9,9,9,9,9,	4,3,0,0,0,0,0,	0,0,0,0,0,0,0,	28, 0, 0, 0, 0, 0, 0,	-1	65536,0,0,0,0,0,
49	9,6,8,9,9,9,9,	0,4,3,0,0,0,0,	0,0,0,0,0,0,0,	0,28, 0, 0, 0, 0, 0,	-1	0,65536,0,0,0,0,
50	6,9,6,8,9,9,9,	4,0,4,3,0,0,0,	0,0,0,0,0,0,0,	31, 0,28, 0, 0, 0, 0,	-1	65536,0,65536,0,0,0,
51	9,6,9,6,8,9,9,	0,4,0,4,3,0,0,	0,0,0,1,0,0,0,	0,31, 0,28, 0, 0, 0,	-1	0,65536,0,65536,0,0,
52	9,9,6,9,6,8,9,	0,0,4,0,4,3,0,	0,0,0,0,1,0,0,	0, 0,31, 0,28, 0, 0,	-1	0,0,65536,0,65536,0,
53	9,9,9,6,9,6,8,	0,0,0,4,0,4,3,	0,0,0,1,0,1,0,	0, 0, 0,31, 0,28, 0,	-1	0,0,0,65536,0,65536,
54	9,9,9,9,6,9,6,	0,0,0,0,4,0,4,	0,0,0,0,1,0,1,	0, 0, 0, 0,31, 0,28,	-1	0,0,0,0,65536,0,65536,
55	9,9,9,9,9,6,9,	0,0,0,0,0,4,0,	0,0,0,0,0,1,0,	0, 0, 0, 0, 0,31, 0,	-1	0,0,0,0,0,65536,0,
56	9,9,9,9,9,9,6,	0,0,0,0,0,0,4,	0,0,0,0,0,0,1,	0, 0, 0, 0, 0, 0,31,	-1	0,0,0,0,0,0,65536,

4.7 Test Case 5: Matrix Multiply

Objectives

- Compute a 2-by-2 matrix multiply

Calculation

Matrix Multiply (MATLAB):

```
A = [exp(1),sqrt(2);sqrt(2),exp(1)]
A =
    2.7183    1.4142
    1.4142    2.7183
```

```
B = [sqrt(2),-1/4;-1/4,sqrt(2)]
B =
    1.4142   -0.2500
   -0.2500    1.4142
```

```
C = A*B
C =
    3.4907    1.3204
    1.3204    3.4907
```

Algorithm

```
Let Matrix A =
      a  c
      b  d
```

```
Let Matrix B =
      e  g
      f  h
```

Step 1: Compute intermediate products

```
p1 = [c,c] * [f,h] = [c*f,c*h]
p2 = [d,d] * [f,h] = [d*f,d*h]
```

Step 2: Compute Matrix Multiply

```
C(1,:) = [a,a] * [e,g] + p1 = [a*e + c*f, a*g + c*h]
C(2,:) = [b,b] * [e,g] + p2 = [b*e + d*f, b*g + d*h]
```

where C(i,:) is the ith row matrix C.

Test Program

```

a 15,1,3
shlqby 16,9,15
a 17,16,10
rotqby 18,17,15
shlqby 19,10,15
a 20,19,11
rotqby 21,20,15
shlqby 22,17,15
rotqby 23,22,15
a 24,22,23
dfm 25,24,21
shlqby 26,18,15
rotqby 27,26,15
a 28,26,27
dfm 29,28,21
rotqby 30,17,15
shlqby 31,30,15
rotqby 32,31,15
a 33,31,32
dfma 25,33,20
rotqby 34,18,15
shlqby 35,34,15
rotqby 36,35,15
a 37,35,36
dfma 29,37,20
halt

```

Expected Calculation Results

```
//Form Matrices
```

```
Reg[15] = Reg[1]+Reg[3] = 1+7 = 8
```

```
Reg[16] = shiftLeftQuadword(Reg[9] by Reg[15] bytes) = [2.71 <double>, 0 <uint32>]
```

```
Reg[17] = Reg[16]+Reg[10] = [2.71 <double>, 1.41 <double>]
```

```
Reg[18] = rotateQuadword(Reg[17] by Reg[15] bytes) = [1.41 <double>, 2.71 <double>]
```

```
Reg[19] = shiftLeftQuadword(Reg[10] by Reg[15] bytes) = [1.41 <double>, 0 <uint32>]
```

```
Reg[20] = Reg[19]+Reg[11] = [1.41 <double>, -0.25 <double>]
```

```
Reg[21] = rotateQuadword(Reg[20] by Reg[15] bytes) = [-0.25 <double>, 1.41 <double>]
```

```
//Reg[17] = A(1,:)
//Reg[18] = A(2,:)
//Reg[20] = B(1,:)
//Reg[21] = B(2,:)
```

```
//Compute Intermediate Products (Only Operating on Matrix Registers)
```

```
Reg[22] = shiftLeftQuadword(Reg[17] by Reg[15] bytes) = [1.41 <double>, 0 <uint32>]
```

```
Reg[23] = rotateQuadword(Reg[22] by Reg[15] bytes) = [0 <uint32>, 1.41 <double>]
```

```

Reg[24] = Reg[22]+Reg[23] = [1.41 <double>, 1.41 <double>]
Reg[25] = Reg[24]*Reg[21] = [-0.3536 <double>, 1.9940 <double>]
Reg[26] = shiftLeftQuadword(Reg[18] by Reg[15] bytes) = [2.71 <double>, 0 <uint32>]
Reg[27] = rotateQuadword(Reg[26] by Reg[15] bytes) = [0 <uint32>, 2.71 <double>]
Reg[28] = Reg[26]+Reg[27] = [2.71 <double>, 2.71 <double>]
Reg[29] = Reg[28]*Reg[21] = [-0.6796 <double>, 3.8328 <double>]

//Reg[25] = p1
//Reg[29] = p2

//Compute Matrix Product (Not Assuming Symmetric Matrices)
Reg[30] = rotateQuadword(Reg[17] by Reg[15] bytes) = [1.41 <double>, 2.71 <double>]
Reg[31] = shiftLeftQuadword(Reg[30] by Reg[15] bytes) = [2.71 <double>, 0 <uint32>]
Reg[32] = rotateQuadword(Reg[31] by Reg[15] bytes) = [0 <uint32>, 2.71 <double>]
Reg[33] = Reg[31]+Reg[32] = [2.71 <double>, 2.71 <double>]
Reg[25] = Reg[33]*Reg[20]+Reg[25] = [3.4907 <double>, 1.3204 <double>]
Reg[34] = rotateQuadword(Reg[18] by Reg[15] bytes) = [2.71 <double>, 1.41 <double>]
Reg[35] = shiftLeftQuadword(Reg[34] by Reg[15] bytes) = [1.41 <double>, 0 <uint32>]
Reg[36] = rotateQuadword(Reg[35] by Reg[15] bytes) = [0 <uint32>, 1.41 <double>]
Reg[37] = Reg[35]+Reg[36] = [1.41 <double>, 1.41 <double>]
Reg[29] = Reg[37]*Reg[20]+Reg[29] = [1.3204 <double>, 3.4907 <double>]

//C(1,:) = Reg[25] = [4615042726053923435,4608625505169953866] = [3.4907,1.3204]
//C(2,:) = Reg[29] = [4608625505169953869,4615042726053923434] = [1.3204,3.4907]

```