Author: Asher Voris
Description: Details of Proof of Concept and Proof of Concept Test Plan

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13/05/2021	Initial Creation

Proof of Concept Description: The proof of concept for the EBC will be a simple breakout board featuring all components except the FPGA. The power system will be present, but will be isolated and not connected to the rest of the system. A test load will be present. The temperature sensor, display, and capacitive button will be present on the system. All ports will be broken out using dupont cables. These dupont cables will be used to connect to the FPGA present on the ICE40UL1K development kit. In this manner the system can be fully developed and tested without the risk of not routing the FPGA properly. Additionally, the size of the PCB can be increased to the maximum permitted by the PCB fabrication house for the minimum cost, this will eliminate the need for compact routing in the initial design.

Test Writer: Asher Voris			
Test Case Name:	**Integration Test: Proof of Concept Power System Test**	Test ID#:	POC_TEST_1
Description:	This test verifies that the power system of the EBC will output sufficient voltage and current in both a brightly lit office environment and outdoors on a bright day.	Type:	Whitebox: X Blackbox:
Tester Information:			
Name of Tester:		Date:	
Hardware Ver:		Time:	
Setup:	-Have access to a bright office environment of at least [TBD] lux -Have access to a bright day of at least [TBD] lux -Connect a voltmeter to the output points designated on the PCB -Have access to a ammeter -Expose the system to the bright office environment		

Step	Action	Expected Result	[Pass]	[Fail]	[N/A]	Comments
1.	Connect jumper one (J1), the five mA load, using the ammeter.	-1.8V is measured on the 1.8V output using the voltmeter -2.5V is measured on the 2.5V output the voltmeter -3.3V is measured on the 3.3V output the voltmeter -5mA is measured on the ammeter				
2.	Connect jumper two (J2), the 10 mA load, using the ammeter	-1.8V is measured on the 1.8V output using the voltmeter -2.5V is measured on the 2.5V output the voltmeter -3.3V is measured on the 3.3V output the voltmeter -10mA is measured on the ammeter				
3.	Connect jumper three (J3), the 15 mA load, using	-1.8V is measured on the 1.8V output using the voltmeter -2.5V is measured on the 2.5V				

	the ammeter	output the voltmeter -3.3V is measured on the 3.3V output the voltmeter -15mA is measured on the ammeter				
4.	Connect jumper four (J4), the 20 mA load, using the ammeter	-1.8V is measured on the 1.8V output using the voltmeter -2.5V is measured on the 2.5V output the voltmeter -3.3V is measured on the 3.3V output the voltmeter -20mA is measured on the ammeter				
5.	Connect jumper five (J5), the 25 mA load, using the ammeter	-1.8V is measured on the 1.8V output using the voltmeter -2.5V is measured on the 2.5V output the voltmeter -3.3V is measured on the 3.3V output the voltmeter -25mA is measured on the ammeter				Failure is acceptable at this point, although operating at this load is desirable.
6.	Repeat steps 1-5 for the outdoor environment and verify the results.	Results are acceptable for the repeated steps.				

Test Writer: Asher Voris			
Test Case Name:	**Integration Test: Proof of Concept Temperature Sensor Test**	Test ID#:	POC_TEST_2
Description:	This test verifies the temperature sensor output is correct and is properly transmitted across the I2C bus to core FPGA logic.	Type:	Whitebox: X Blackbox:
Tester Information:			
Name of Tester:		Date:	
Hardware Ver:		Time:	
Setup:	- Have access to a thermometer, a calibrated one is preferable (however, since this system is not accuracy dependent anything that provides an accuracy of +-2 degrees fahrenheit is fine). - Have air dusting can present. - Have a logic analyzer connected to the I2C bus between the sensor and the FPGA - Compile and Upload the HDL code		

Step	Action	Expected Result	[Pass]	[Fail]	[N/A]	Comments
1.	Execute the HDL code on the system.	The configuration communications should be observed				
2.	Continue observing the system using the logic analyzer.	A temperature is transmitted across the I2C bus that is within 2 degrees of the temperature on the thermometer. (This value will need to be converted to the parsed value as per the data sheet of the sensor.)				
3.	Tester places finger on the sensor and on the other thermometer.	A temperature is transmitted across the I2C bus that is within 2 degrees of the temperature on the thermometer.				
4.	Tester turns the can of air duster upside down and	A temperature is transmitted across the I2C bus that is within 2 degrees of the temperature on				

	sprays the sensor and thermometer until they are lightly coated with ice.	the thermometer.				

Test Writer: Asher Voris			
Test Case Name:	**Integration Test: Proof of Concept Display Test**	Test ID#:	POC_TEST_3
Description:	This test verifies that the FPGA display driver logic functions correctly.	Type:	Whitebox: X Blackbox:
Tester Information:			
Name of Tester:		Date:	
Hardware Ver:		Time:	
Setup:	- Compile and Upload the HDL code - Connect an Oscilloscope to DTP1		

Step	Action	Expected Result	[Pass]	[Fail]	[N/A]	Comments
1.	Execute the HDL code on the system.	The system should blink all segments off and on at one second intervals				
2.	Observe the oscilloscope for several periods of the flashing.	The RMS voltage should be zero.				

Test Writer: Asher Voris			
Test Case Name:	**Integration Test: Proof of Concept User Interface Test**	Test ID#:	POC_TEST_4
Description:	This test verifies that the PCB button and FPGA touch detection logic function properly	Type:	Whitebox: Blackbox: X
Tester Information:			
Name of Tester:		Date:	
Hardware Ver:		Time:	
Setup:	- Compile and Upload the HDL code - Connect an oscilloscope to CTP1		

Step	Action	Expected Result	[Pass]	[Fail]	[N/A]	Comments
1.	Execute the HDL code on the system.	The oscilloscope shows 0 volts.				
2.	Tester touches the capacitive button	The oscilloscope logic level rises to the FPGA I/O logic level.				
3.	Tester Releases the capacitive button	The oscilloscope logic level falls back to 0 volts.				