Department of Computer Science and Engineering
Jahangirnagar University
Savar, Dhaka

Laboratory Report

CSE-406: VLSI Circuits Design Laboratory

Submitted by

Md. Ashick Areafin
Exam Roll: 160054
Class Roll: 2130
Session: 2015-16
4th year 1st Semester

Submitted to

Dr. Abu Sayed Mohammed Mustafizur Rahman
Professor
Department of Computer Science and Engineering
Jahangirnagar University

Experiment No:04
Experiment Name: Observation & Verification of Transfer Characteristics of CMOS INVERTER.

Objectives:

- Simulation of the inverter as a function of time
- To display transfer characteristics curve of CMOS inverter
- To verify the variation of transfer characteristics as a function of $\frac{\beta_n}{\beta_p}$ ratio
- Find the noise margins of a gate

Theory:

The CMOS inverter includes two transistors. One is a n-channel transistor, the other is a p-channel transistor. The device symbols are reported below. In order to build the inverter, the nMOS and pMOS gates are interconnected as well as the outputs as shown in Figure 1.

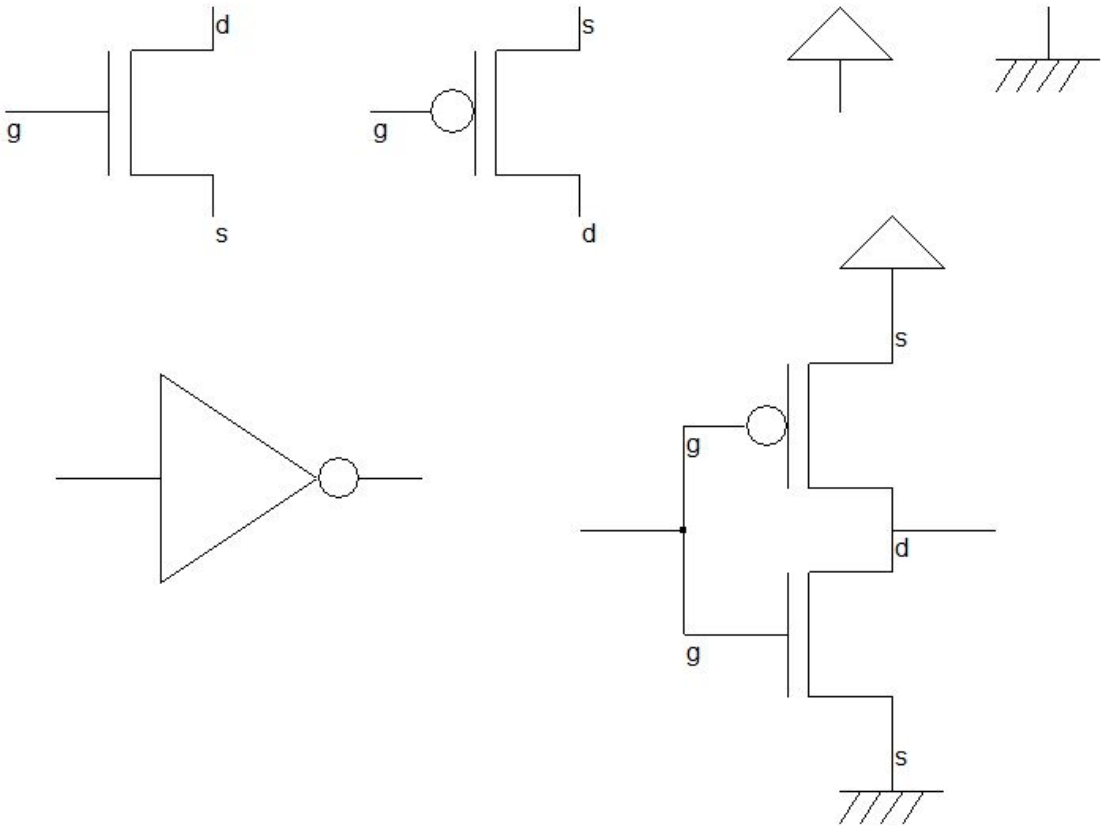

Figure 1: The schematic diagram of the CMOS inverter with one nMOS at the bottom and pMOS at the top

Procedure:

a) The simulation of CMOS inverter as a function of time

➢ Open the microwind window and check the selected boundary is 0.25 micrometer.

➢ Generate the nMOS and pMOS transistors for creating CMOS inverter with width and length ratio specified in table 1. In this experiment we will generate three inverters that we need for experimenting $\frac{\beta_n}{\beta_p}$ ratio effect. The layout diagram is shown in figure 2.

Table 1: Inverters width and length

Name	pMOS		nMOS		$\frac{\beta_n}{\beta_p}$
	Width(γ)	Length(γ)	Width(γ)	Length(γ)	
1st inverter	50	1	5	1	0.1
2nd inverter	5	1	5	1	1
3rd inverter	5	1	50	1	10

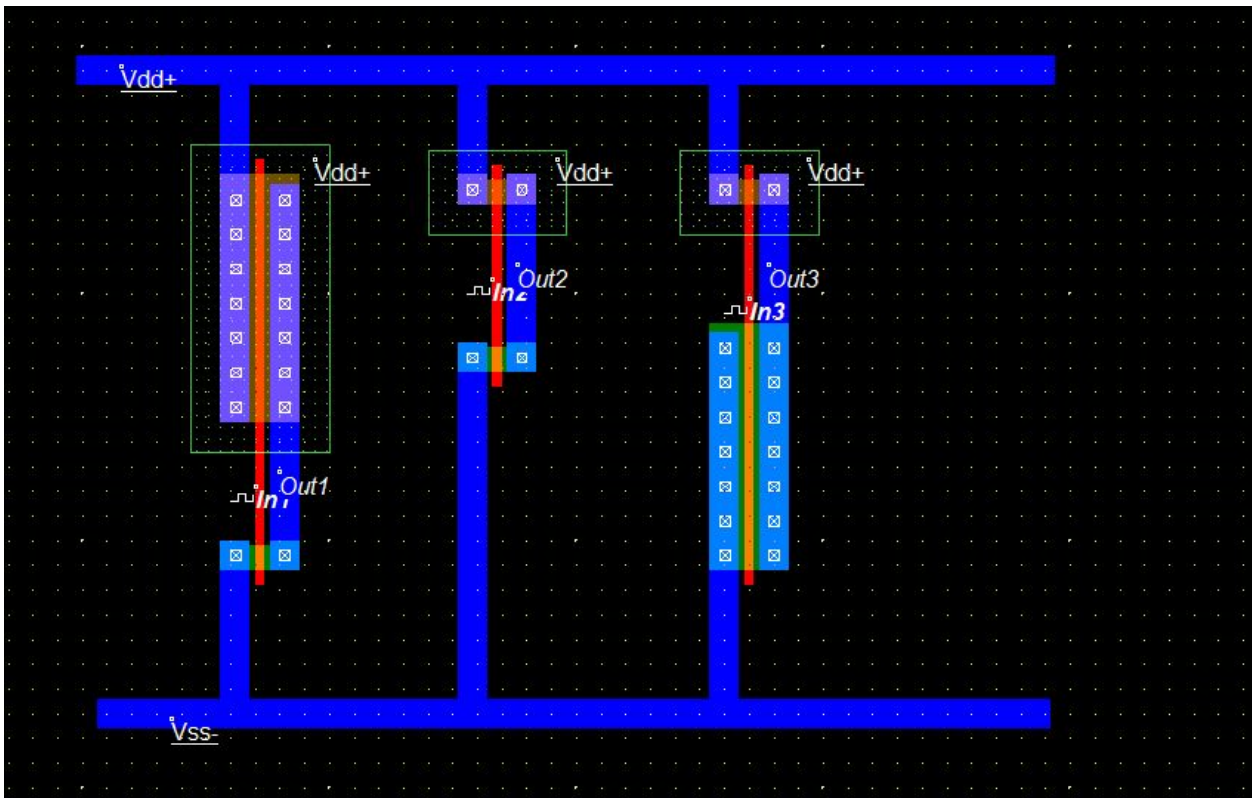

Figure 2: Layout diagram of CMOS inverters

➢ Run the simulation button to display the time diagram of the three CMOS inverters as shown in figure 3.

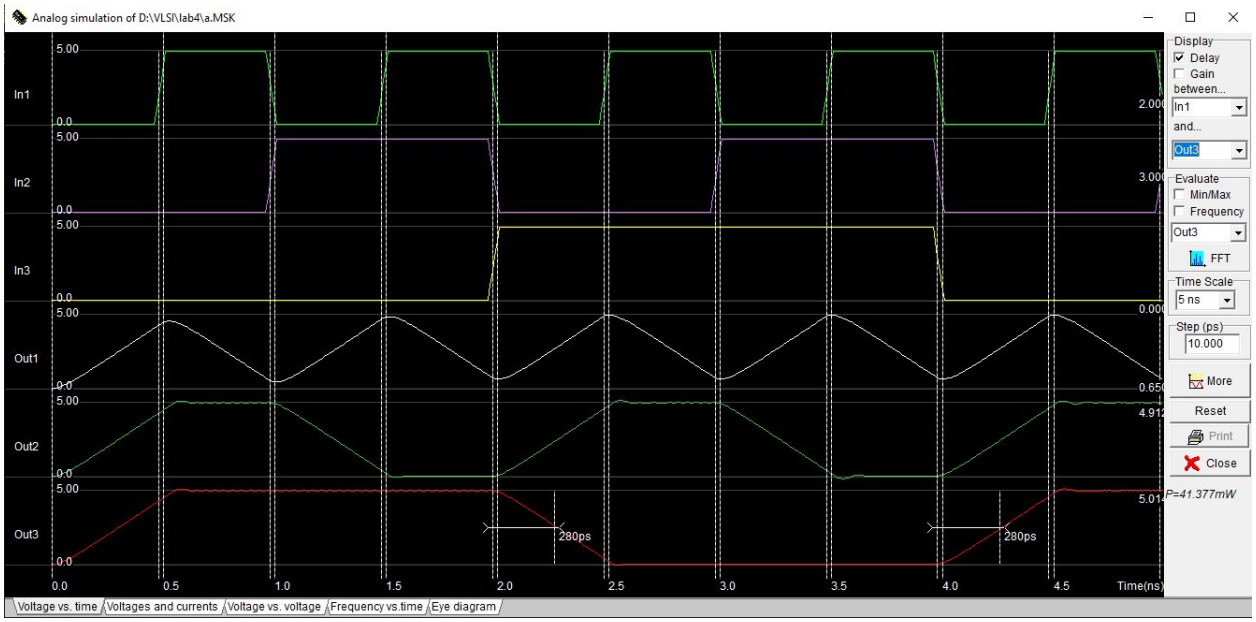

Figure 3:Timing diagram of the three CMOS inverters

b) Observe the transfer characteristics curve of CMOS inverter and ratio effects.

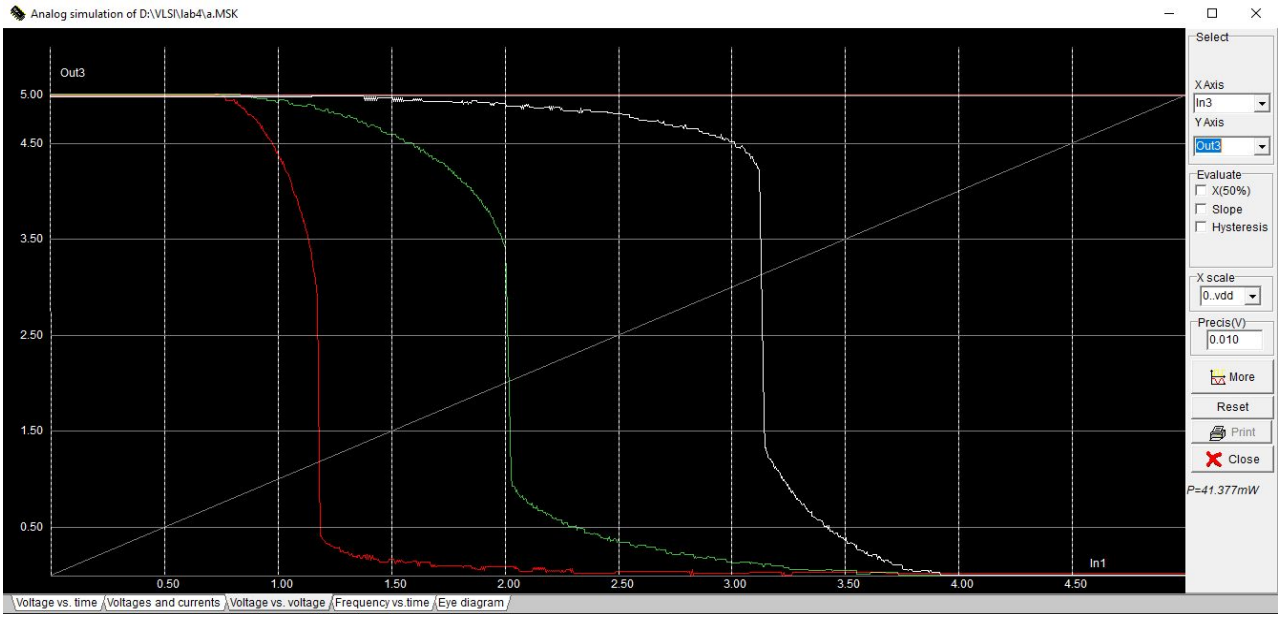

Figure 4: The transfer characteristics curves the three inverters

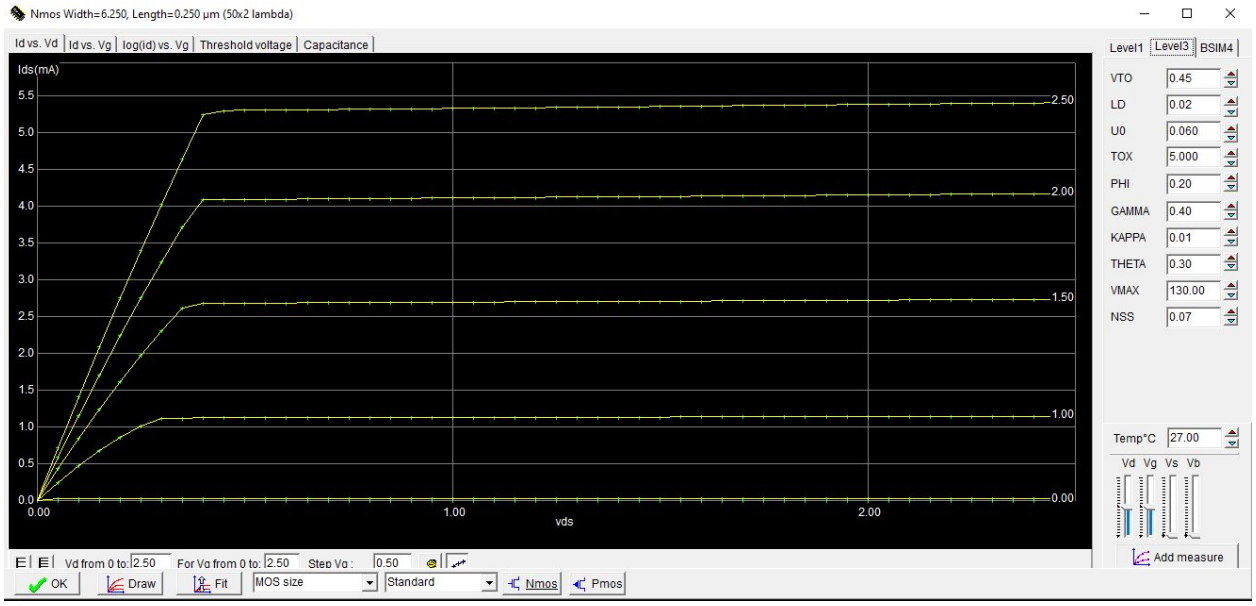

Figure 5: MOS Characteristics

Result:

The inverters are designed and the truth table is successfully verified. The required waveforms were obtained, observe and noted down using microwind2.