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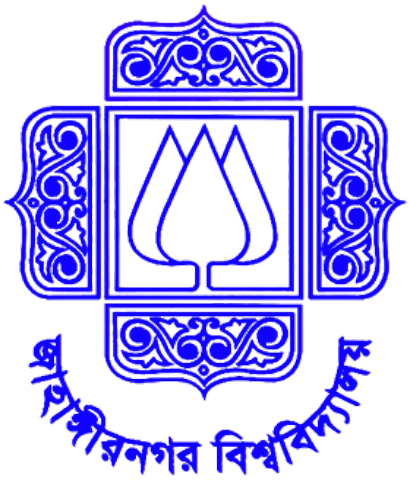

Laboratory Report

CSE-406: VLSI Circuits Design Laboratory

Submitted by

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Experiment No: 05
Experiment Name: Verification of nMOS and pMOS DC-Characteristics.

Objectives:

- To find the MOS model parameters for the transistors & then by paper and pencil manually calculate the DC characteristics of I_{Ds} current vs V_{GS} voltage using simple current equations for MOS model level 1 to determine the number of corresponding value pairs of (Ids,Vds) with the gate source voltage V_{GS} = a constant > V_{th}.
- Use circuit simulator of Microwind to do a DC simulation of the Ids current vs Vds voltage and the result of the two methods compared.
- Calculation of the threshold voltage.

Theory:

The nMOS transistor Ids current vs Vds voltage equations are as follows:
Cut-off mode: I_{Ds} = 0 when V_{GS}<0
Triod/Linear region: $I_{Ds} = K_n \{(V_{GS} - V_{Tn}) V_{DS} - \frac{1}{2} V_{DS}^2\}$ *when* $V_{DS} < V_{GS} - V_{Tn}$ .... (1)
In Level 1 SPICE model, $I_{Ds} = U_O \frac{\varepsilon_0 \varepsilon_{Sio2}}{TOX} \frac{W}{L} \{(V_{GS} - V_{Tn}) V_{DS} - \frac{1}{2} V_{DS}^2\}$
Saturation region: $I_{Ds} = \frac{1}{2} K_n \{(V_{GS} - V_{Tn})^2 (1 + \lambda V_{DS})\}$ *when* $V_{DS} > V_{GS} - V_{Tn}$ .... (2)
In Level 1 SPICE model, $I_{Ds} = \frac{1}{2} U_O \frac{\varepsilon_0 \varepsilon_{Sio2}}{TOX} \frac{W}{L} \{(V_{GS} - V_{Tn})^2\}$
When the channel modulation effect is neglected the drain current equation (2) can be simplified as, $I_{Ds} = \frac{1}{2} K_n \{(V_{GS} - V_{Tn})^2\}$ *when* $V_{DS} > V_{GS} - V_{Tn}$ .... (3)
The current gain factor K_n is constant with unit [A / V^2] This is depended on MOS transistor geometry,fabrication process parameters(elector mobility, μ_n and gate oxide capacitance C_{ox}).
The factor K_n can be calculated as $K_n = K_n' Wn/Ln$ where the process conductance parameter K_n' = $\mu_n C_{ox}$ [A /V^2]. The parameter Cox stands for gate oxide capacitance per unit area depend on gate oxide thickness t_{ox}. This can be expressed as Cox = $\varepsilon_{0x} / t_{ox}$.
The additional parameter of the I_{Ds} and V_{Ds} is the threshold voltage V_{th}.

Procedure:

1. Level 1 MOS model equations to calculate DC values for the drain-current I_{Ds} vs drain-source voltage V_{Ds}.

Table 1: VGS = +2.0V and Wn/Ln = 2

V_{Ds} (V)	0.5	1.0	1.5	2.0	2.5
$V_{DS} - (V_{GS} - V_{Tn})$	-1.05	-0.55	-0.05	0.45	0.95
	(1)	(1)	(1)	(2)	(2)
Manual Calculation I_{DS} (micro amp.)	547.56	884.52	1010.88	1011.933	1011.933

2. Use of "simulate>MOS characteristics" to generate the DC characteristics I_{Ds} vs V_{Ds} for the nMOS transistor in Microwind.

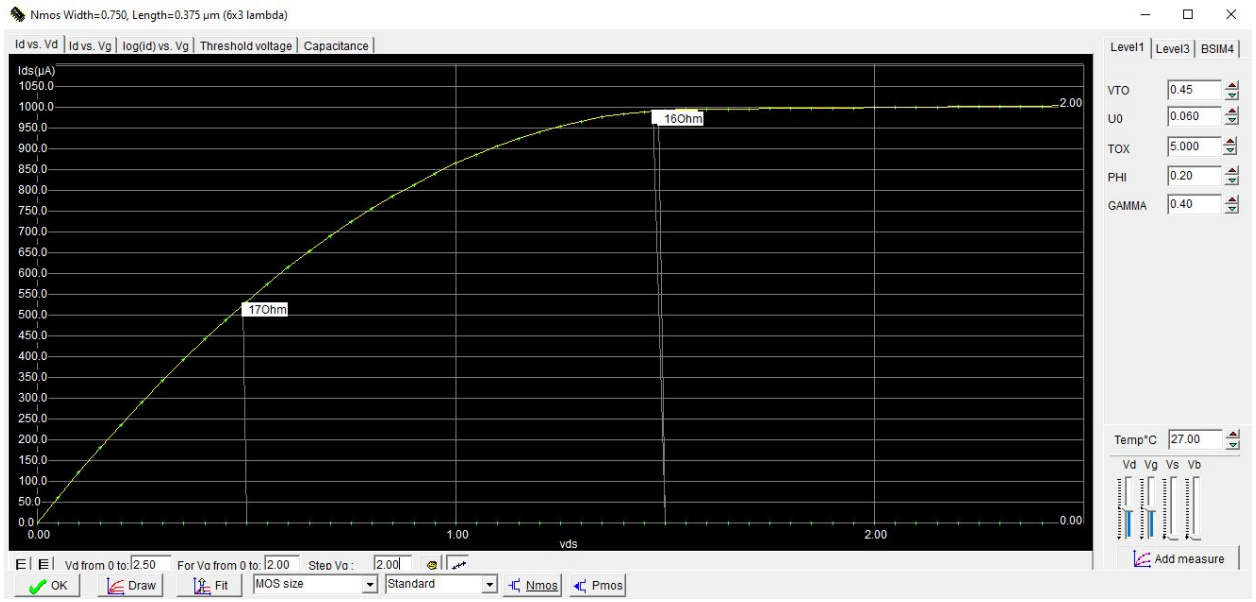

Figure 1: nMOS characteristics curve(simulated)

Result:

The lab objectives are successfully observed and verified with theoretical calculation.