Department of Computer Science and Engineering
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Laboratory Report

CSE-406: VLSI Circuits Design Laboratory

Submitted by

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Experiment No:03
Experiment Name: Layout Design of The following Logic Function, $Y = \overline{AB + CD}$.

Objectives:
The main objective of this experiment is to design the logic function using Microwind2 and verifying the result using different input patterns .

Introduction:
CMOS stands for complementary Metal-oxide Semiconductor.It is a logical combination of p-type MOS and n-type MOS.It Works as an inverter. The circuit shows the realization of CMOS NAND and CMOS NOR gate which consists of four pMOS and four nMOS gate.

Simulation Of The Logic Function:

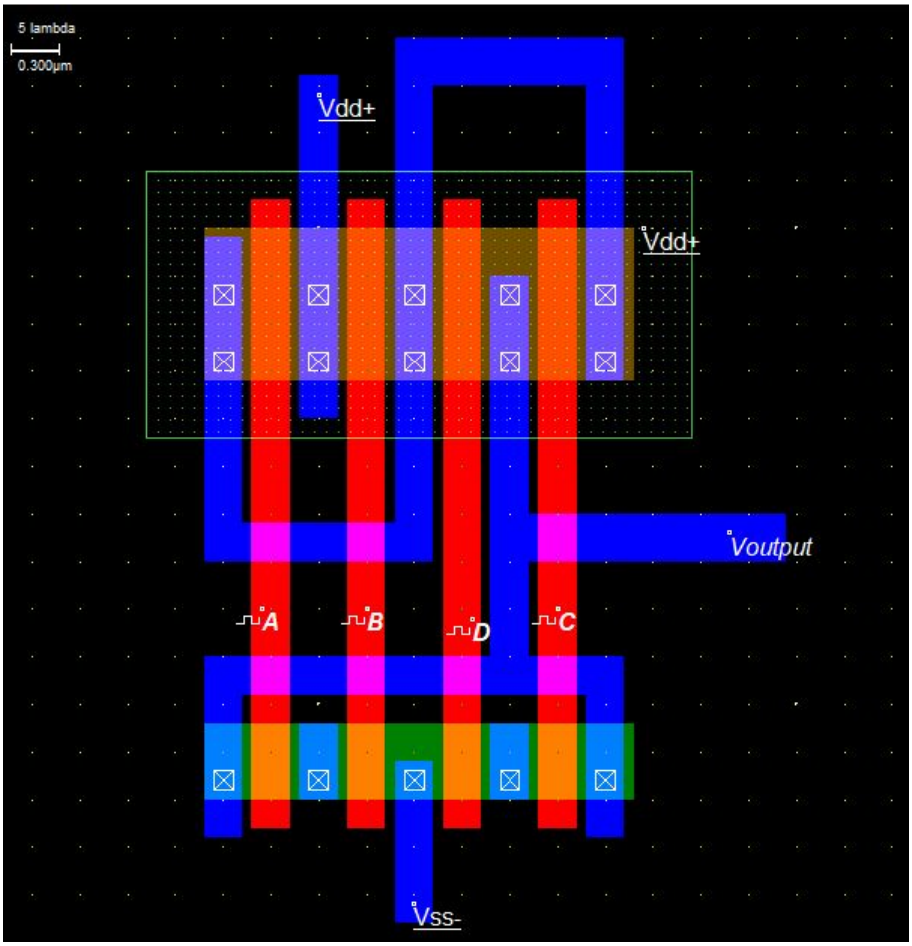

Figure 1: Stack Diagram of the logic Function

Caption: Truth Table for the logic Function

A	B	C	D	AB	CD	$AB + CD$	$\overline{AB + CD}$
0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	1
0	0	1	0	0	0	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	0	1
0	1	1	0	0	0	0	1
0	1	1	1	0	1	1	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	0	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	0
1	1	1	0	1	0	1	0
1	1	1	1	1	1	1	0

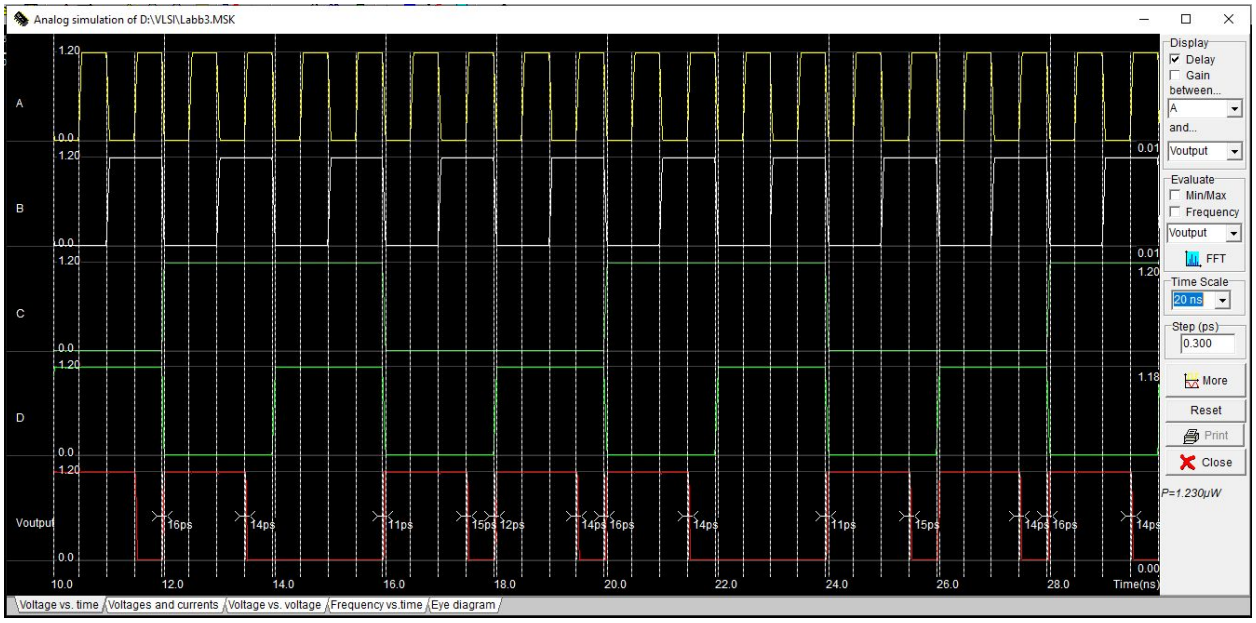

Figure 2: Timing Diagram for the logic Function