Address Decoding

- Decoding makes memory function at a unique section or partition of memory map.
- Without an address decoder, only one memory device can be connected to a MP, which make it virtually useless.
- **Why Decode Memory?**
- 2716(EPROM) has 11 address pin & MP has 20
- means that MP sends out a 20-bit memory address whenever it reads or writes data

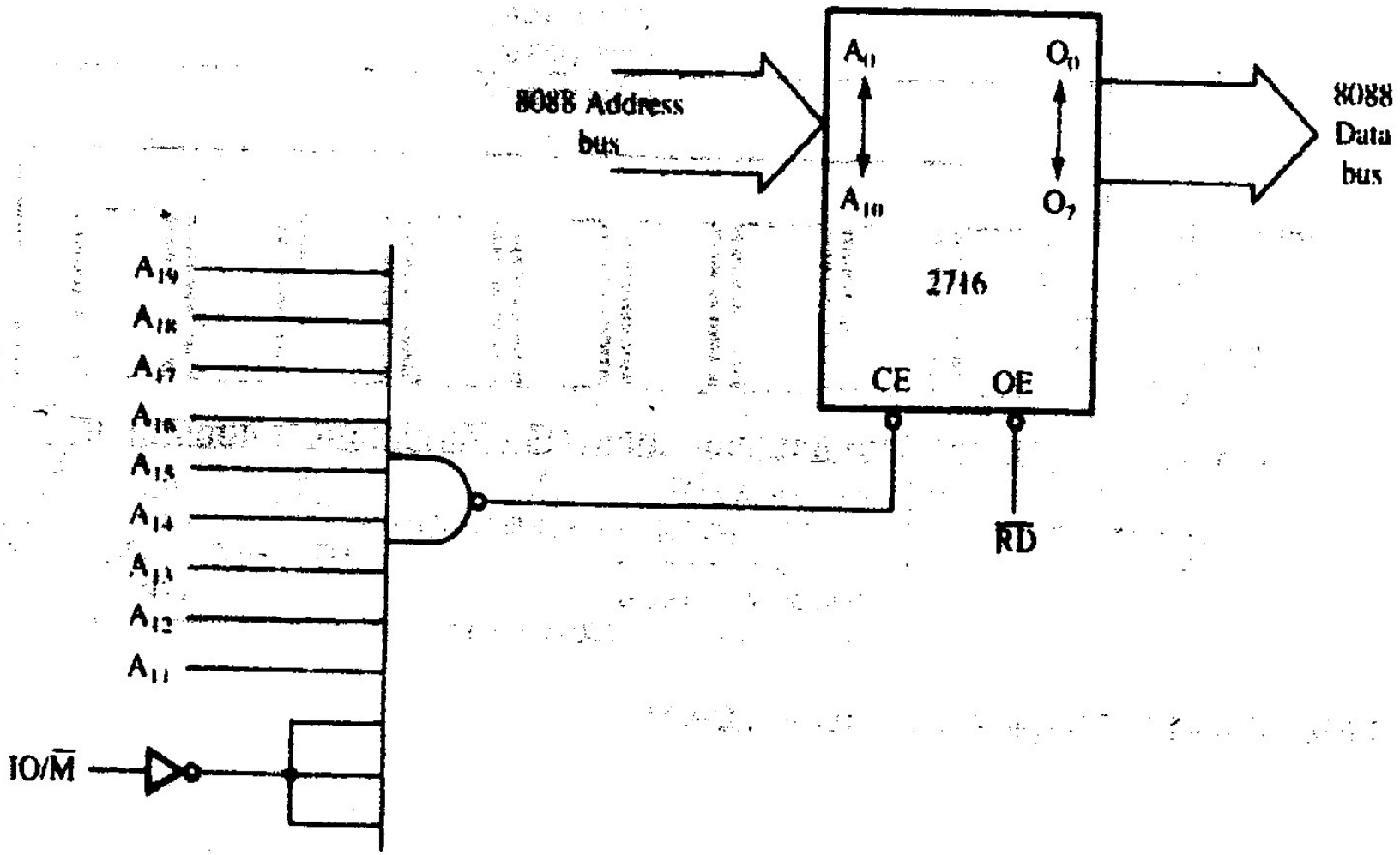
Continued

- Because EPROM has only 11 address pins, there is a mismatch that corrected
- If only 11 address pin are connected to memory, MP see only 2exp(11)=2KB of memory instead of 1MB that it “expects” the memory to contain
- Decoder corrects the mismatch by decoding address pins that do not connect to memory component.

Simple NAND Gate Decoder

- When 2K*8 RPROM is used, address connections A0-A10 of MP are connected to address inputs A0-A10 of EPROM
- Remaining 09 address pins (A19-A11) are connected to inputs of a NAND gate decoder
- **See fig 10-13, p-348,Brey**
- $\overline{CE}$=0, data will be read from EPROM only if $\overline{OE}$=0
- OE pin activated by MP, $\overline{RD}$ signal

Fig 10.13: A simple NAND gate decoder used to select a 2716 EPROM memory component for memory location FF800H-FFFFFH.



Continued

- If 20-bit address, decoded by NAND gate, leftmost 09 bits are 1 & rightmost 11 bits are don't care (X), actual address range of EPROM can be determined
- **Example:**2 KB EPROM decoded at memory location, FF800H~FFFFFH

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	1	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X

Lowest add=1111 1111 1000 0000 0000=FF800H
Highest add=1111 1111 1111 1111 1111=FFFFFH

3-to-8 Line Decoder

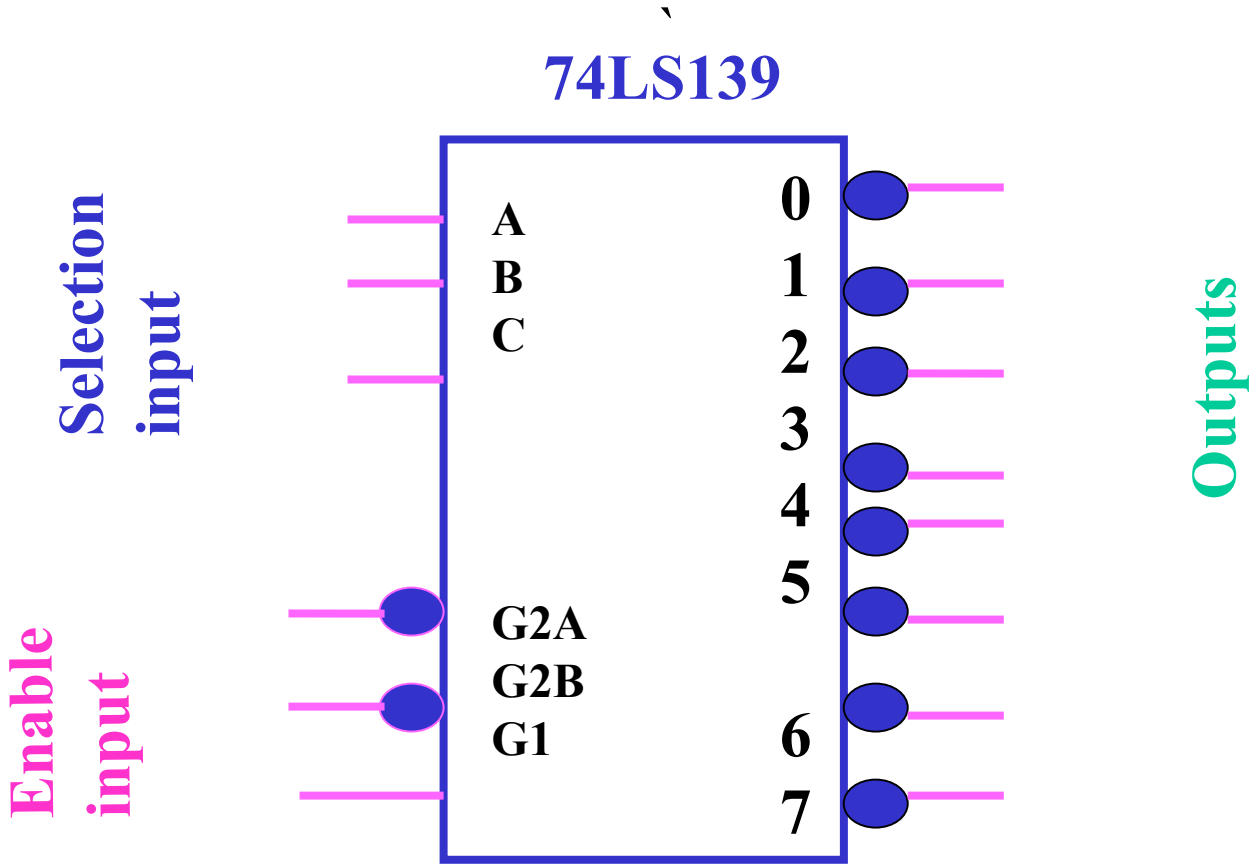


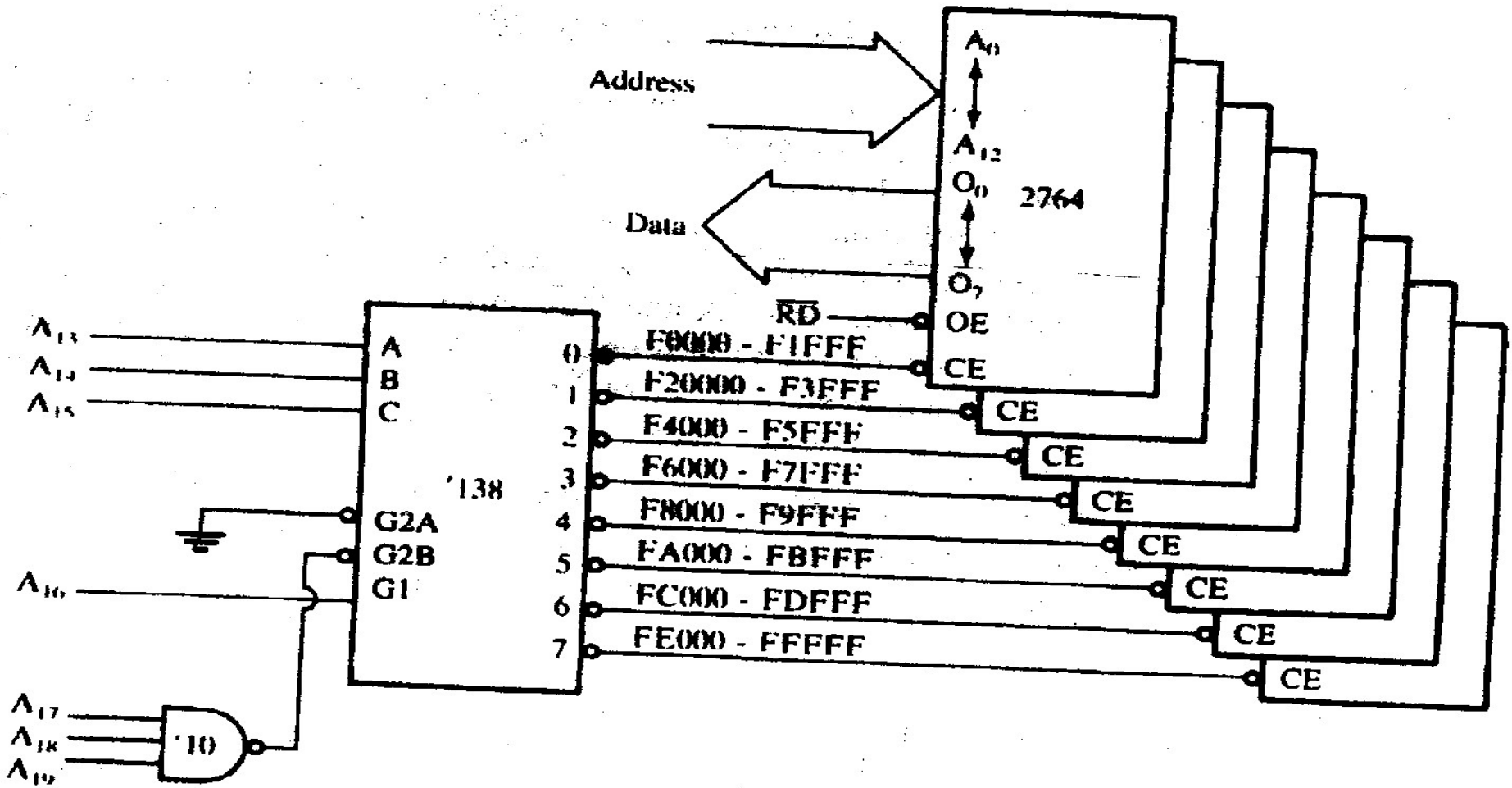
Fig 10.14: Function table for 3-8 line decoder

Inputs						Outputs							
Enable			Select										
$\overline{G2A}$	$\overline{G2B}$	G1	C	B	A	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

3-to-8 Line Decoder(74LS138)

- **see fig 10-14, p-349,Brey**
- for an output(O0-O7) to go low, 03 enable input ($\overline{G2A}$, $\overline{G2B}$, & G1) must be active
- to be active, $\overline{G2A}$= $\overline{G2B}$=0,& G1=1
- once 74LS138 is enabled, address input (C,B,A) select which output pin goes low.
- **see fig 10-15, p-350, Brey**
- address inputs (C,B,A) connect to MP address pin (A15,A14,A13), determines output pin low & select EPROM

Fig 10-15: Addresses selected in this ckt: F0000H-FFFFFH.



Example

01. Addresses range for entire decoder:

A19 A18 A17 A16	A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
1 1 1 1	X X X X X X X X X X X X X X X X

Lowest add=1111 0000 0000 0000 0000 =F0000H

Highest add=1111 1111 1111 1111 1111 =FFFFFH

Address Range= F0000H~FFFFFH = 64KB of memory

Continued

02. For output pin (0):

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	1	1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X
				C	B	A													

Lowest add=1111 0000 0000 0000 0000 = F0000H

Highest add = 1111 0001 1111 1111 1111 = F1FFFH

Continued

03. For output pin (1):

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	1	1	1	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X
				C	B	A													

Lowest add = 1111 0010 0000 0000 0000 = F2000H

Highest add = 1111 0011 1111 1111 1111 = F3FFFH

Problems

01. Design a NAND gate Decoder to select the memory for address range DF800H~DFFFFH.

02. Design a NAND gate Decoder to select the memory for address range 40000H~407FFH.

03.Design a 3-to-8 line Decoder to select the memory for address range 40000H~4FFFFH.