EC2.201-VLSI Design (Monsoon 2021)

Assignment 2

Q1. Design JK FF using SR FF.

Q2. Construct XY flipflop using JK flipflop and additional gates.

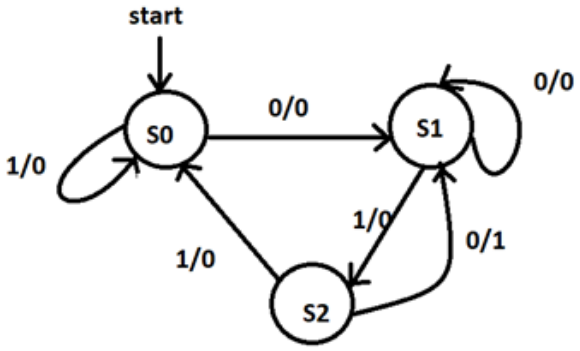
X	Y	Q^+
0	0	$\bar{Q}$
0	1	Q
1	0	0
1	1	1

Q3. Design a counter with following sequence using D flipflop

0,2,3,1,0

Q4. Draw state diagram for a sequence detector detecting the sequence 101.

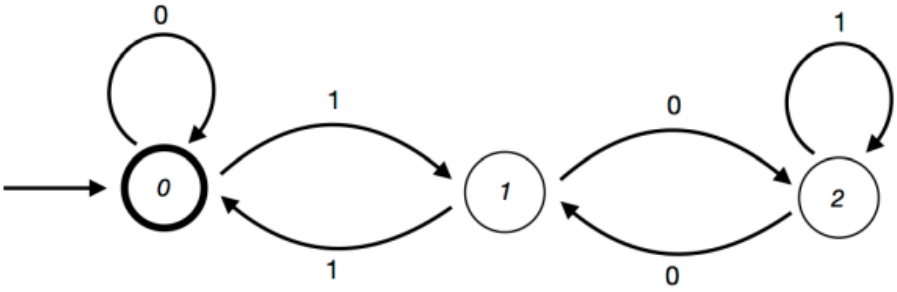
Q5. Find the sequence detected



Q6. Design a Mealy machine that performs a 2's complement of input using D flip flops. Assume that the input is given serially and LSB first.

Q7. Design a 3-bit counter with control input c, such that when c=0 it produces 3-bit binary sequence and when c=1 it produces 3-bit Gray code sequence.

Q8. Consider a "divisible-by-3" FSM that accepts a binary number entered one bit at a time, most significant bit first. The FSM has a one-bit output that indicates if the number entered so far is divisible by 3. If the value of the number entered so far is N, then after the digit b is entered, the value of the new number N' is 2N + b. This leads to the following state-transition diagram where the states are labelled with the value of N mod 3



a) Construct a truth table for the FSM logic. Inputs include the state bits (i.e., 00, 01, or 11) and the next (least significant) bit of the number; outputs include the next state bits and the output.

b) Based on the truth table, implement the FSM using D flip-flops.

Q9. In this problem, we construct a sequential circuit to compute the Nth Fibonacci number denoted by FN. The following recurrence relation defines the Fibonacci sequence.

$$F_0 = 0,\ F_1 = 1,\ F_N = F_{N-1} + F_{N-2}\ \forall\ N >= 2$$

There are two registers **x** and **y** that store the Fibonacci values for two consecutive integers. In addition, a counter register **i** is initialized to N-1 and decremented each cycle. The computation stops when register **i** goes down to 0 and the result (FN) is available in register **x.**

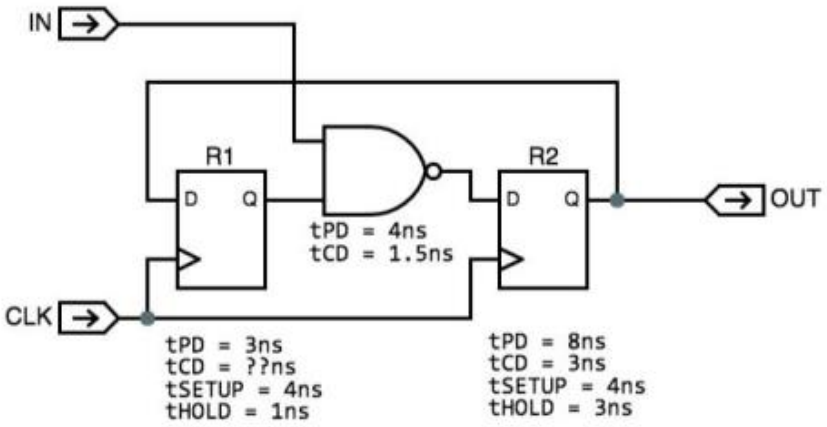
c) What are the initial values for registers x and y

d) Derive the next state computation equations for the three registers.

e) Derive the logic for the enable signal that determines when the registers are updated using the next state logic. Note that all three registers are controlled by a single enable signal.

f) Implement the sequential circuit using the next state and enable logic derived above.

Q10. Consider the following sequential logic circuit. The timing specifications are shown below each component. Note that the two registers do NOT have the same specifications



g) What is the smallest value for the period of CLK (i.e., t_{CLK}) that will allow both registers in the circuit to operate correctly?

h) What is the smallest value for the t_{CD} of R1 that will allow both registers in the circuit to operate correctly?

i) Suppose two of these sequential circuits were connected in series, with the OUT signal of the first circuit connected to the IN signal of the second circuit. The same CLK signal is used for both circuits. Now what is the smallest value for the period of CLK (i.e., t_{CLK}) that will allow both registers in the circuit to operate correctly?