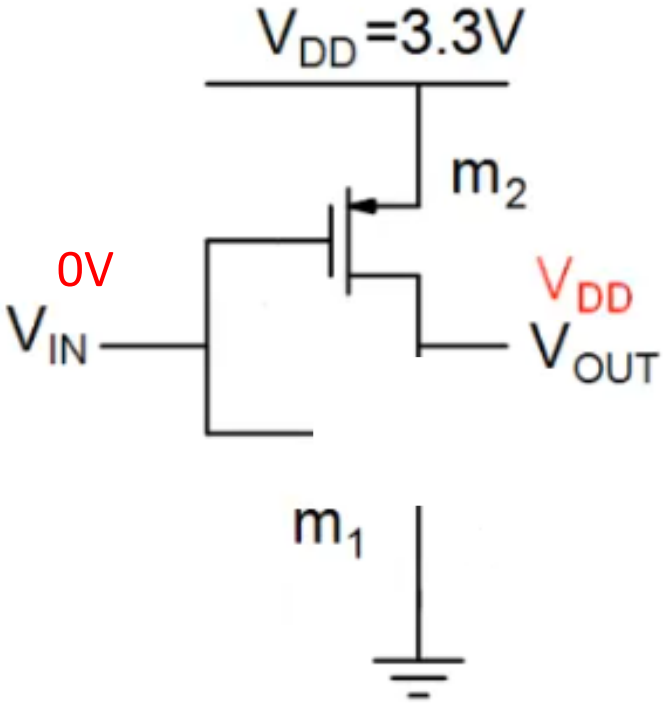
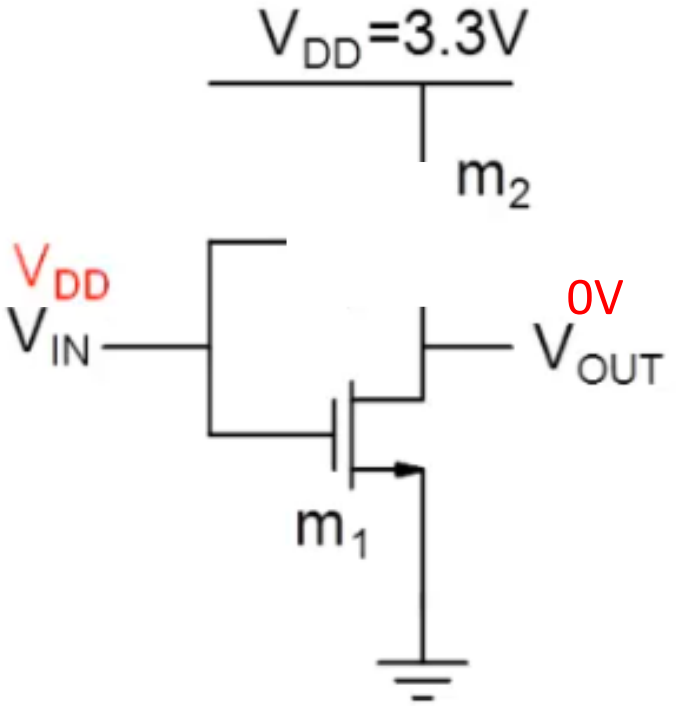
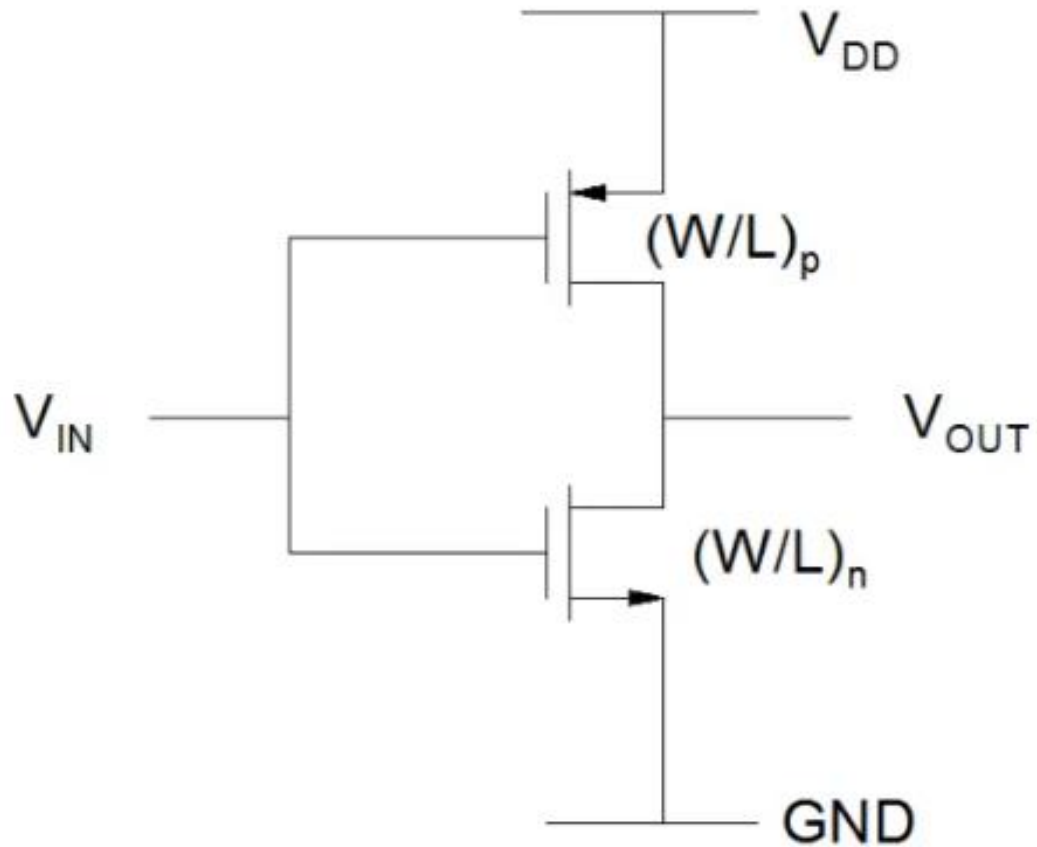




Logic "1" is VDD and "logic "0" is GND independent of size of transistors.

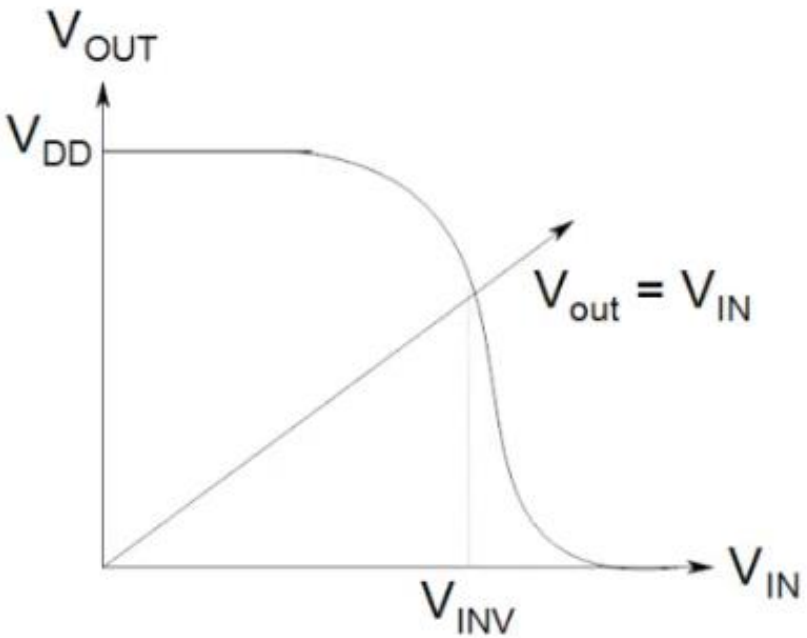
There is "no" static power dissipation in the circuit

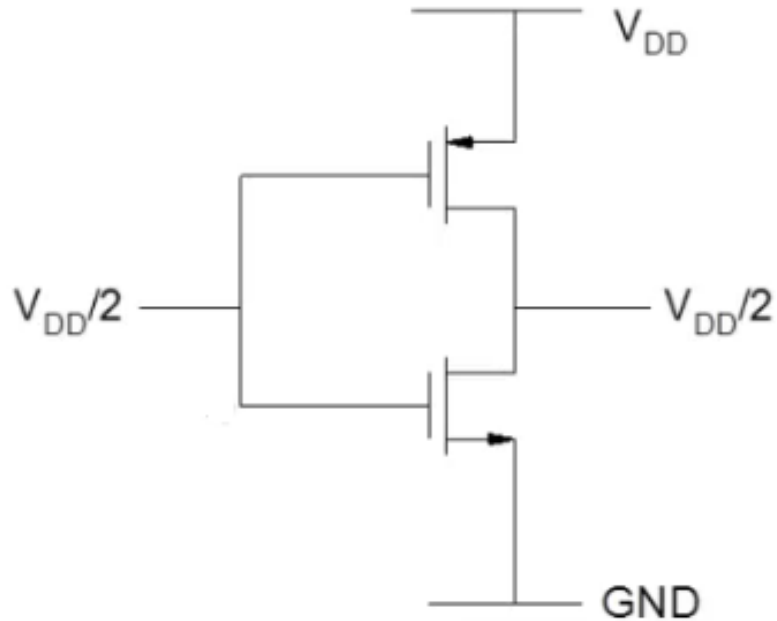
CMOS Inverter



How should we size to obtain symmetrical VTC ?

CMOS Inverter : VTC

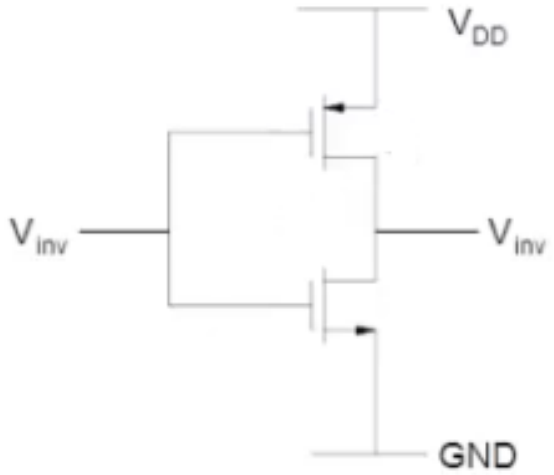




Both NMOS and PMOS are in saturation region

CMOS Inverter : VTC

$$I_{DSN} = I_{SDP}$$



$$\frac{\beta_N}{2}(V_{inv} - V_{THN})^2 = \frac{\beta_P}{2}(V_{SGP} + V_{THP})^2$$

$$V_{SGP} = V_{DD} - V_{inv}$$

$$\beta_N = W_N / L_N KP_N$$

$$\beta_P = W_p / L_P KP_P$$

$$V_{INV} = \frac{V_{THN} + \frac{1}{\sqrt{\beta_R}}(V_{DD} + V_{THP})}{1 + \frac{1}{\sqrt{\beta_R}}}$$

$$\beta_R = \frac{\beta_N}{\beta_P} = \left(\frac{W_N / L_N}{W_P / L_P}\right) \times \left(\frac{KP_N}{KP_P}\right)$$

CMOS Inverter : VTC

$$V_{INV} = \frac{V_{THN} + \frac{1}{\sqrt{\beta_R}}(V_{DD} + V_{THP})}{1 + \frac{1}{\sqrt{\beta_R}}}$$

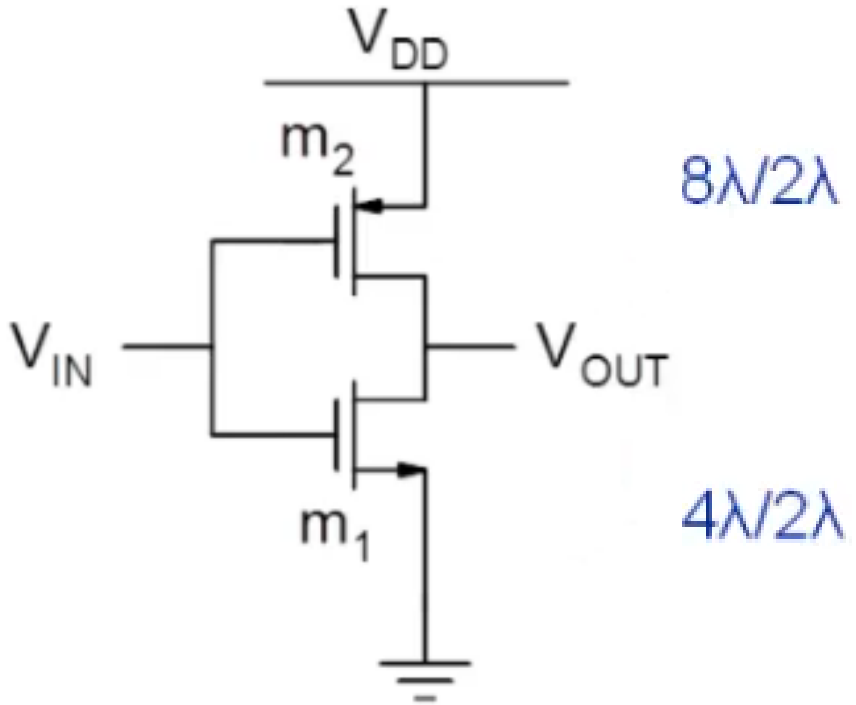
$$V_{INV} = 0.5V_{DD}$$

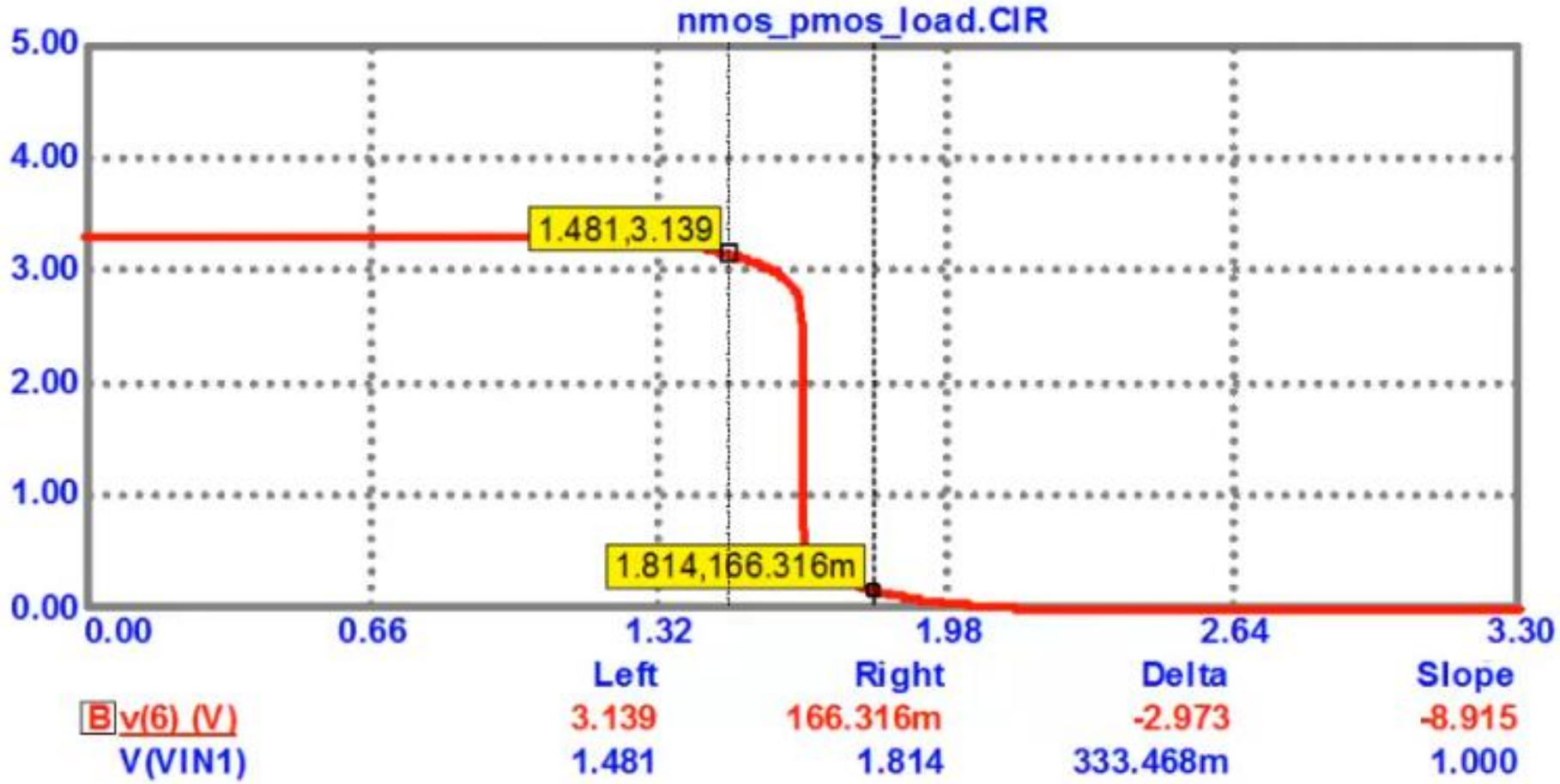
$$\beta_R = \frac{0.5V_{DD} + V_{THP}}{0.5V_{DD} - V_{THN}}$$

$$\Rightarrow \beta_R = 1$$

$$\frac{W_P/L_P}{W_N/L_N} = \frac{KP_N}{KP_P}$$

2.0





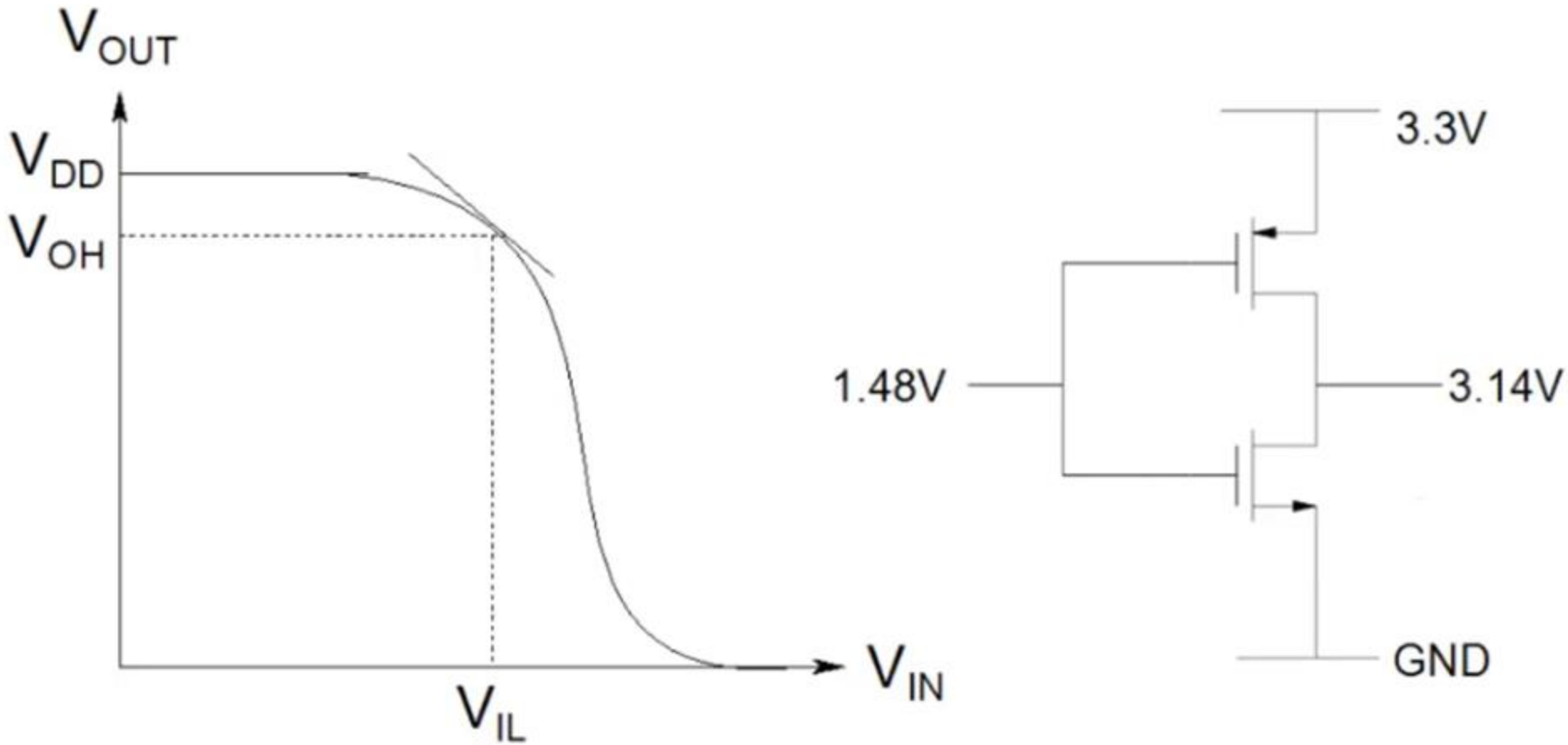
$$V_{IL} = 1.48V; v_{ol} = 0V$$

$$V_{IH} = 1.814V; v_{oh} = 3.3V$$

$$NM_H = 1.48V; NM_L = 1.48V$$

$$\frac{NM_H}{0.5V_{DD}} = 0.9$$

CMOS Inverter : V_{IH} ; V_{IL}



At V_{IL} , PMOS in Linear and NMOS in Saturation

CMOS Inverter : V_{IH} ; V_{IL}

W_P/W_N	V_{INV}	V_{IH}	V_{IL}	V_{OH}	V_{OL}
1	1.53	1.67	1.34	3.16	0.177
2	1.65	1.81	1.48	3.14	0.166
3	1.7	1.9	1.575	3.12	0.148

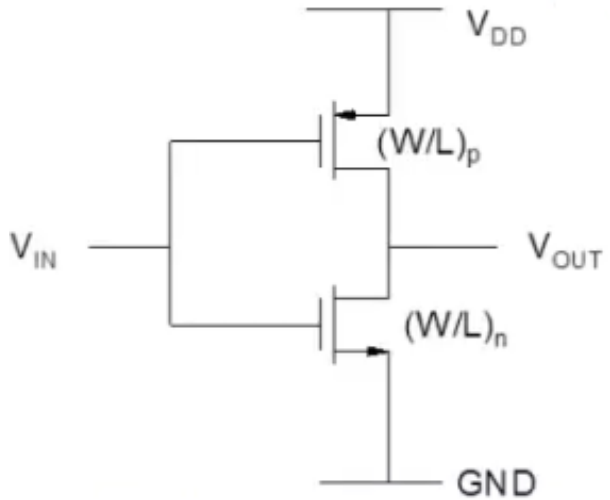
CMOS Inverter : V_{IL}

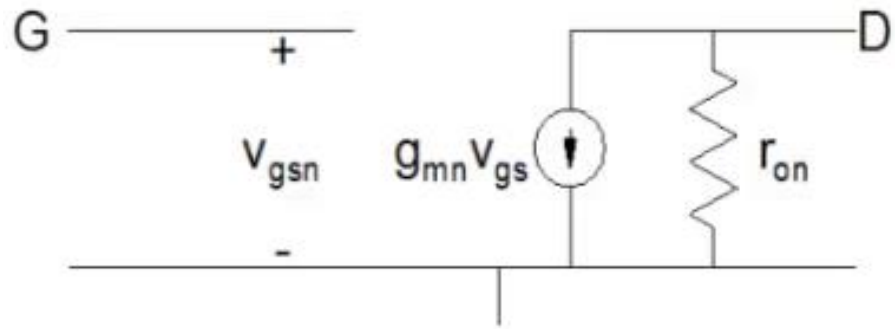
$$\frac{\beta_N}{2}(V_{IL} - V_{THN})^2 =$$

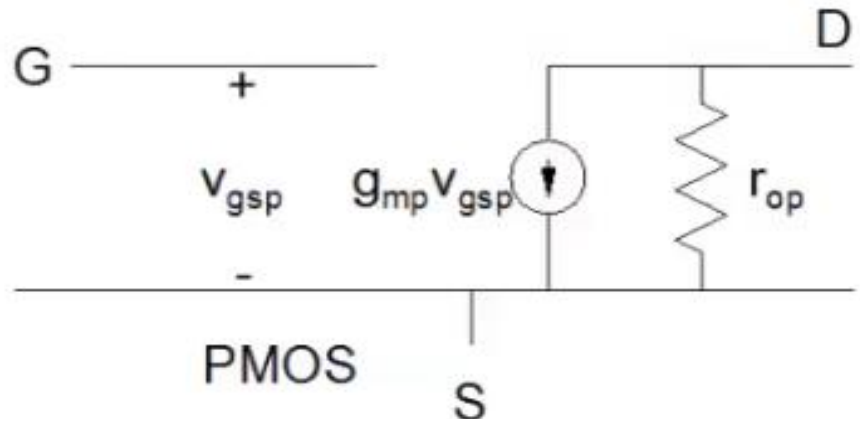
$$\beta_P((V_{DD} - V_{IL} + V_{THP})(V_{DD} - V_{OUT}) - 0.5(V_{DD} - V_{OUT})^2)$$

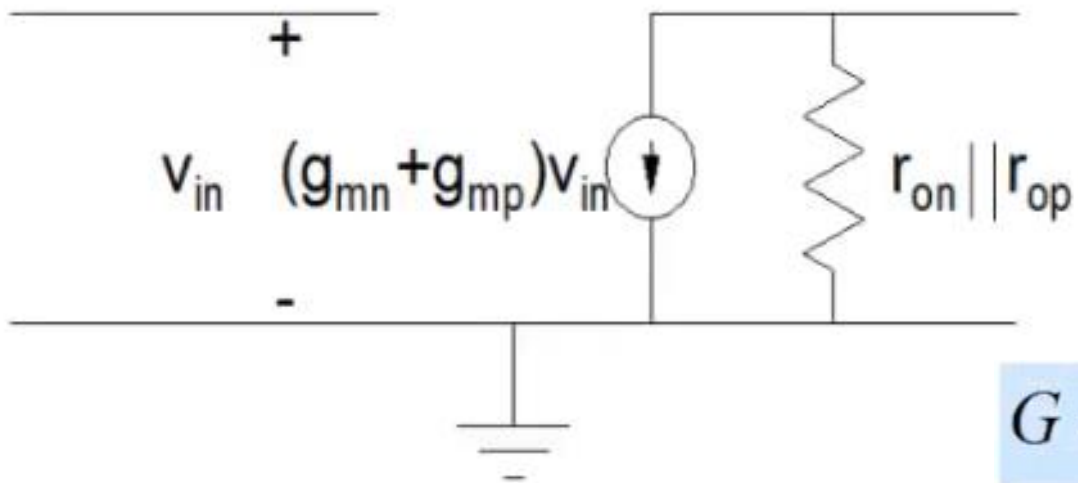
- Gain of inverter is Unity

CMOS Inverter : V_{IH} ; V_{IL}









$$G = -(g_{MN} + g_{MP}) \times r_{ON} \| r_{OP}$$

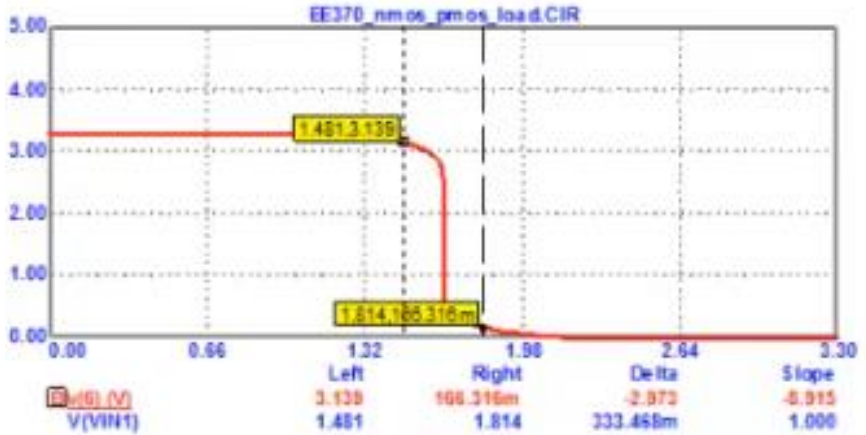
CMOS Inverter : V_{IL}

$$G = -(g_{MN} + g_{MP}) \times r_{ON} \| r_{OP} = -1$$
$$\Rightarrow (g_{MN} + g_{MP}) \times r_{OP} \cong 1$$

$$g_{mn} = \beta_N \times (V_{IL} - V_{THN}) \; ; \; g_{mp} = \beta_P \times (V_{DD} - V_{OUT})$$
$$r_{op} = \frac{1}{\beta_P \times (V_{DD} - V_{IL} + V_{THP} + V_{DD} - V_{OUT})}$$

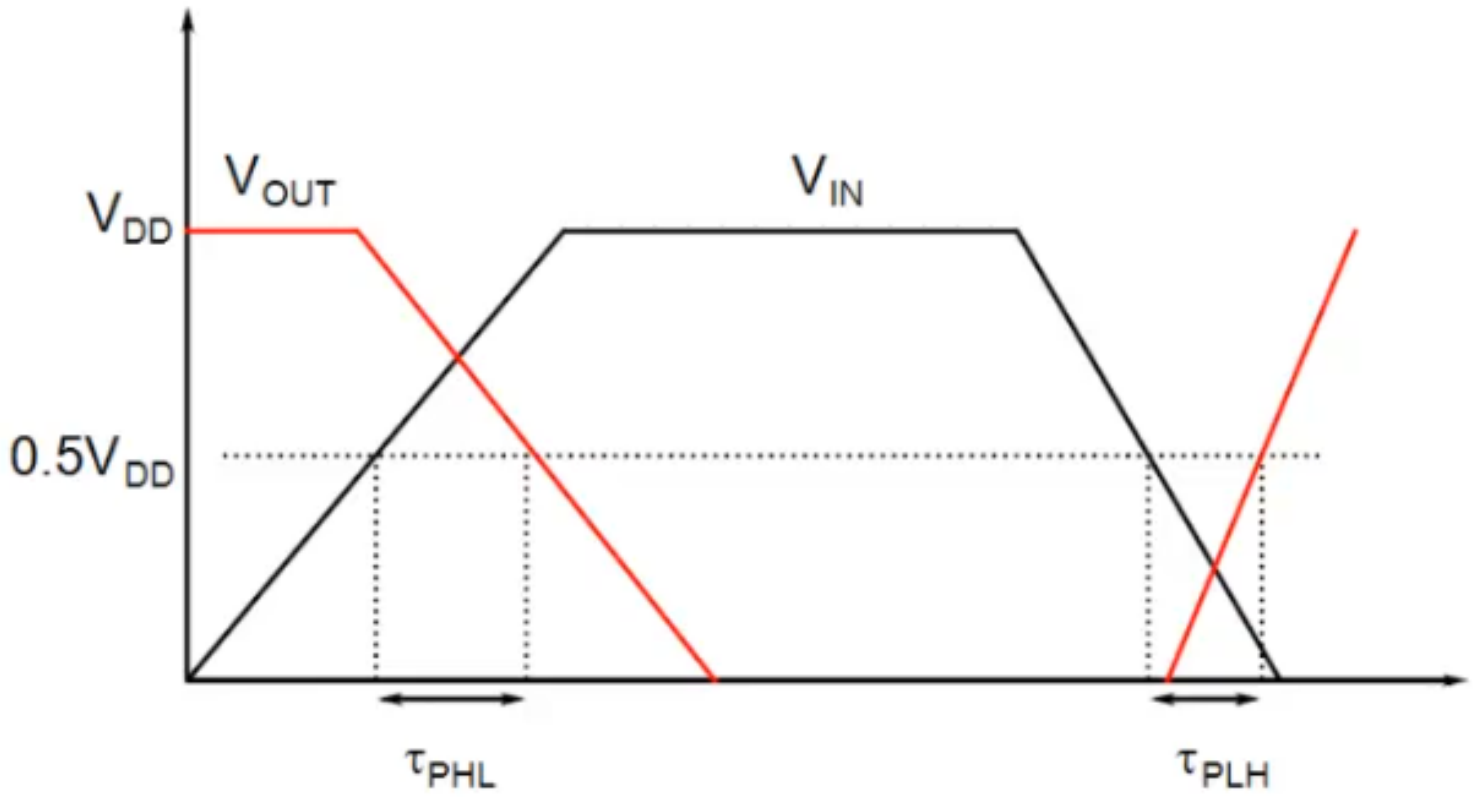
$$\frac{\beta_N}{2}(V_{IL} - V_{THN})^2 =$$
$$\beta_P((V_{DD} - V_{IL} + V_{THP})(V_{DD} - V_{OUT}) - 0.5(V_{DD} - V_{OUT})^2)$$

$$V_{IL} \sim V_{inv} - \delta V \; ; \; V_{IH} \sim V_{inv} + \delta V$$



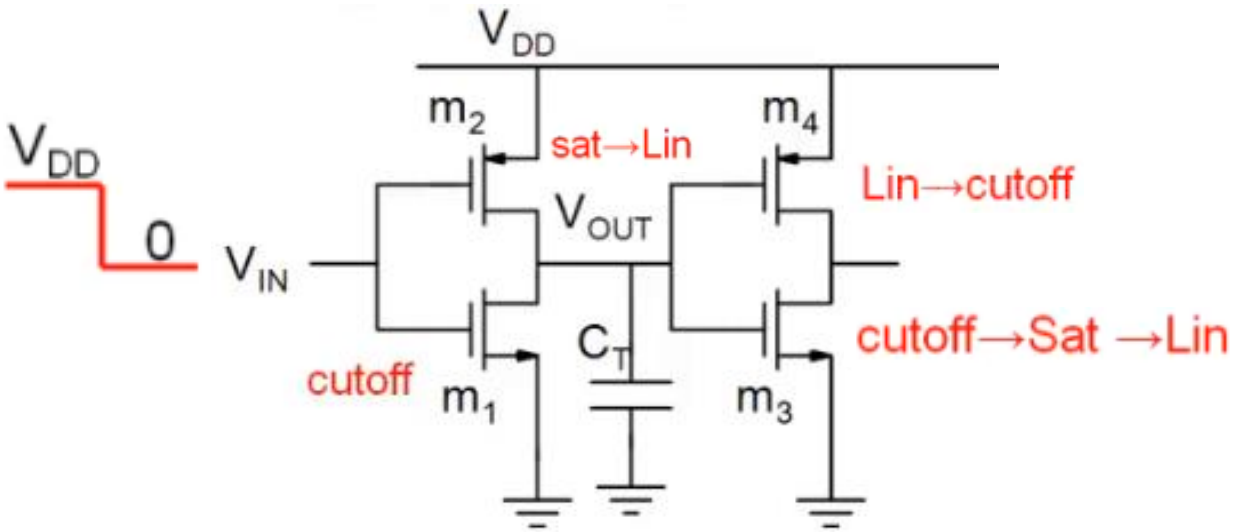
$$\delta V \sim 0.17V$$

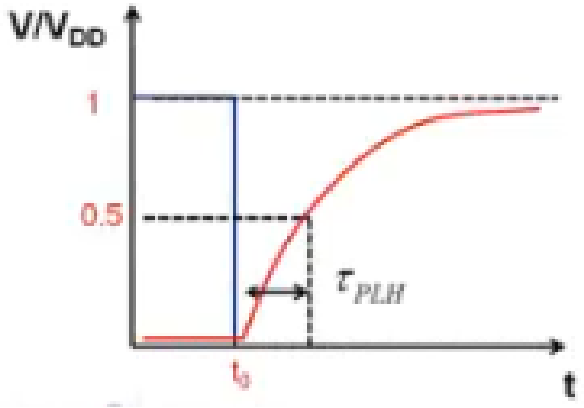
CMOS: Propagation Delay



$$\tau_R \; ; \tau_F \; ; \tau_{PHL} \; ; \tau_{PLH}$$

Low to high propagation delay



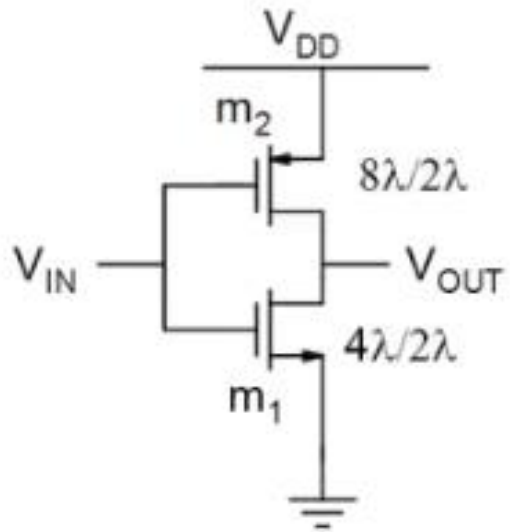


$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}}$$

$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$$

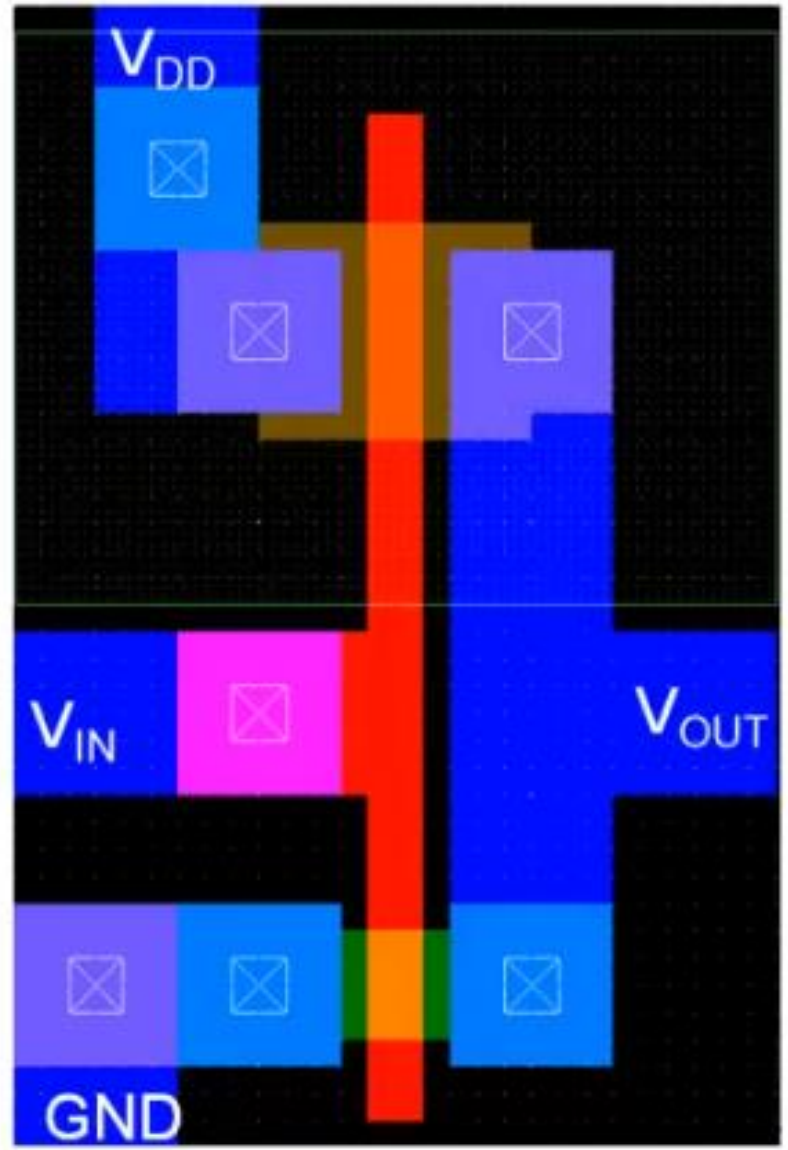
$$C_T = \left(C_{gdn1} + C_{dbn1} + C_{gdp2} + C_{dbp2}\right) +$$

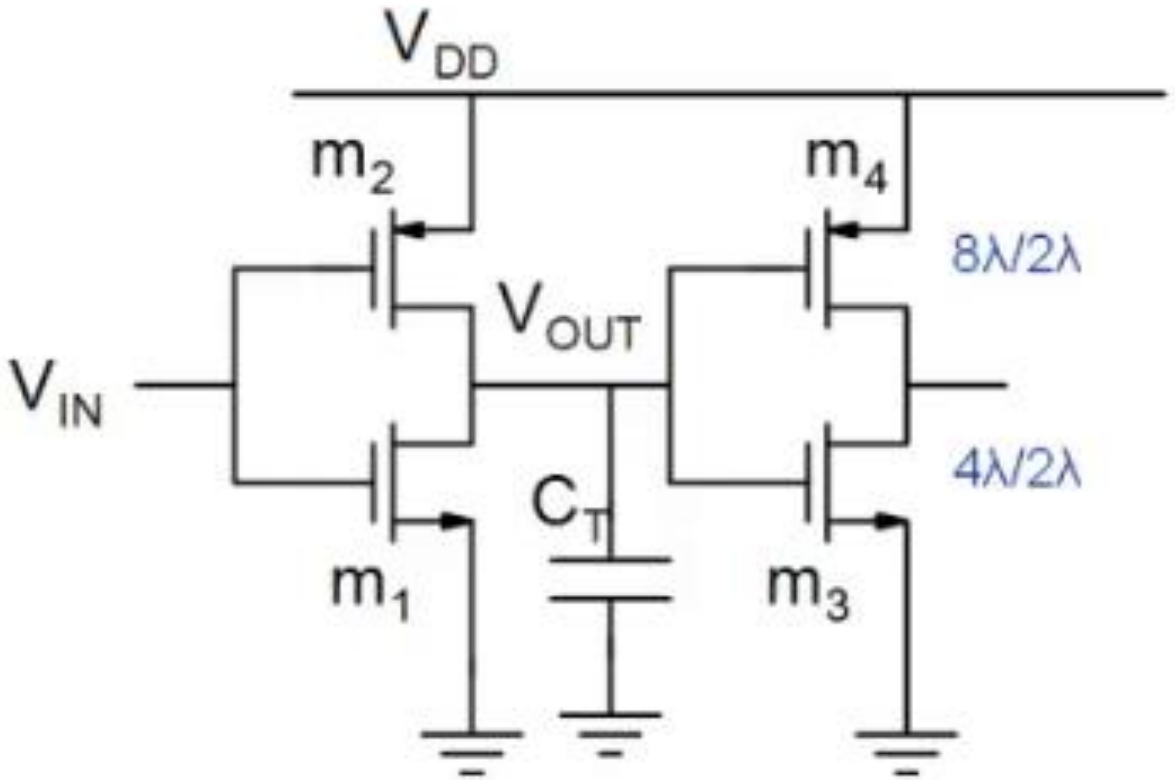
$$\left(C_{gsn3} + C_{gdn3} + C_{gbn3} + C_{gsp4} + C_{gdp4} + C_{gbp4}\right)$$



$$A_{D1} = 4 \times 1 + 6 \times 6 = 40;$$
$$P_{D1} = (1 + 1 + 6) \times 2 + 6 = 22$$

$$A_{D2} = 8 \times 4 + 3 \times 6 = 50;$$
$$P_{D2} = (4 + 1 + 3) \times 2 + 6 = 22$$





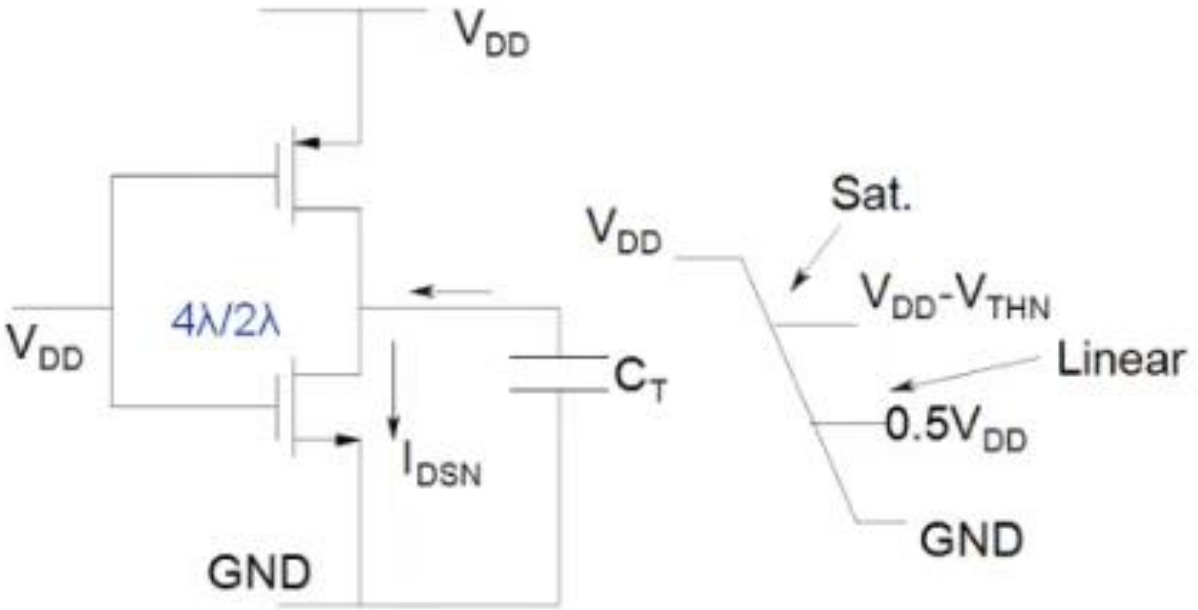
~0.3fF ~6fF ~0.6fF ~6fF

$$C_T = \left(C_{gdn1} + C_{dbn1} + C_{gdp2} + C_{dbp2}\right) + \left(C_{gsn3} + C_{gdn3} + C_{gbn3} + C_{gsp4} + C_{gdp4} + C_{gbp43}\right)$$

~13+7fF

~2.0fF ~5fF

Delay Analysis :



$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}}$$

$\tau_{phl} \sim 65ps$

42+23

$$I_{DS}(t=0) = \left(KP_N \times \frac{W_N}{L_N} \right) \times \frac{(V_{DD} - V_{THN})^2}{2}$$

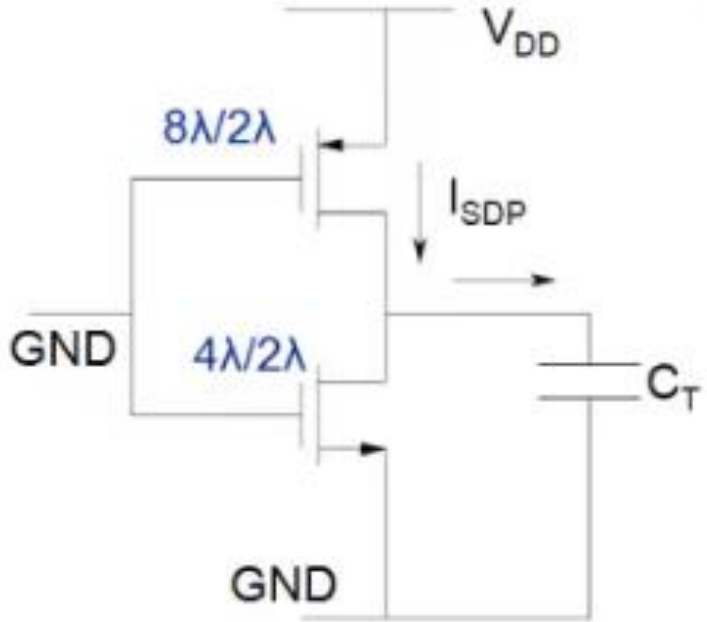
$$I_{DS}(t=\tau_{phl}) = \left(KP_N \times \frac{W_N}{L_N} \right) \times \left((V_{DD} - V_{THN}) \frac{V_{DD}}{2} - \frac{V_{DD}^2}{8} \right)$$

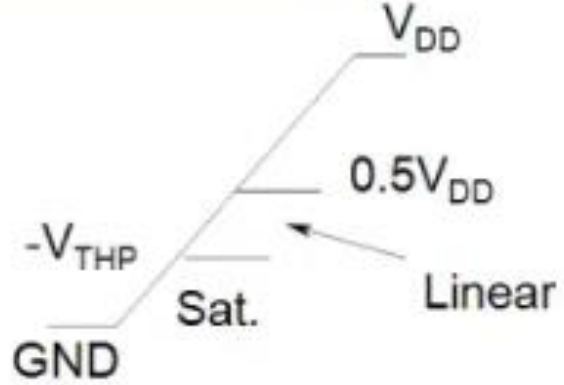
~0.53mA → $\tilde{I}_{pd} \sim 0.5mA$

~0.487mA

Delay Analysis :

$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu.}} \qquad \tau_{plh} \sim 65\,ps$$

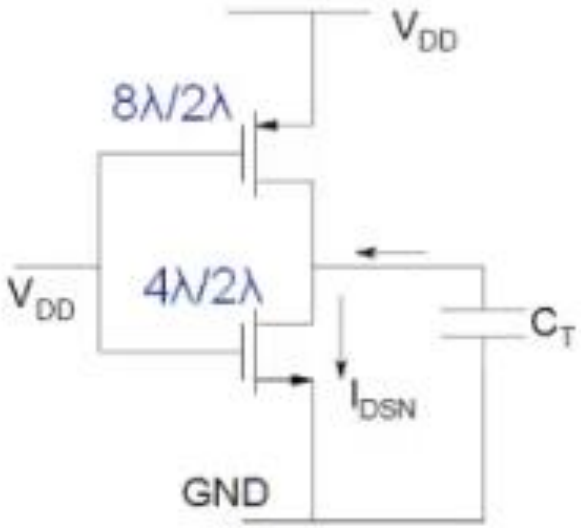




$$I_{SDP}(t=0) = \left(KP_P \times \frac{W_P}{L_P} \right) \times \frac{(V_{DD} + V_{THP})^2}{2} \qquad \sim 0.53mA$$

$$I_{SDP}(t=\tau_{plh}) = \left(KP_P \times \frac{W_P}{L_P} \right) \times \left((V_{DD} + V_{THP}) \frac{V_{DD}}{2} - \frac{V_{DD}^2}{8} \right) \qquad \sim 0.487mA$$

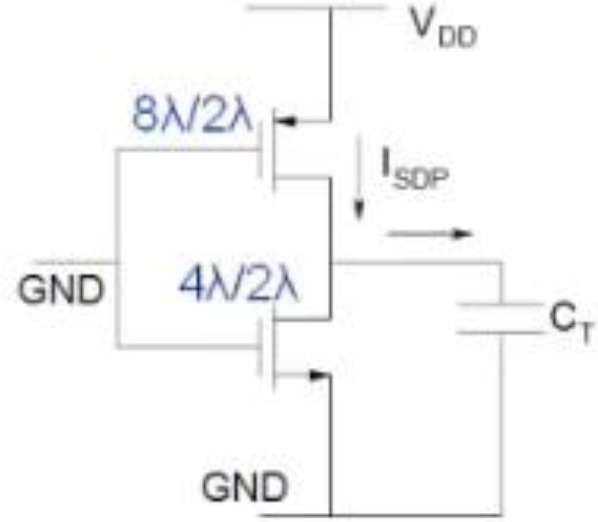
$$\tilde{I}_{pu} \sim 0.5mA$$



$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}}$$

$$I_{DS}(t=0) = \left(KP_N \times \frac{W_N}{L_N} \right) \times \frac{(V_{DD} - V_{THN})^2}{2}$$

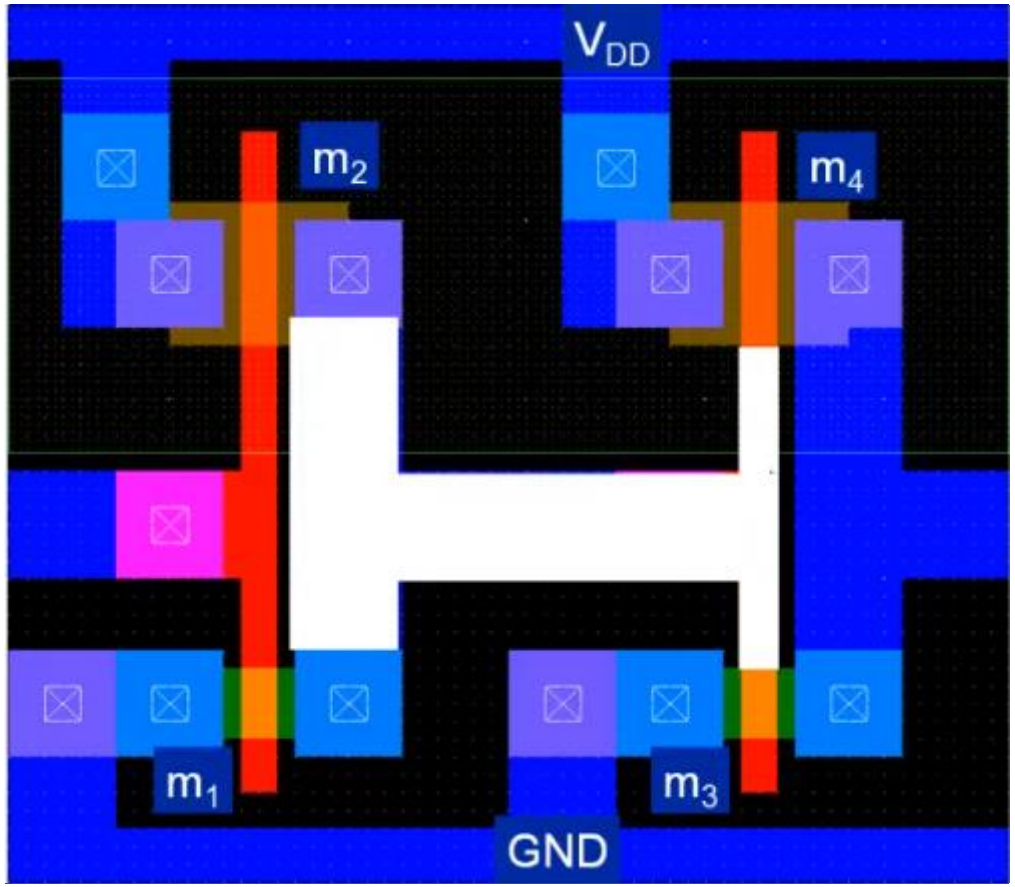
$$I_{DS}(t=\tau_{phl}) = \left(KP_N \times \frac{W_N}{L_N} \right) \times \left((V_{DD} - V_{THN}) \frac{V_{DD}}{2} - \frac{V_{DD}^2}{8} \right)$$

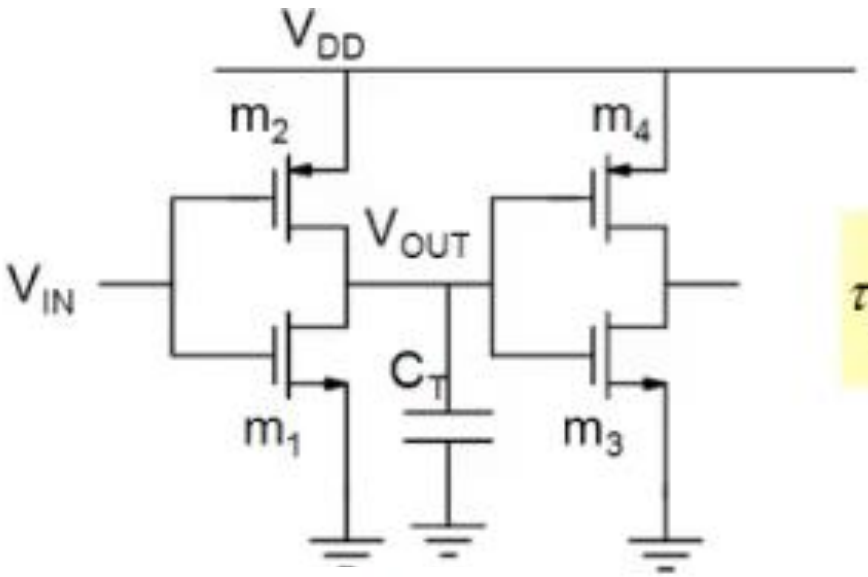


$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu.}}$$

$$I_{SDP}(t=0) = \left(KP_P \times \frac{W_P}{L_P} \right) \times \frac{(V_{DD} + V_{THP})^2}{2}$$

$$I_{SDP}(t=\tau_{plh}) = \left(KP_P \times \frac{W_P}{L_P} \right) \times \left((V_{DD} + V_{THP}) \frac{V_{DD}}{2} - \frac{V_{DD}^2}{8} \right)$$


V_{DD}
m_2
m_4
m_1
m_3
GND



$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}}$$

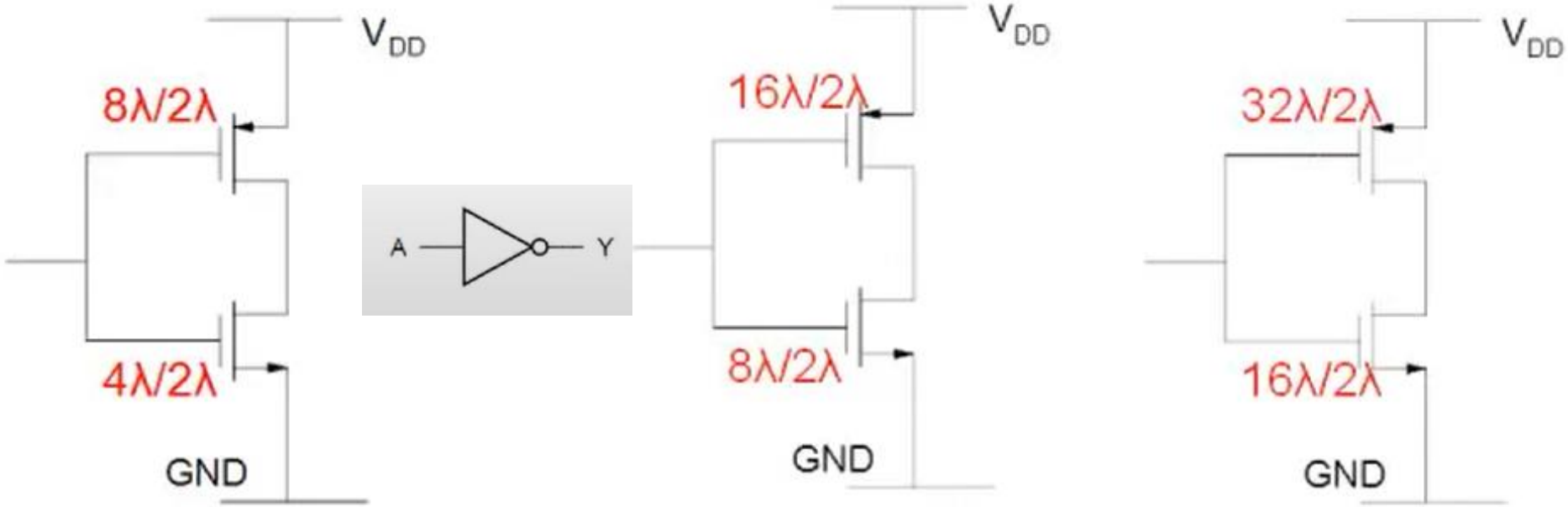
~13fF

~7fF

$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_{in} V_{DD}}{\tilde{I}_{pd.}} + 0.5 \times \frac{\tilde{C}_L V_{DD}}{\tilde{I}_{pd.}}$$

$$\tau_{phl}(ps) \cong 42 + a \times C_L(fF);\ a = 3.25$$

ps/fF or ns/pF



1X Inverter

2X Inverter

4X Inverter

$$\tau_{phl}(ps) \cong 42 + a \times C_L(fF);\ a = 1.625$$

$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_{in} V_{DD}}{\tilde{I}_{pd.}} + 0.5 \times \frac{\tilde{C}_L V_{DD}}{\tilde{I}_{pd.}}$$

$$\tau_{phl}(ps) \cong 42 + a \times C_L(fF);\ a = 3.25$$

0.18µm technology, 1.8V VDD

Cell Description

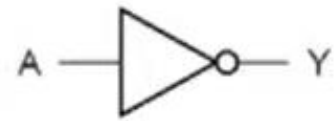
The INV cell provides the logical inversion of a single input (A). The output (Y) is represented by the logic equation:

$$Y = \overline{A}$$

Functions

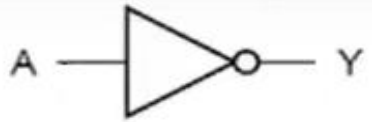
A	Y
0	1
1	0

Logic Symbol



Cell Size

Drive Strength	Height (µm)	Width (µm)
INVXL	5.0	1.3
INVX1	5.0	1.3
INVX2	5.0	2.0
INVX3	5.0	2.6
INVX4	5.0	2.6
INVX8	5.04	3.96
INVX12	5.04	8.58
INVX16	5.04	11.22
INVX20	5.04	12.54



$$P_{dynamic} = C_T \times V_{DD}^2 \times f$$

AC Power

Pin	Power (µW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0087	0.0114	0.0209	0.0315	0.0378	0.0775	0.1665	0.2250	0.2804

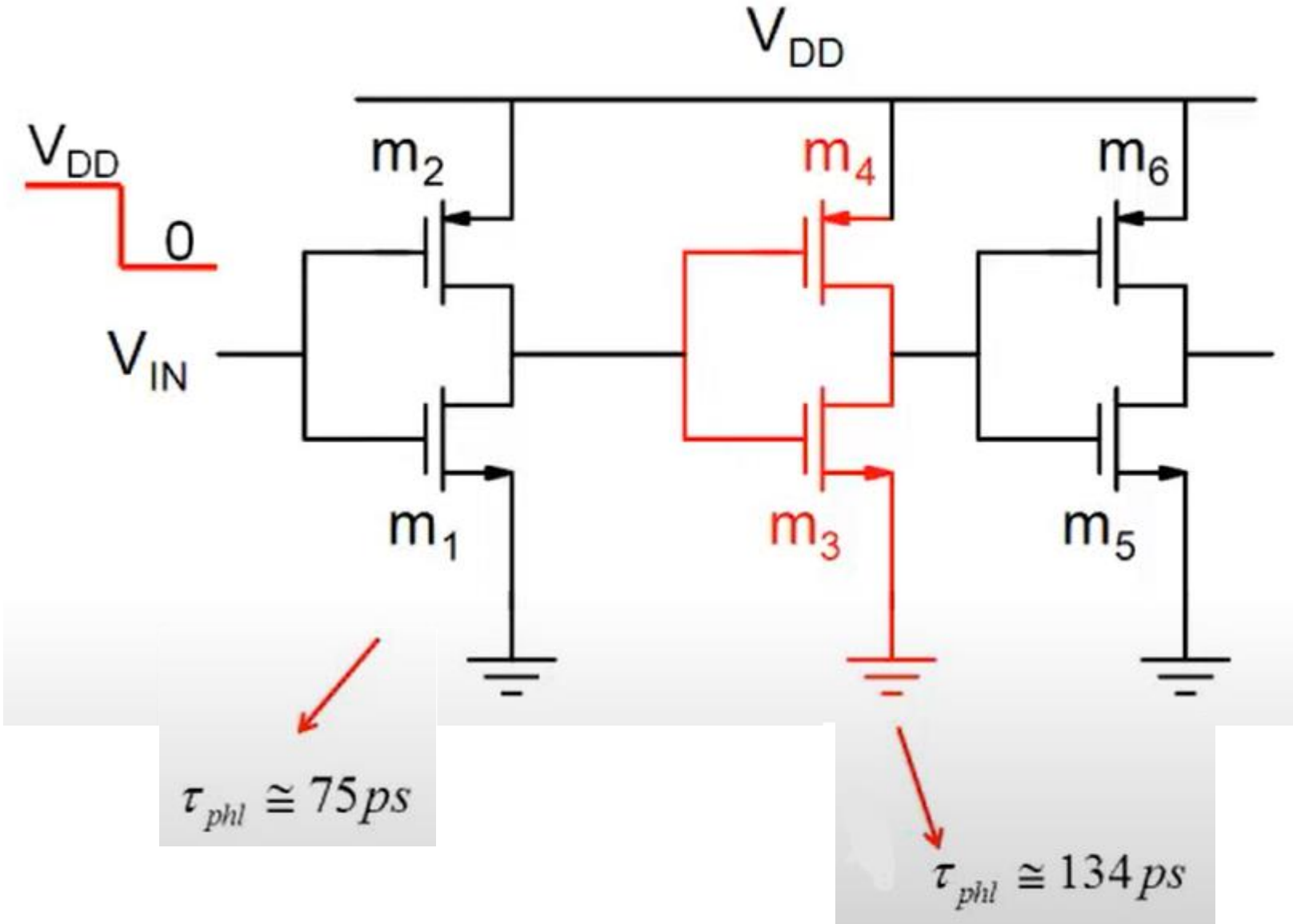
Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0026	0.0036	0.0070	0.0100	0.0129	0.0267	0.0067	0.0088	0.0109

Delays at 25°C, 1.8V, Typical Process

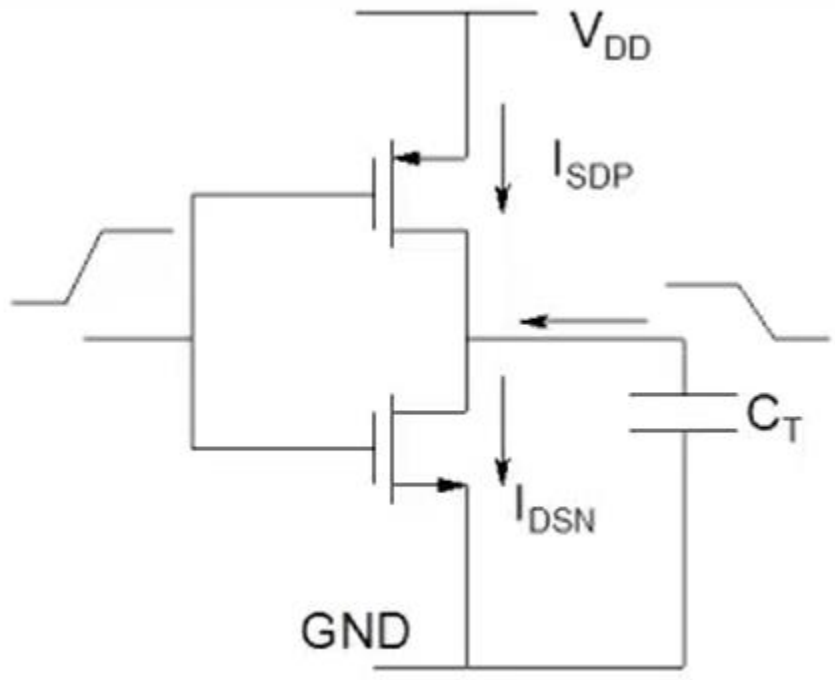
Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0.023	0.023	0.020	0.022	0.018	0.018	0.122	0.119	0.117
A → Y↓	0.015	0.014	0.012	0.013	0.011	0.012	0.119	0.113	0.110

Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	6.229	4.512	2.256	1.507	1.137	0.519	0.346	0.260	0.208
A → Y↓	3.237	2.401	1.195	0.798	0.598	0.356	0.240	0.180	0.144


V_DD
V_DD
0
V_IN
m_2
m_4
m_6
m_1
m_3
m_5
τ_phl ≅ 75ps
τ_phl ≅ 134ps

Effect of Input Rise/Fall time

$$I_{DSN} - I_{SDP} = - C_T \frac{dV_{OUT}}{dt}$$



- The PMOS does not switch off immediately thereby reducing the discharge current.
- The NMOS does not reach its full current drive capability immediately.

$\Rightarrow$ Propagation delay increases !

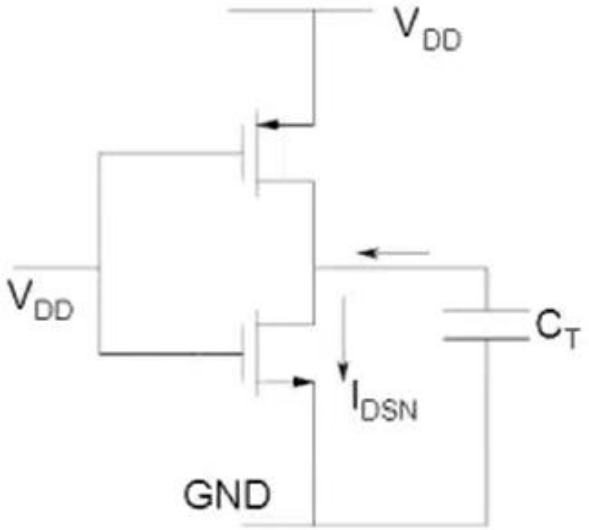
Effect of Input Rise/Fall time

Empirical Model :

$$\tau_{PHL} = \sqrt{\tau_{PHLO}^2 + (t_R/2)^2}$$

τ_R / τ_{PHL}	τ_{PHLO} / τ_{PHL}
0.0	1.0
0.5	0.968
1.0	0.866
1.5	0.66

Impact of process variations



$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}}$$

$$I_{DS}(t=0) = \left(KP_N \times \frac{W_N}{L_N} \right) \times \frac{(V_{DD} - V_{THN})^2}{2}$$

$$\mu_N C'_{ox}$$

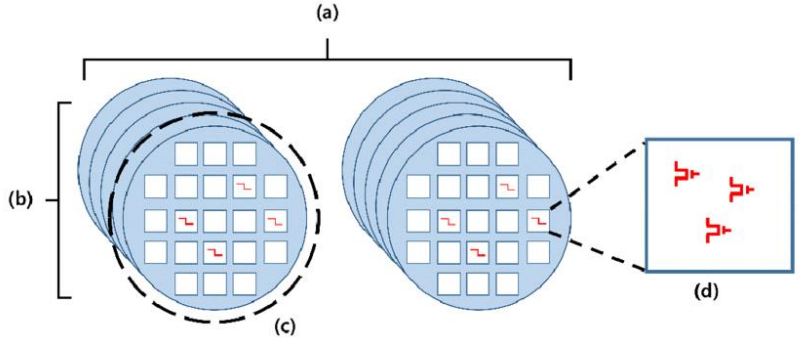
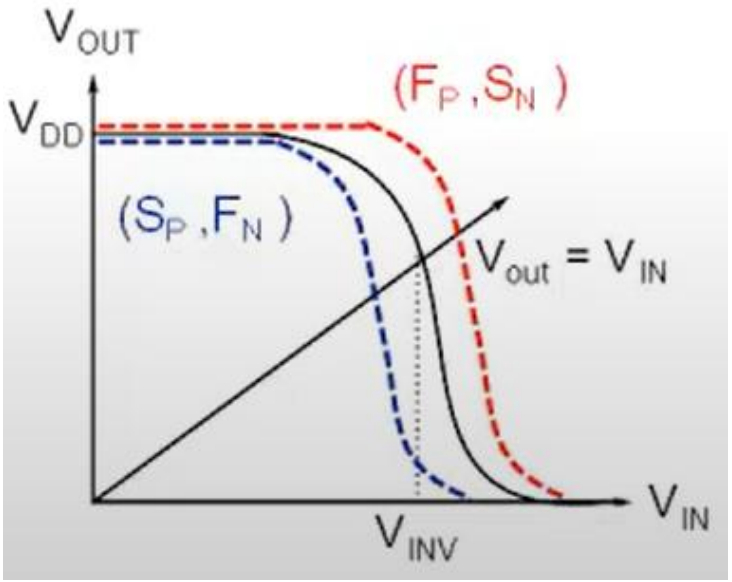


Fig. 1: Classification of variations. Global variations include (a) lot-to-lot variation (LTLV), (b) wafer-to-wafer variation (WTWV), and (c) die-to-die variation (DTDV). Local variation means (d) within-die variation (WIDV) [1]



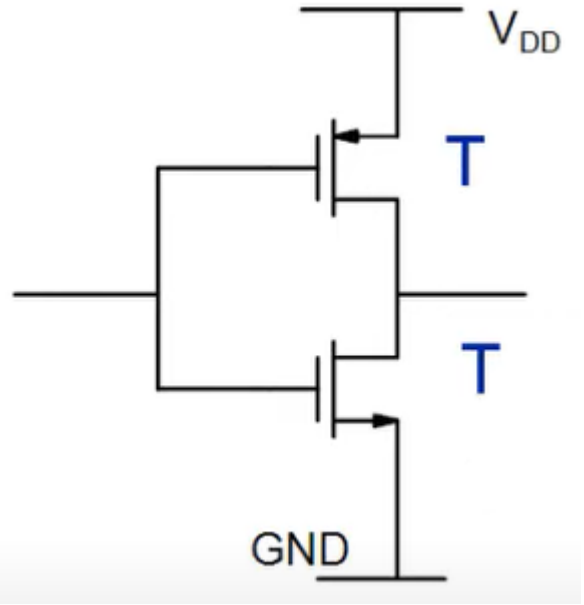
Case	NMOS	PMOS
1	nominal	nominal
2	slow	slow
3	slow	fast
4	fast	slow
5	fast	fast

Delay under variations

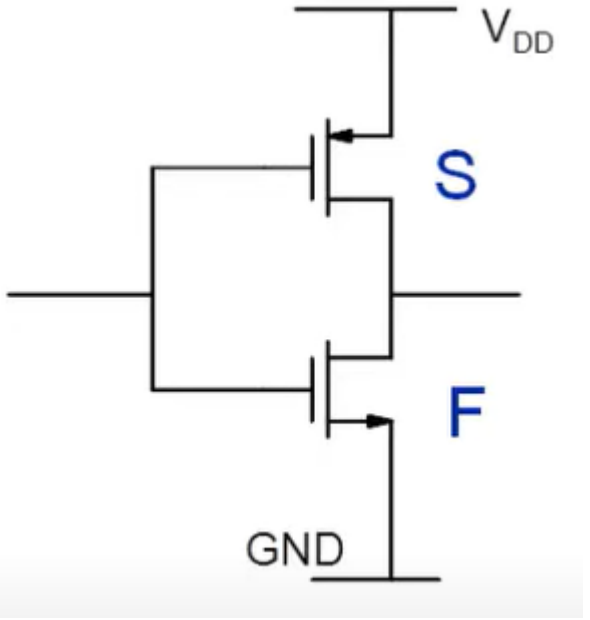
- Temperatures varying between 0 – 125°C,
- Supply voltage varying between VDD (± 10%)
- Process variations of 3σ.

Case	NMOS	PMOS
1	nominal	nominal
2	slow	slow
3	slow	fast
4	fast	slow
5	fast	fast

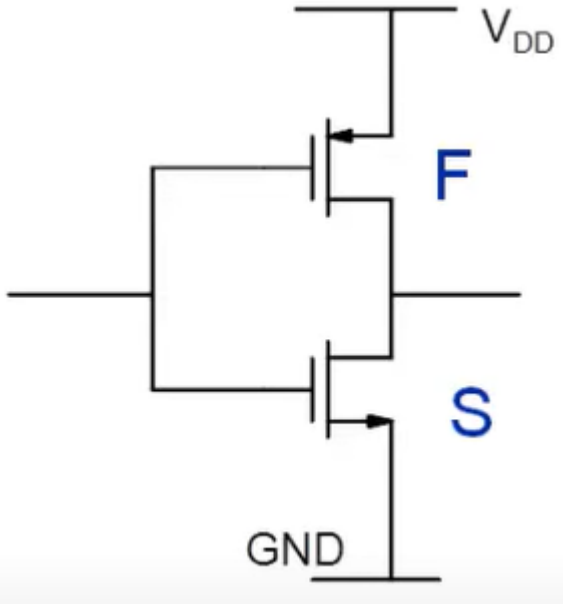
$$KP_N = 100 \pm 20\%;\ V_{THN} = 1 \pm 0.1V$$
$$KP_P = 50 \pm 20\%;\ V_{THP} = -1 \pm 0.1V$$



$$V_{IL} = 1.48V; V_{IH} = 1.814V$$
$$N_{ML} = N_{MH} = 1.48V$$



$$V_{IL} = 1.3V; V_{IH} = 1.63V$$



$$V_{IL} = 1.67V; V_{IH} = 2V$$

$$N'_{ML} = 1.3V;\ N'_{MH} = 1.3V$$

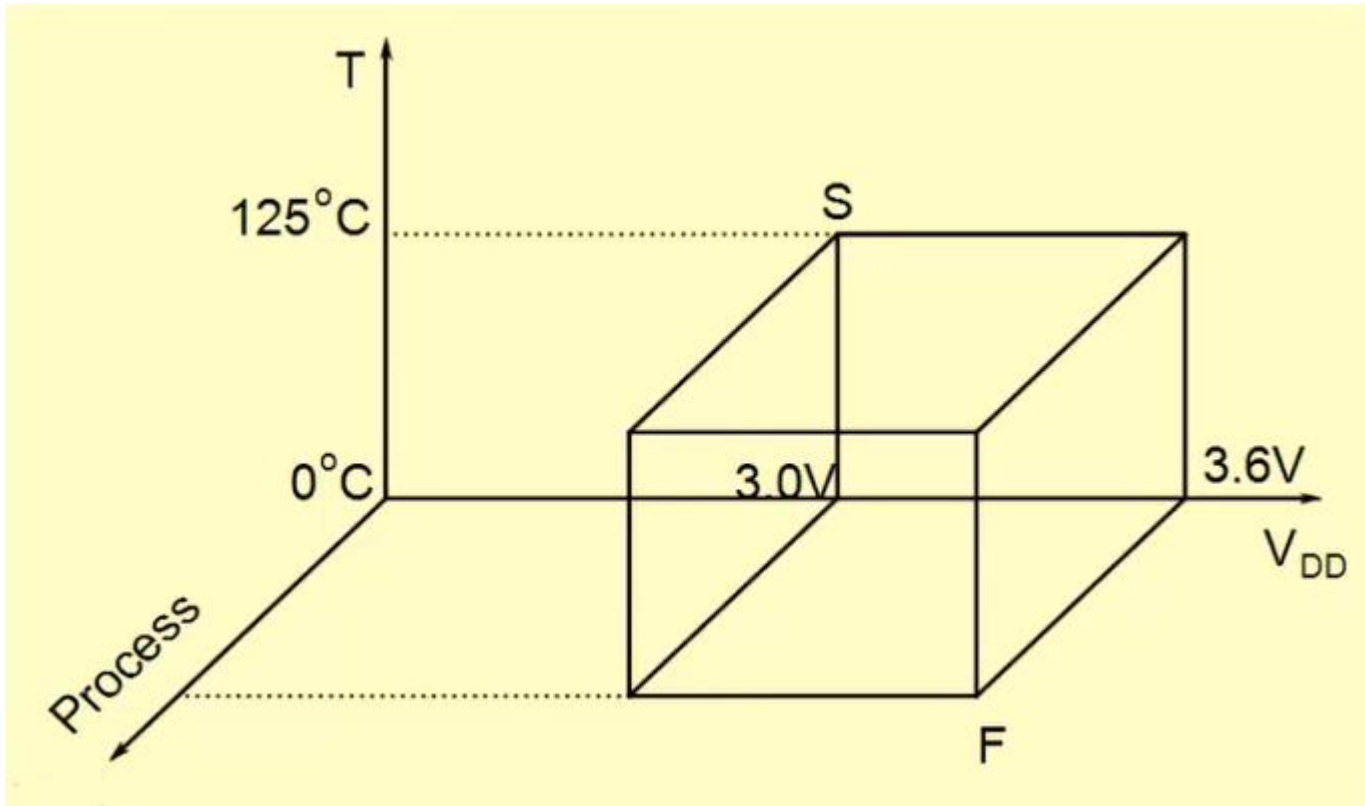
Delay under variations

- Temperatures varying between 0 – 125°C,
- Supply voltage varying between VDD (± 10%)
- Process variations of 3σ.

Case	NMOS	PMOS
1	nominal	nominal
2	slow	slow
3	slow	fast
4	fast	slow
5	fast	fast

Best and Worst Case Delay values

- Temperatures varying between 0 – 125°C,
- Supply voltage varying between VDD (1 ± 10%)
- Process variations of 3σ.



Delay Calculation

Using the delay data in the datasheets ($t_{intrinsic}$, K_{load}, and C_{load}) and the delay derating factors, the estimated total propagation delay is

$$t_{TPD} = (K_{Process}) \bullet [1+(K_{Volt} \bullet \Delta Vdd)] \bullet [1+(K_{Temp} \bullet \Delta T)] \bullet t_{typical}$$

$$t_{typical} = t_{intrinsic} + (K_{load} \bullet C_{load})$$

where:

t_{TPD}	=	total propagation delay (ns);
$t_{typical}$	=	delay at typical corner—1.8 V, 25 °C, typical process (ns);
$t_{intrinsic}$	=	delay through the cell when there is no output load (ns);
K_{load}	=	load delay multiplier (ns/pF);
C_{load}	=	total output load capacitance (pF);
$K_{Process}$	=	process derating factor, where process is slow, typical, or fast;
K_{Volt}	=	voltage derating factor (/V);
ΔVdd	=	Vdd —1.8 V;
K_{Temp}	=	temperature derating factor (/°C);
ΔT	=	junction temperature — 25 °C.

$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}}$$

$$I_{DS}(t=0) = \left(KP_N \times \frac{W_N}{L_N} \right) \times \frac{(V_{DD} - V_{THN})^2}{2}$$

$$\mu_N C'_{ox}$$

Table 3. Derating Factors

$K_{Process}$ (slow)	1.293
$K_{Process}$ (typical)	1.000 (by definition)
$K_{Process}$ (fast)	0.781
K_{Volt} (1.8V to 1.62V)	-0.731/V
K_{Volt} (1.8V to 1.98V)	-0.511/V

Table 3. Derating Factors

$K_{Process}$ (slow)	1.293
K_{Temp} (25°C to 0°C)	0.00137/°C
K_{Temp} (25°C to125°C)	0.00123/°C

$$\frac{\tau_p(\min)}{\tau_{po}} = 0.78 \times (1 - 0.51 \times 0.18) \times (1 - .00137 \times 25) = 0.68$$

$$\frac{\tau_p(\max)}{\tau_{po}} = 1.293 \times (1 + 0.73 \times 0.18) \times (1 + .00123 \times 100) = 1.64$$

Methods for decreasing delay

-Increase the supply voltage

$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}}$$

$$P_{dynamic} = C_T \times V_{DD}^2 \times f$$

Supply Voltage	τ_{PHL} (ps)
3.3	75
3.6	65.5
4.0	54.8
5.0	36.6

$$P_{dynamic} = 0.22\mu W / MHz$$

$$P_{dynamic} = 0.5\mu W / MHz$$

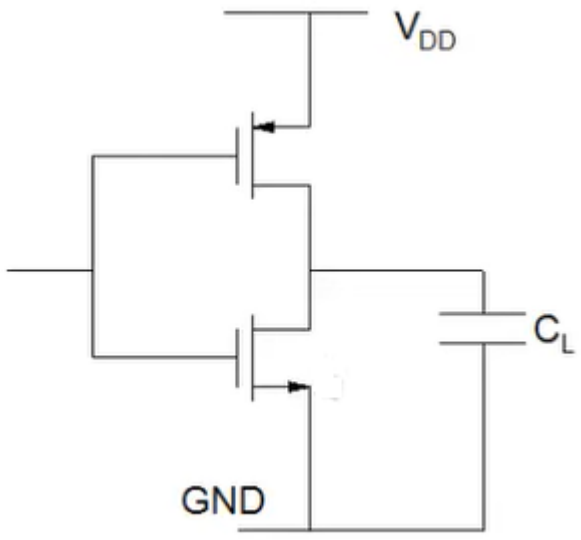
Size-

$$\tau_{phl}(ps) \cong \tau_{ins} + a \times C_L(fF); a \propto {}^{1}/W_N$$

Power Dissipation

$$P_T = P_{static} + P_{dynamic} + P_{SC}$$

Static power Dissipation

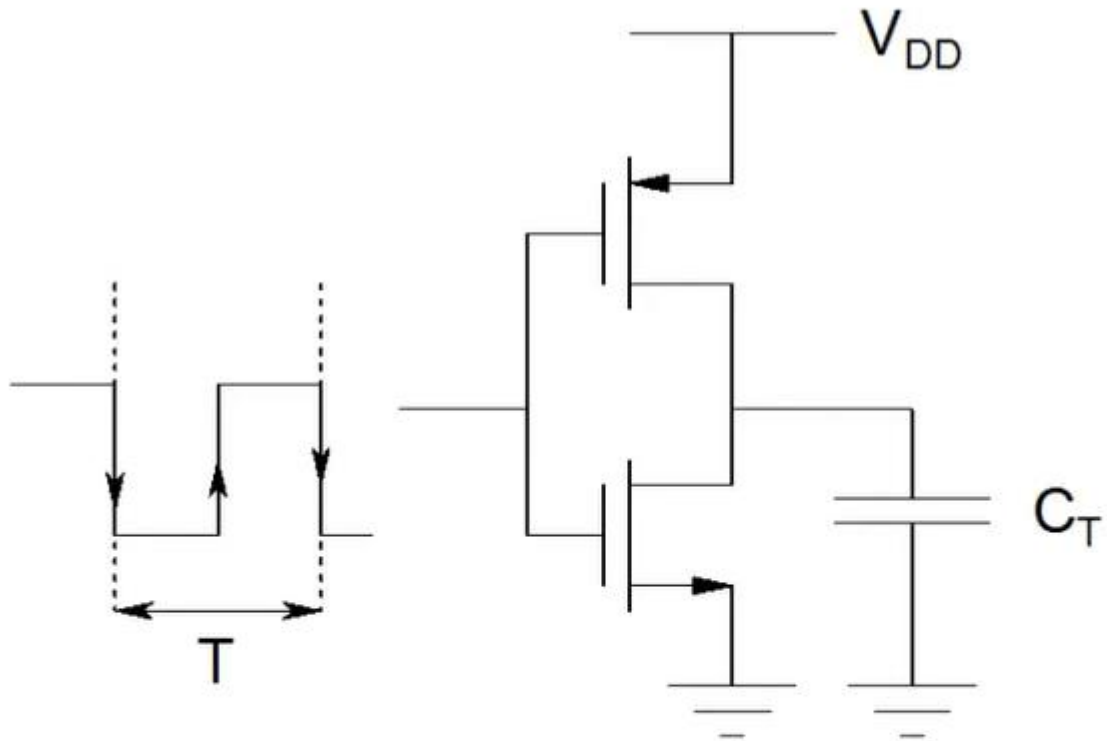


- "no" dc path exists between supply and ground under steady state conditions.
-leakage currents, although 'small' compared to ON state current, can still be significant .

- Not so true for the state-of-the-art scaled technology nodes
- Leakage power is significant in SOTA Tech. node

-depends on the threshold voltage and increases exponentially as its value is reduced

Dynamic power Dissipation



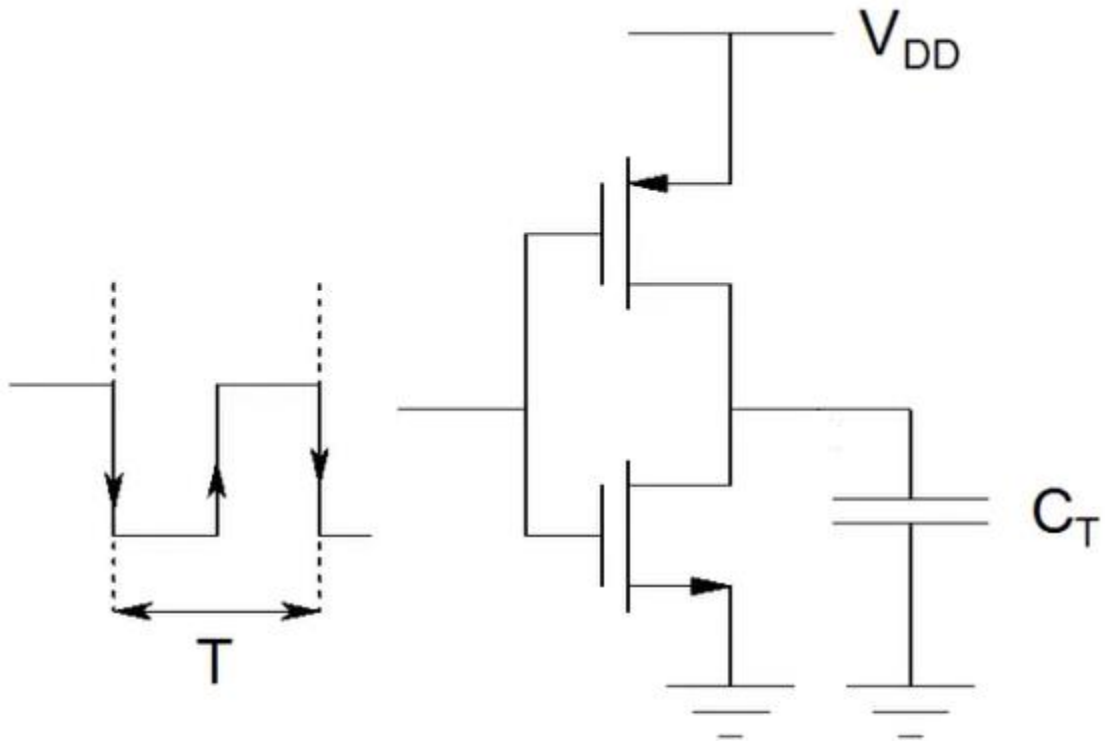
$$E_{Supply} = \int V_{DD} I_{Supply}\, dt$$

$$I_{Supply} = I_{SDP}$$

$$\int I_{SDP}\, dt = C_T\, V_{DD}$$

$$E_{Supply} = C_T\, V_{DD}^2$$

Dynamic power Dissipation

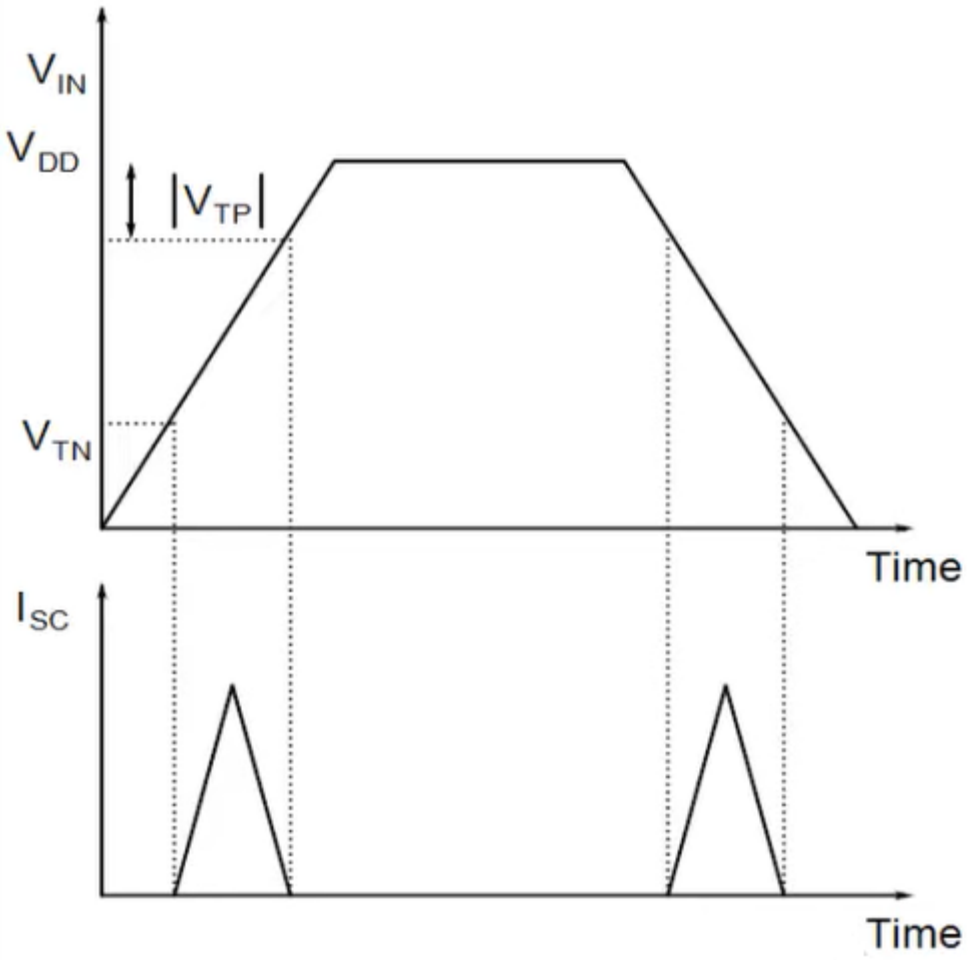


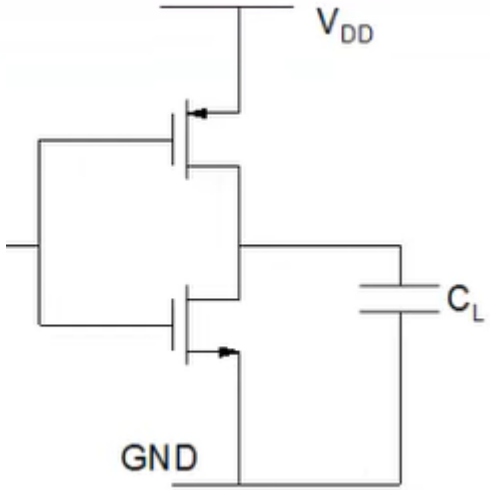
$$E_{Supply} = C_T \, V_{DD}^2$$

$$E_C = 0.5 \times C_T \, V_{DD}^2$$

$$P_{dynamic} = f \times C_T \times V_{DD}^2 = 0.22 \mu W \, / \, MHz$$

Short-circuit Power Dissipation





$$P_{SC} \cong \frac{1}{2} I_{Peak} \frac{(\tau_R + \tau_F)}{T} V_{DD}$$

- Therefore, a small rise and fall time is advantageous from both power as well as delay viewpoints

$$I_{peak} = \left(KP_N \times \frac{W_N}{L_N} \right) \times \frac{(0.5V_{DD} - V_{THN})^2}{2} = 42.25\,\mu A$$

$$P_{SC} \cong \frac{1}{2} I_{Peak} \frac{(\tau_R + \tau_F)}{2T} V_{DD} = 0.007\,\mu W / MHz$$

for $\tau_R = \tau_F = 0.1\text{ns}$

Power Reduction techniques

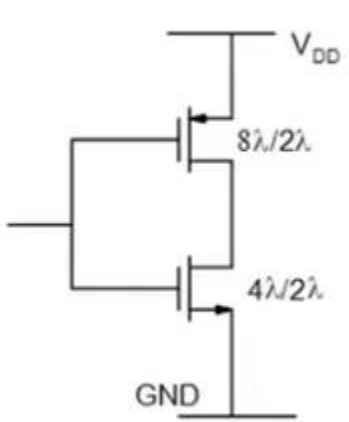
- Reducing the supply voltage:

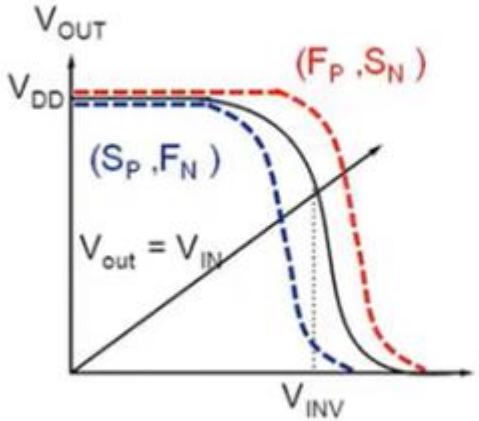
(This however, increases the propagation delay. could be countered through reduction in threshold voltage.)

- Reduce the nodal capacitance through layout techniques.

- Reduce the switching activity of nodes

CMOS Inverter : Summary



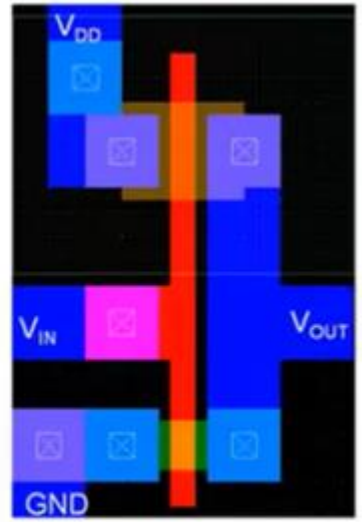


$$V_{INV} = \frac{V_{THN} + \frac{1}{\sqrt{\beta_R}}(V_{DD} + V_{THP})}{1 + \frac{1}{\sqrt{\beta_R}}}$$

$V_{inv} = 1.65V; V_{IL} = 1.48V; v_{ol} = 0V$

$V_{IH} = 1.814V; v_{oh} = 3.3V$

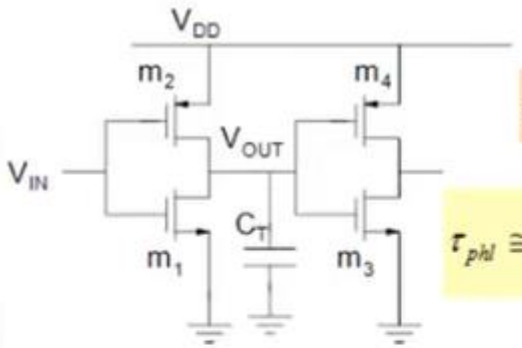
$NM_H = 1.48V; NM_L = 1.48V$



$A = 28 \times 40 = 1120\lambda^2$

$A_{DN} = 40; P_{DN} = 22$

$A_{DP} = 50; P_{DP} = 22$



$\tau_{phl}(ps) \cong 42 + a \times C_L(fF);\ a = 3.25$

$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}}$

$P_{dynamic} = f \times C_T \times V_{DD}^2$
$= 0.22\mu W / MHz$

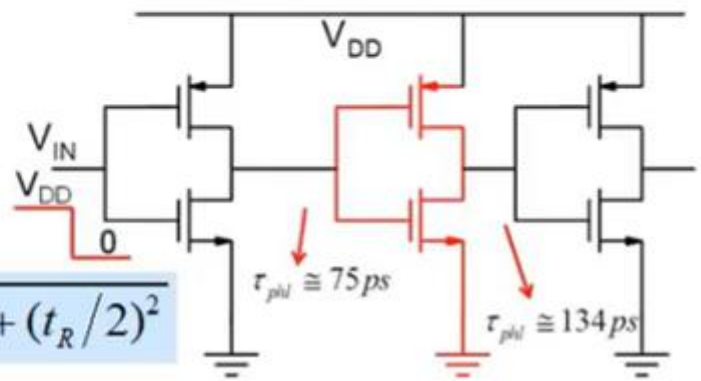
~0.3fF ~6fF ~0.6fF ~6fF

$C_T = \left(C_{gdn1} + C_{dbn1} + C_{gdp2} + C_{dbp2}\right) +$ ~13+7fF

$\left(C_{gsn3} + C_{gdn3} + C_{gbn3} + C_{gsp4} + C_{gdp4} + C_{gbp43}\right)$

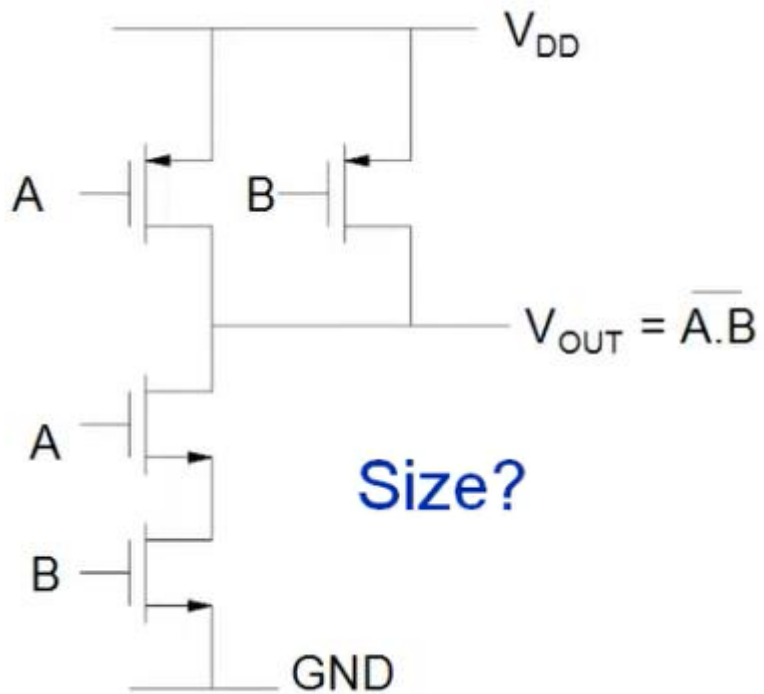
~2.0fF ~5fF

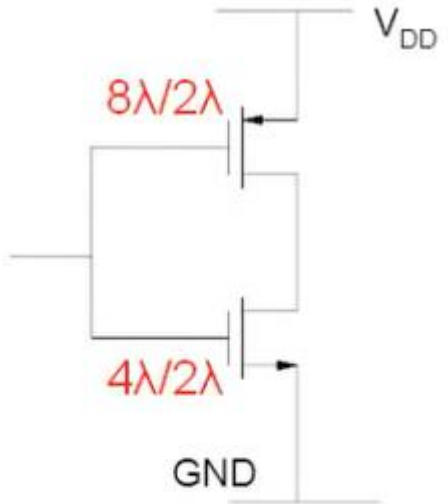
Impact of input rise/fall time



$\tau_{PHL} = \sqrt{\tau_{PHLO}^2 + (t_R/2)^2}$

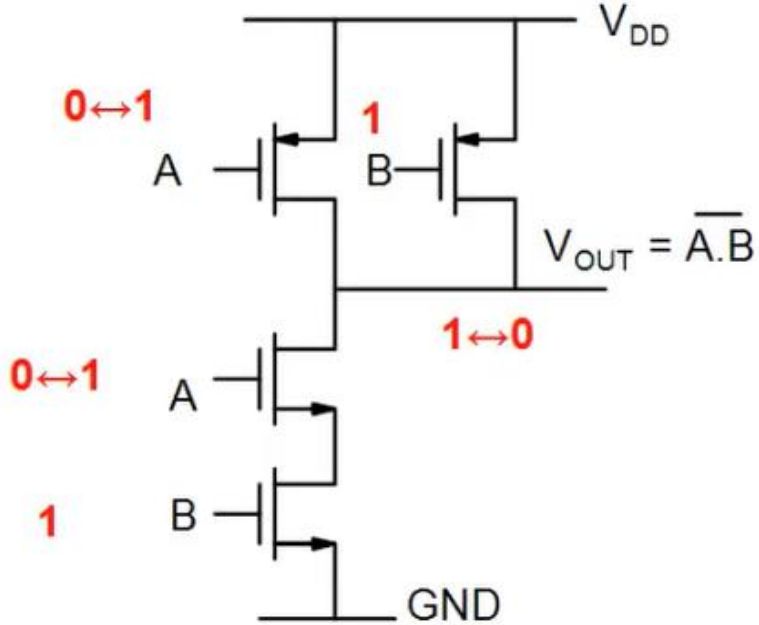
2-input CMOS NAND Gate

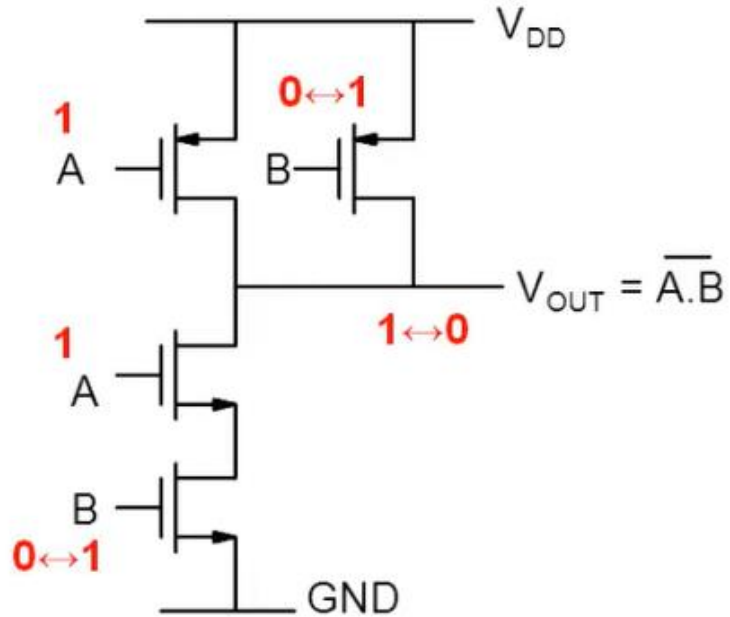


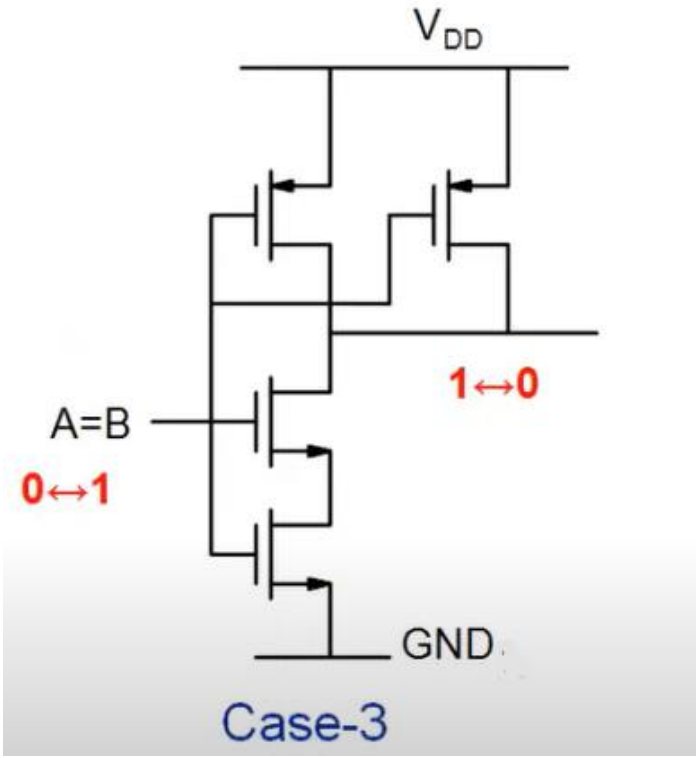


1X Inverter

1. Noise Margins
2. Delay
3. Power
4. Area

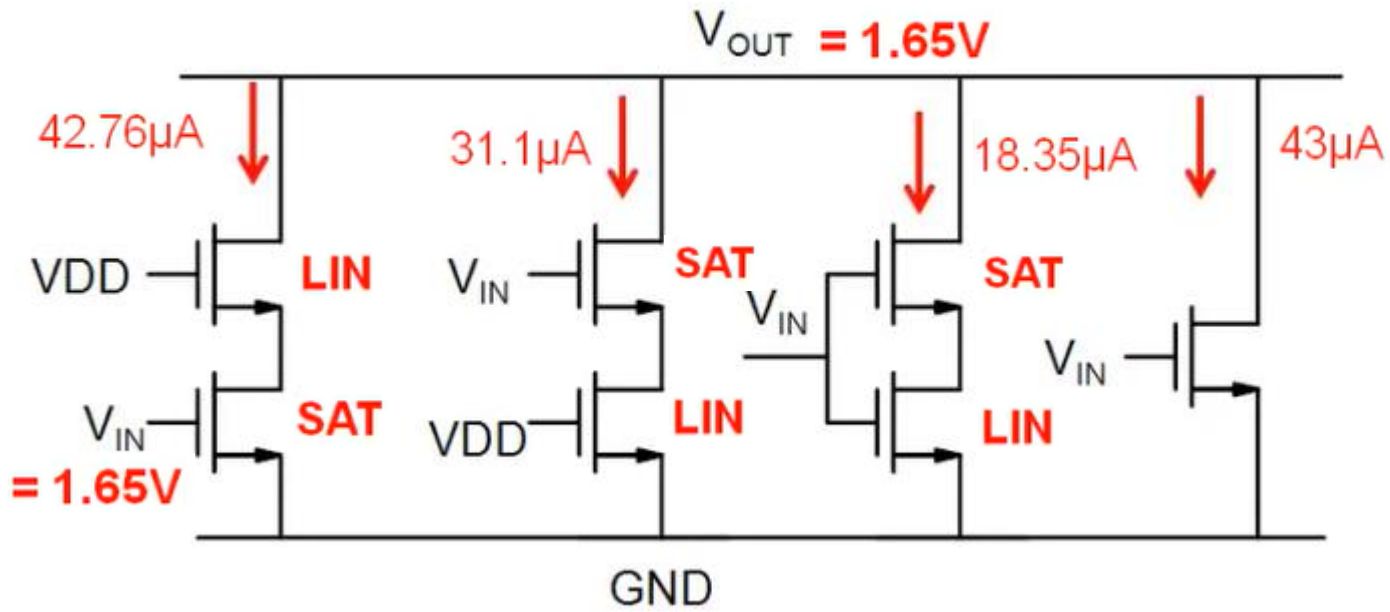

V_{DD}
0↔1
1
A
B
$V_{OUT} = \overline{A.B}$
1↔0
0↔1
A
1
B
GND

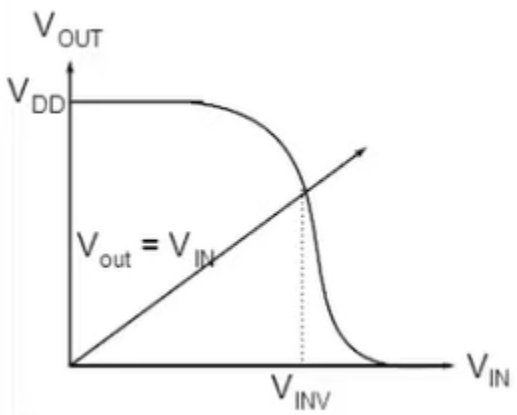

V_{DD}
0↔1
1
A
B
$V_{OUT} = \overline{A.B}$
1↔0
1
A
B
0↔1
GND


V_{DD}
1↔0
A=B
0↔1
GND
Case-3

Series Connected Transistors

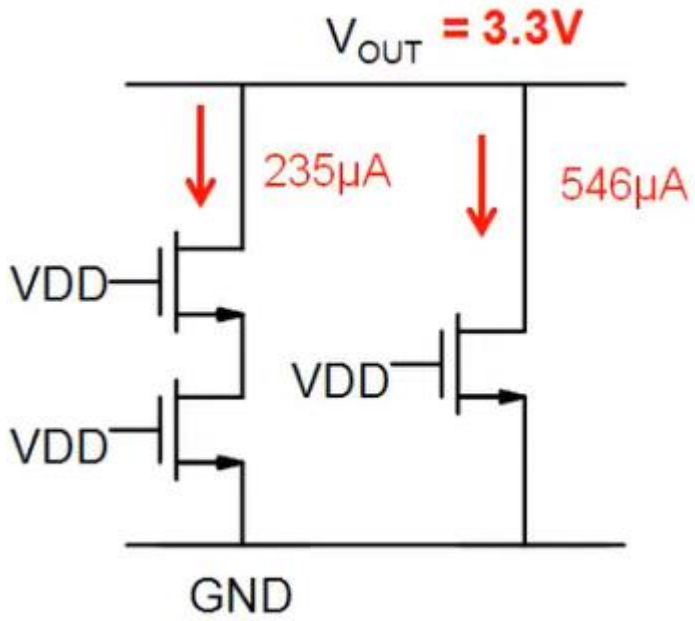
All transistors are 4λ/2λ

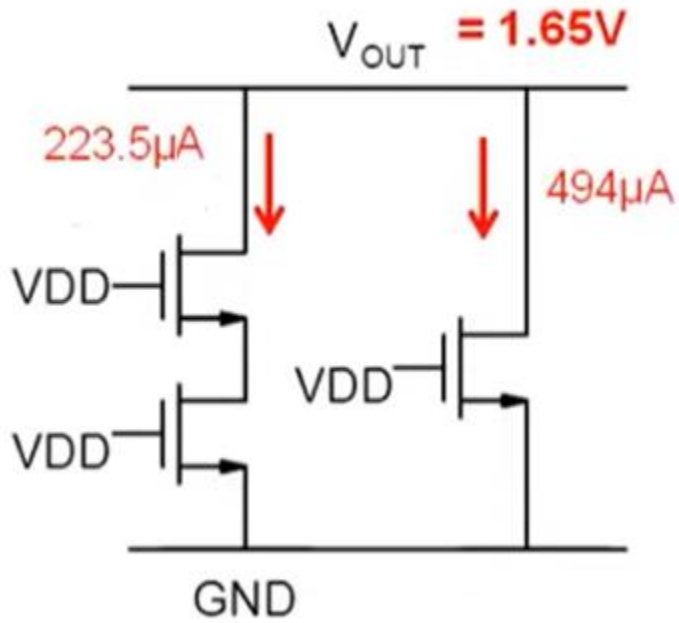


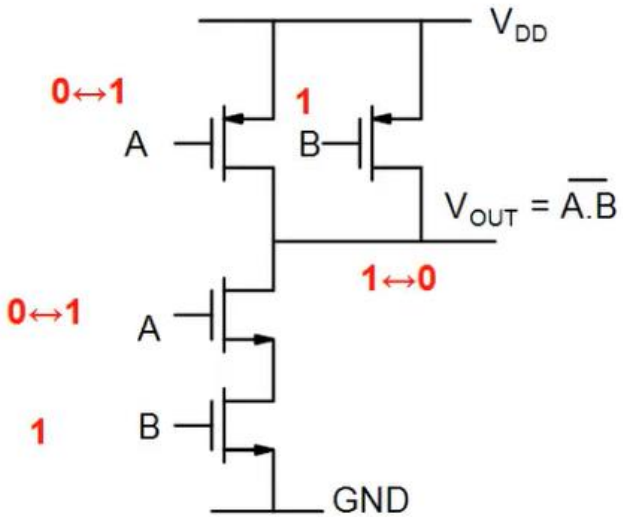


Series Connected Transistors

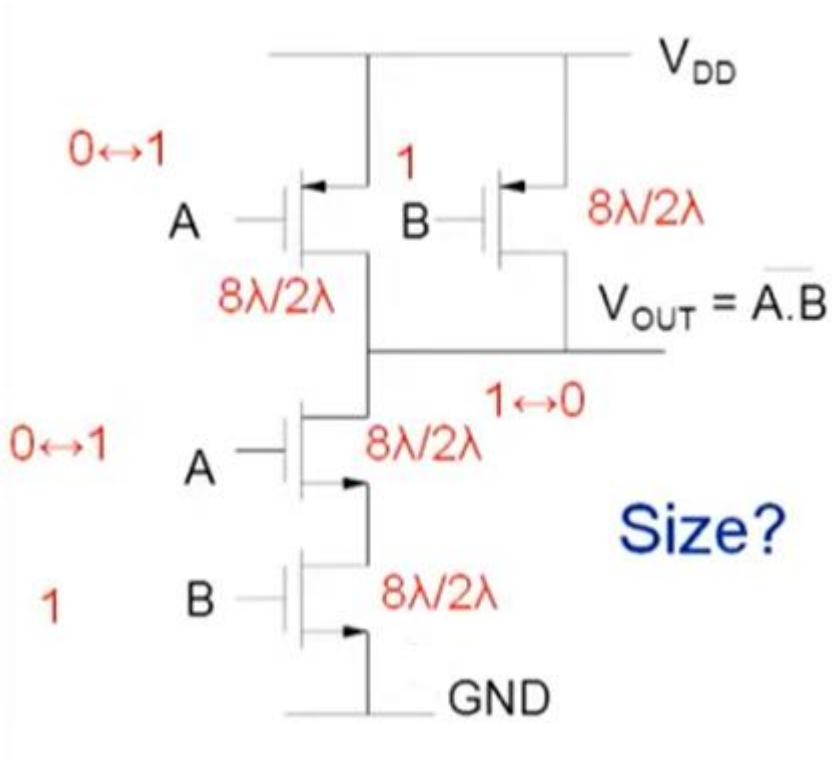
All transistors are 4λ/2λ

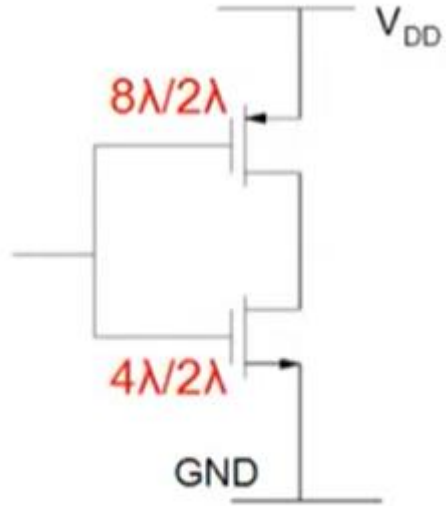






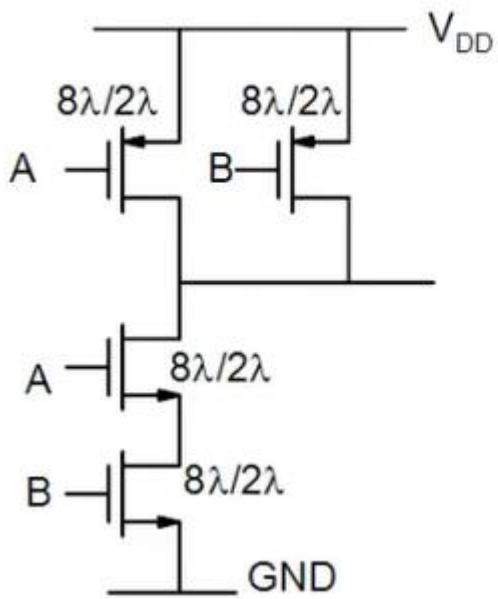
2-input CMOS NAND Gate

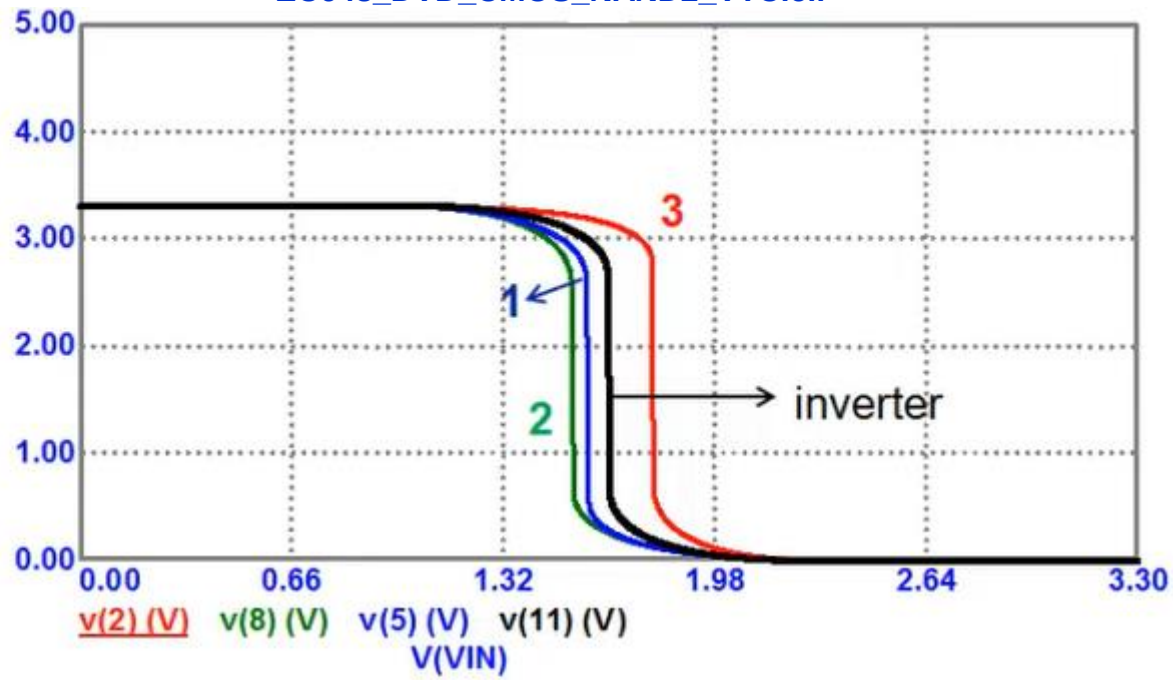


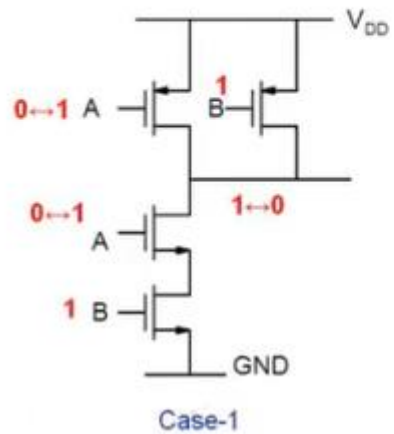


1X Inverter

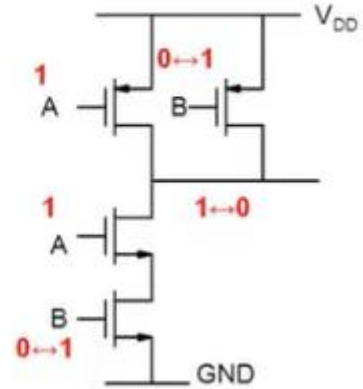
EC643_DVD_CMOS_NAND2_VTC.cir



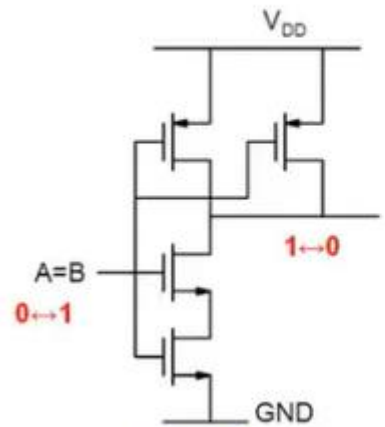




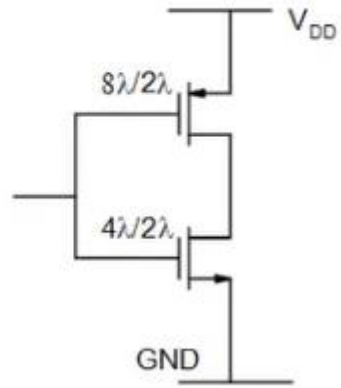
Case-1



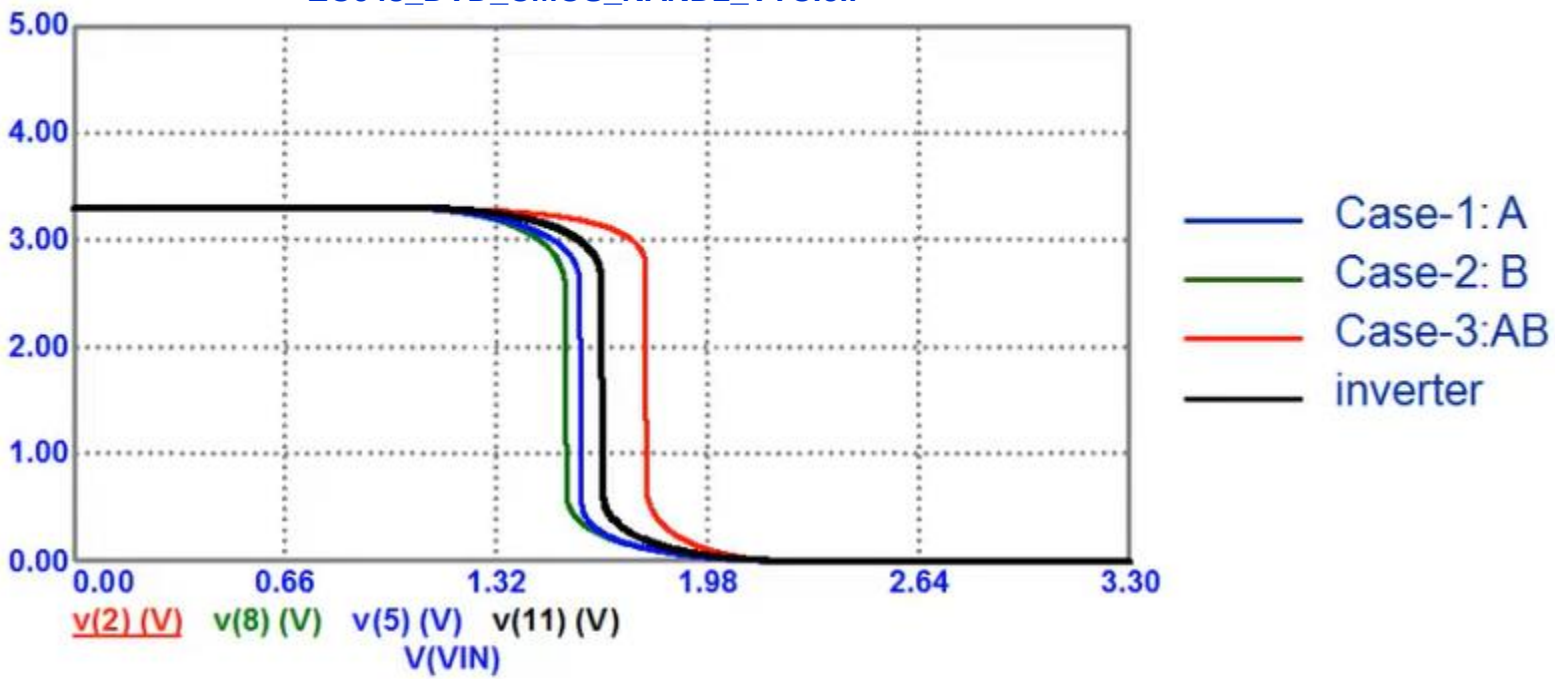
Case-2



Case-3



EC643_DVD_CMOS_NAND2_VTC.cir



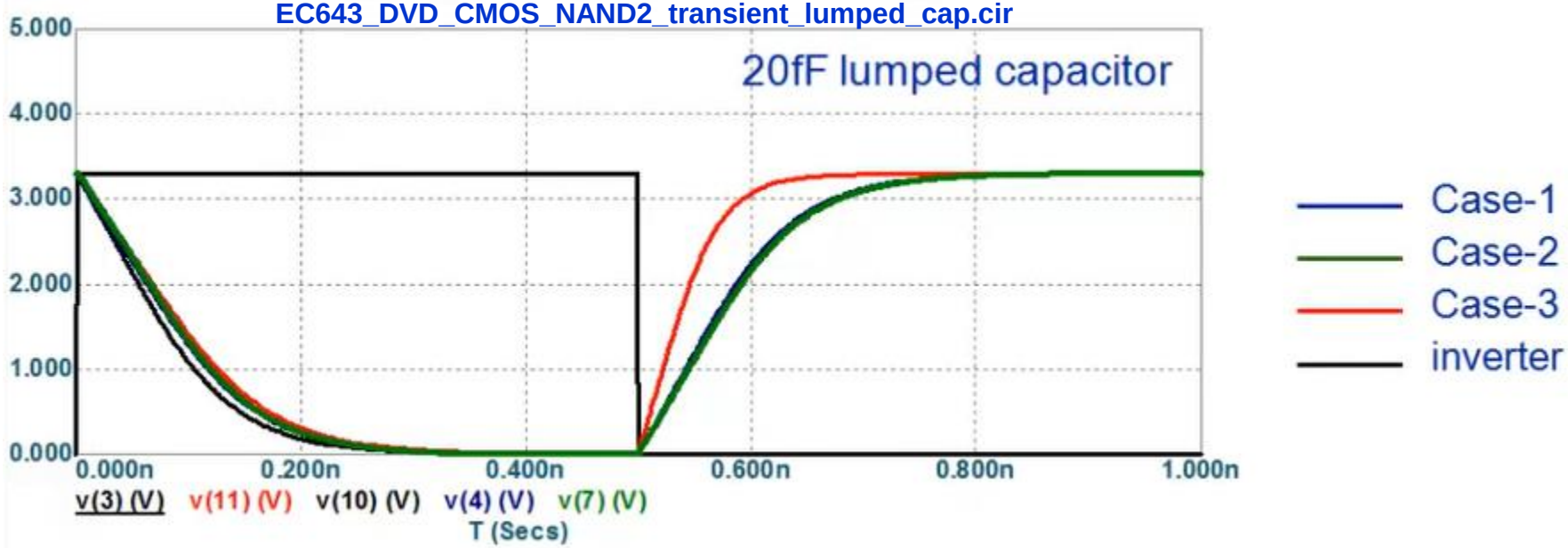
Case-1 (A): V_{inv}=1.58V ;V_{IL}=1.4V; V_{IH}=1.72V

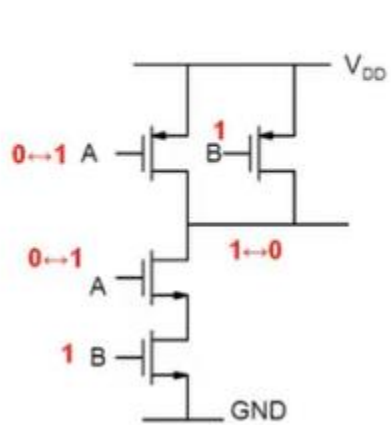
Case-2(B): V_{inv}=1.53V ;V_{IL}=1.35V; V_{IH}=1.7V

Case-3 (AB): V_{inv}=1.78V ;V_{IL}=1.67V; V_{IH}=1.96V

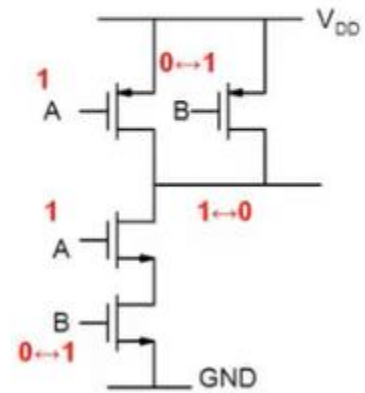
Inverter: V_{inv}=1.65V ;V_{IL}=1.48V; V_{IH}=1.814V

EC643_DVD_CMOS_NAND2_transient_lumped_cap.cir

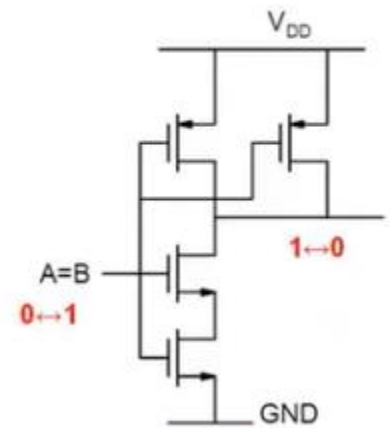




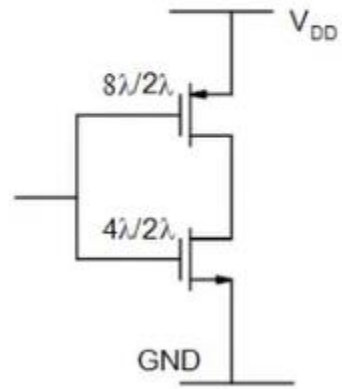
Case-1

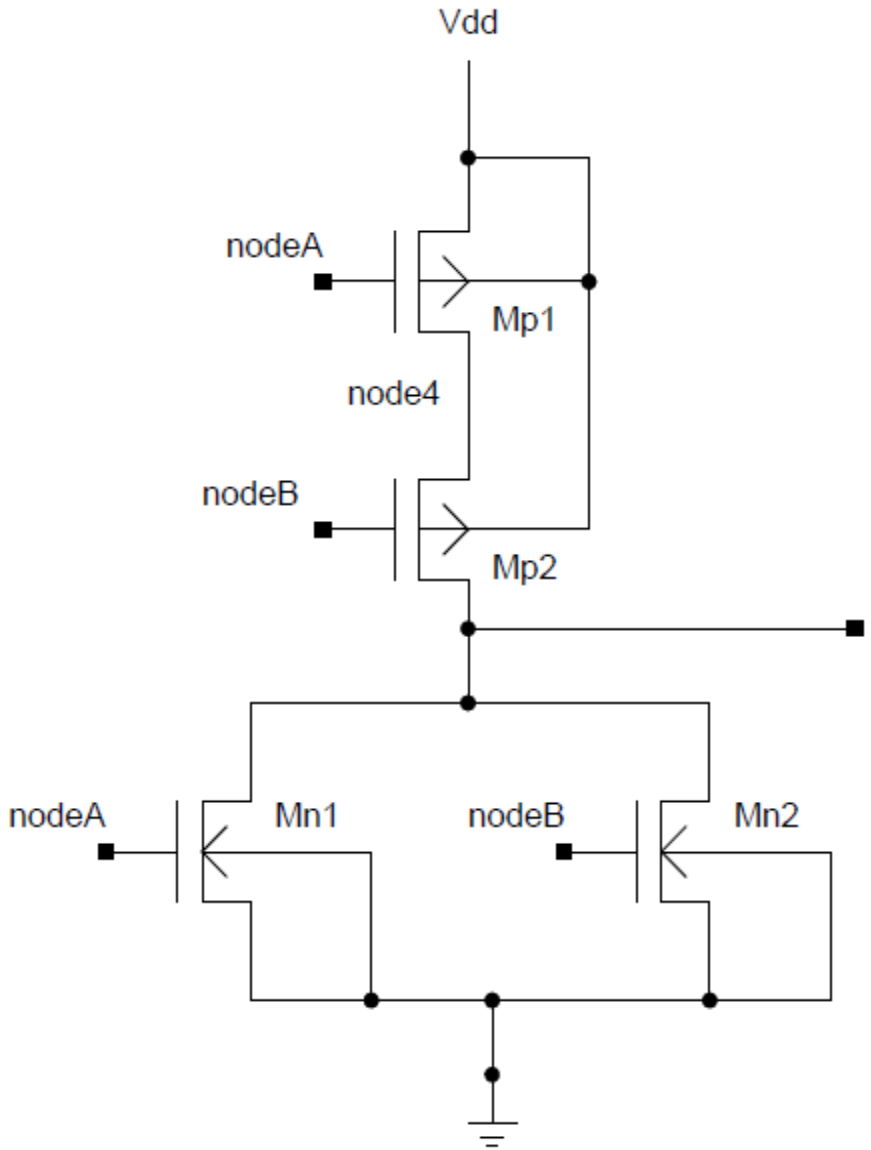


Case-2

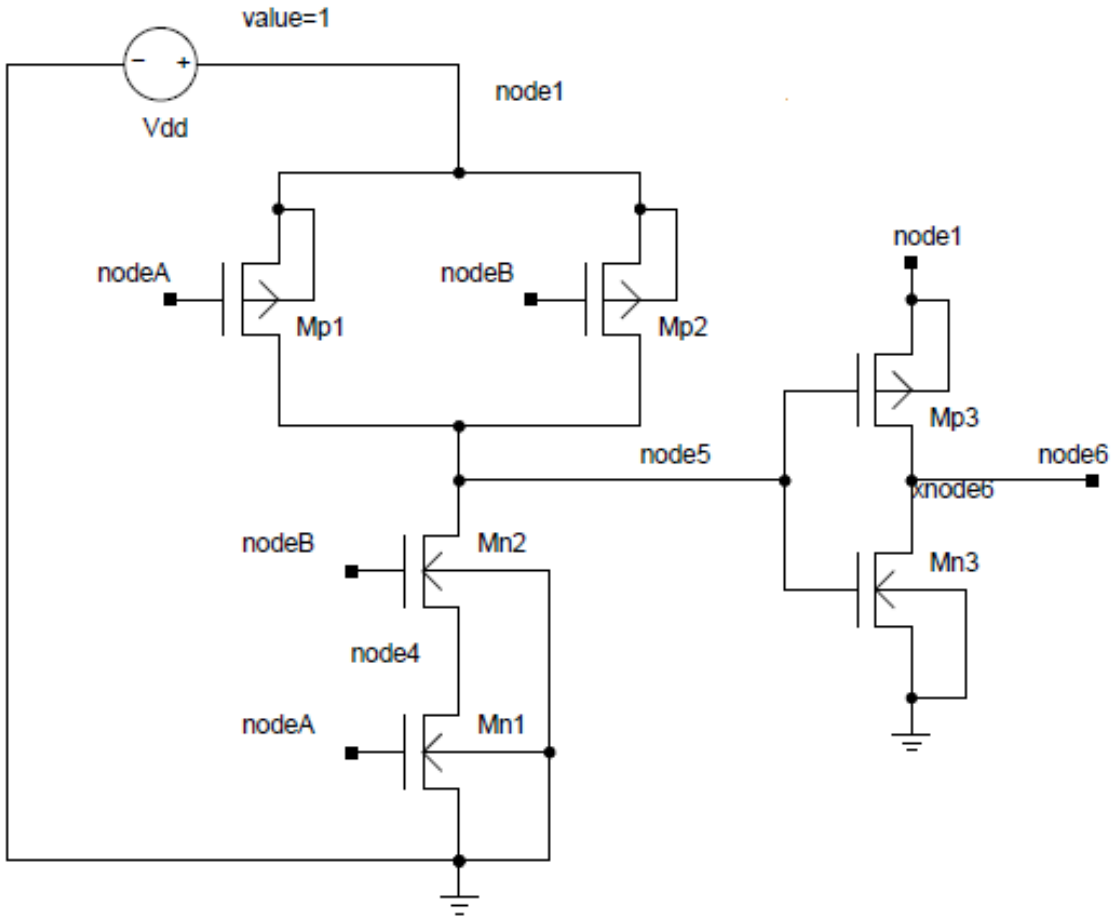


Case-3

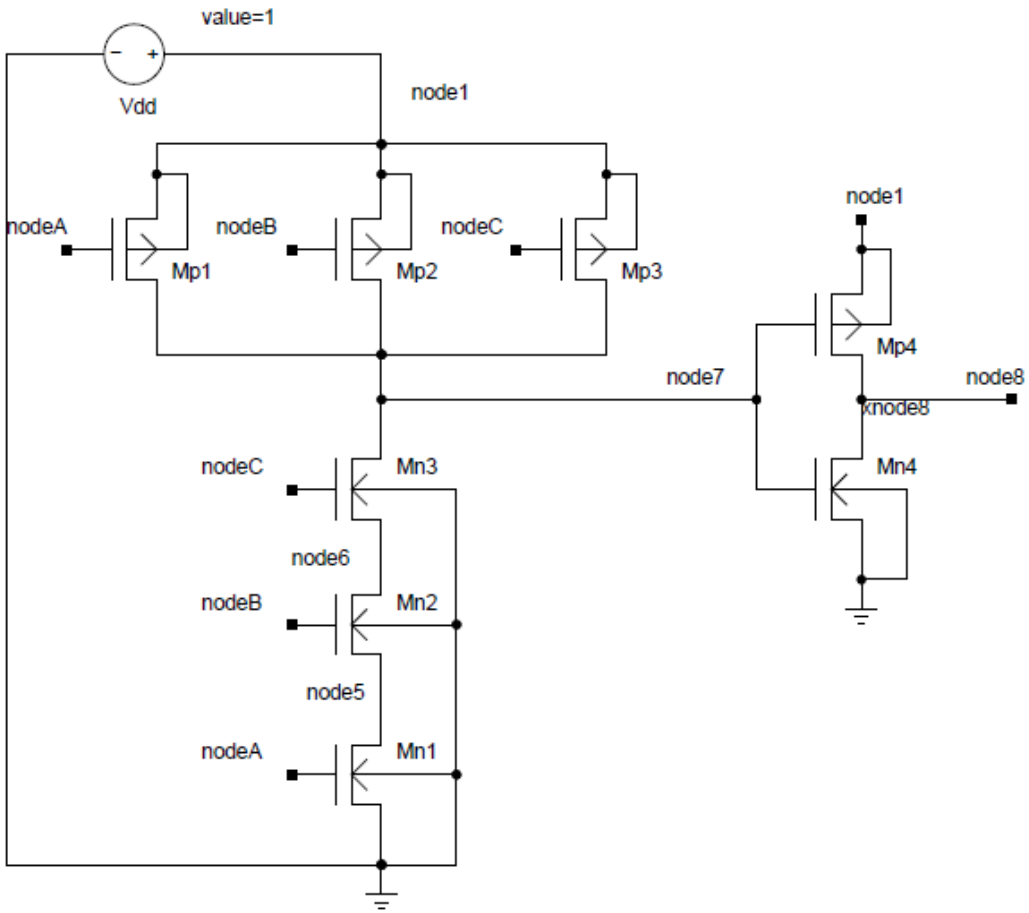




NOR2

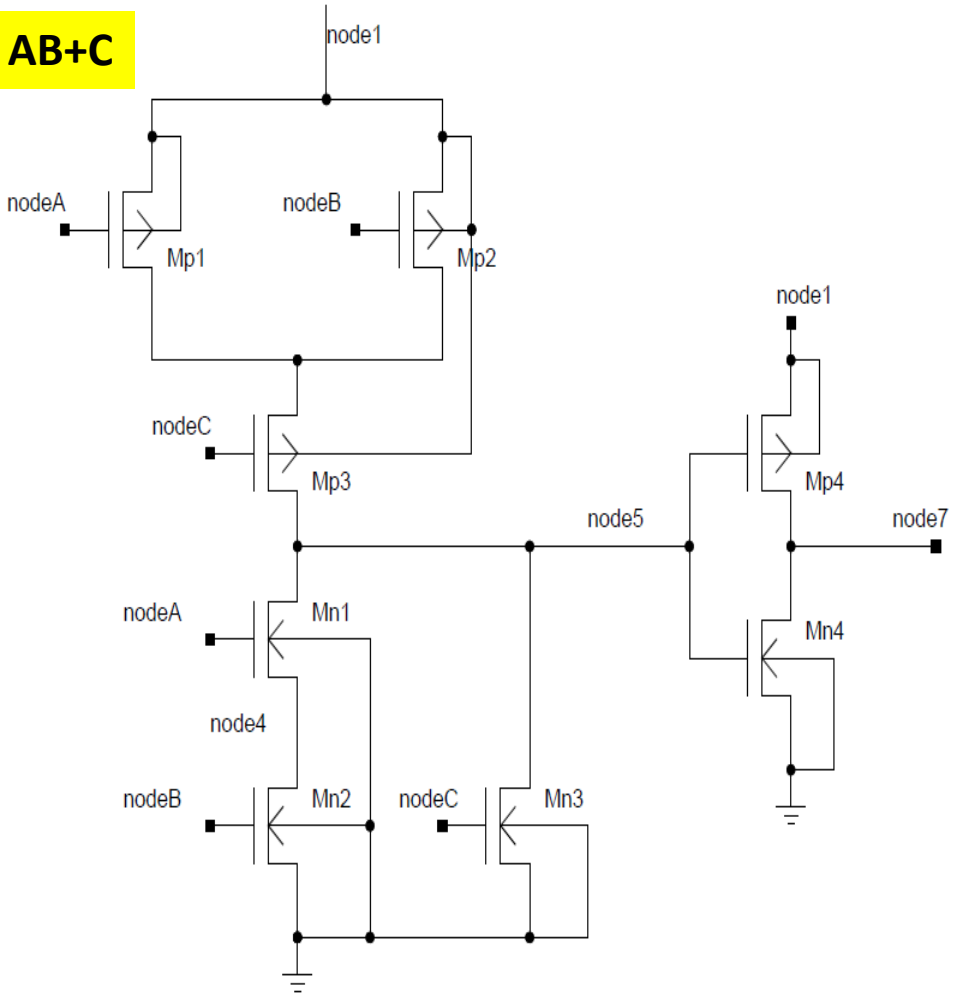

value=1
Vdd
node1
nodeA
Mp1
nodeB
Mp2
node1
Mp3
node5
node6
xnode6
nodeB
Mn2
Mn3
node4
nodeA
Mn1

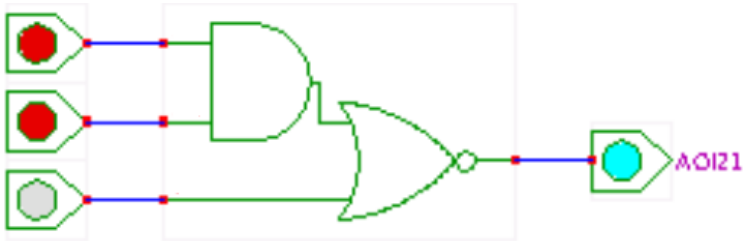
AND2


value=1
Vdd
node1
nodeA
Mp1
nodeB
Mp2
nodeC
Mp3
node1
Mp4
node7
node8
xnode8
nodeC
Mn3
Mn4
node6
nodeB
Mn2
node5
nodeA
Mn1

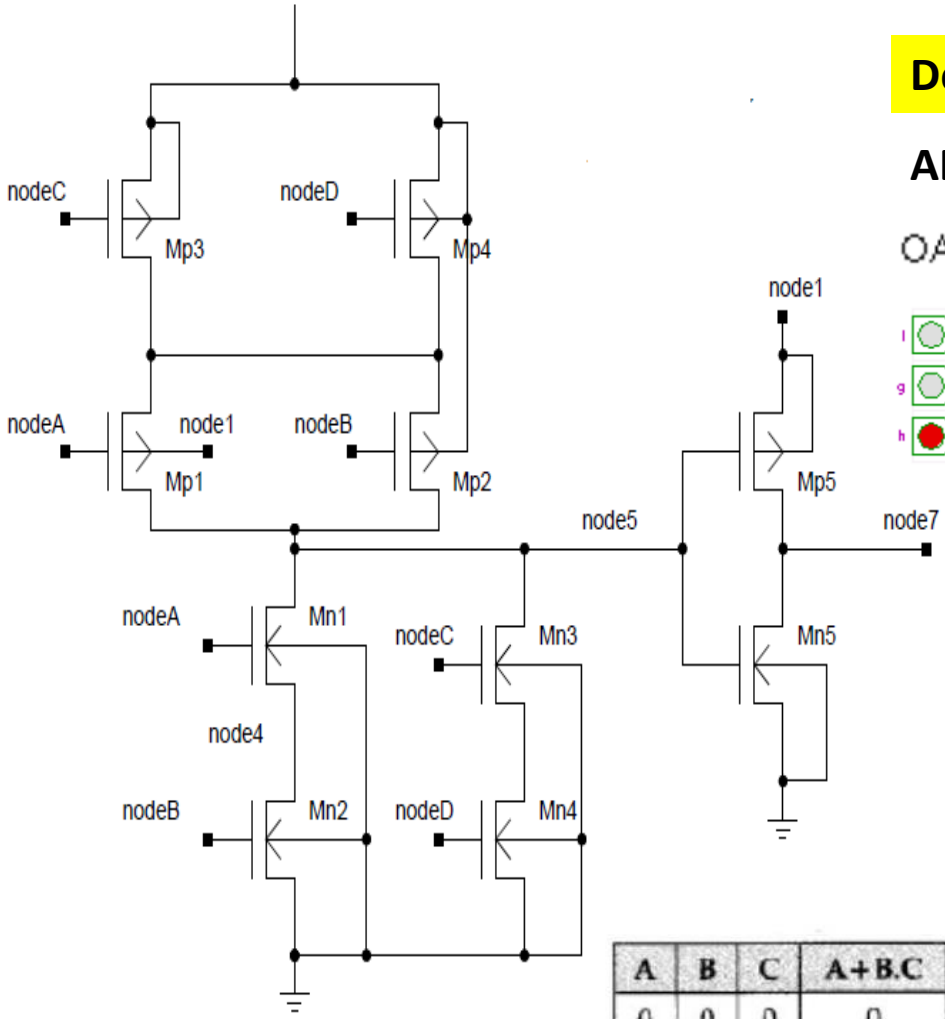
AND3

AB+C





AO12

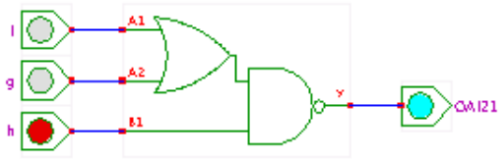


AO22

Design

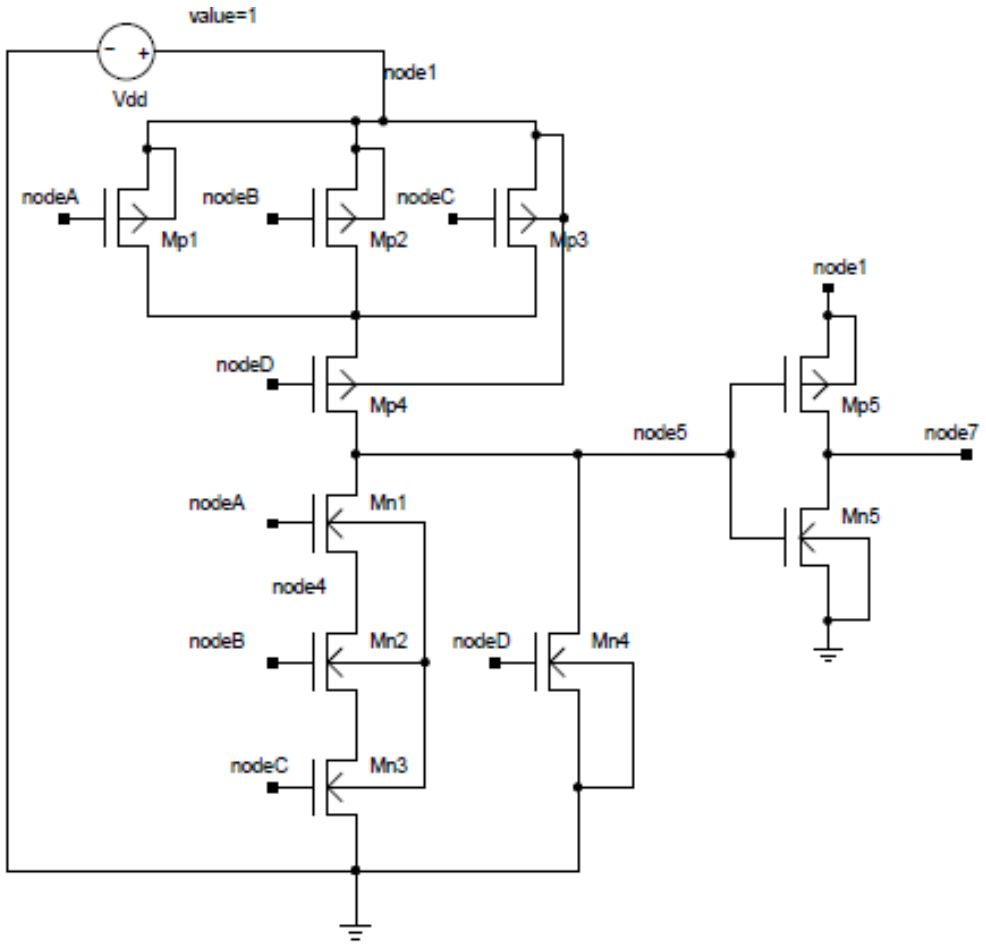
ABC+DE

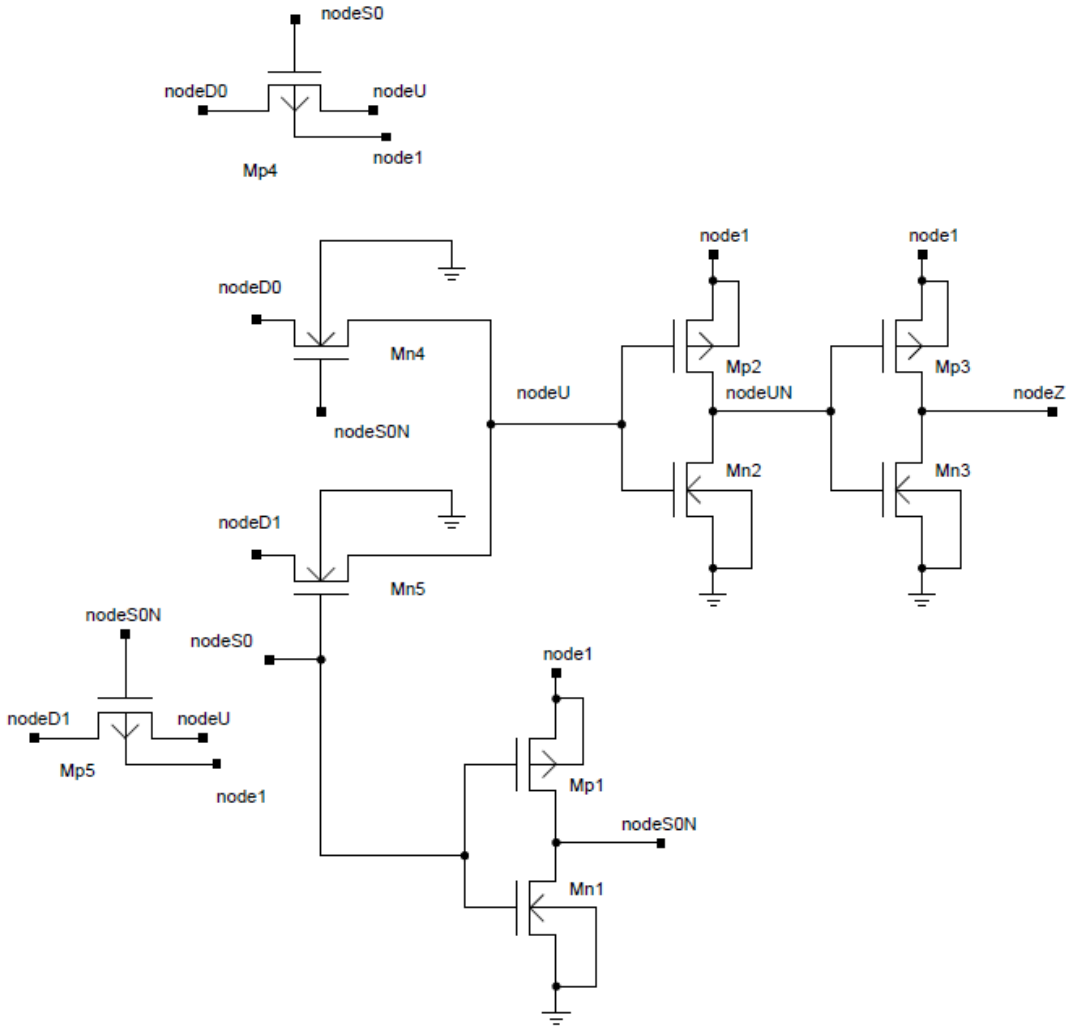
OAI21 (Or-And-Invert)



A	B	C	A+B.C	A+B	A+C	(A+B).(A+C)
0	0	0	0	0	0	0
0	0	1	0	0	1	0
0	1	0	0	1	0	0
0	1	1	1	1	1	1
1	0	0	1	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

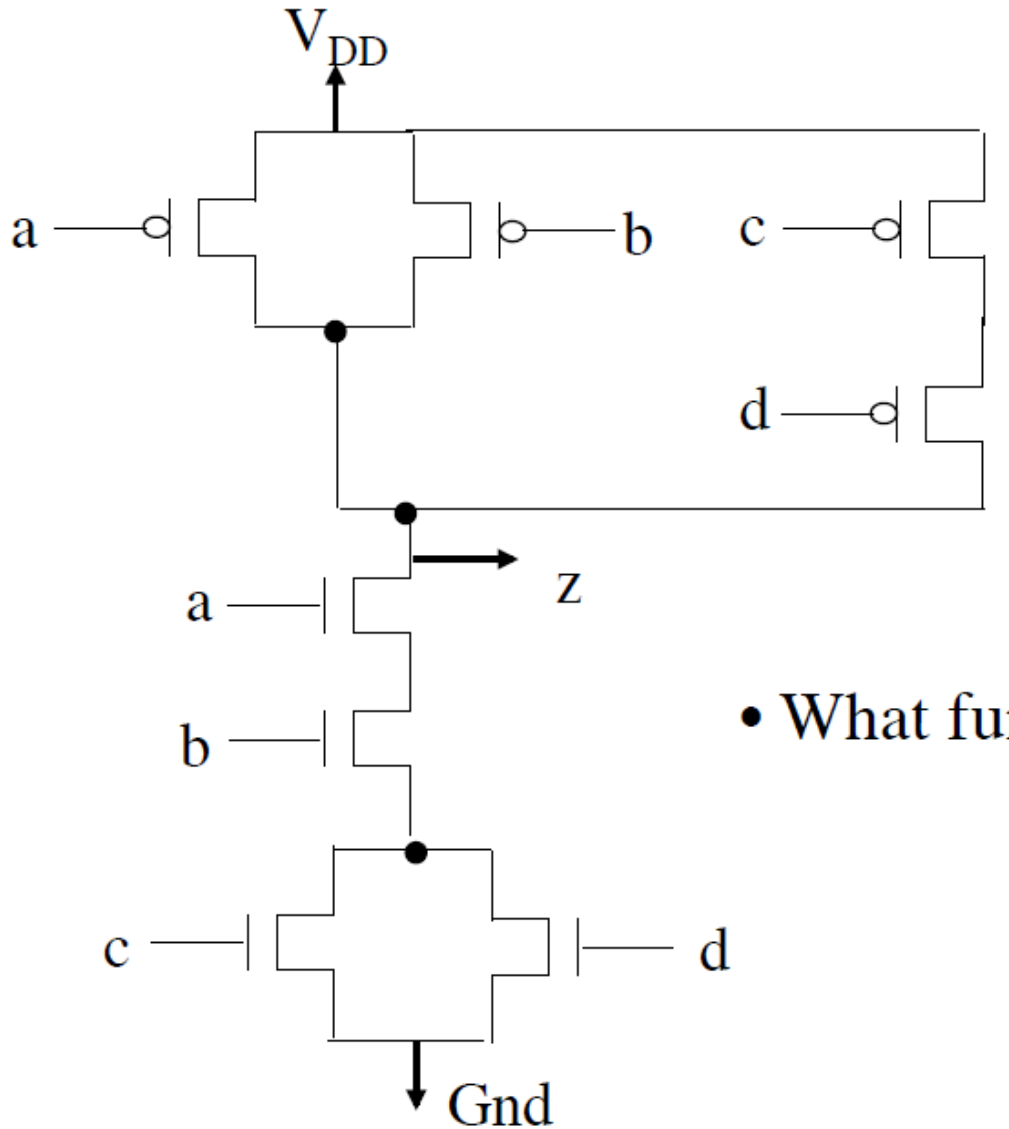
AO31





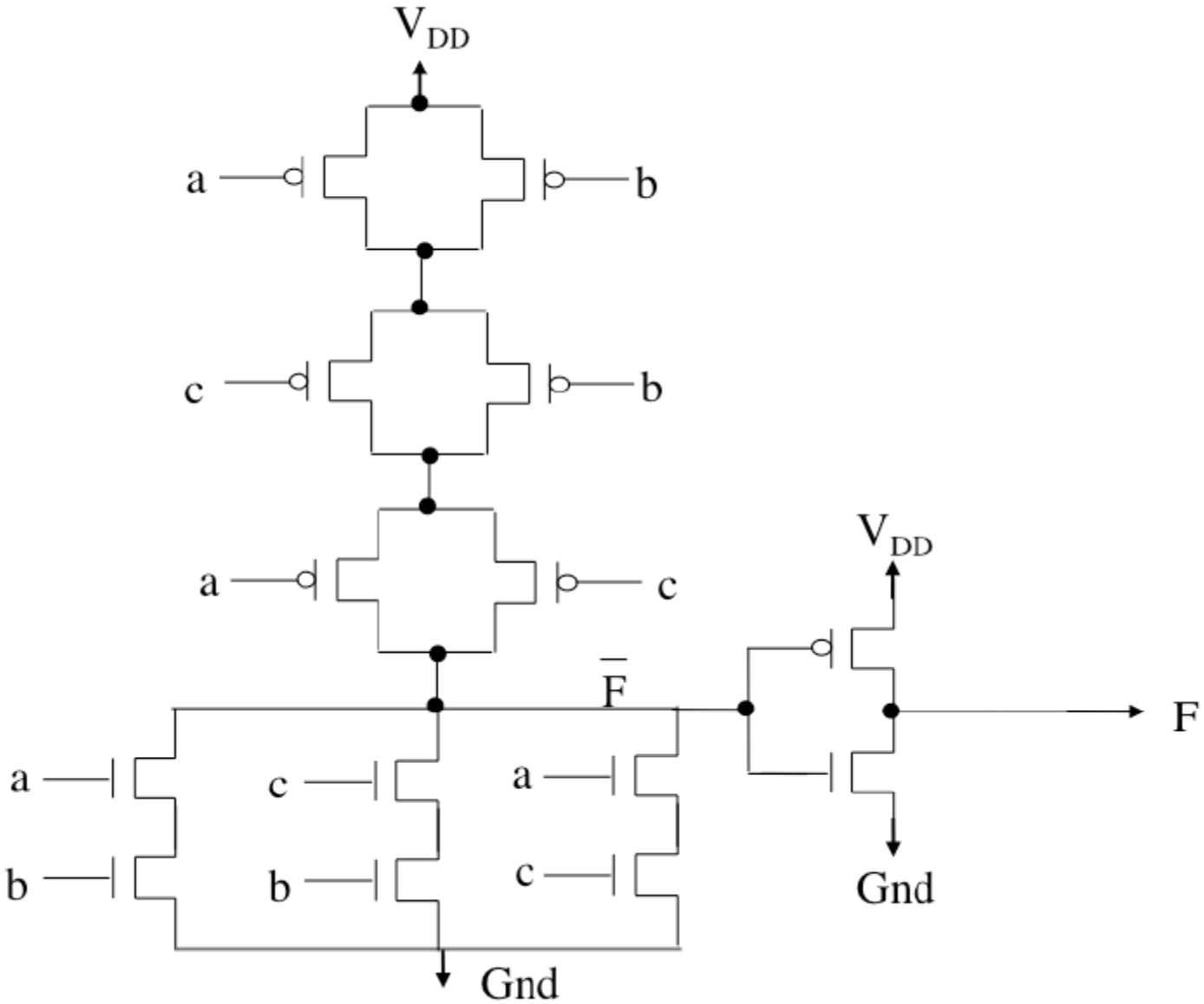
2:1 MUX

How to design? $Y = \overline{(A + B + C) \bullet D}$



- What function is implemented by this circuit?

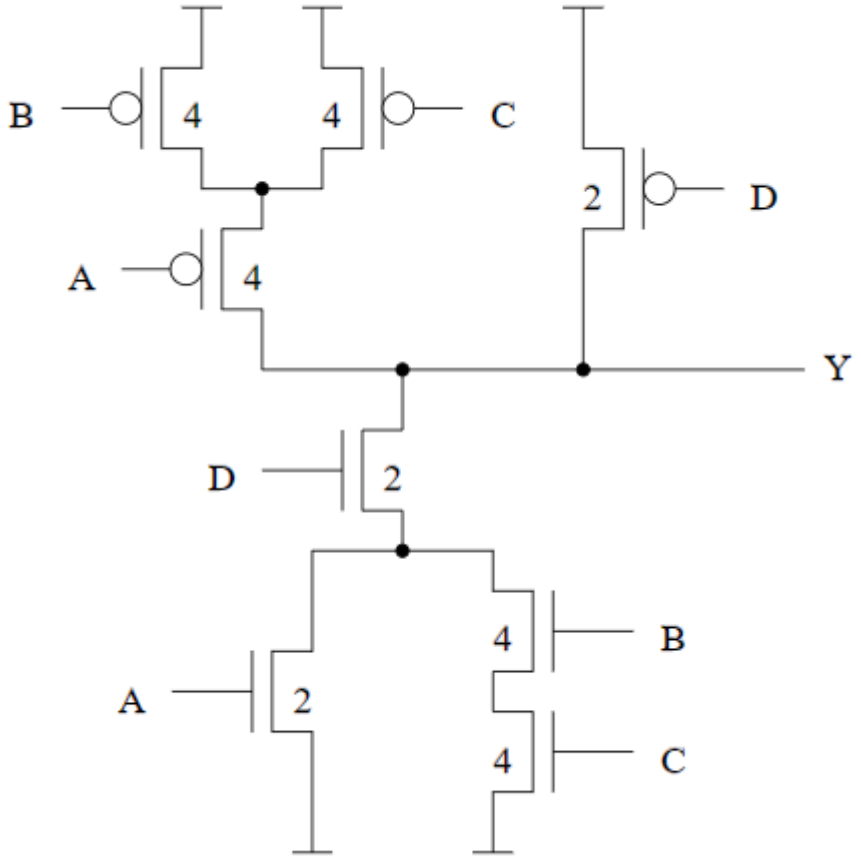
How to implement
F = ab + bc + ca?

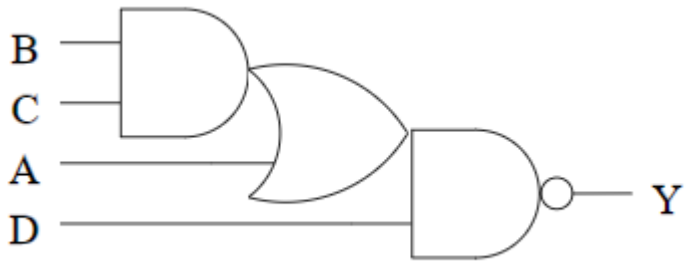


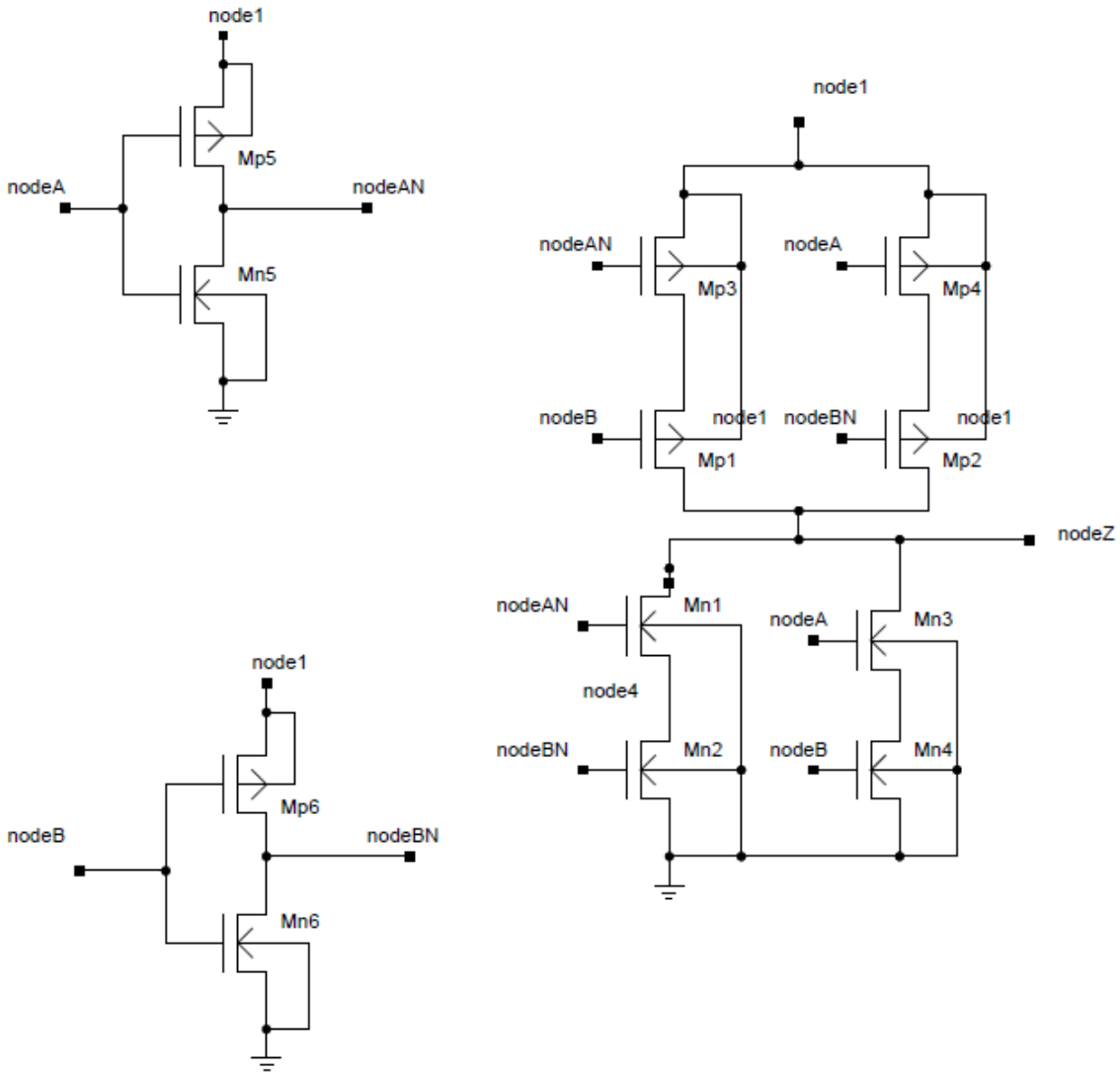
Besides the AOI and OAI gates for complemented two-level normal forms, we can design compound gates for multilevel expressions as well. For example, Boolean expression

$$Y = \overline{(A + BC) \cdot D}$$

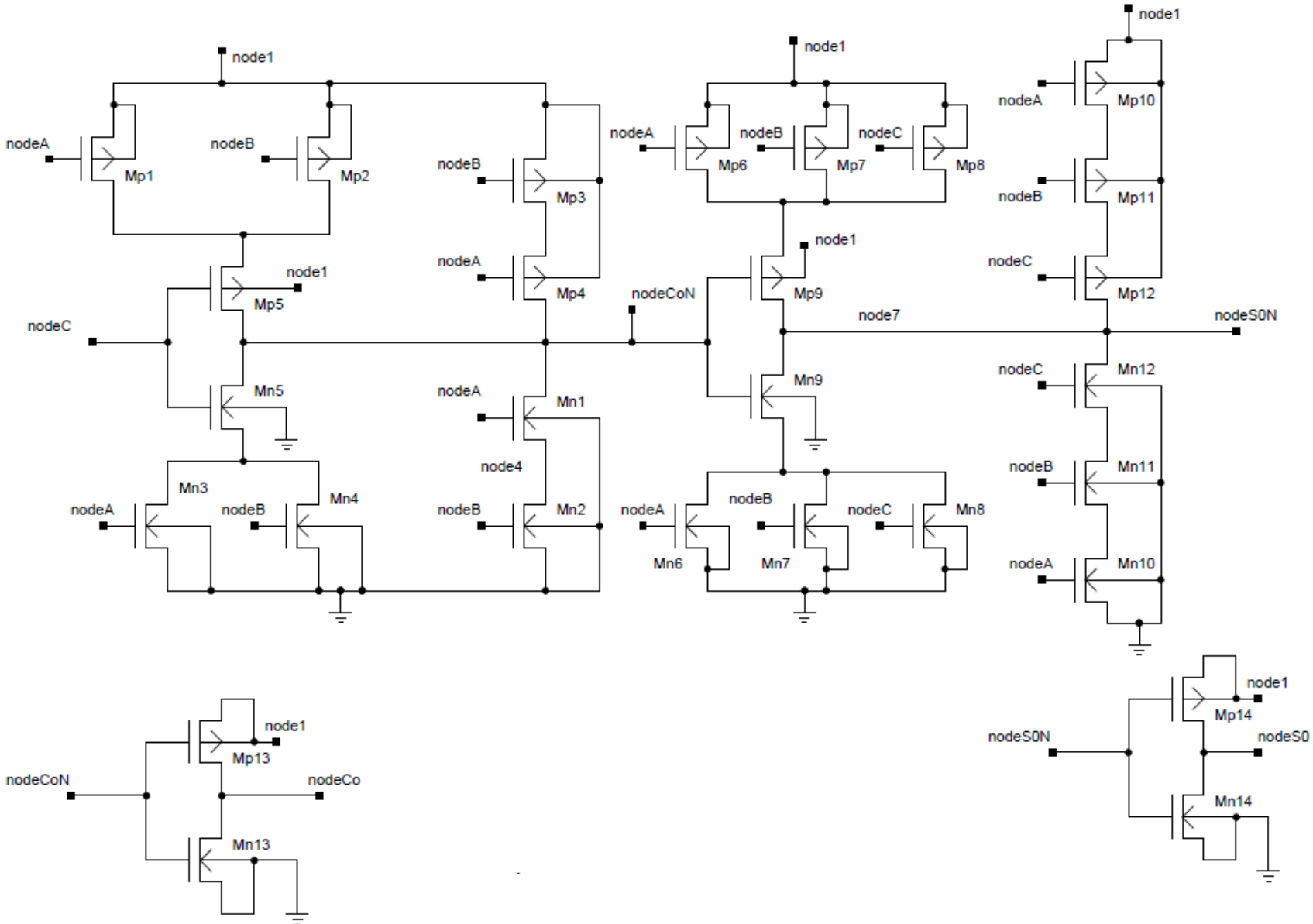
has a pull-down network consisting of a series composition of D and a parallel composition of A and a series composition of B and C.



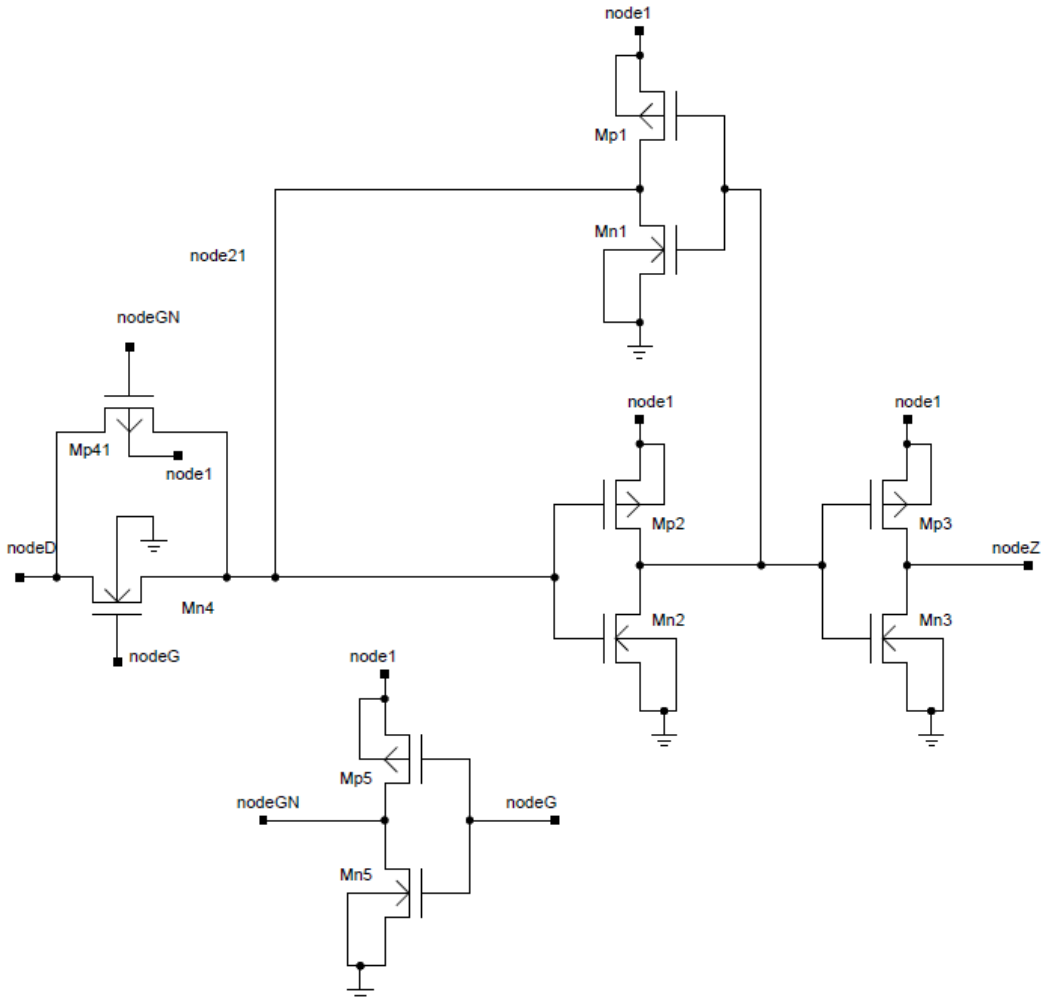



node1
Mp5
nodeA
nodeAN
Mn5
node1
nodeAN
nodeA
Mp3
Mp4
nodeB
node1
nodeBN
node1
Mp1
Mp2
nodeZ
nodeAN
Mn1
nodeA
Mn3
node4
nodeBN
Mn2
nodeB
Mn4
node1
Mp6
nodeB
nodeBN
Mn6

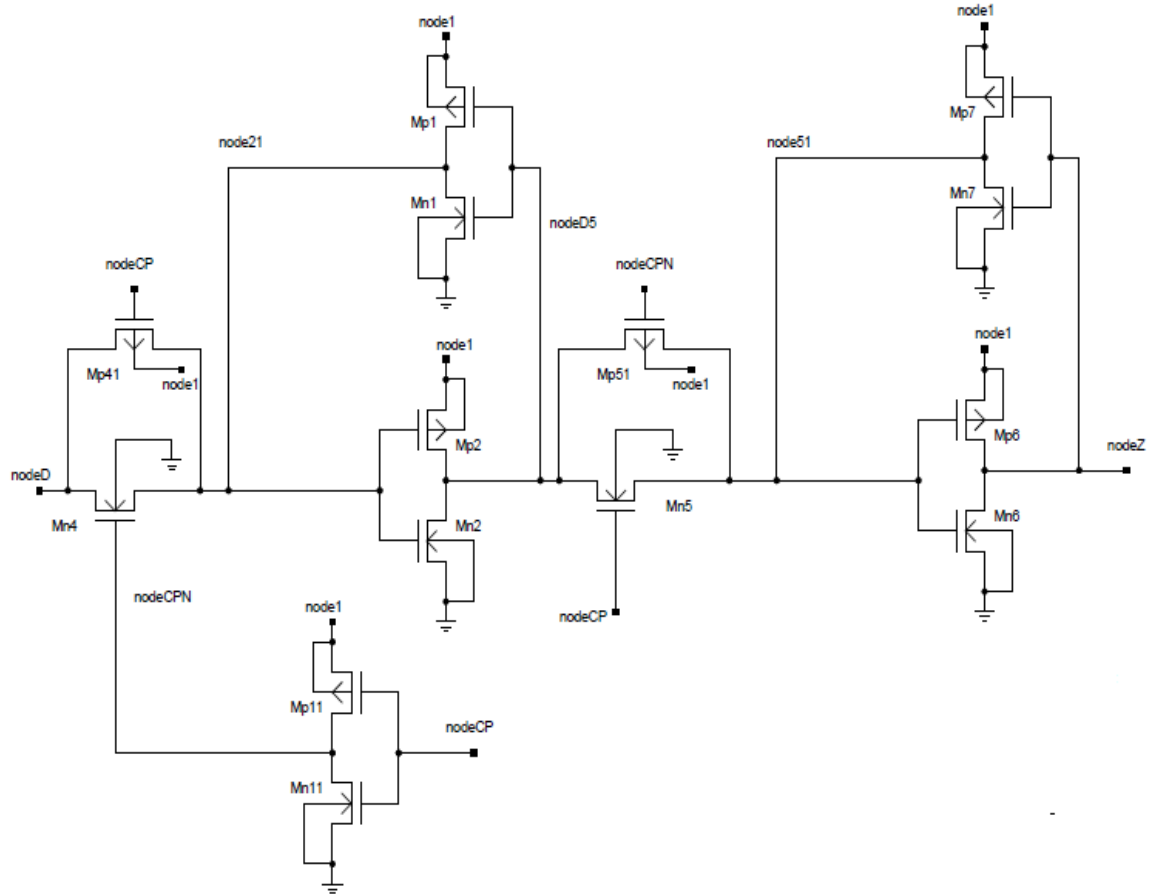
XOR2


node1
nodeA
nodeB
Mp1
Mp2
Mp3
Mp4
Mp5
nodeC
Mn5
Mn3
Mn4
Mn1
Mn2
node4
Mp6
Mp7
Mp8
nodeCoN
Mp9
Mn9
Mn6
Mn7
Mn8
node7
Mp10
Mp11
Mp12
nodeS0N
Mn12
Mn11
Mn10
Mp13
nodeCo
Mn13
Mp14
nodeS0
Mn14

Full Adder


node1
Mp1
Mn1
node21
nodeGN
Mp41
node1
nodeD
Mn4
nodeG
node1
Mp2
Mn2
node1
Mp3
Mn3
nodeZ
node1
Mp5
nodeGN
nodeG
Mn5

LDHQ


node1
Mp1
node21
Mn1
nodeD5
nodeCP
Mp41
node1
nodeD
Mn4
nodeCPN
node1
Mp2
Mn2
nodeCPN
Mp51
node1
Mn5
nodeCP
node51
node1
Mp7
Mn7
node1
Mp6
Mn6
nodeZ
node1
Mp11
nodeCP
Mn11

DFPQ