International Institute of Information Technology – Hyderabad

EC2.201 – VLSI Design

Quiz 2
Max Marks – 40
Max Time – 60 minutes

Questions

1. Draw transistor level schematic, stick diagram and layout of a 3 input XOR gate in complementary CMOS logic using 8 nmos and 8 pmos transistors. Minimize the diffusion points in stick diagram and area of layout. Display the dimensions and spacing in units of λ. Finally write the area of your layout. **(20)**

2. Mention step by step fabrication process with the help of cross-section diagrams to achieve a CMOS 2 input NOR gate using n-well CMOS process. Mention number of masks required and draw clear and dark fields for each mask.

   (20)