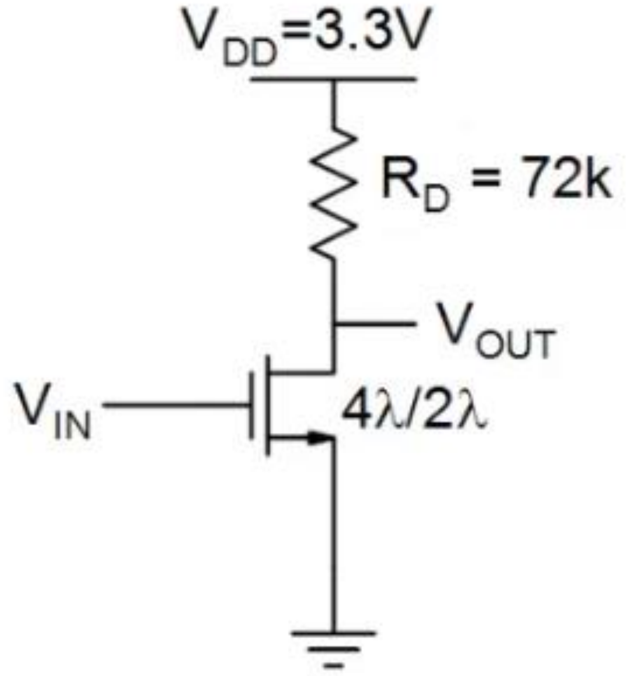
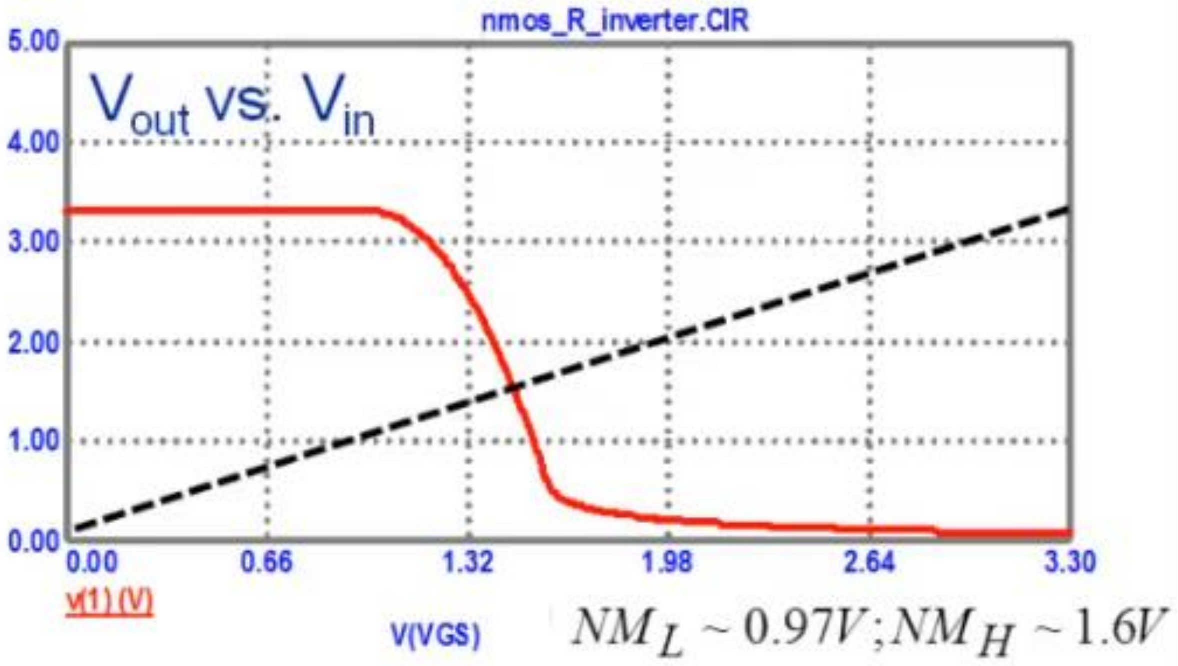




$NM_L \sim 0.97V; NM_H \sim 1.6V$

$$V_{out} = V_{in}$$

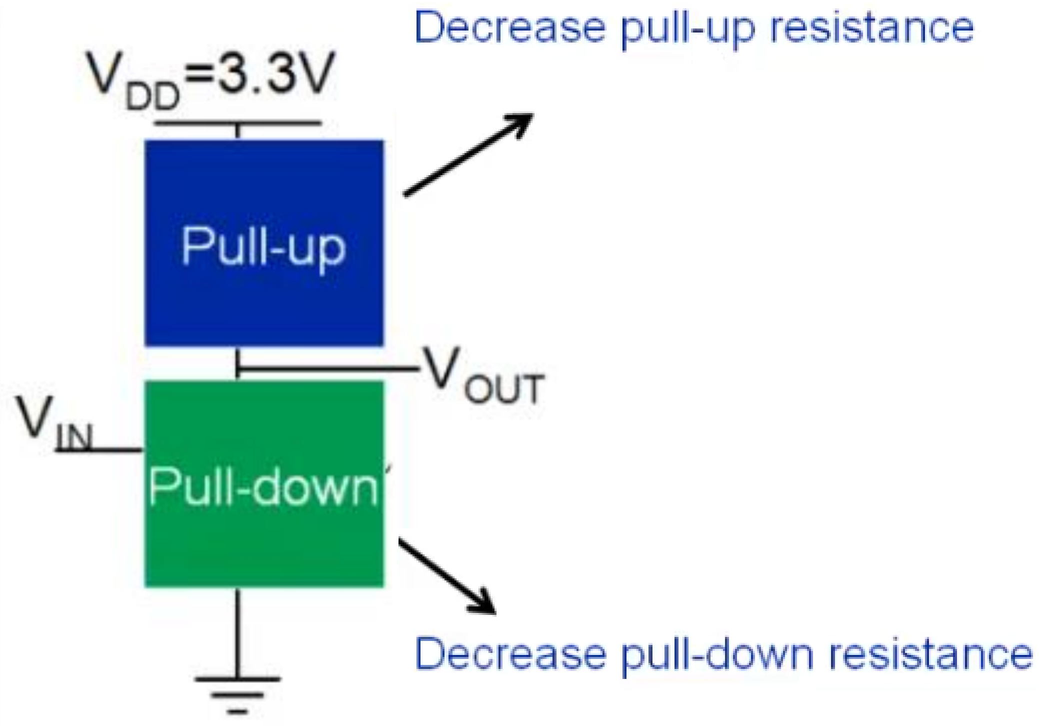
Transistor in saturation

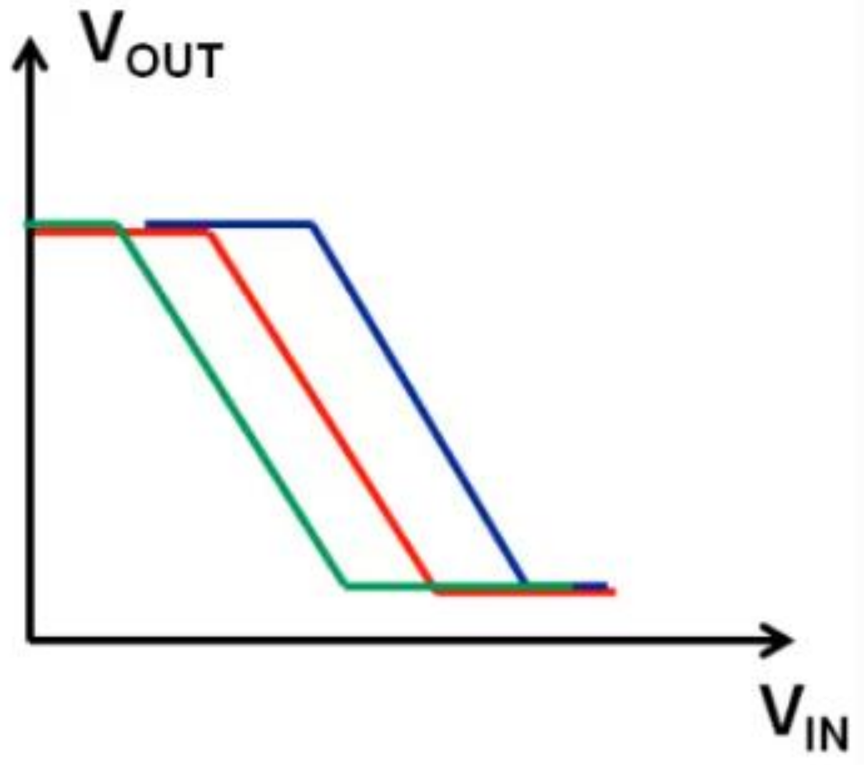
$$I_{DS} = \left(KP_N \times \frac{W}{L}\right) \times \frac{(V_{out} - V_{THN})^2}{2} = \frac{V_{DD} - V_{out}}{R_D}$$

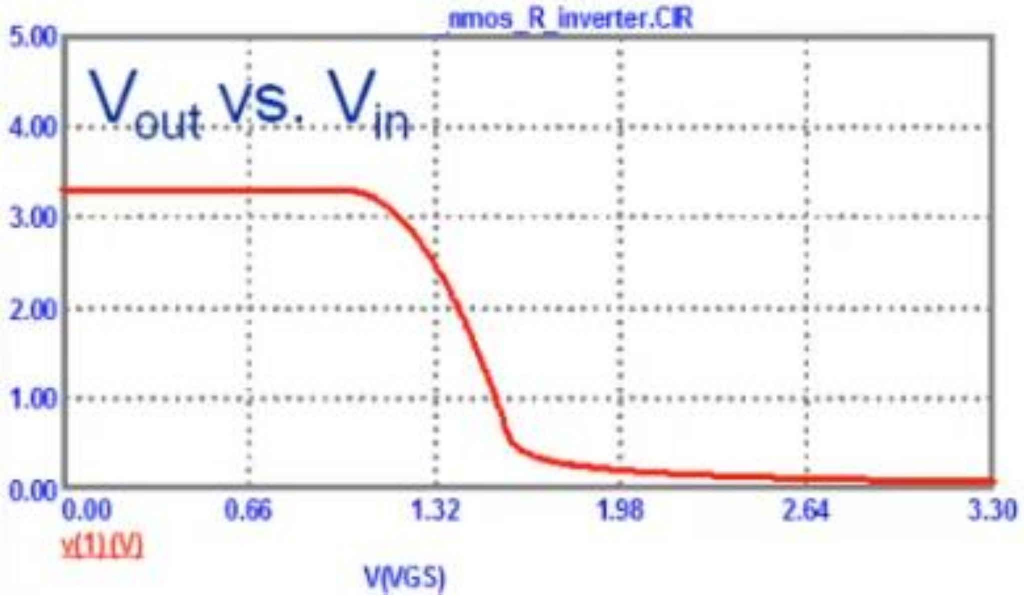
For R_D = 72k, $V_{out} = V_{in} = V_{inv} = 1.5V$

Shift characteristics to right to improve NM_L

1. Decrease R_D
2. Decrease W/L

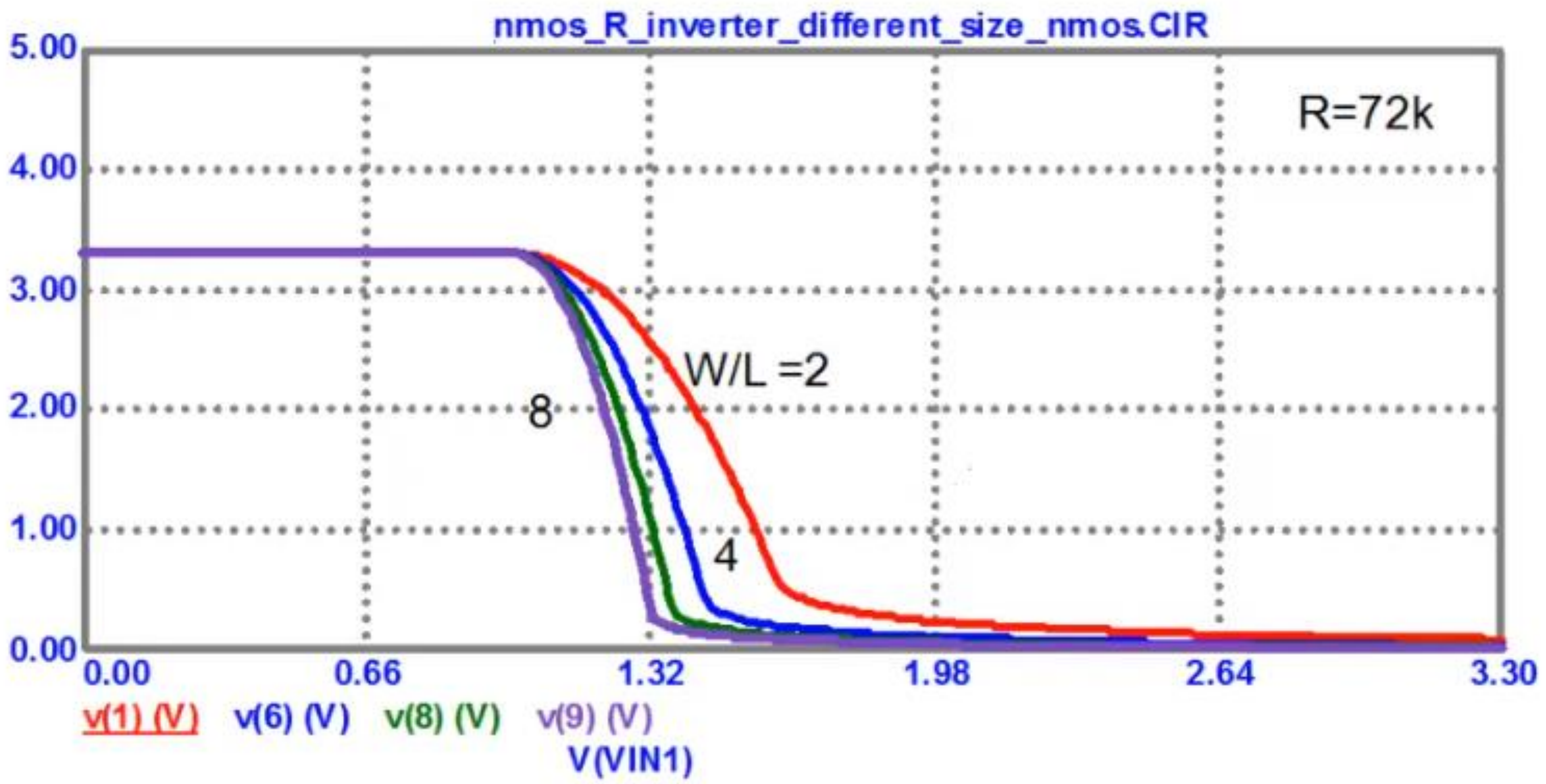




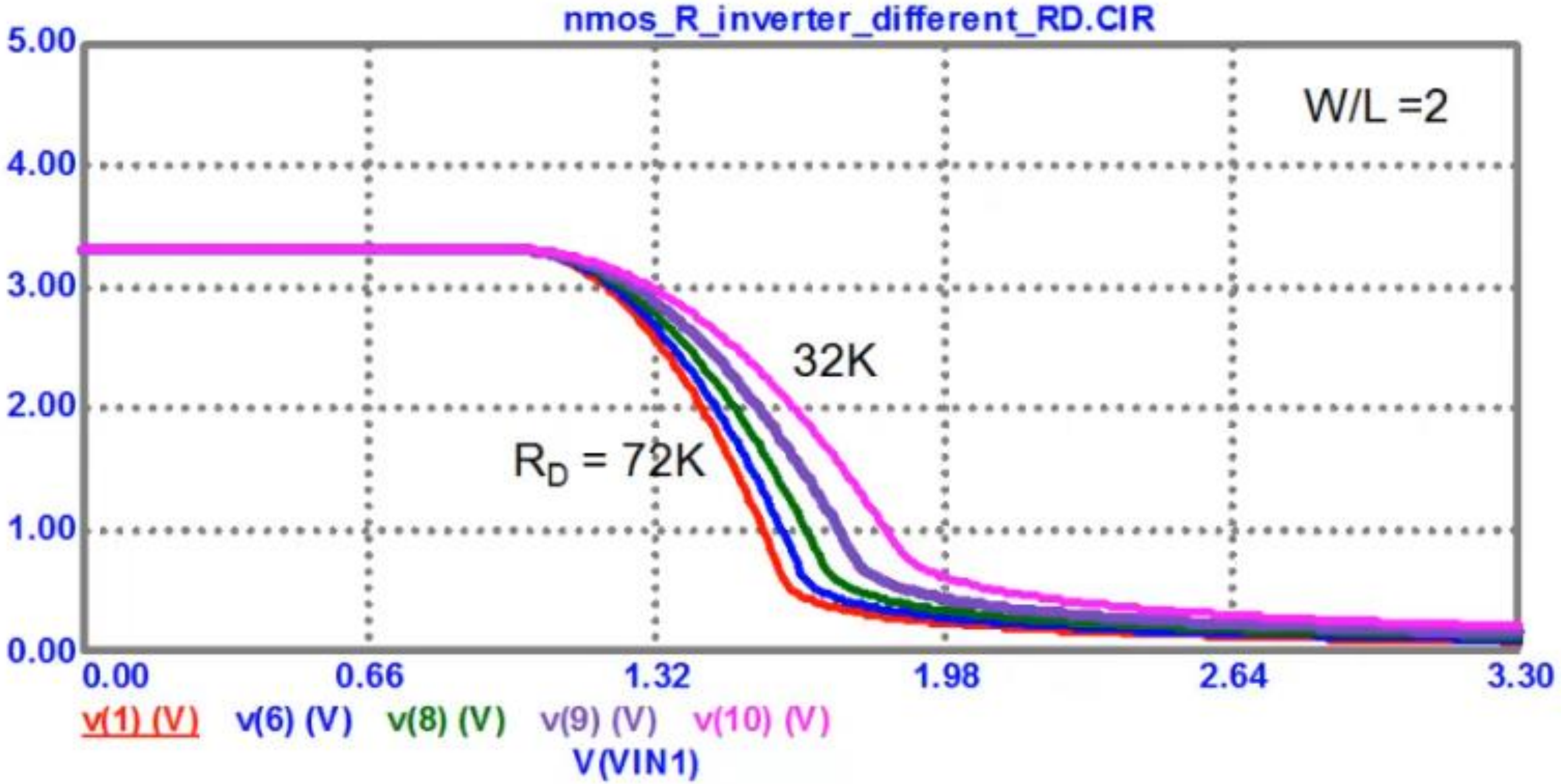


Shift characteristics to right to improve NM_L

1. Decrease R_D
2. Decrease W/L



Decreasing the pull down resistor shifts characteristics left



$R_D = 72k \Rightarrow V_{OL} = 0.1V; V_{OH} = 3.3V$

$V_{IL} = 1.07V; V_{IH} = 1.7V$

$NM_L \sim 0.97V; NM_H \sim 1.6V$

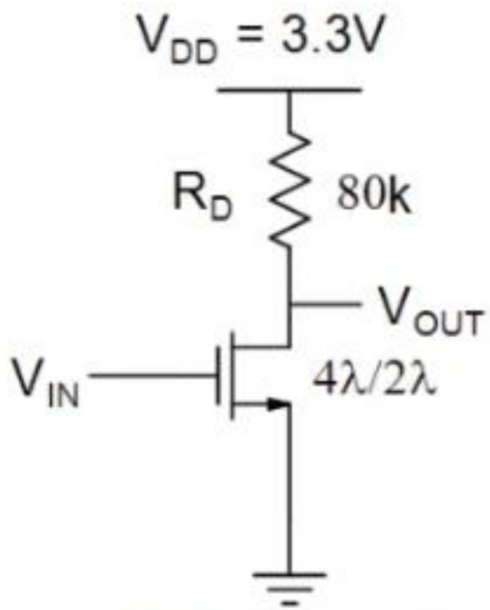
$V_{inv} = 1.5V$

$R_D = 32k \Rightarrow V_{OL} = 0.22V; V_{OH} = 3.3V$

$V_{IL} = 1.16V; V_{IH} = 2V$

$NM_L \sim 0.94V; NM_H \sim 1.3V$

$V_{inv} = 1.72V$



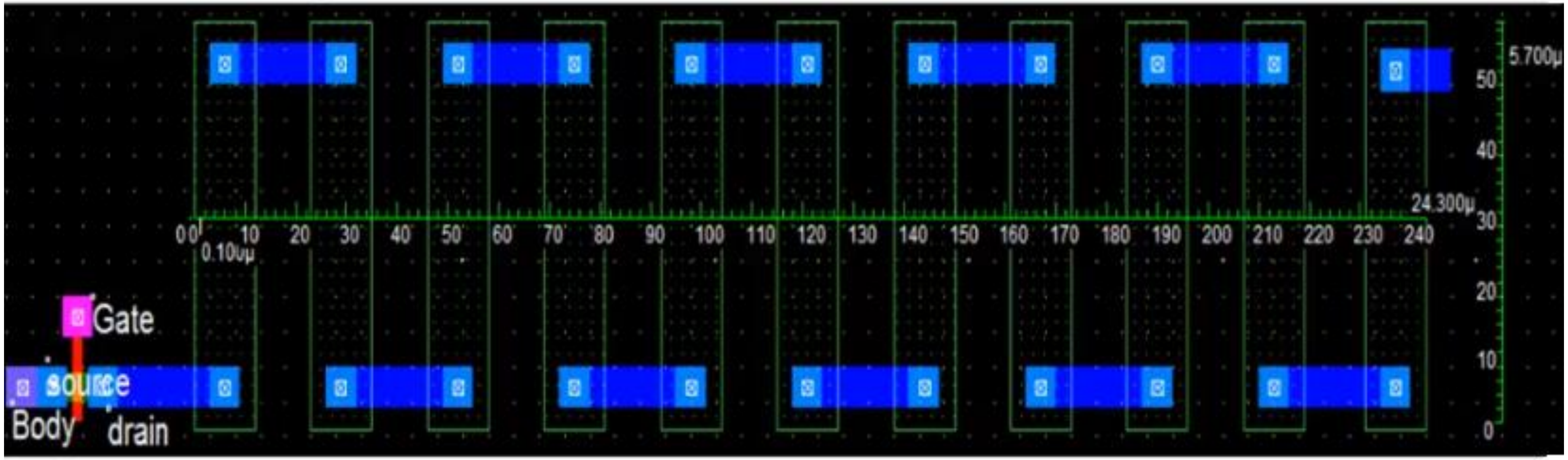
$NM_L \sim 0.97V; NM_H \sim 1.6V$

$R_D = 10k$

$W/L = 4\lambda/2\lambda; R_D = 10k \Rightarrow V_{OL} \sim 0.72V$

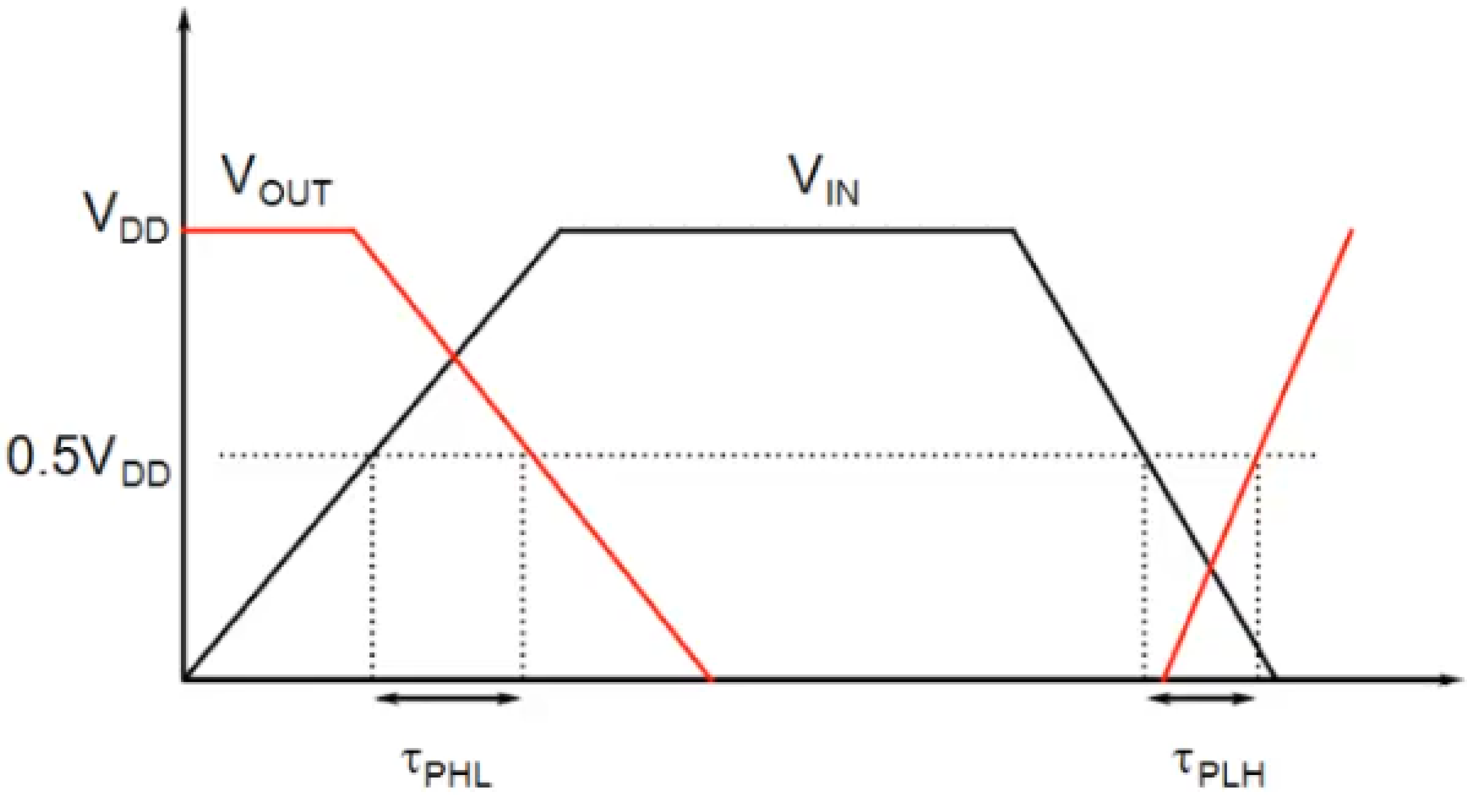
$NM_L = V_{IL} - V_{OL} \sim 0.28V$

1. Area
2. Delay
3. Power
4. Noise Margins

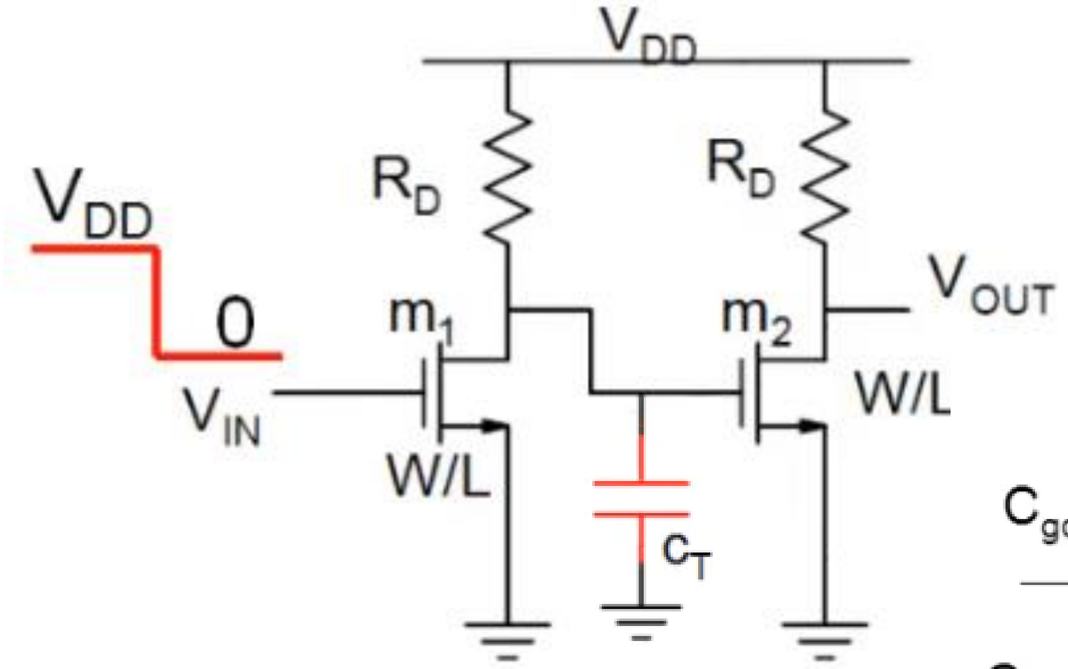


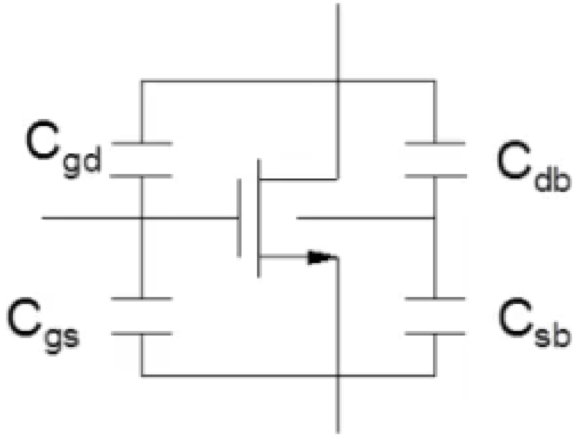
$$\frac{A_{RD}}{A_{tr1}} \sim 35$$

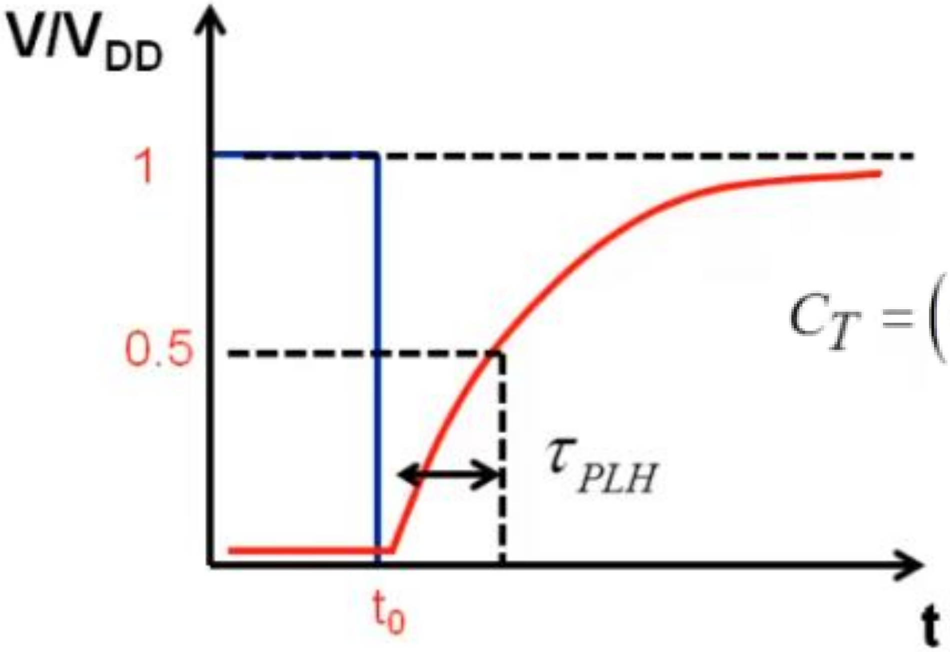
Propagation Delay



$$\tau_R \;;\; \tau_F \;;\; \tau_{PHL} \;;\tau_{PLH}$$

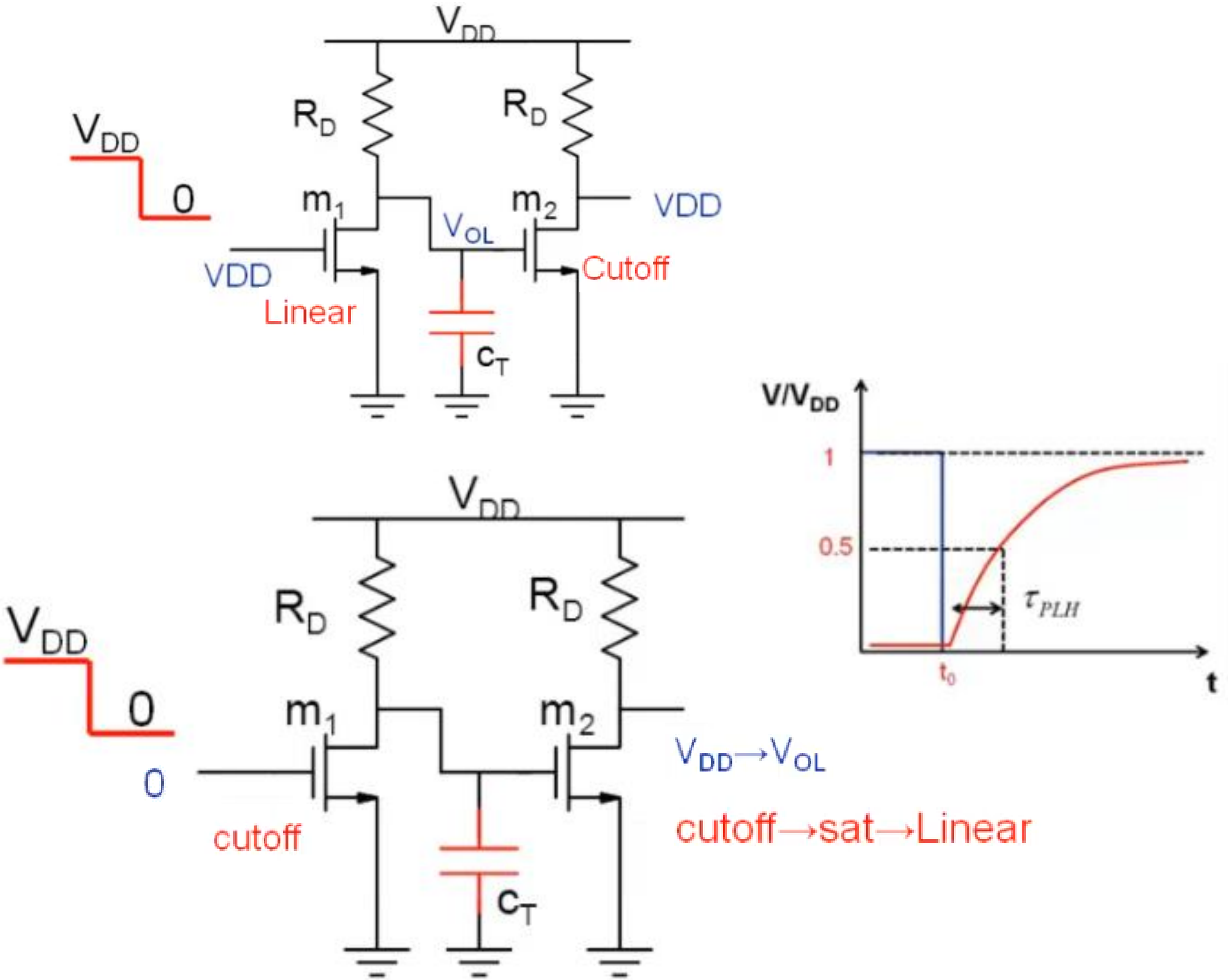




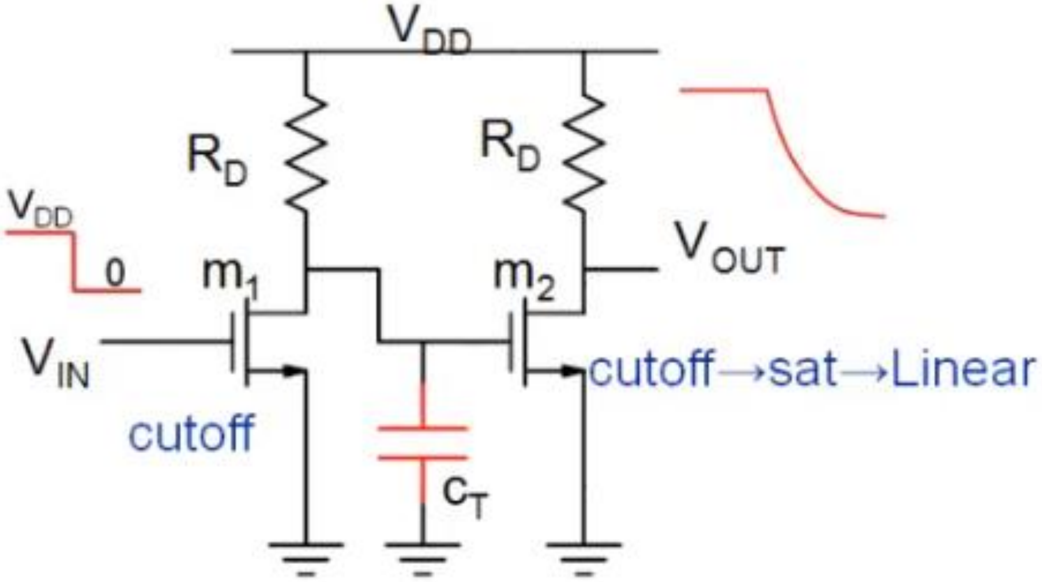


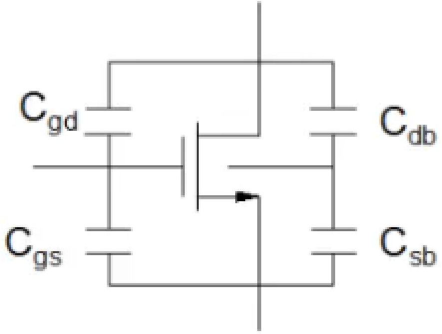
$$C_T = \left(C_{gd1} + C_{db1}\right) + \left(C_{gs2} + C_{gd2}\right)$$

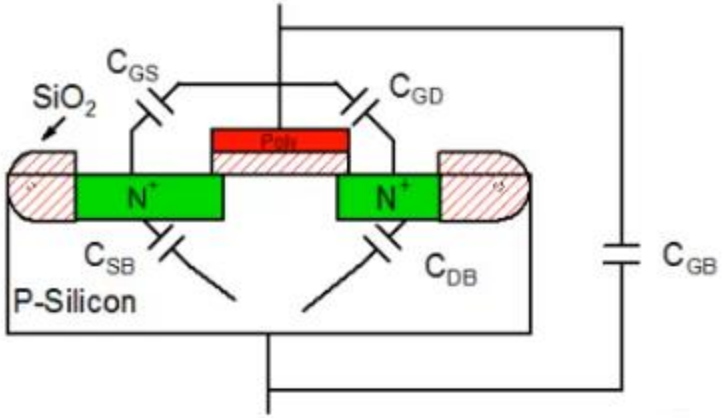
Parameter	NMOS	PMOS
V_{THNO}(V)	0.69	-0.869
λ (for L = 1μm)	0.015	0.065
γ	0.696	0.456
KP (μA/V²)	100	40
CGSO (pF)	281	252
CGDO(pF/m)	281	252
CJ (μF/m²)	467.7	932
PB	0.9	0.92
MJ	0.5	0.466
CJSW(pF/m)	616.95	181
MJSW	0.235	0.5

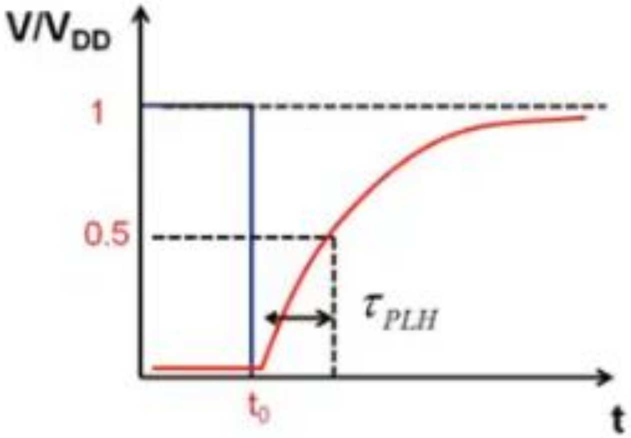


V_DD
R_D
R_D
V_DD
0
m_1
m_2
VDD
V_OL
VDD
Cutoff
Linear
c_T
V_DD
R_D
R_D
V_DD
0
m_1
m_2
0
V_DD→V_OL
cutoff
cutoff→sat→Linear
c_T
V/V_DD
1
0.5
τ_PLH
t_0
t









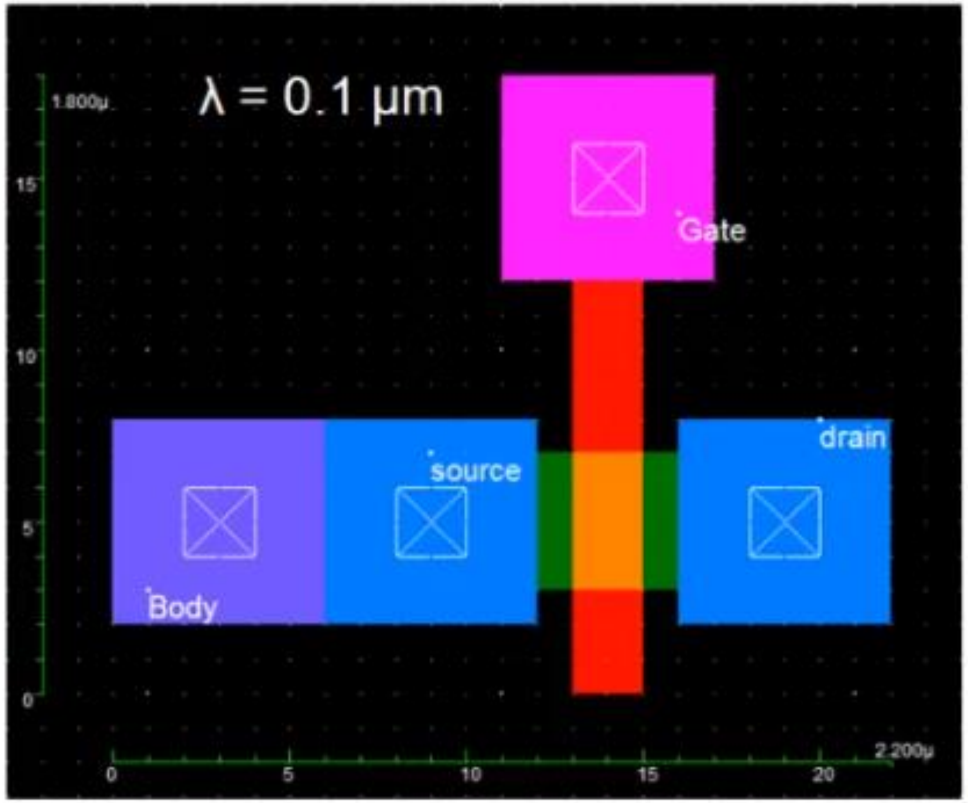
$$C_T = \left(C_{gd1} + C_{db1}\right) + \left(C_{gs2} + C_{gd2}\right)$$

$$C_{gd1} = C_{GDO}.W_1 \qquad C_{gd2} = C_{GDO}.W_2$$

$$C_{db1} = \frac{C_{jsw}.P_D}{\left(1 + \frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}} + \frac{C_j.A_D}{\left(1 + \frac{V_{DB}}{P_B}\right)^{M_j}}$$

V_{DB} = 0→0.5VDD

$$C_{gs1} \cong \left(C_{gso}.W\right) \rightarrow \frac{2}{3} C_{ox'}.W.L + C_{gso}.W$$



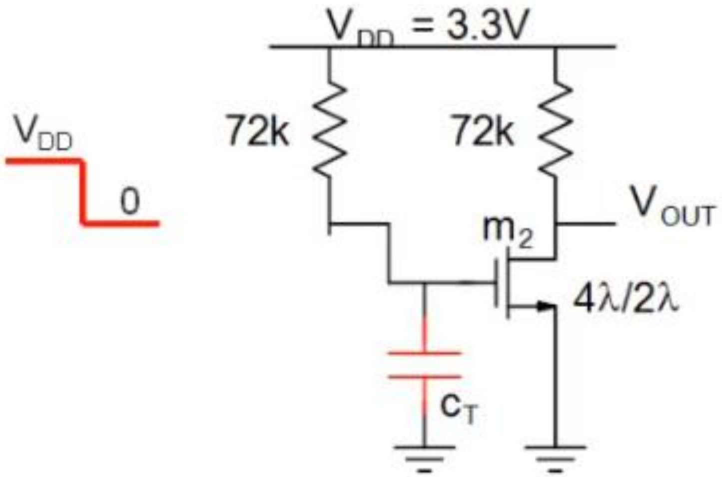
$$A_D = 4\times 1 + 6\times 6 = 40;$$
$$P_D = 2\times(1+1+6)+6 = 22$$

$V_{DB} = 0$

$$C_{db1} = \frac{C_{jsw}.P_D}{\left(1+\frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}} + \frac{C_j.A_D}{\left(1+\frac{V_{DB}}{P_B}\right)^{M_j}} = 5.7\,fF$$

~4fF

1.7fF

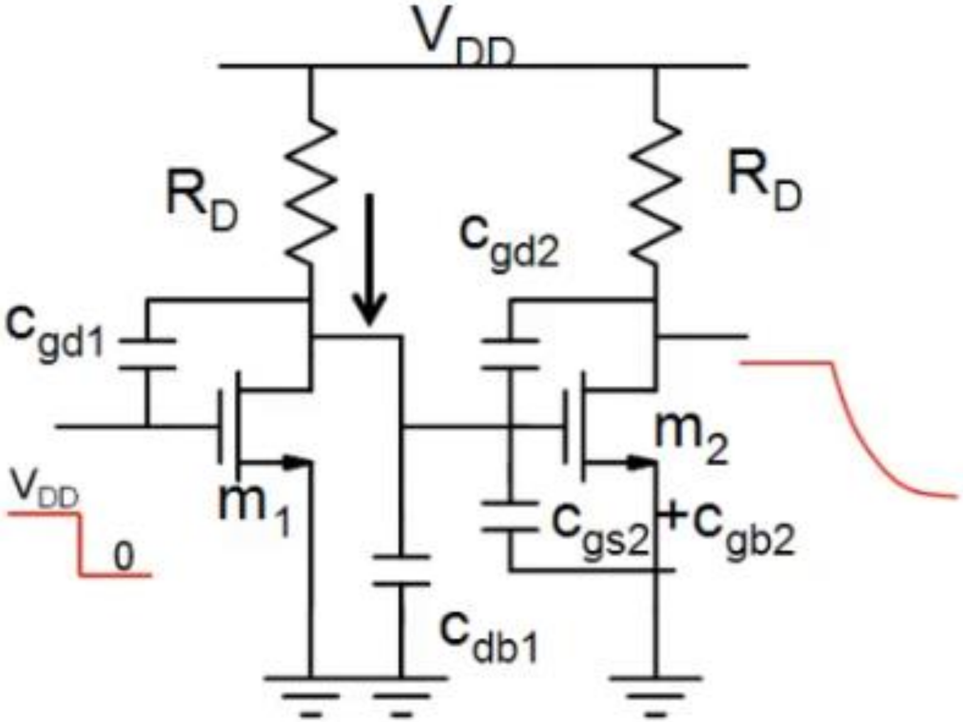


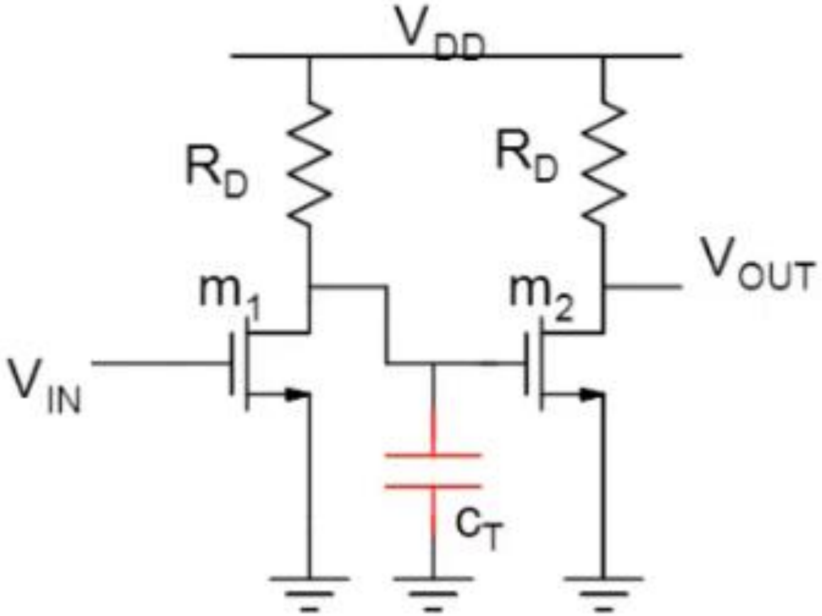
$$C_T = \left(C_{gd1} + C_{db1}\right) + \left(C_{gs2} + C_{gd2}\right)$$

$$C_{To} = 8.5\,fF$$

$$\tau_{PLH} \cong 0.693 \times R_D \times \tilde{C}_T$$
$$= 424\,ps$$

$\tau_{PLH} \cong 137\,ps$ if C_{db} is not considered





M1 : linear →cutoff

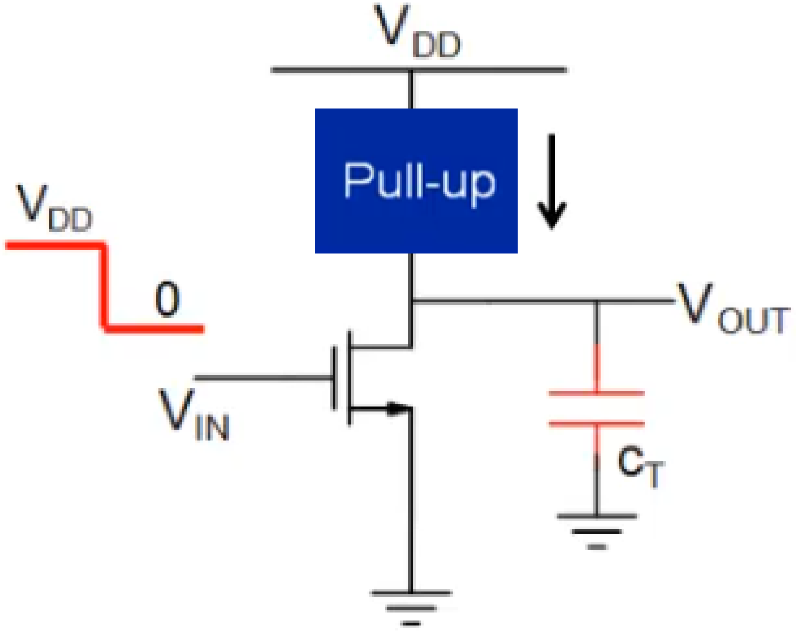
M2: cutoff→sat→Linear

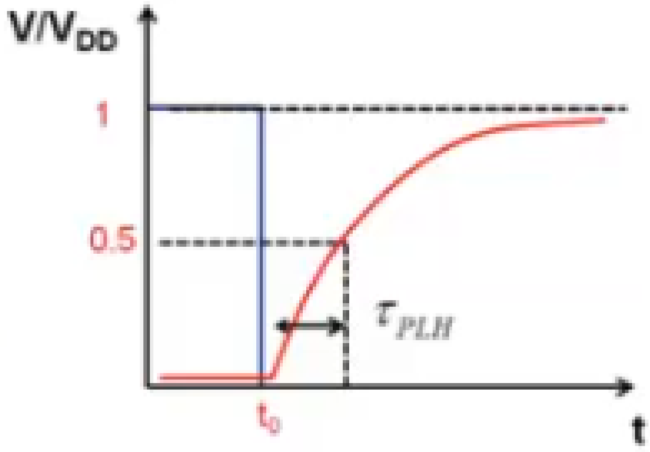
$$C_T = (C_{gd1} + C_{db1}) + (C_{gs2} + C_{gd2} + C_{gb2})$$

$$I = \sum \frac{dQ_j}{dt}$$

$$I = C_{gd1} \times \frac{d(V_{D1} - V_{G1})}{dt} + C_{gd2} \times \frac{d(V_{D1} - V_{D2})}{dt} + C_{db1} \times \frac{dV_{D1}}{dt} + (C_{gs2} + C_{gb2}) \times \frac{dV_{D1}}{dt}$$

$$I = \left(C_{gd1} \times \left(1 - \overbrace{\frac{dV_{G1}}{dV_{D1}}}^{\sim -1} \right) + C_{gd2} \times \left(1 - \overbrace{\frac{dV_{D2}}{dV_{D1}}}^{\sim -1} \right) + C_{db1} + C_{gs2} + C_{gb2} \right) \times \frac{dV_{D1}}{dt}$$

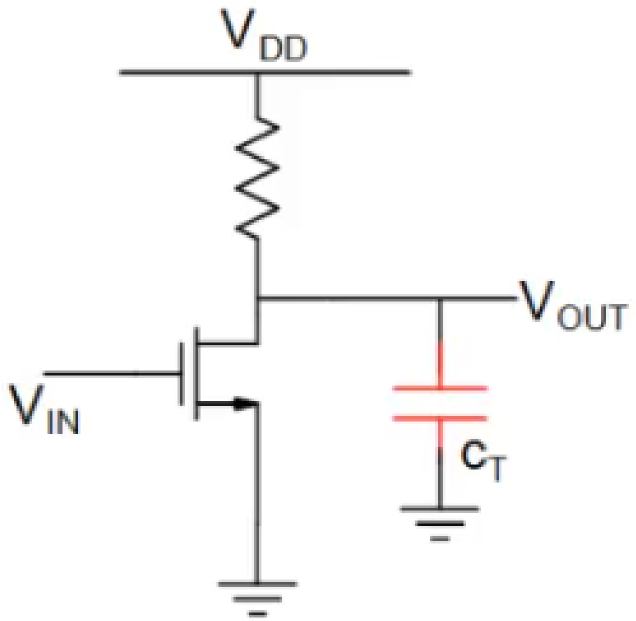




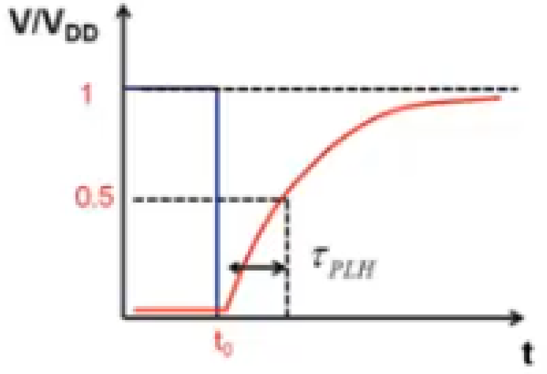
$$I_{pu} = C_T \times \frac{dV_{out}}{dt}$$

$$\tau_{plh} = \int_0^{0.5V_{DD}} \frac{C_T}{I_{pu}} \times dV_{out}$$

$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$$

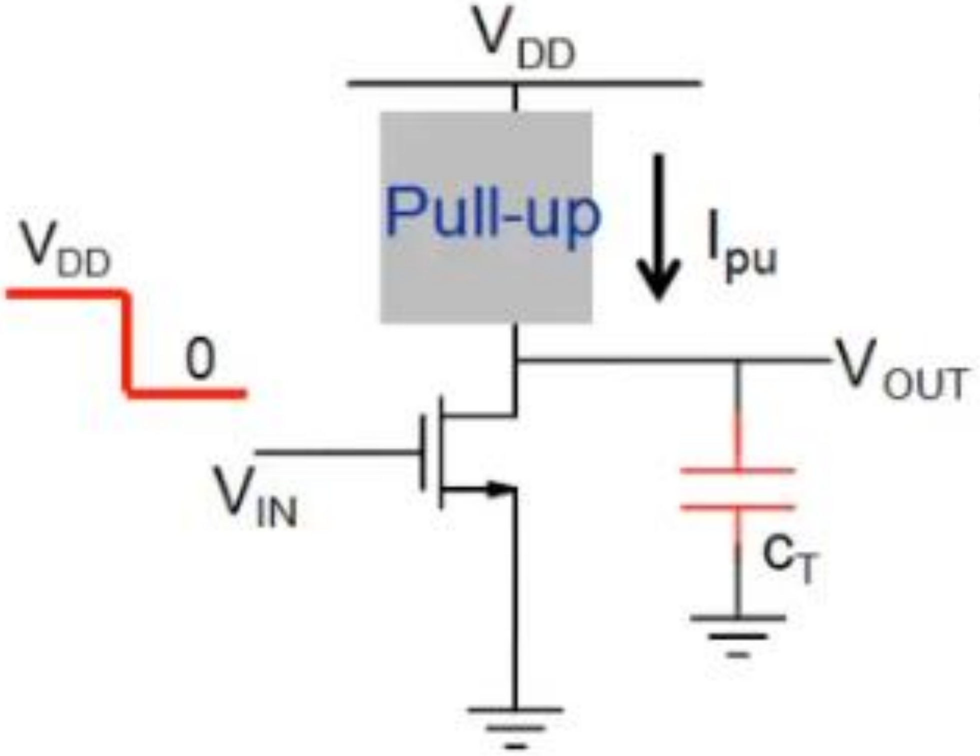


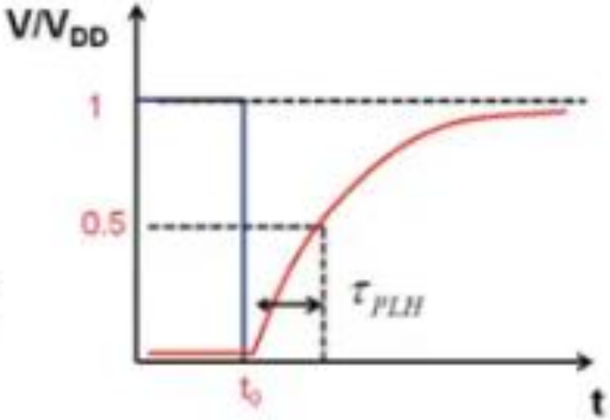
$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$$



$$I_{pu} = \frac{V_{DD}}{R_D} \rightarrow \frac{0.5V_{DD}}{R_D} \qquad \tilde{I}_{pu} \cong 0.75\frac{V_{DD}}{R_D}$$

$$\tau_{plh} \cong 0.67 \times R_D \tilde{C}_T$$



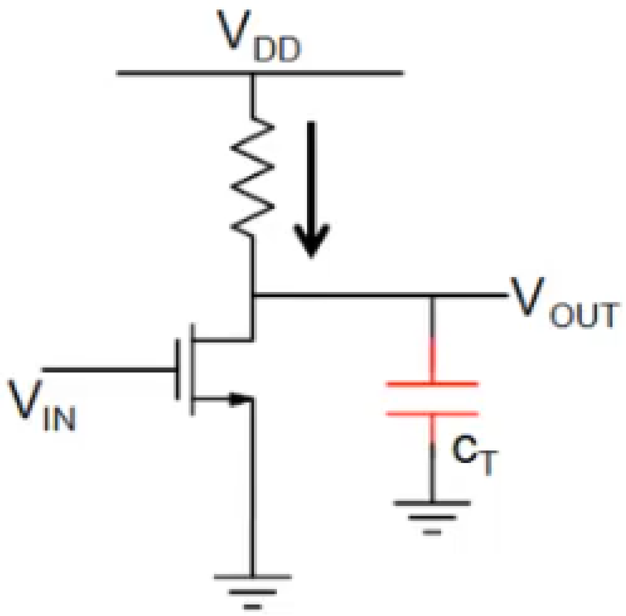


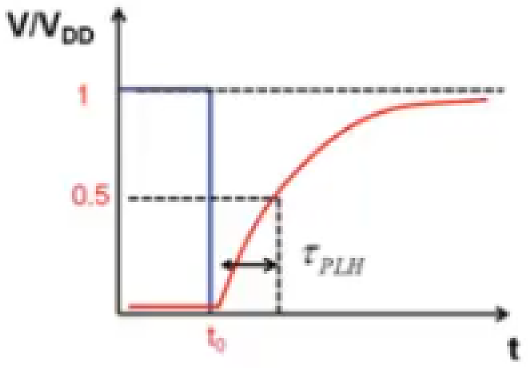
$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$$

$$I_{pu} \propto V_{DD}^{m}; m > 1 \qquad P_{diss} \propto V_{DD}$$

In general delay decreases with increase in supply voltage

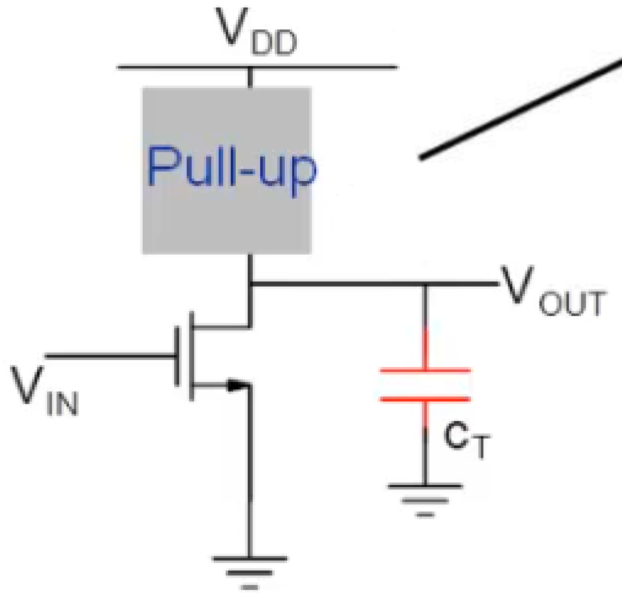
There is a power delay tradeoff





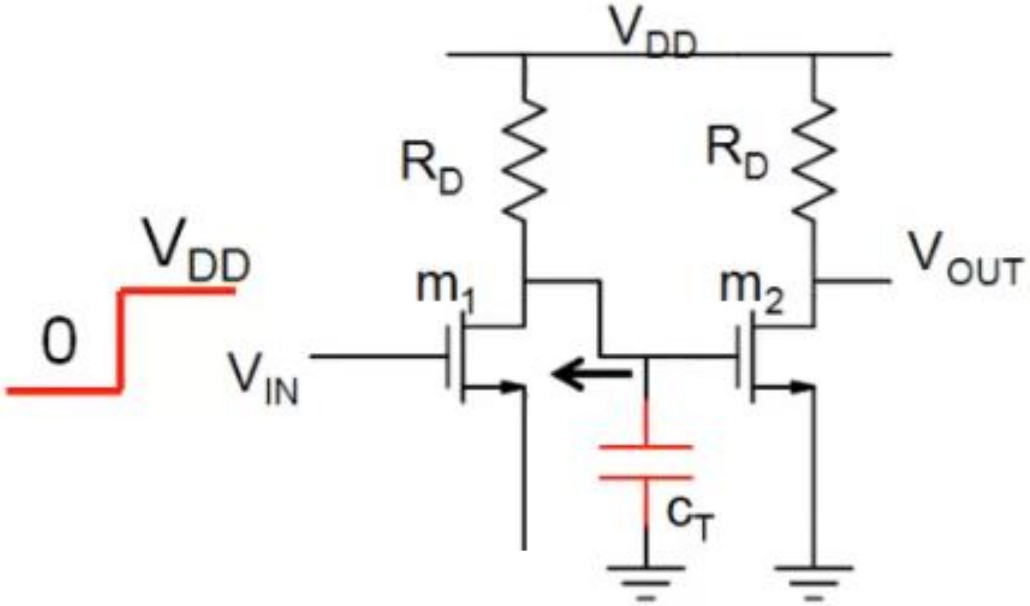
$$I_{pu} = \frac{V_{DD}}{R_D} \rightarrow \frac{0.5V_{DD}}{R_D}$$

$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$$



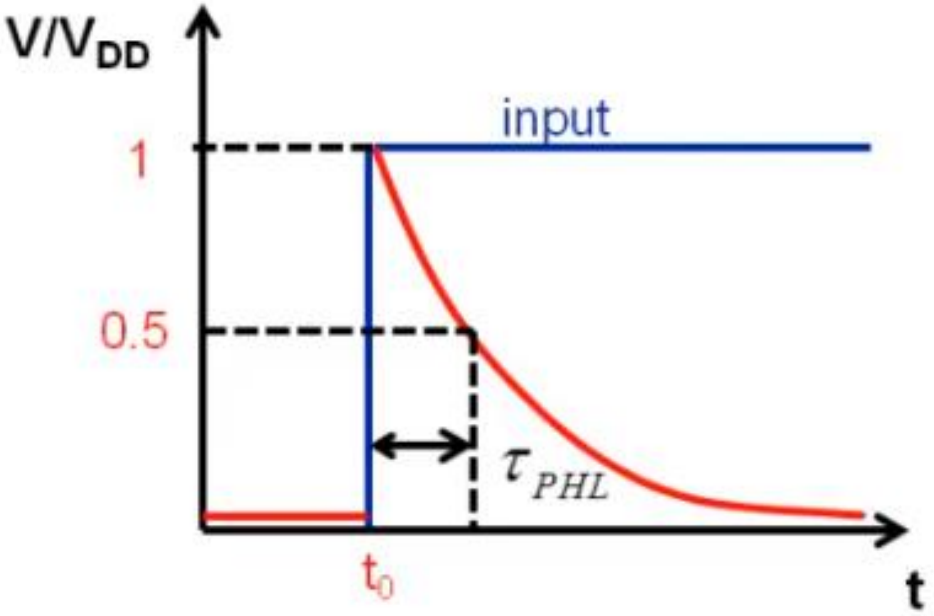
Ideally should be like a current source which switches on during charging.

High to Low delay propagation Delay



$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{dis.}}$$

$$I_{dis.} = I_{DS1} - \frac{V_{DD} - V_{D1}}{R_D}$$

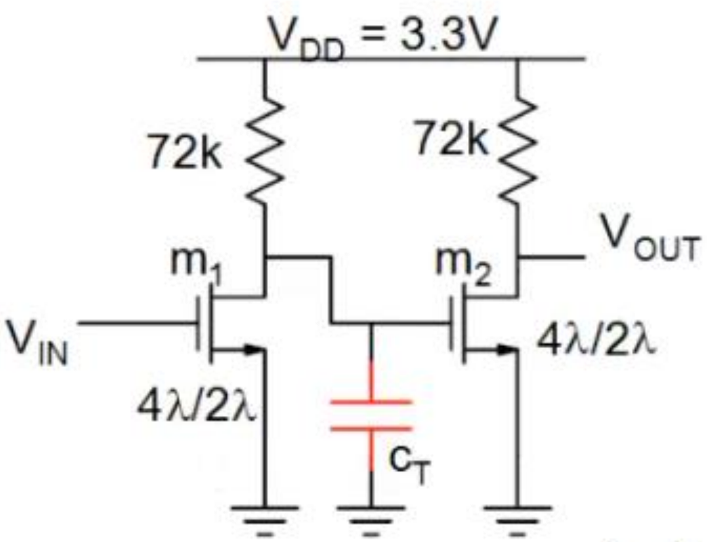


M1 : sat (3.3→2.3)
lin. (2.3→1.65)

$$I_{DS}(t=0) = \left(KP_N \times \frac{W}{L}\right) \times \frac{(V_{DD} - V_{THN})^2}{2}$$

$$I_{DS}(t=\tau_{phl}) = \left(KP_N \times \frac{W}{L}\right) \times \left((V_{DD} - V_{THN})\frac{V_{DD}}{2} - \frac{V_{DD}^2}{4}\right) - \frac{V_{DD}}{2R_D}$$

High to Low delay propagation Delay



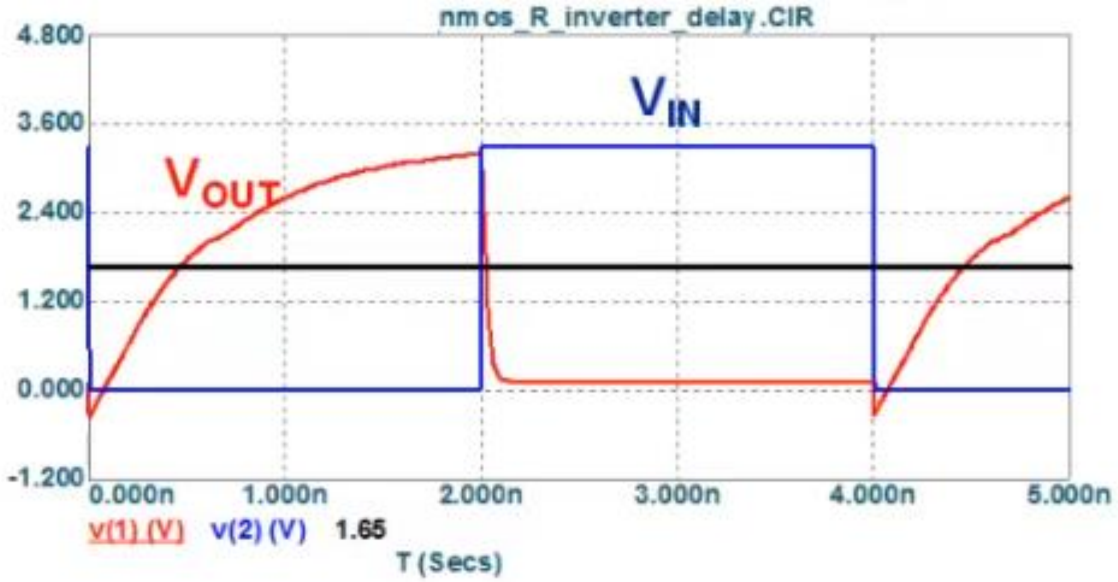
$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{dis.}}$$ ~39 ps

$$\tau_{PLH} \cong 424\,ps$$

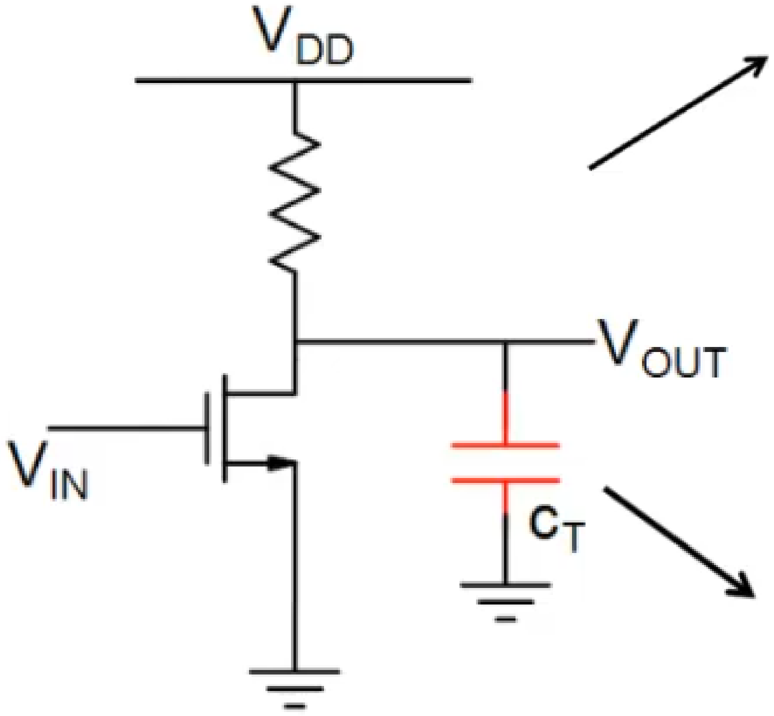
$$I_{dis.} = I_{DS1} - \frac{V_{DD} - V_{D1}}{R_D}$$

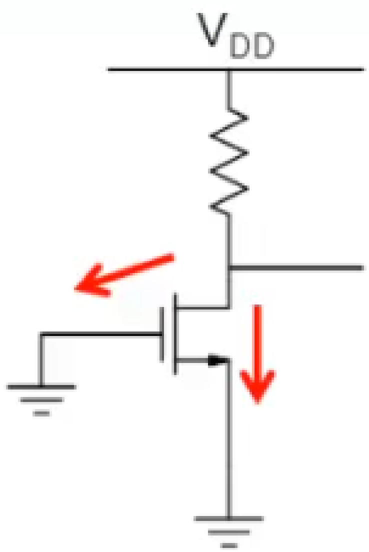
$$I_{DS}(t=0) = \left(KP_N \times \frac{W}{L}\right) \times \frac{(V_{DD} - V_{THN})^2}{2}$$ 0.53mA

$$I_{DS}(t=\tau_{phl}) = \left(KP_N \times \frac{W}{L}\right) \times \left((V_{DD} - V_{THN})\frac{V_{DD}}{2} - \frac{V_{DD}^2}{4}\right) - \frac{V_{DD}}{2R_D}$$ 0.19mA

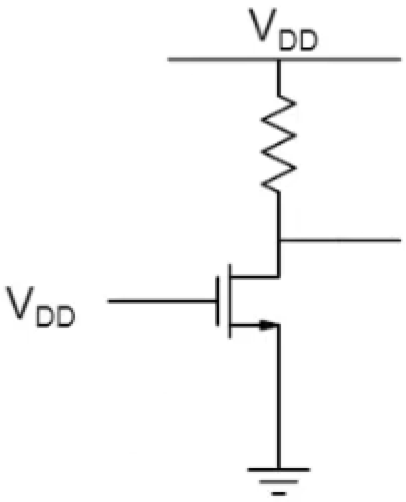


Power dissipation

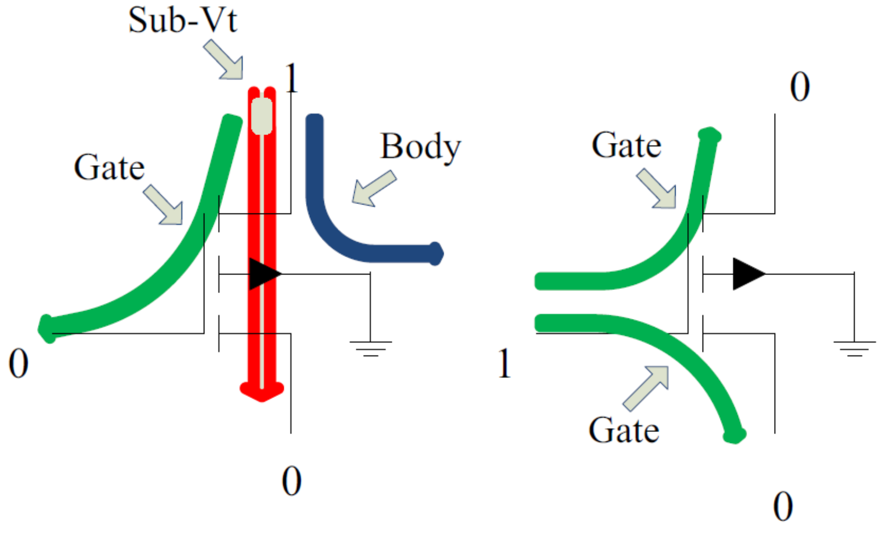


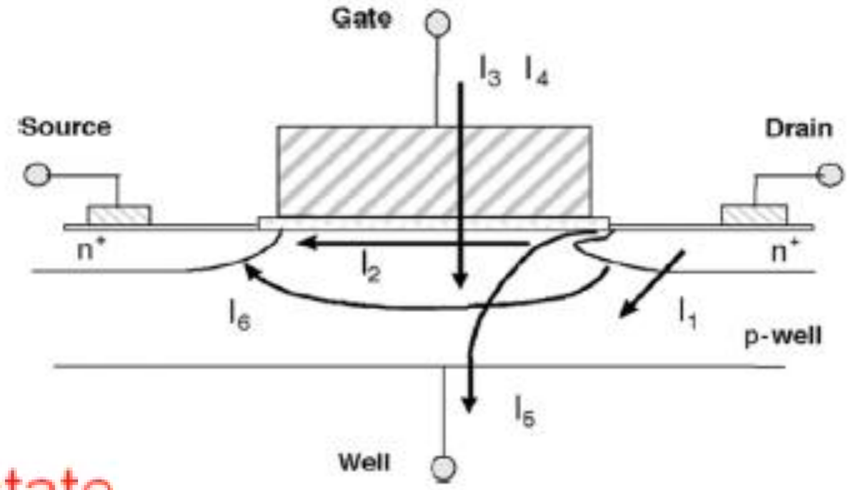


$$P = V_{DD} \times I_{leakage}$$



$$P \sim \frac{V_{DD}^2}{R_D}$$

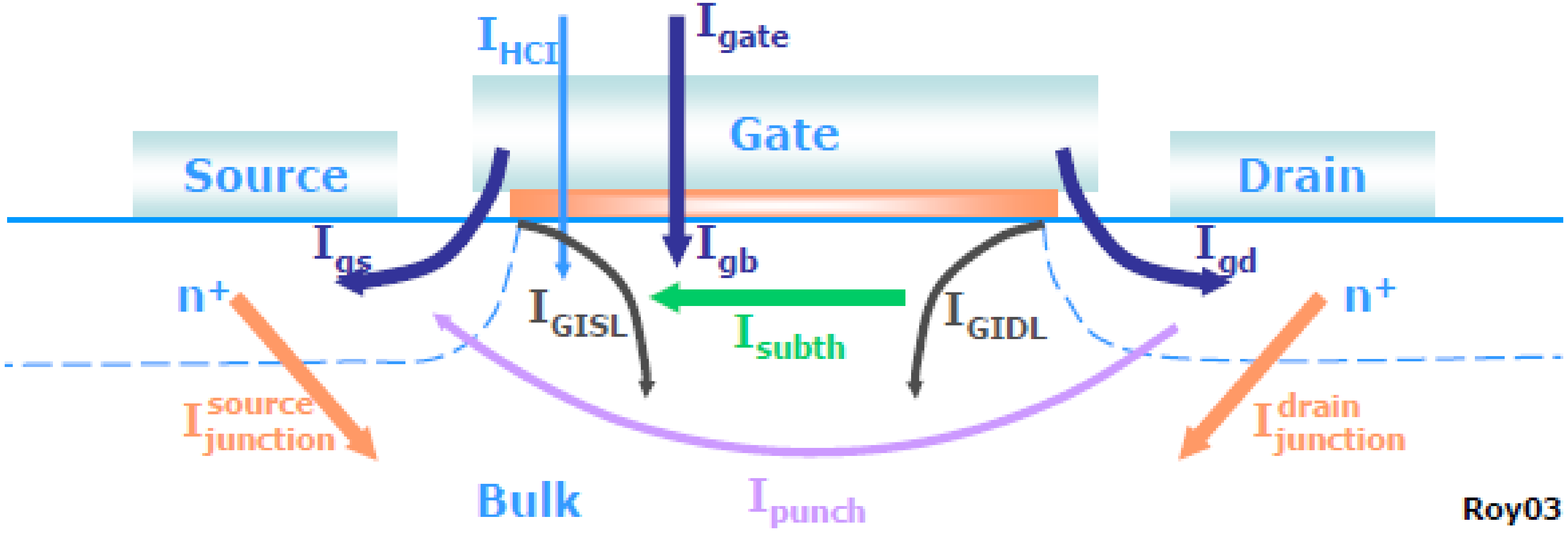




1. Static
2. Dynamic

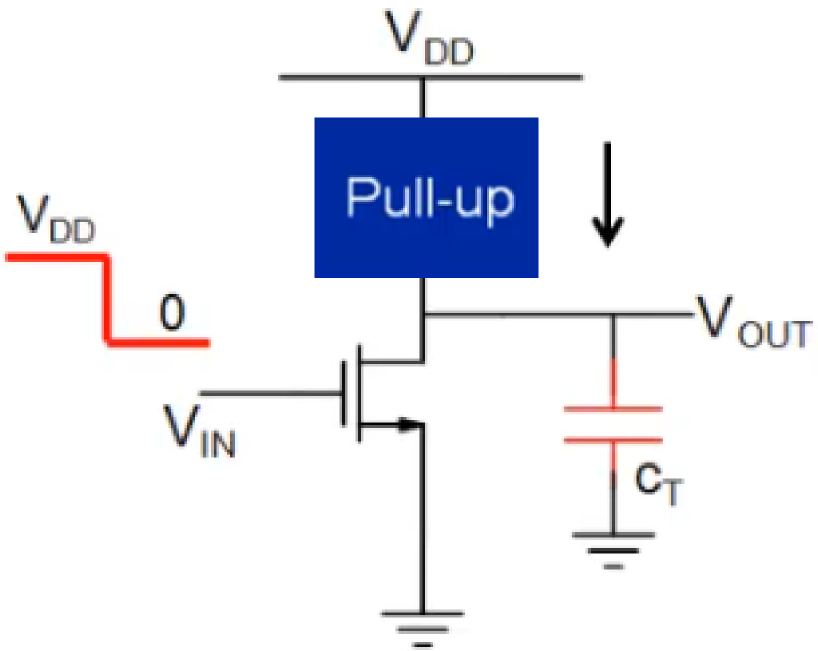
Energy should be drawn only to change the state

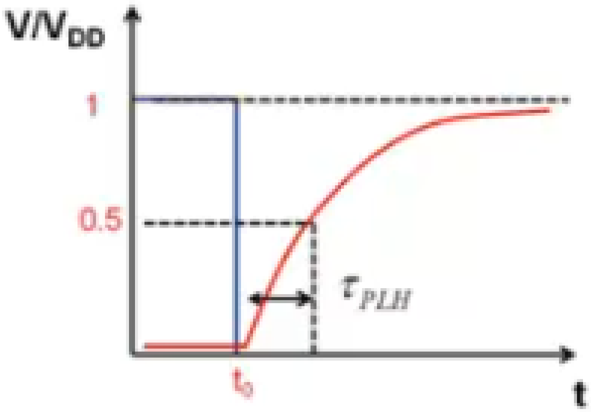
- **If channel is locking:**
  - subthreshold current (I_{subth}) ≤180nm
  - gate tunnelling to S/D (I_{gate}) ≤90nm
  - pn-junction leakage ($I_{junction}$) ≤65nm
  - gate induced drain leakage (I_{GIDL})
  - depletion punchthrough (I_{punch})
- **If channel is conducting:**
  - gate tunnelling (I_{gate})
  - pn-junction leakage ($I_{junction}$)
- **If channel is switching:**
  - hot carrier injection (I_{HCI})



Long Channels (L> 1μm) Leakages are very small.	Short Channels L > 180nm t_{ox} > 3nm Sub-threshold leakage	Very Short Channels L > 90nm t_{ox} > 2nm Sub-threshold leakage + Gate leakage	Nano scale Channels L < 90nm t_{ox} < 2nm Sub-threshold leakage + Gate leakage + Junction leakage / BTBT

Contribution of new leakage currents with scaled technologies

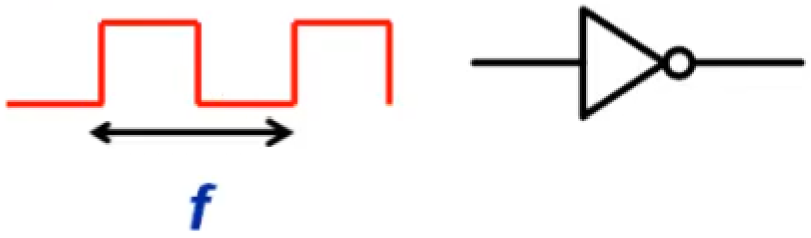




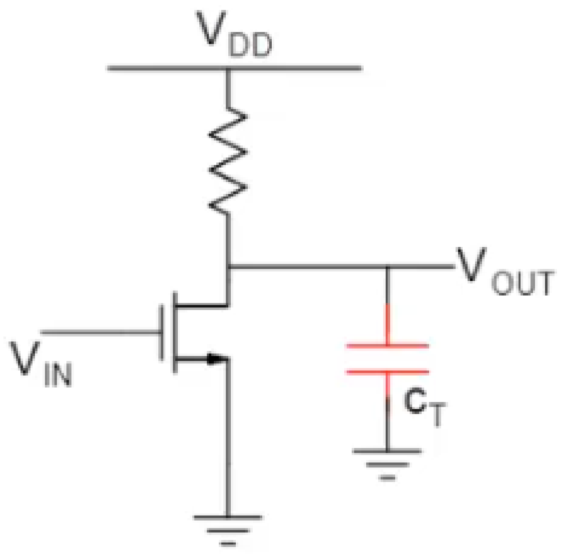
$$E_{\sup ply} = \int V_{DD} \times I_{pu} dt = C_T \times V_{DD}^2$$

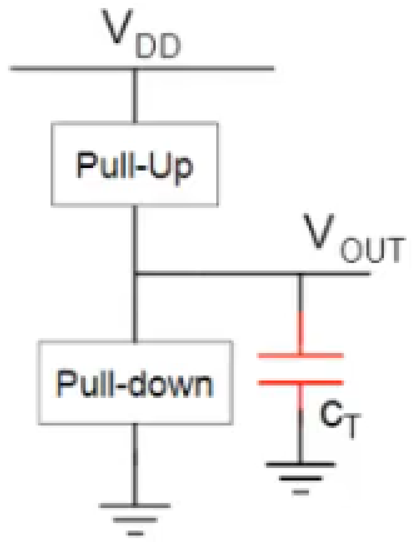
Half of it is dissipated in the resistor and the other half is stored in capacitor

When the inverter switches back to zero, the energy stored on capacitor is also dissipated

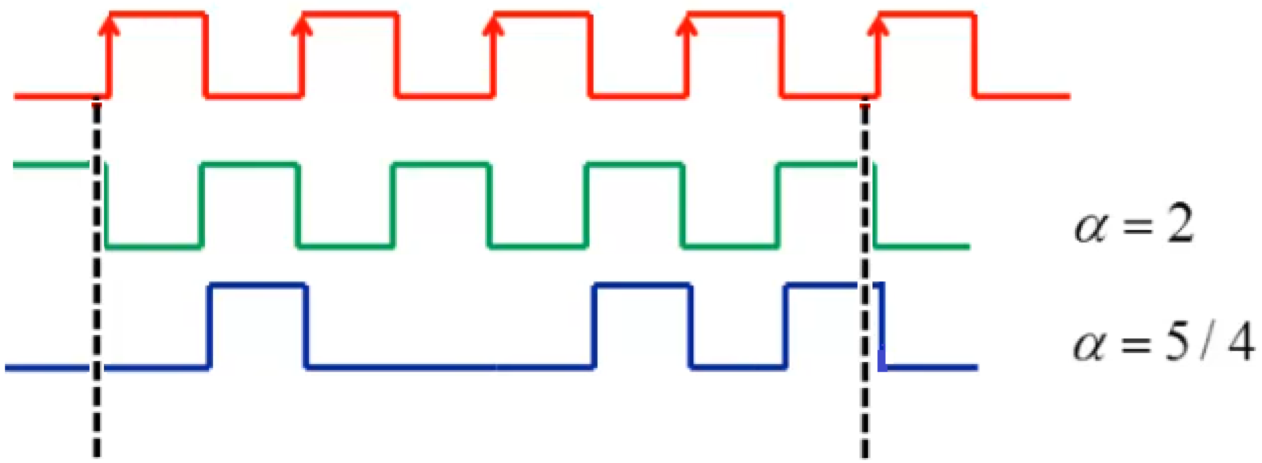


$$P_{dynamic} = \frac{0.5C_T \times V_{DD}^2 + 0.5C_T \times V_{DD}^2}{T} = C_T \times V_{DD}^2 \times f$$





$$P_{dynamic} = C_T \times V_{DD}^2 \times f$$



$$P_{dynamic} = \sum \left(0.5 C_j \times V_j^2\right) \times f \times \alpha_j$$