EC2.201-VLSI Design (Monsoon 2021)

Assignment 1

---

1) Explain VLSI design flow with diagram [2M]
2) What is the difference between execution of blocking and non-blocking assignments? [2M]
3) Realize W = AB+CD+EF using [2+2=4M]
   a) NAND gates of any size
   b) Two input NAND gates only
4) What are the minimum number of two input NAND gates required to realize $f = (\bar{X} + \bar{Y}).(W + Z)$? [2M]
5) What are the minimum number of two input NOR gates required to realize f = C+AB? [2M]
6) Design a combinational circuit that multiplies two 2-bit numbers; a1, a0 and b1, b0 to have 4-bit product as output. Use AND gates and half-adders. [2M]
7) Implement Y = (A ⊕ **B** ⊕ **C)** using 2:1 MUXs. [2M]
8) A shopkeeper uses a unique safety box with an alarm to protect his valuables. Its input control is determined from four sources: [2+2=4M]
   i. S_1: A manual switch on the safety box; S_2: Safety box position; S_3: Time of the day and S_4: safety box door position.
   ii. These lines are activated on the following conditions:
   iii. S_1: Switch is closed; S_2: Normal position; S_3: Working hours from 9:00 am to 7:00 pm; S_4: Safety box door closed;
   iv. The alarm is sounded when it turns ON. This happens when the safety box is moved from its position and the switch is closed, or when the safety box is opened at night (say 8:00pm) after working hours, or when the door of the box is left ajar and switch is opened.
   a) As a digital design engineer, you wish to help the shopkeeper design the control circuit for the box.
   b) The shopkeeper could only find an alarm that sounds when it is OFF. Help him redesign the control with minimum hardware.
9) In a company the digital design team consists of two managers and two engineers. Whenever there is conflict, they decide they will either hold a conference or they will pause from work and have fun. So, each of them casts a vote. The majority wins always, except when the managers agree on each other, i.e., when everyone has to agree on the same thing as the managers. Any other tie will cause everyone to pause from work and have fun. As a digital design engineer as part of the team you wish to design a circuit that resolves this conflict. [4M]
10) Consider the function $f = ((a + b).c).(c.d)$. Write a structural code for the function. Draw the truth table and verify the same with the Verilog test bench. [3 M]
11)
   a) Implement Half adder and Full adder using structural modelling in Verilog and write a testbench to verify its functionality. [2M]

b) Implement Half adder and Full adder using behavioural modelling in Verilog and write a testbench to verify its functionality. [2M]

12) Consider the below circuit and write the respective structural and behavioural code and test bench to verify the functionality. [4M]