Quiz-2: Monsoon2022: VLSI Digital (EC2.201)

Max. Time: 45 Mins [8:30 to 9:15 AM] Date: 17/10/2022

Note(s): No query is allowed during exam. Write your assumptions (if any) for each question.

Q 1 (a). You received a wafer from the process with parameters listed below. **[5 Marks]** [CO-4]

W = 50 µm, L = 5 µm, $\mu_n C_{ox}$ = 50 µA/V^2, V_{To} = 1 V, Υ_n = 0.6 V$^{1/2}$, λ_n = 0.1/L V^{-1}, ϕ_s = 0.84 V.

You decide to measure the Id-Vd characteristics for devices with varying L, and then compare the measured data against your calculations. When you measure a short channel device (L=0.18um), you notice that the measured saturation current is much lower than what you would expect from the calculations. What could be the possible reasons?

(b) Would the threshold voltage of a short channel device be the same, lower than, or higher than the long channel V_T value of 1V? Please explain why.

(c) What happens to the threshold voltage and to the saturation current when the temperature increases?

(d) What happens to the subthreshold leakage when you increase the threshold voltage.

OR

Q1. Consider a CMOS inverter with the following parameters: **[5 Marks]** [CO-2]

nMOS	VTn= 0.8V	µnCox = 50 µA/V2
pMOS	VTp= -1.0V	µpCox = 20 µA/V2

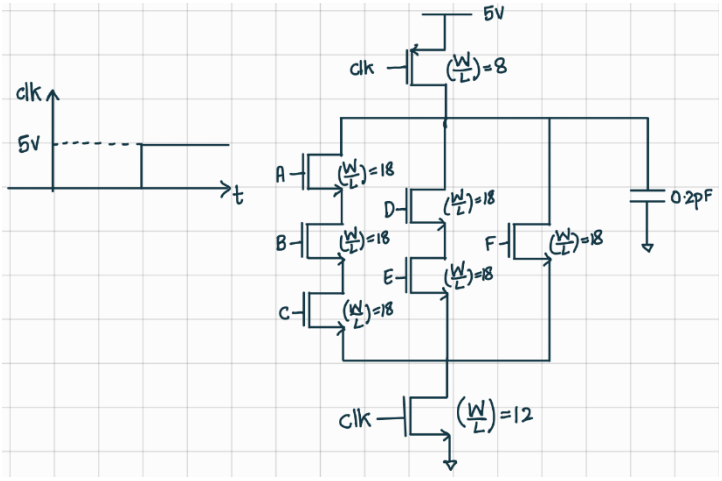
The power supply voltage is V_{DD} = 5 V. Both transistors have a channel length of L_n = L_p = 1µm. The total output load capacitance of this circuit is C_{out}= 2 pF, which is independent of transistor dimensions.

(a) Determine the channel width of the nMOS and the pMOS transistors such that the switching threshold voltage is equal to 2.2V and the output rise time is τ_{rise} = 5ns.

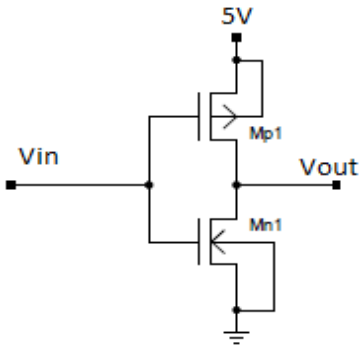
(b) Calculate the average propagation delay time τ_p for the circuit designed in part-(a).

(c) How do the switching threshold Vth and the delay times change if the power supply voltage is dropped from 5 V to 3.3 V. Provide an interpretation of the results.

Q2. Consider the circuit shown here. C_L= 0.2pF, V_{TN}= 1V, Kn= 50µA/V^2, V_{TP}= -1V, Kp= 25µA/V^2. Initial voltage across C_L=0 and the input to 'E' is 0 & that of A, B, C, D, F is 5V.
The waveform for clock (clk) is as shown. Sketch the output waveform clearly marking the 50% transition in both rise and fall across C_L.
[5 Marks] [CO-5]

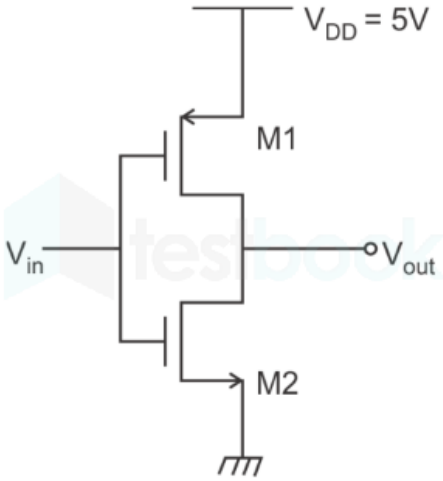


Q3. In the CMOS circuit shown in Fig, let's consider the *electron* and *hole* mobility are equal, and p-channel MOS (Mp1) and n-channel MOS (Mn1) are equally sized. Then, which of the conditions is satisfying the Mp1 to be in linear region. Justify your answer with required calculation. Only picking an option will not lead to marks. **[5 Marks]** [CO-3]



(a) $V_{in} > 3.12V$
(b) $1.875V < V_{in} < 3.125V$
(c) $V_{in} < 1.875V$
(d) $0 < V_{in} < 5V$

SOLUTION



M1 will be in linear region if $V_{out} > V_{in} + V_T$

At the edge of the linear region $V_{out} = V_{in} + V_T$

$$\frac{1}{2}K_n(V_{in} - V_{thn})^2 = K_p\left[(V_{DD} - V_{in} - V_{thp})(V_{DD} - V_{out}) - \frac{1}{2}(V_{DD} - V_{out})^2\right]$$

$$Or,\ \frac{1}{2}K_n[V_{in} - V_T]^2 = K_p\left[(V_{DD} - V_{in} - V_T)(V_{DD} - V_{in} - V_T) - \frac{1}{2}(V_{DD} - V_{in} - V_T)^2\right]$$

$$Or,\ [V_{in} - V_T]^2 = (V_{DD} - V_{in} - V_T)^2$$

$$Or,\ (V_{in} - 1)^2 = (4 - V_{in})^2$$

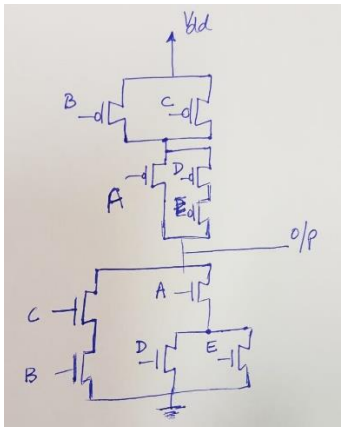
$$Or,\ V_{in} - 1 = (4 - V_{in})$$

$$Or,\ V_{in} = 2.5$$

So, for Vin< 2.5 the PMOS will be in a linear region so the correct option is (1)

Q4 (a). Draw transistor (CMOS) level schematic for the Y= A.(D+E) + BC. **[2 Marks]** [CO-5]

SOLUTION



(b) For the circuits below, size the transistors, so that the pull-up and pull-down resistances are matched. **[3 Marks]** [CO-4]