DVD Quiz 1 Solutions

February 21, 2024

1)

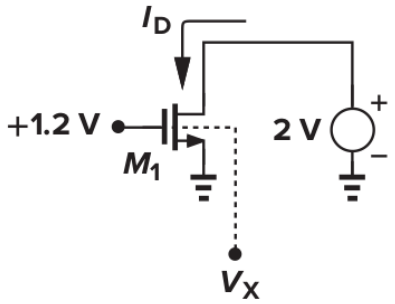

Figure 1: Circuit for question 1

(a) Threshold Voltage,

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

$$\implies V_{th} = 0.3 + 0.4(\sqrt{0.7 - V_X} - \sqrt{0.7})$$

$$\implies V_{th} = 0.3V \qquad (\because V_X = 0)$$

Since $V_{DS} > V_{GS} - V_{th}$, apply the drain current equation for saturation,

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2$$

$$\implies I_D = \frac{50 \times 10^{-6}}{2} \times 10 \times (1.2 - 0.3)^2$$

$$\implies I_D = 2.5 \times 10^{-4} \times (0.81)$$

$$\implies I_D = 202.5uA$$

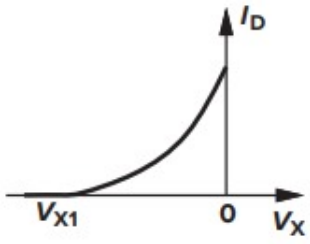

Figure 2: Vx vs Id curve

(b) As shown in Fig.2 if V_X is sufficiently negative, the threshold voltage of M1 exceeds 1.2 V and the device is off. Applying,

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

$$\implies 1.2V = 0.3 + 0.4(\sqrt{0.7 - V_X} - \sqrt{0.7})$$
$$\implies V_X = -8.83V$$

2) In saturation region.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2$$

Saturation $V_{DS} >= V_{GS} - V_{TH}$
The saturation condition is satisfied in the given operating points.
$V_{TH} = V_{TH0}$ when $V_{SB} = 0$

In 1st case $I_{D1} = 256\mu A, V_{GS1} = 4V, V_{DS1} = 4V, V_{SB1} = 0V$
In 2nd case $I_{D2} = 441\mu A V_{GS2} = 5V V_{DS2} = 5V V_{SB2} = 0V$

Therefore

$$256u = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(4 - V_{TH})^2$$

$$441u = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(5 - V_{TH})^2$$

$$\frac{256}{441} = \frac{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(4 - V_{TH})^2}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(5 - V_{TH})^2}$$

$$\frac{256}{441} = \frac{(4 - V_{TH})^2}{(5 - V_{TH})^2}$$

$$\frac{16}{21} = \frac{(4 - V_{TH})}{(5 - V_{TH})}$$

$$80 - 16V_{TH} = 84 - 21V_{TH}$$

$$4 = 5V_{TH}$$

$$V_{TH} = 0.8$$

$\therefore V_{TH0} = 0.8$

3) (a) Body voltage refers to the voltage difference between the body/bulk terminal and the source terminal of the MOSFET.

Generally, for an n-MOS transistor, the body voltage is typically connected to the lowest voltage in the circuit, usually the ground (0 volts). An n-MOS transistor operates with positive gate voltages to turn it on.

For a p-MOS transistor, the body voltage is typically connected to the highest voltage in the circuit, usually the supply voltage (VDD). A p-MOS transistor operates with negative gate voltages to turn it on.

If the body voltage is reversed, i.e., applied opposite to the convention mentioned above, it leads to undesirable effects such as:

- **Increased leakage current**: Reversing the body voltage can lead to increased substrate leakage currents in the transistor, reducing its performance and efficiency.
- **Threshold voltage shifts**: The threshold voltage of the transistor might increase from its desired value, leading to difficulty in channel formation.

(b) High V_t devices are preferred for low leakage current but have higher delays. Low V_t devices are preferred when low delays (better performance) are required but have higher leakage currents.

(c) Reducing channel length reduces the number of minority charges required for inversion, thereby decreasing the V_{GS} required to create an inversion layer. So, the threshold voltage decreases if the channel length decreases and vice-versa.

(d) When V_{in} is 0V, the drain voltage of NMOS is V_{DD}. When V_{GS} just crosses V_{thn}, V_{DS} $(= V_{DD})$ is greater than $(V_{GS} - V_{thn})$. The NMOS turns on in the saturation region.

(e) i) increase
ii) decrease
iii) increases
iv) increase
v) increase
vi) not change

4) i) E=V/L. If length is reduced by 2, the electric field is doubled
ii)

- Mobility degradation
- Velocity saturation
- Drain-Induced Barrier Lowering (DIBL)
- Hot carriers
- Higher leakage currents due to reduced threshold voltage.

iii) By reducing the doping concentration of drain, source, and bulk, the depletion region around the source and drain reduces. Another solution can be to reduce the supply voltage to prevent velocity saturation.

- Mobility degradation - Implementing advanced material engineering techniques to enhance carrier mobility, such as using high-k dielectrics and strained silicon.
- Velocity saturation - Designing transistors with shorter channel lengths and optimizing doping profiles to mitigate velocity saturation effects.
- Drain-Induced Barrier Lowering (DIBL) - Utilizing engineering solutions like shallow trench isolation (STI) and adjusting device geometries to minimize DIBL impact.
- Hot carriers - Incorporating techniques like channel engineering and adopting gate dielectrics with higher bandgaps to mitigate hot carrier effects.
- Higher leakage currents due to reduced threshold voltage - Implementing innovative gate stack engineering methods and exploring materials with higher electron affinity to mitigate threshold voltage reduction and subsequent leakage currents.