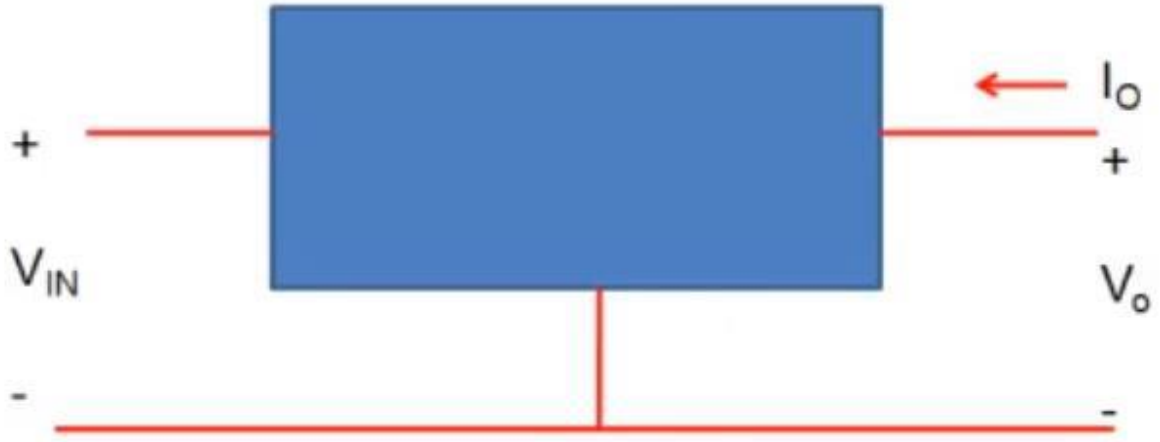
MOSFET

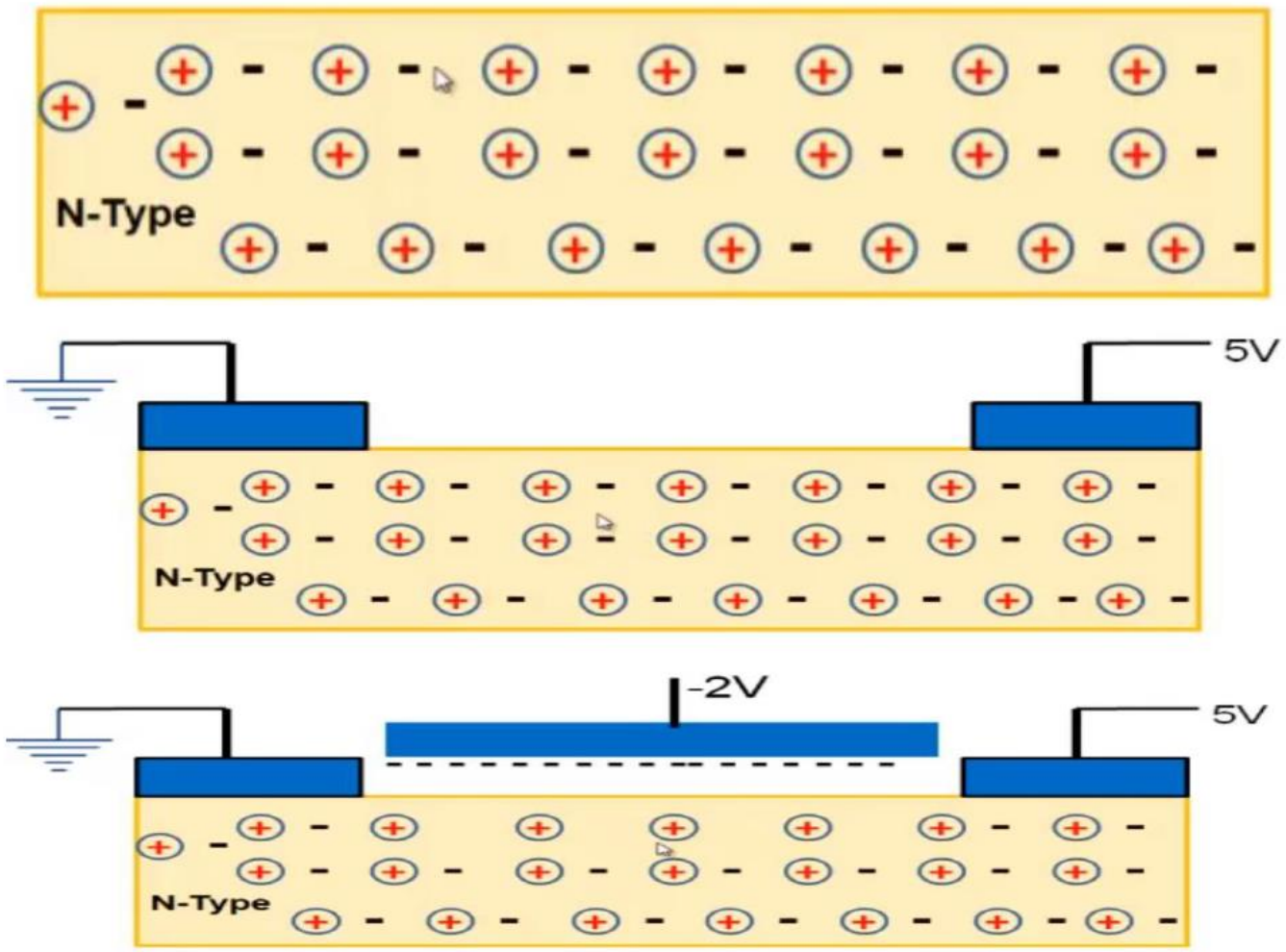
Transistor



Current I_O is much more sensitive to V_{IN} than V_O

$$\frac{\partial I_O}{\partial V_{in}} >> \frac{\partial I_O}{\partial V_o}$$

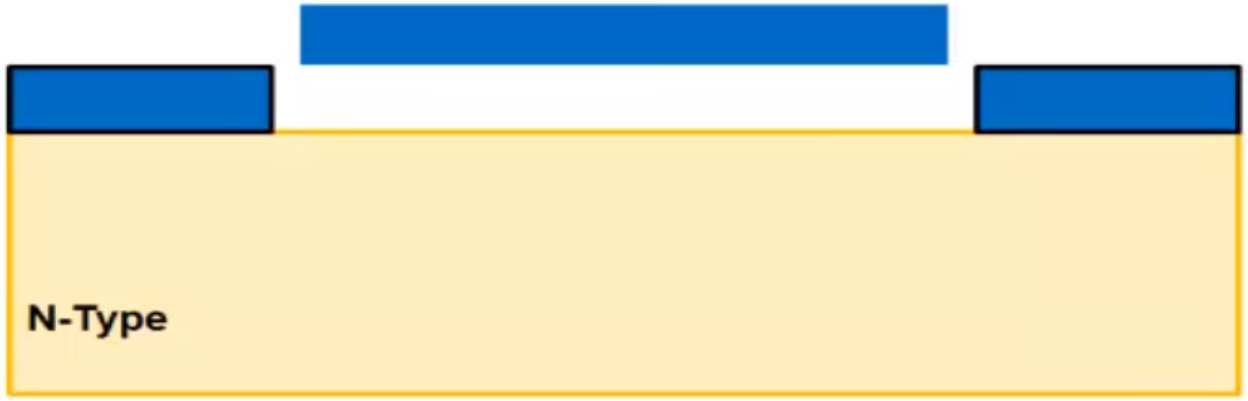
Field Effect Principle

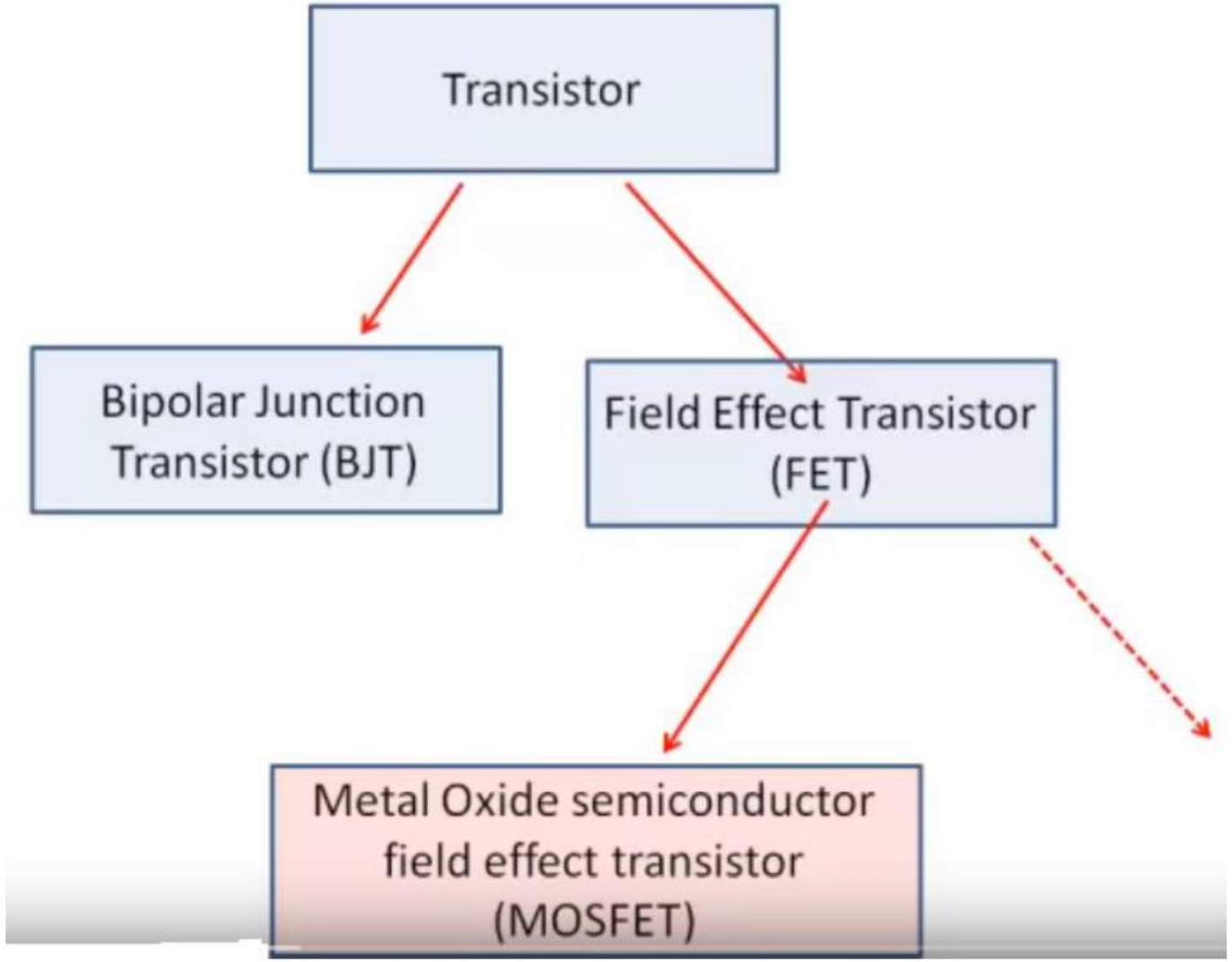


Modulation of conductivity using electric field

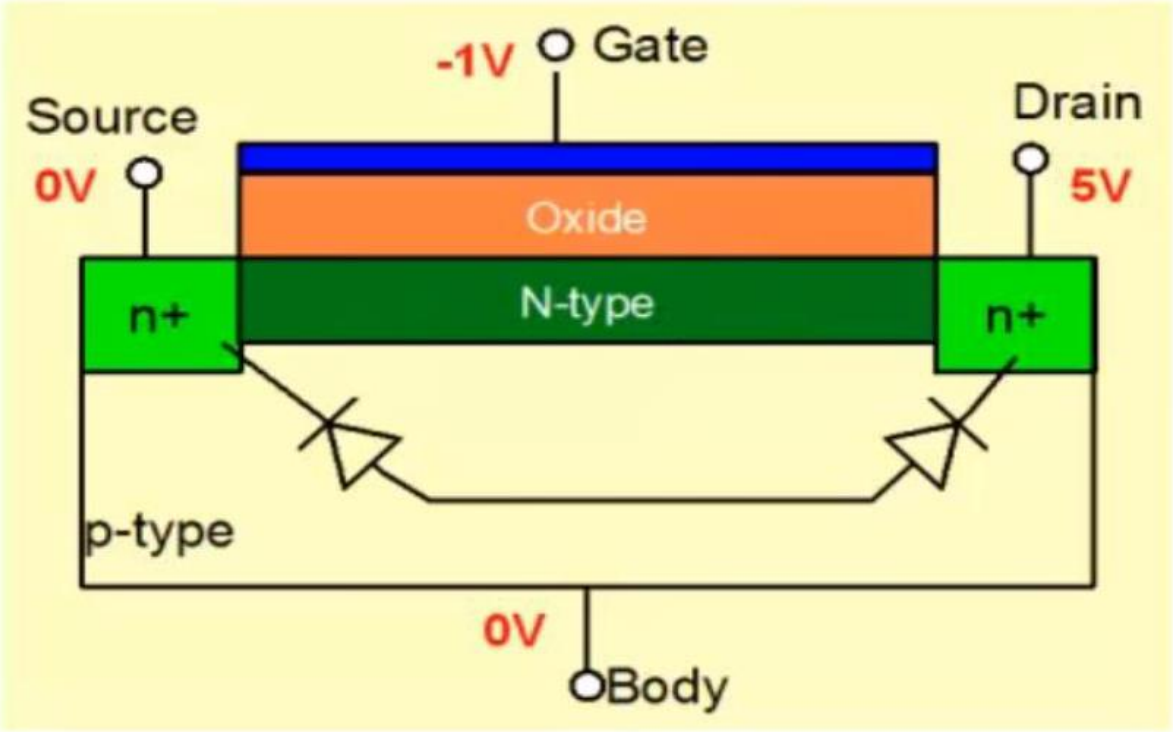
Transconductance

Field Effect Principle




Transistor
Bipolar Junction Transistor (BJT)
Field Effect Transistor (FET)
Metal Oxide semiconductor field effect transistor (MOSFET)

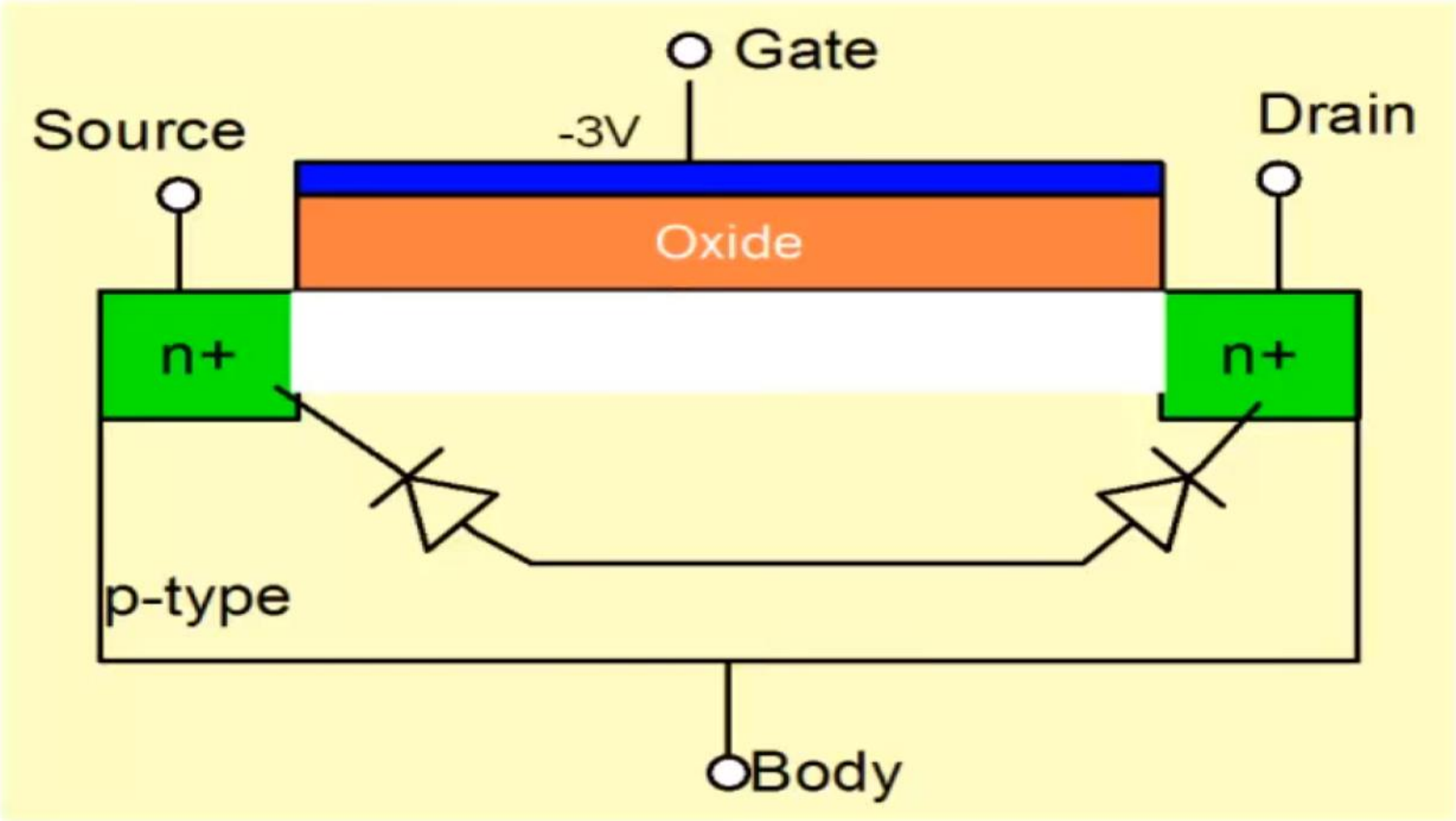
Depletion-Mode Transistor



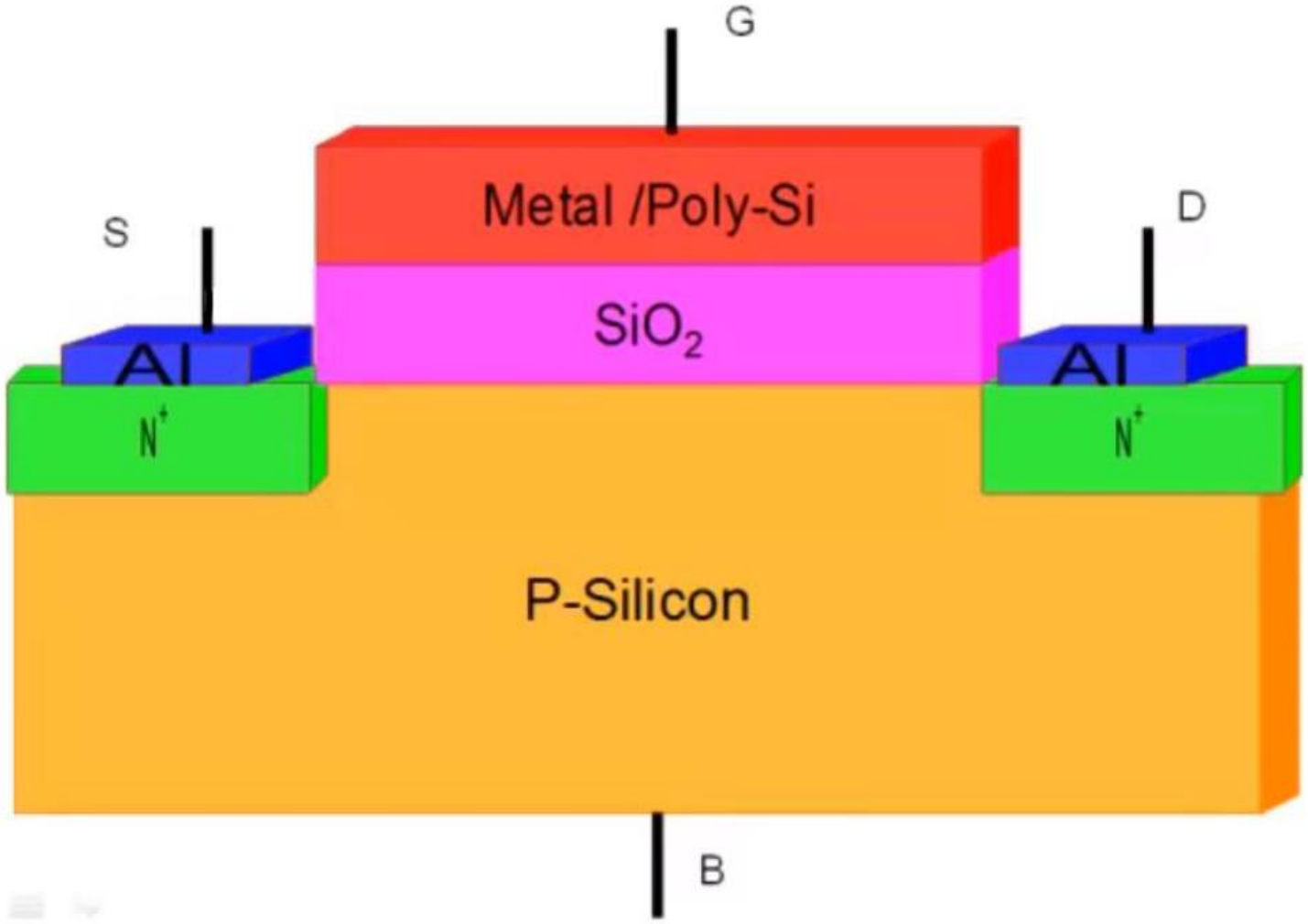
In a depletion-mode transistor, a channel exists without any gate voltage being applied and current flows when drain voltage is applied.

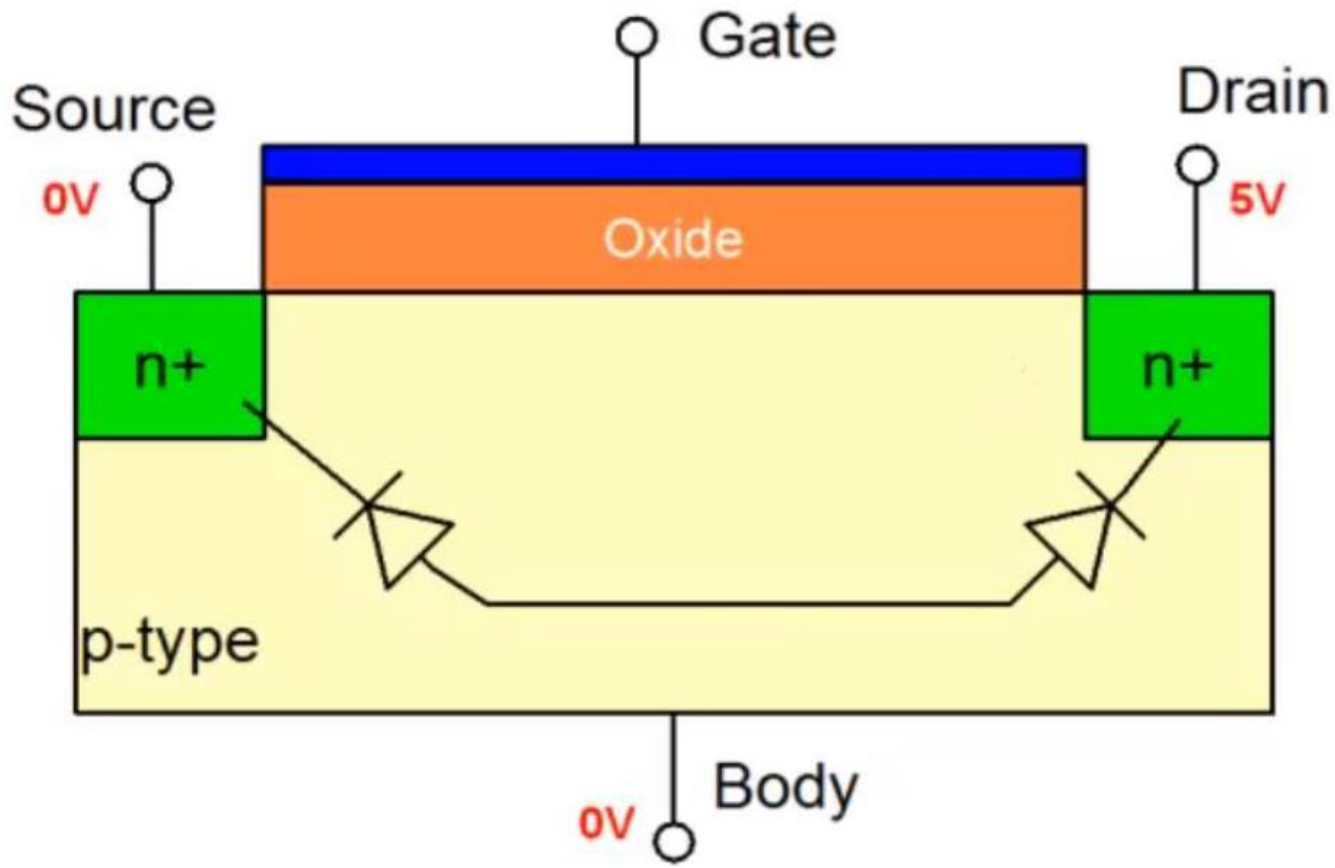
Negative gate voltage is applied to deplete the channel of carriers and cause current to reduce.

Channel exists at zero gate voltage and is depleted by gate voltage

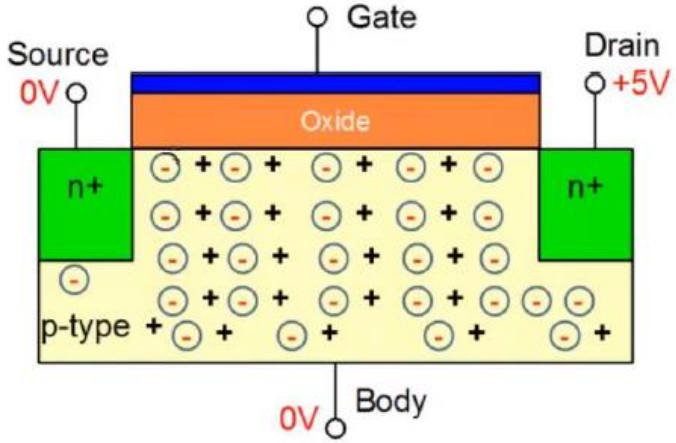


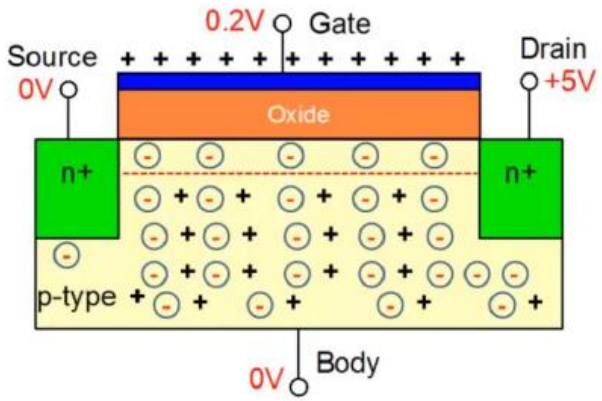
Channel is completely pinched off and current ~zero


G
Metal /Poly-Si
S
D
SiO_2
Al
Al
N^+
N^+
P-Silicon
B

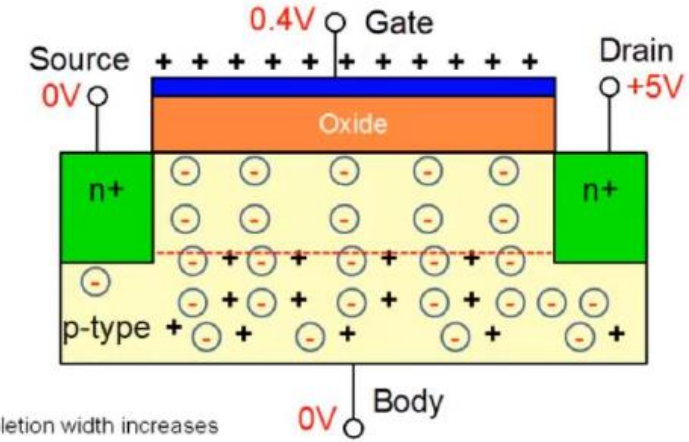


No channel exists when gate voltage is zero and current is zero as well.

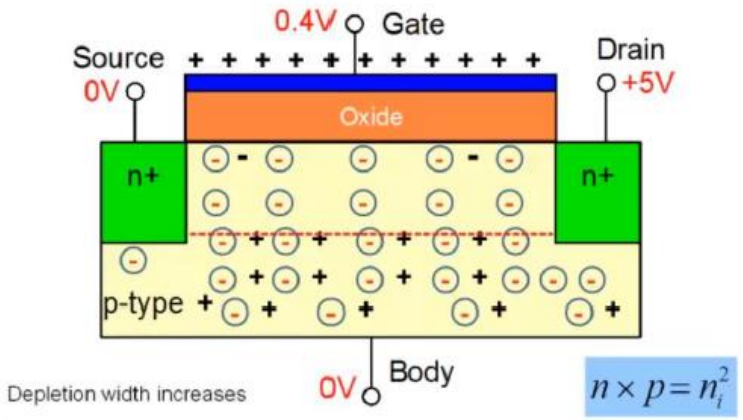




Depletion Region is formed near the Si/SiO_2 interface



Depletion width increases

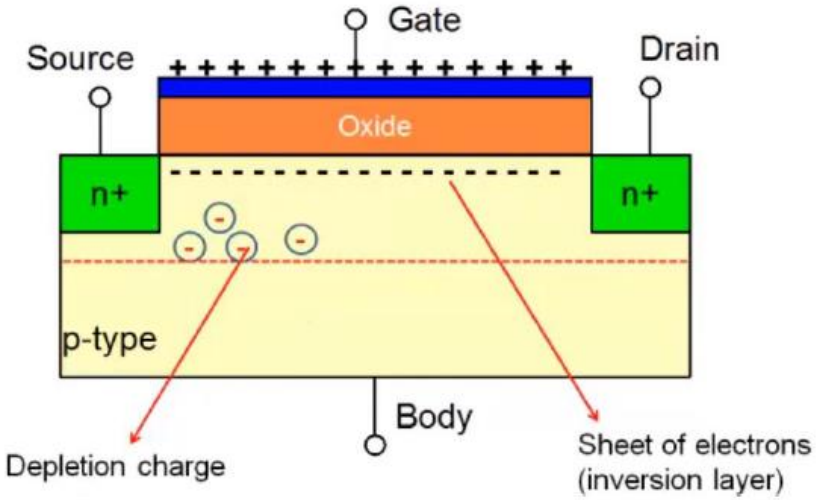


Depletion width increases

$$n \times p = n_i^2$$

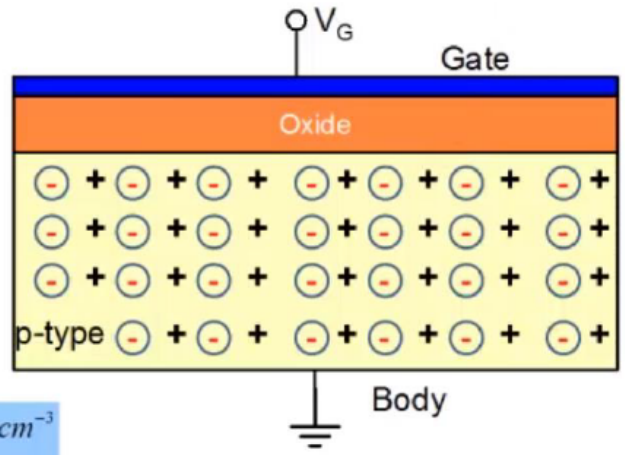
But something interesting happens: electron density at the surface also increases

At a sufficiently large voltage ($>V_{THN}$) a channel of electrons forms at the Si/SiO2 interface.



Conductivity modulation at the surface?

MOS capacitor constitutes the heart of a MOSFET

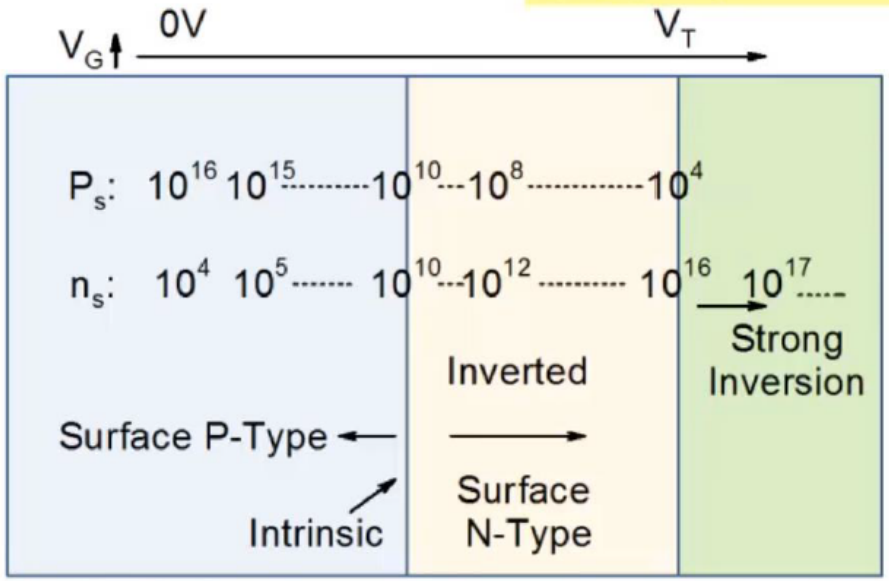


$$p = N_A = 10^{16} cm^{-3}$$

$$n = \frac{n_i^2}{N_A} \cong 10^4 cm^{-3}$$

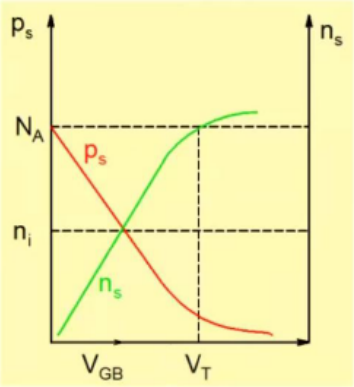
Field Effect...

$$n_s \times p_s = n_1^2 \cong 10^{20} cm^{-3}$$



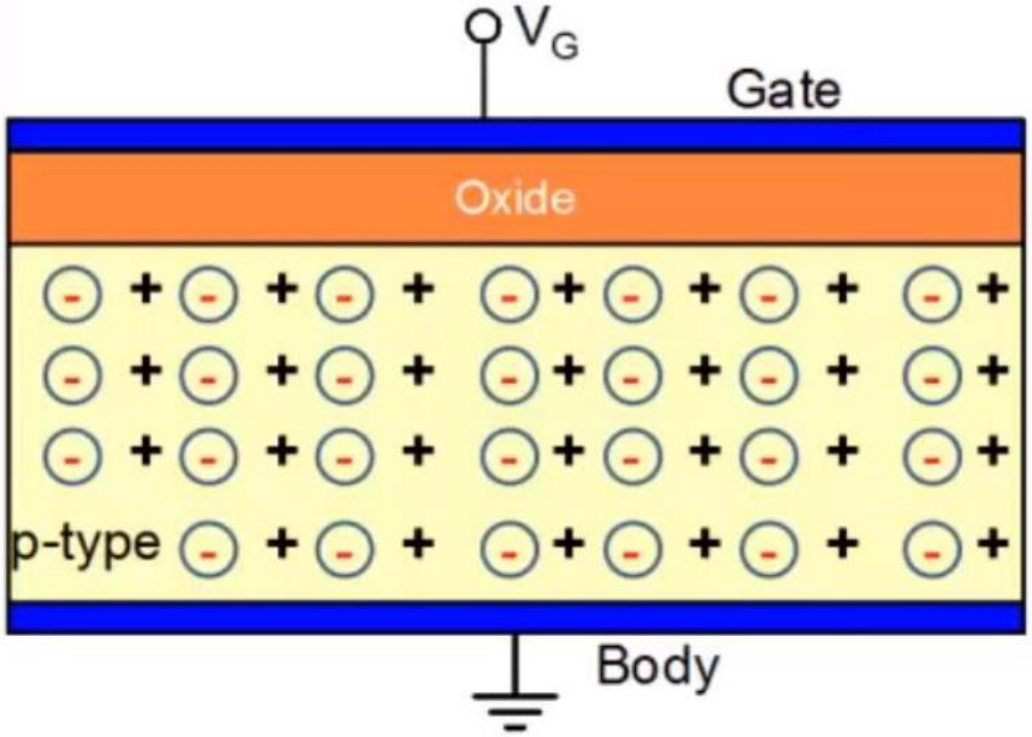
Surface carrier density can be changed from P-type to N-type

Surface Carrier Density



Flat band condition

$$V_G = V_{FB}$$

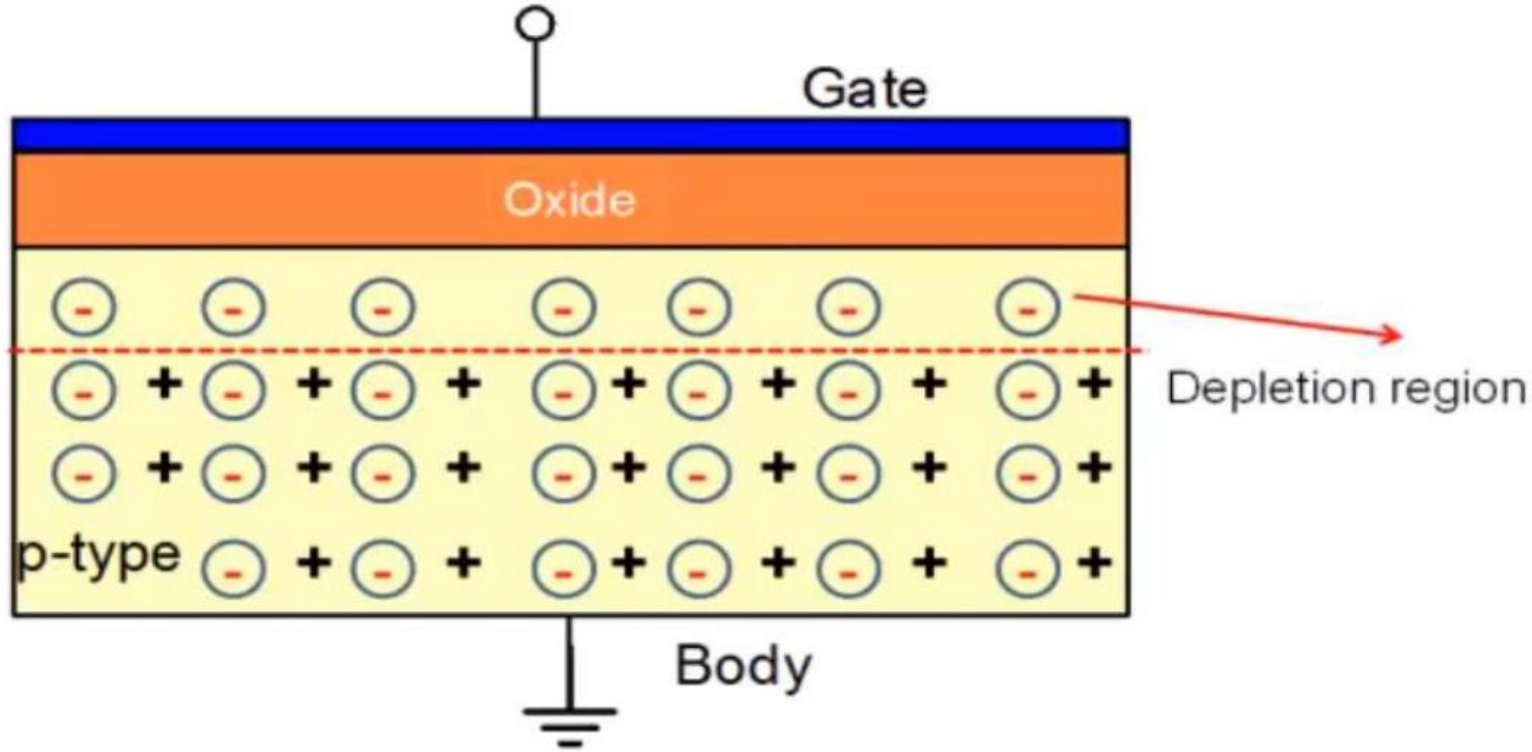


Whenever two different material are brought into contact, an internal potential difference develops like in a pn junction. Thus even when no gate voltage is applied, there is a voltage across the mos capacitor.

$V_G = V_{FB}$; Flat-band condition meaning no NET voltage across the capacitor.
Uniform hole density everywhere

Depletion

$$V_G > V_{FB} \text{ but } V_G < V_{THN}$$

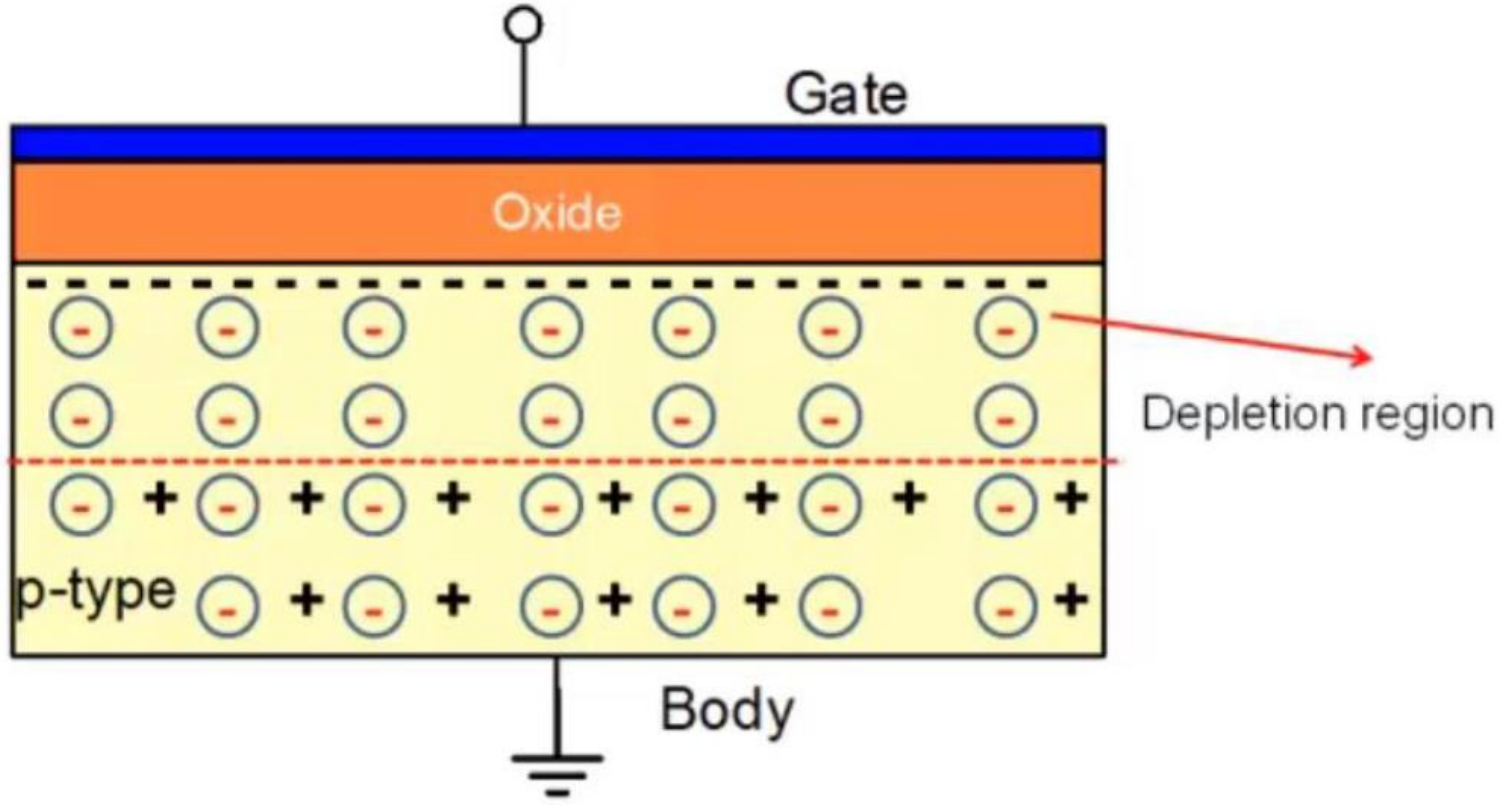


Holes are depleted from the surface $p_S < p_B$

Although $n_S > n_B$ electron density is also very small

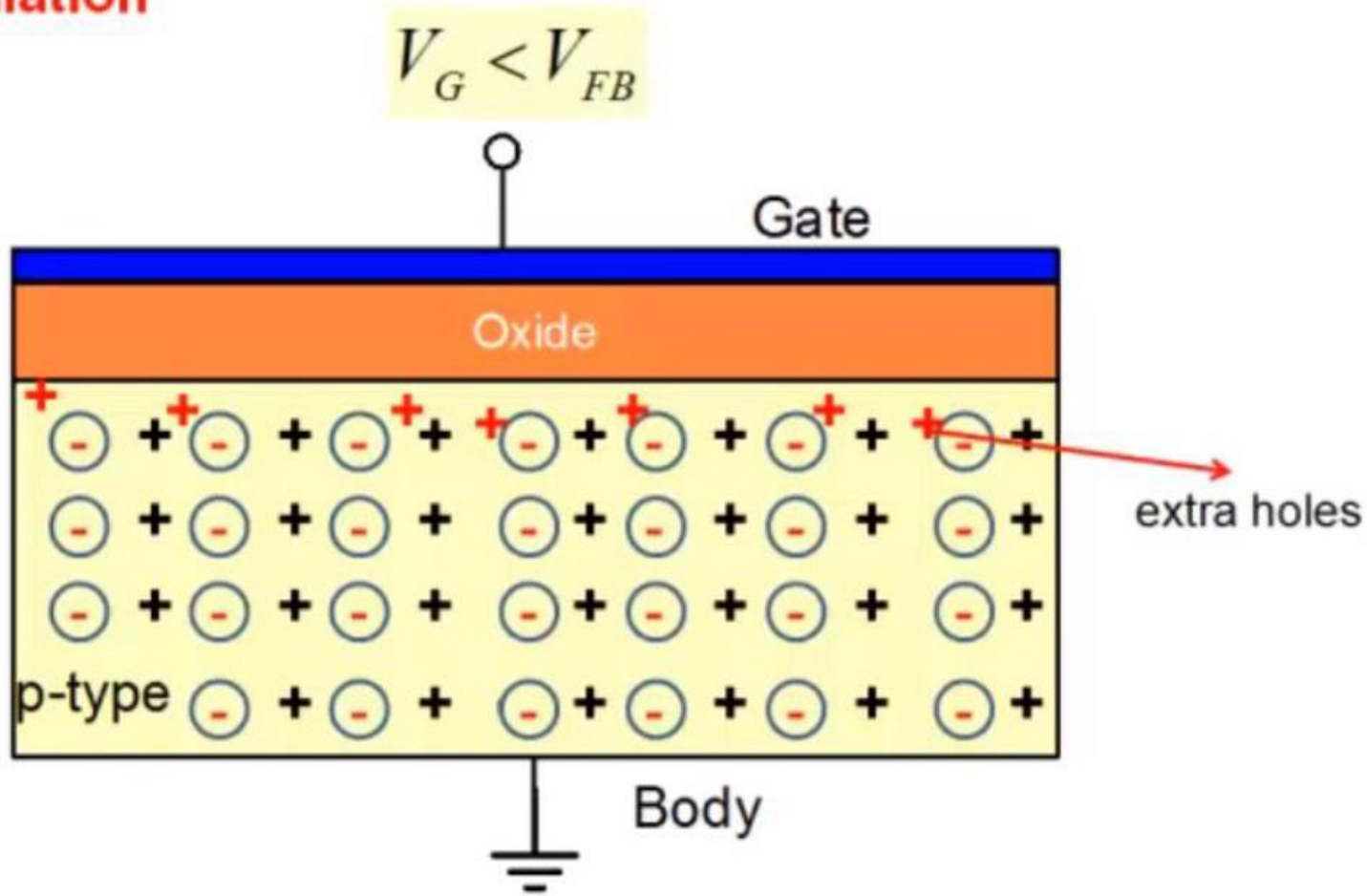
Strong Inversion

$$V_G > V_{THN}$$



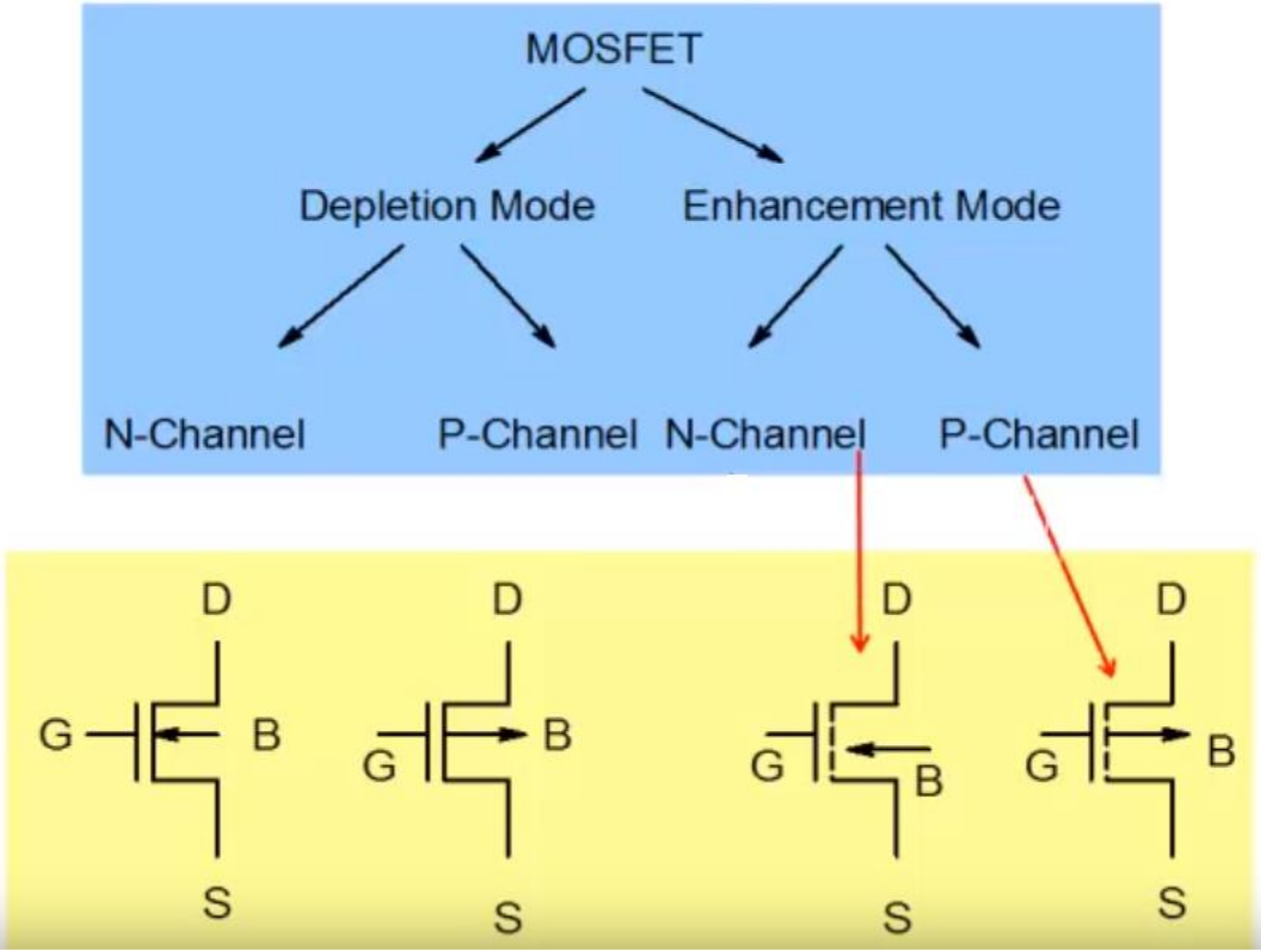
Electrons are accumulated at the surface $n_S >> N_A$

Accumulation

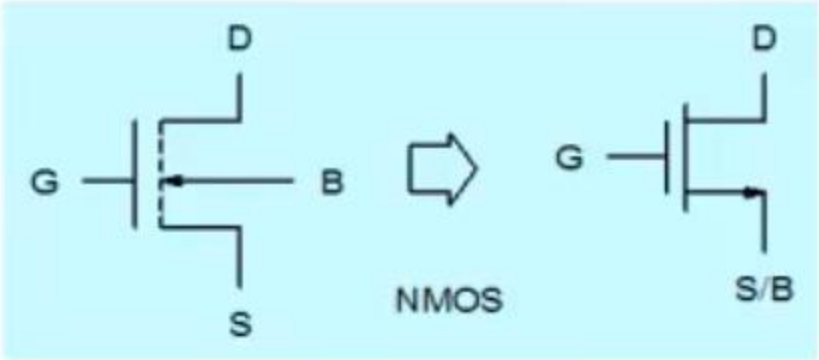


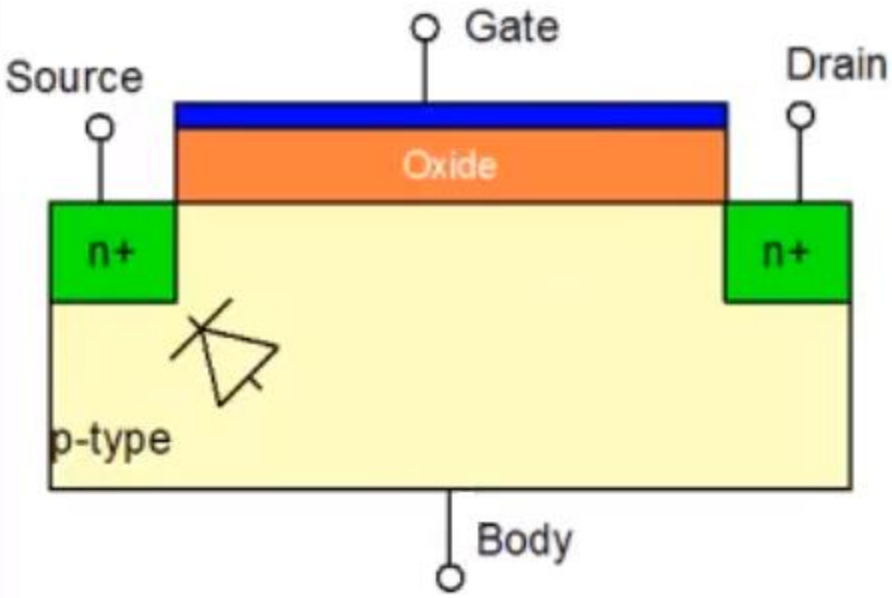
Holes are accumulated at the surface $p_S > p_B$

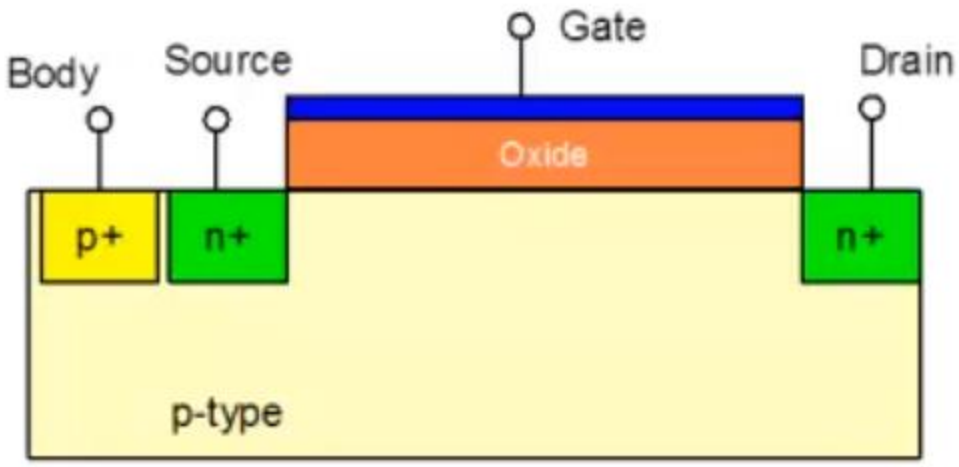
Metal Oxide Semiconductor Field Effect Transistor:



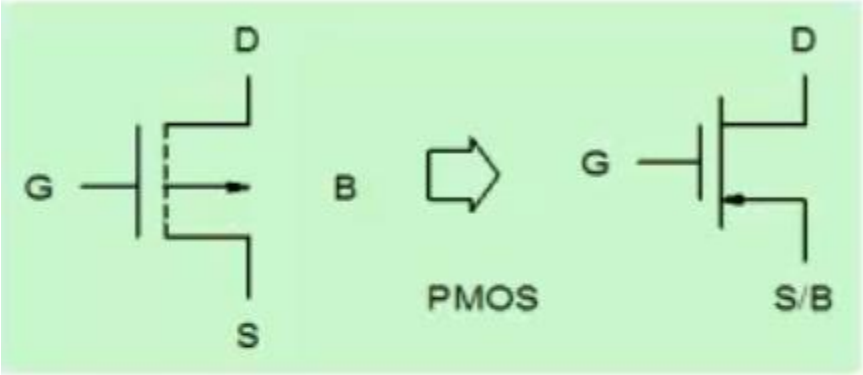
Simplified Symbols and structure

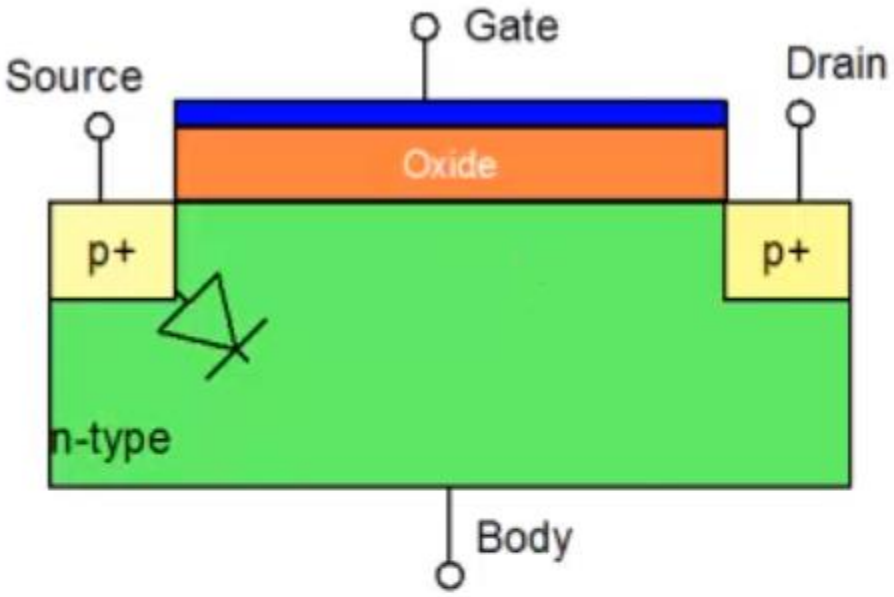


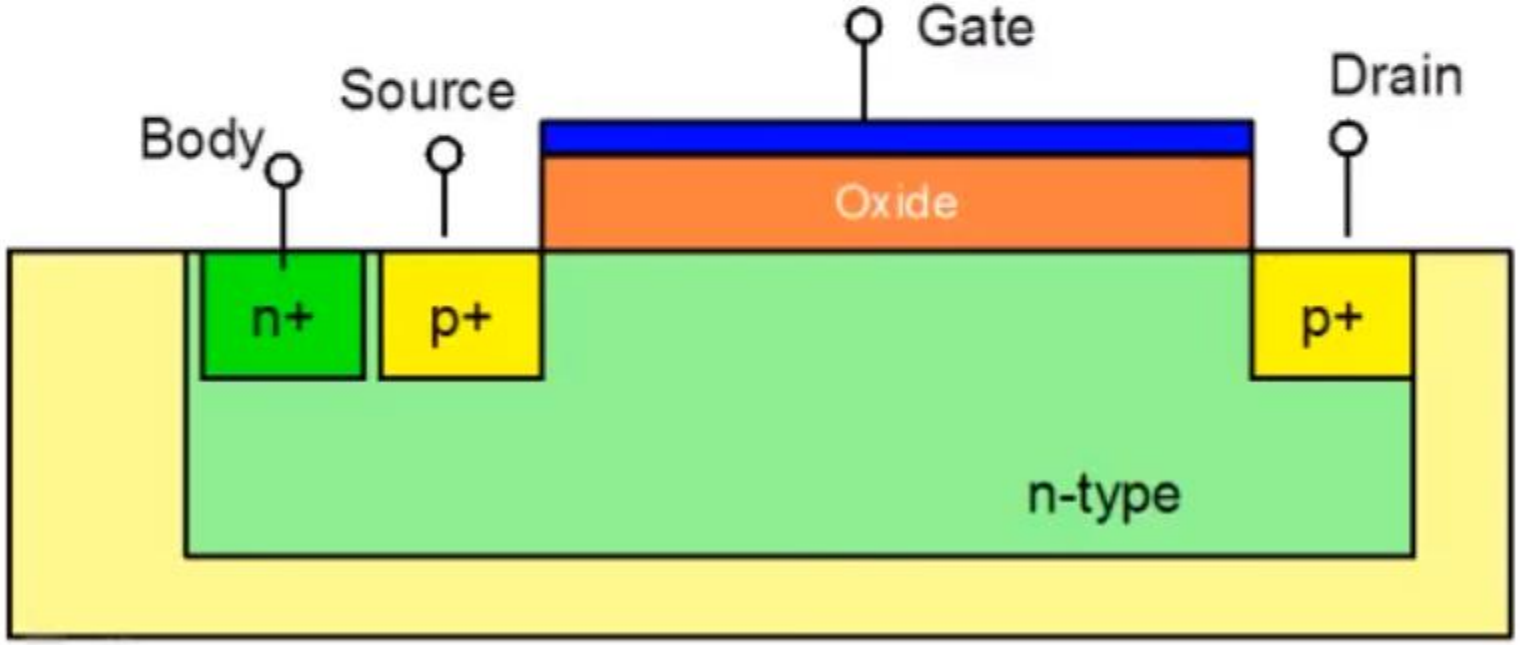


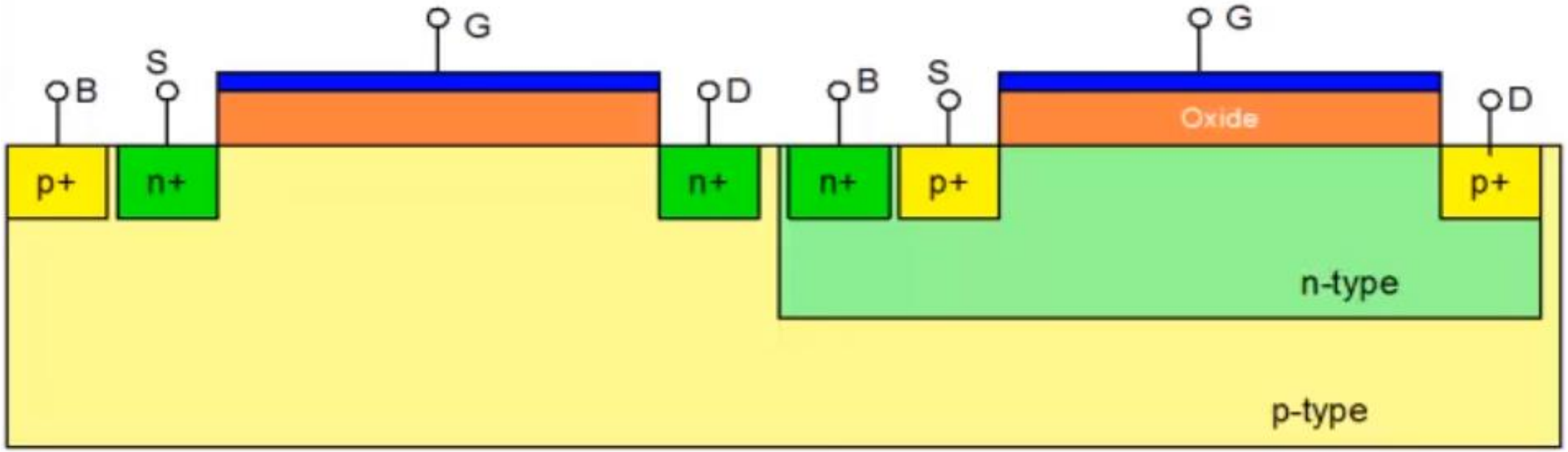


Simplified Symbols and structure



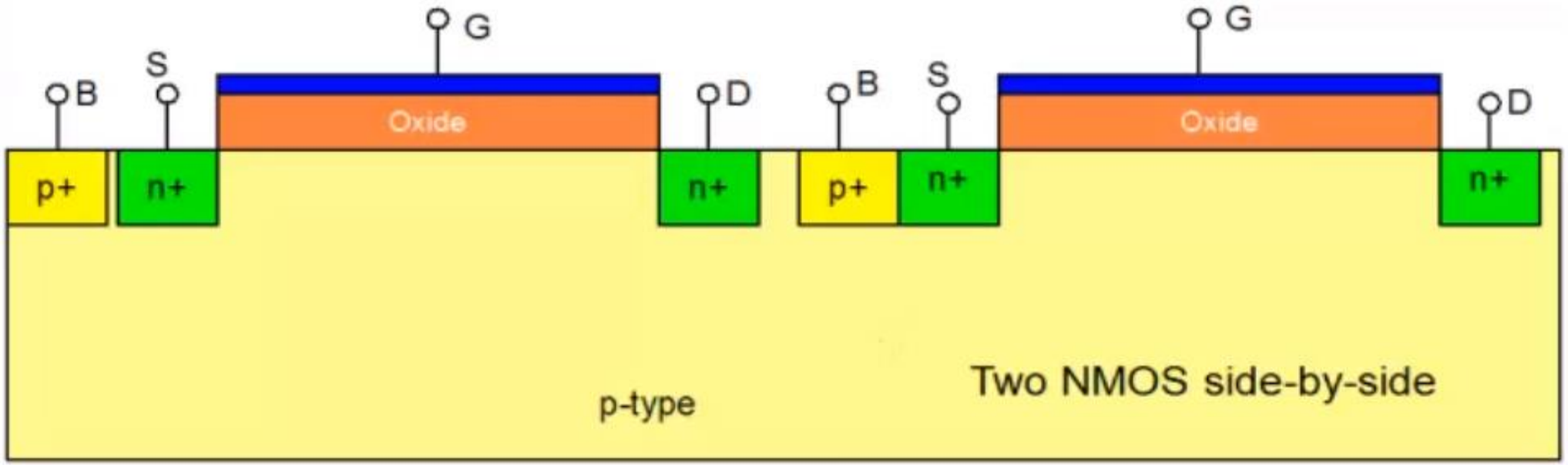


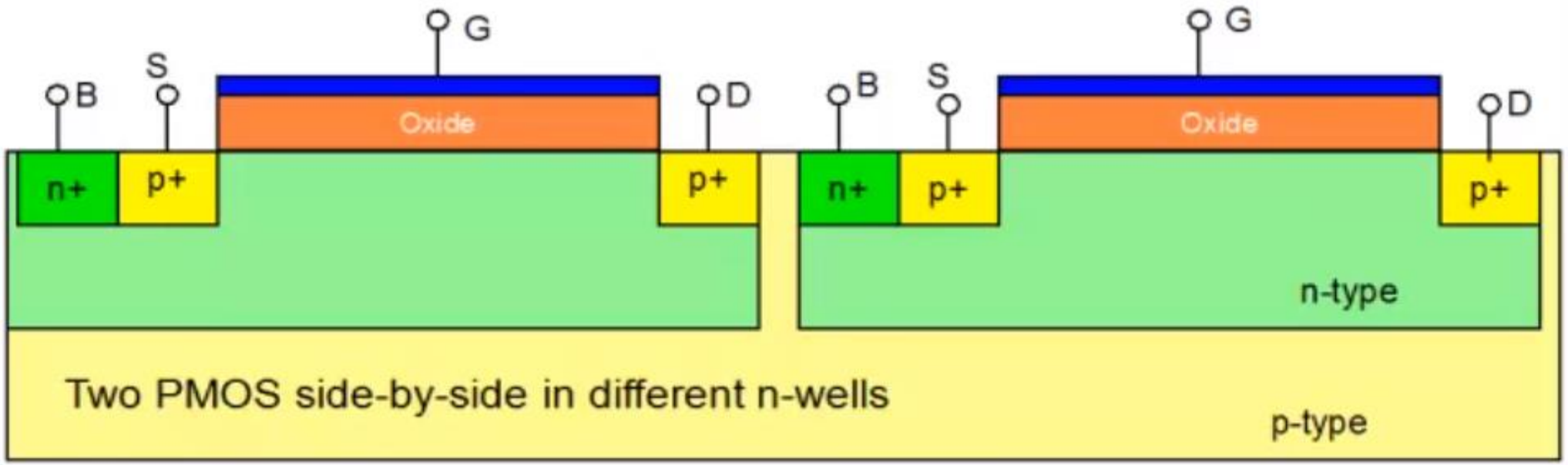


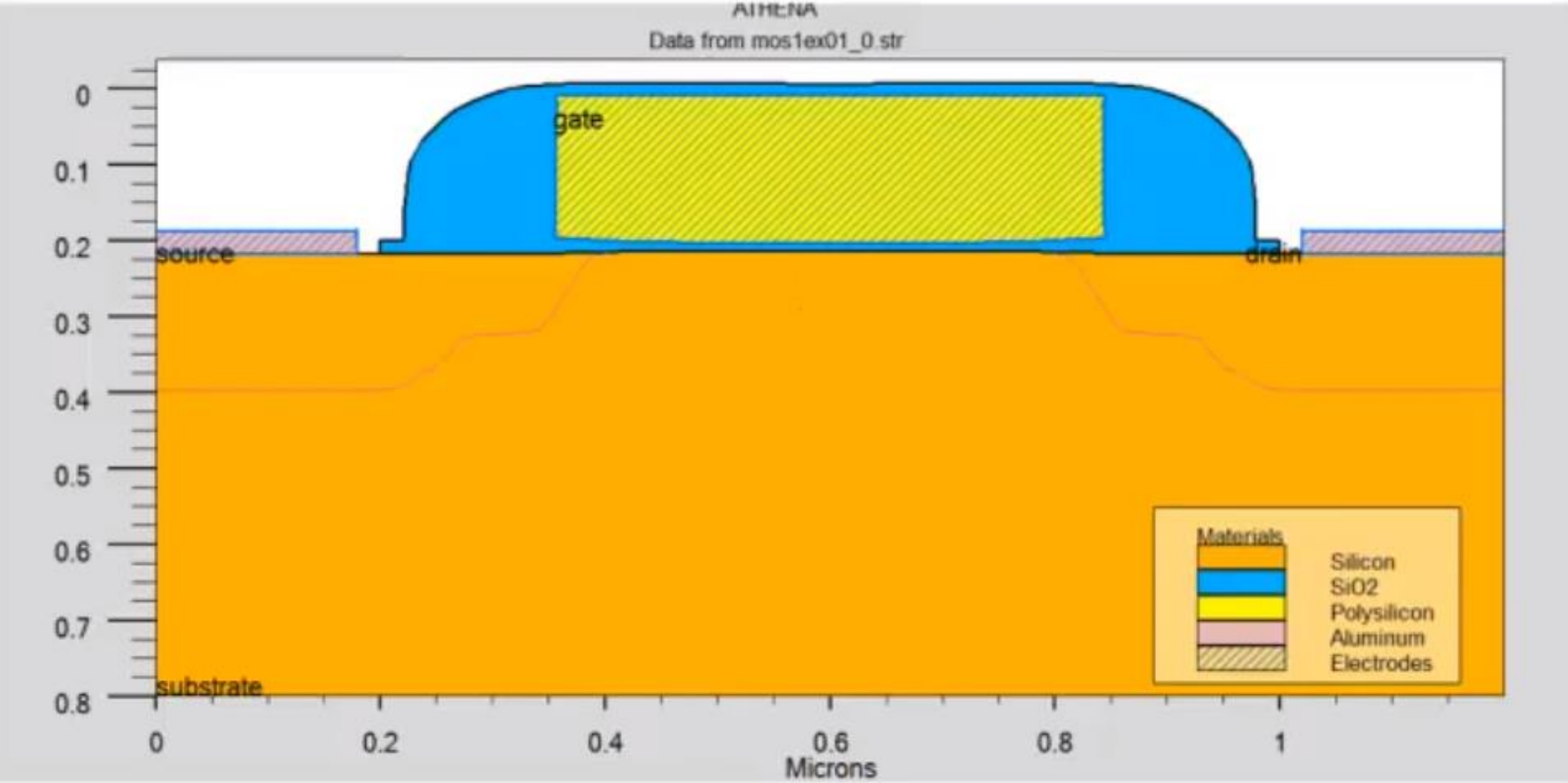


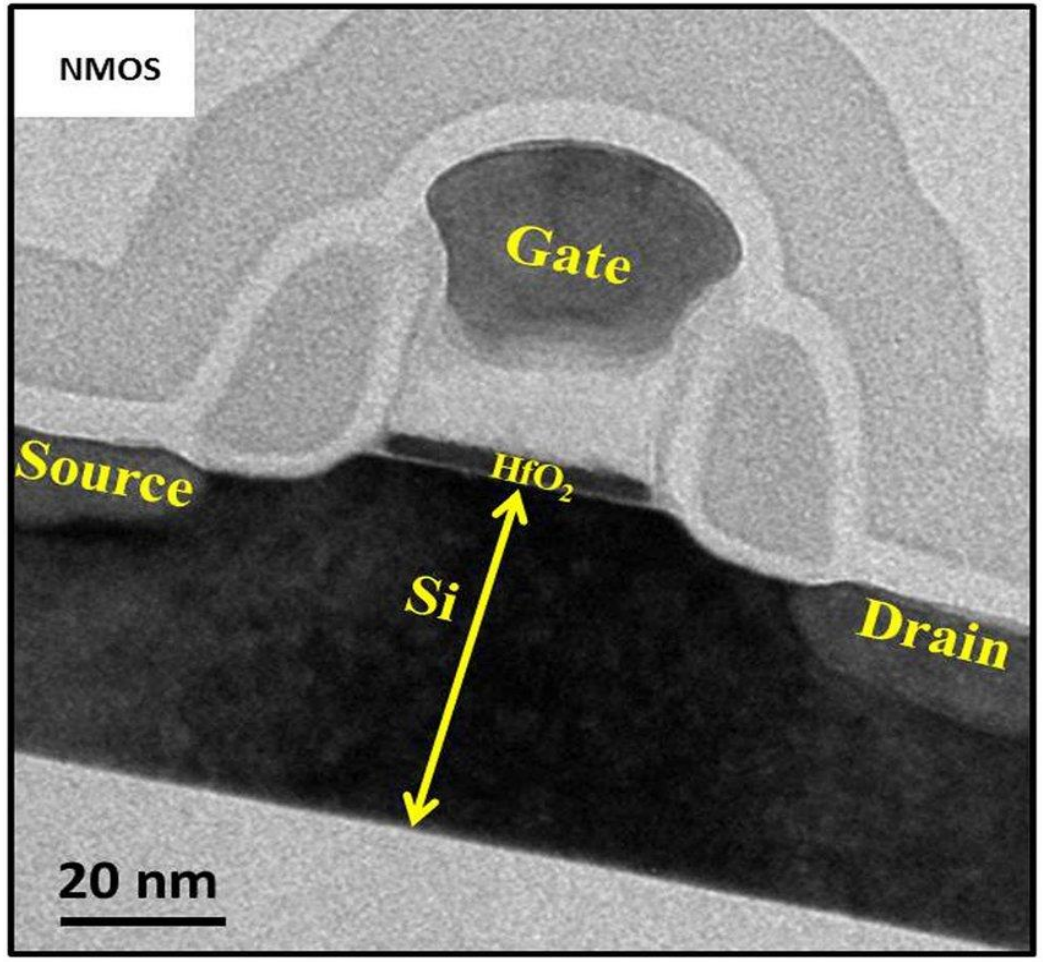
- Body potential of NMOS transistors is same and is normally connected to the most negative voltage in the circuit to ensure that VBS < 0 and thus body-source PN junction is reverse biased.

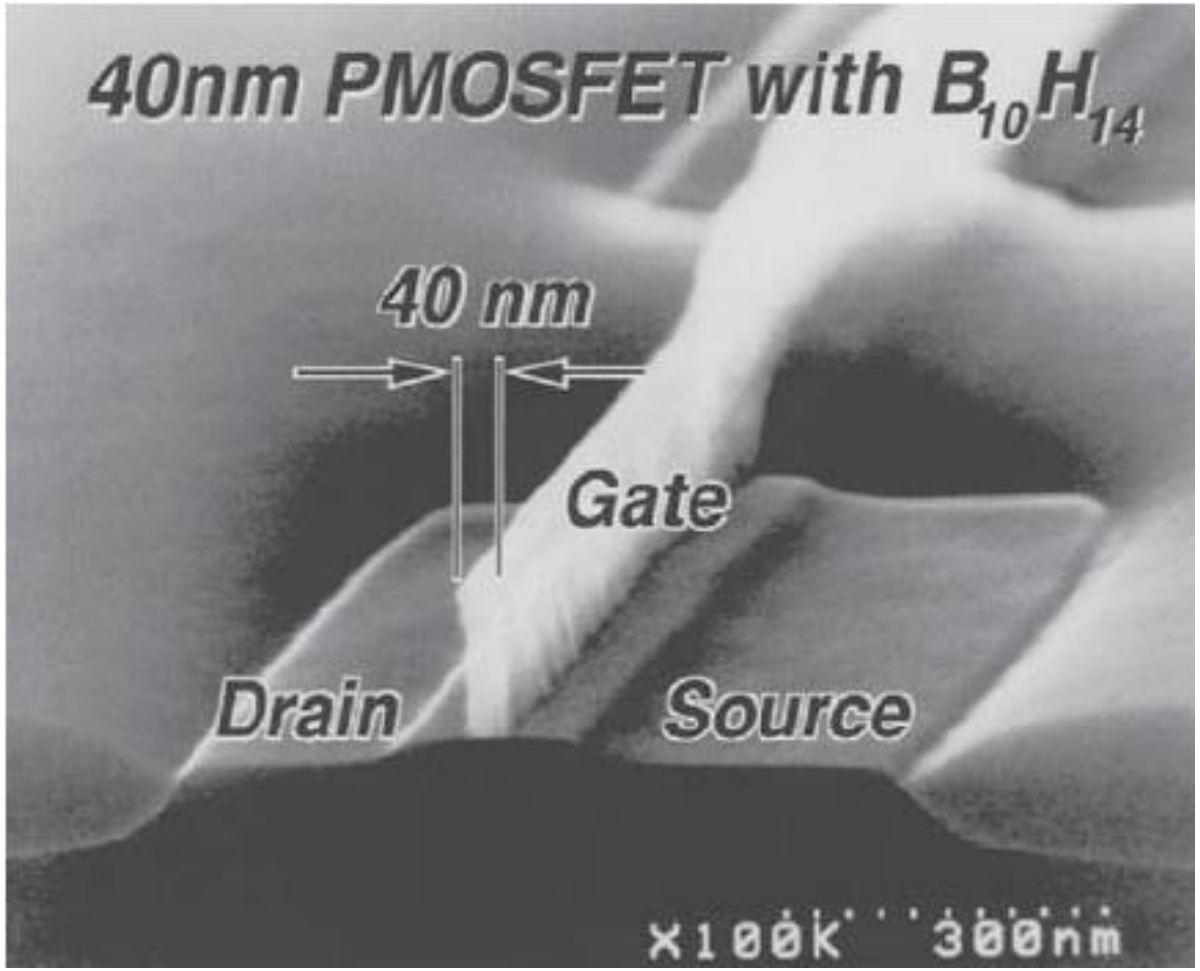
- Each PMOS can be fabricated in a separate individual N-well and thus each pmos body terminal can have a distinct voltage. Normally body and source terminals of PMOS are shorted together.


G
S
B
D
Oxide
p+
n+
n+
p+
n+
Oxide
n+
p-type
Two NMOS side-by-side

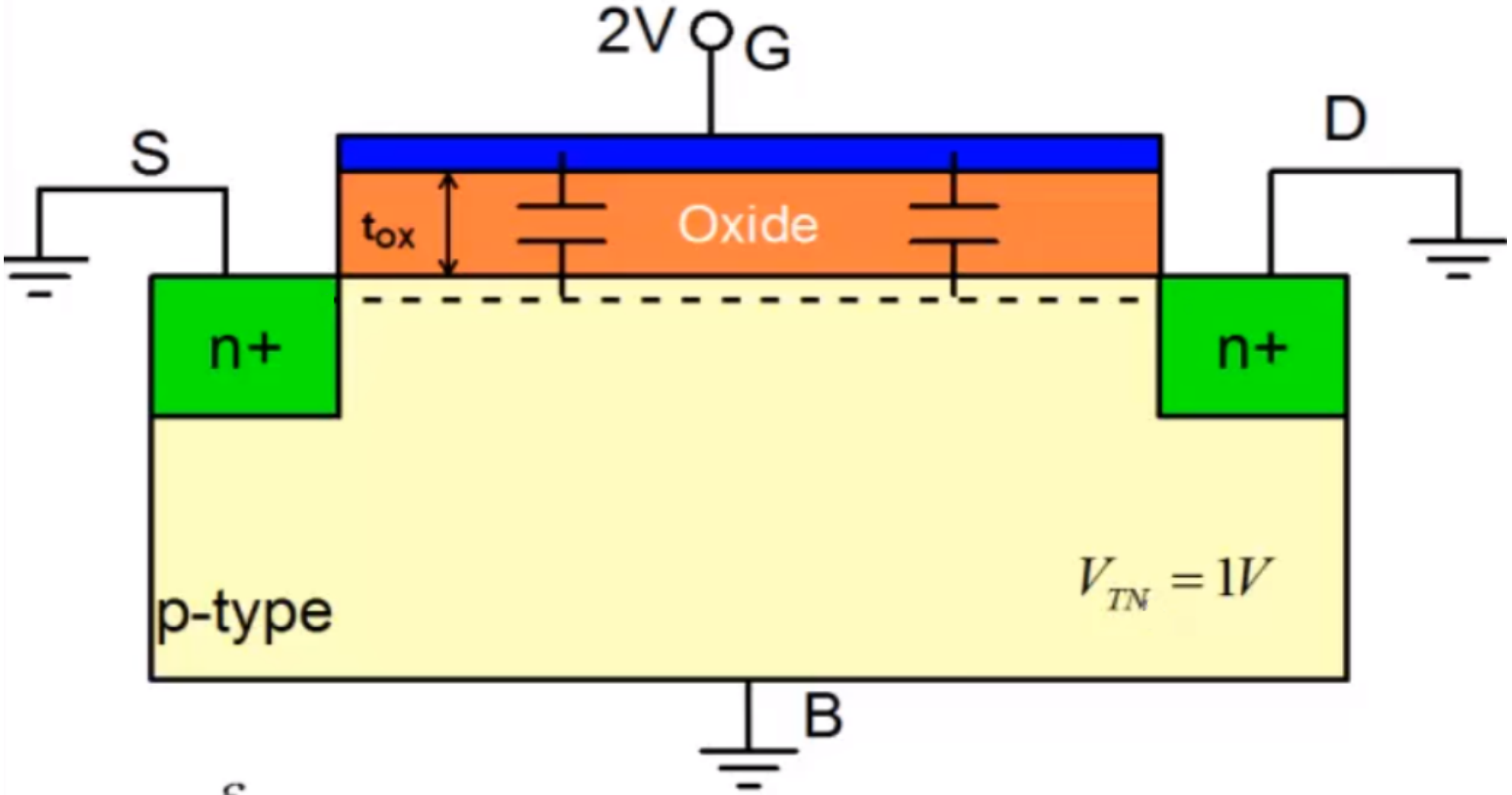

G
S
B
D
Oxide
n+
p+
p+
n+
p+
Oxide
p+
n-type
Two PMOS side-by-side in different n-wells
p-type


ATHENA
Data from mos1ex01_0.str
gate
source
drain
substrate
Materials
Silicon
SiO2
Polysilicon
Aluminum
Electrodes
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0
0.2
0.4
0.6
0.8
1
Microns


NMOS
Gate
Source
HfO_2
Si
Drain
20 nm


40nm PMOSFET with $B_{10}H_{14}$
40 nm
Gate
Drain
Source
X100K 300nm

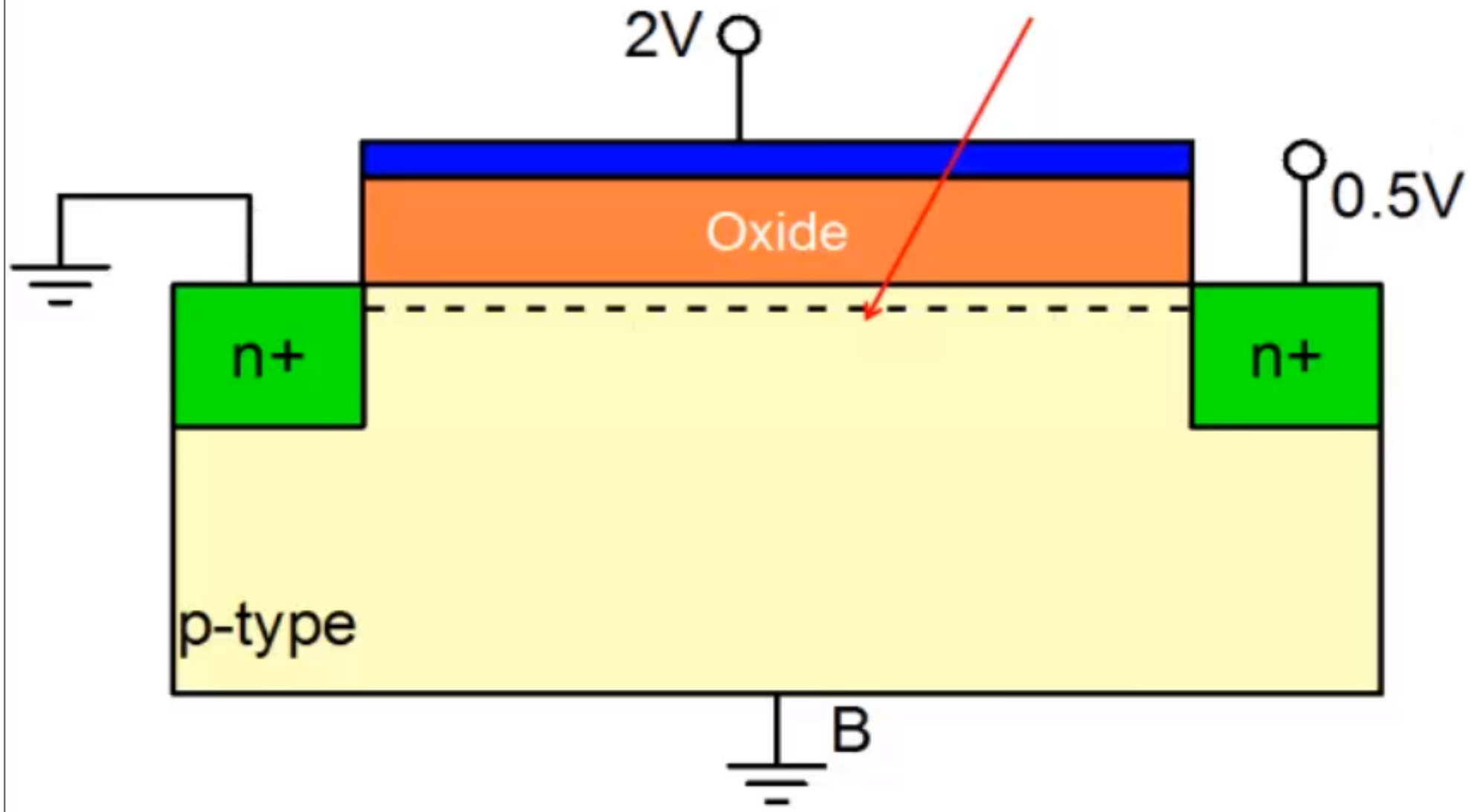
Operation of the MOSFET



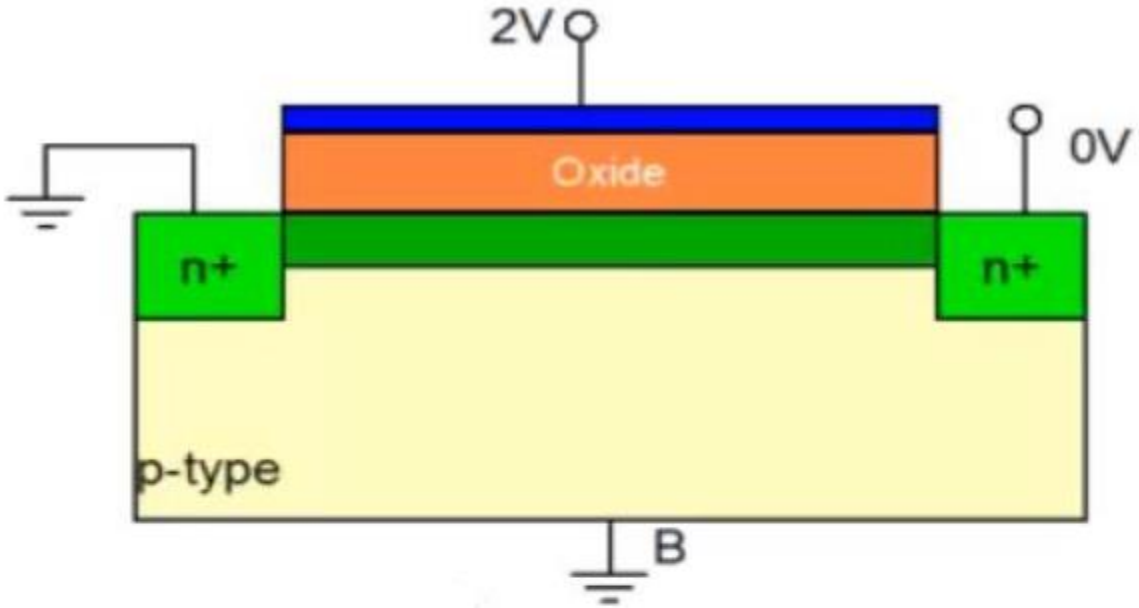
$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

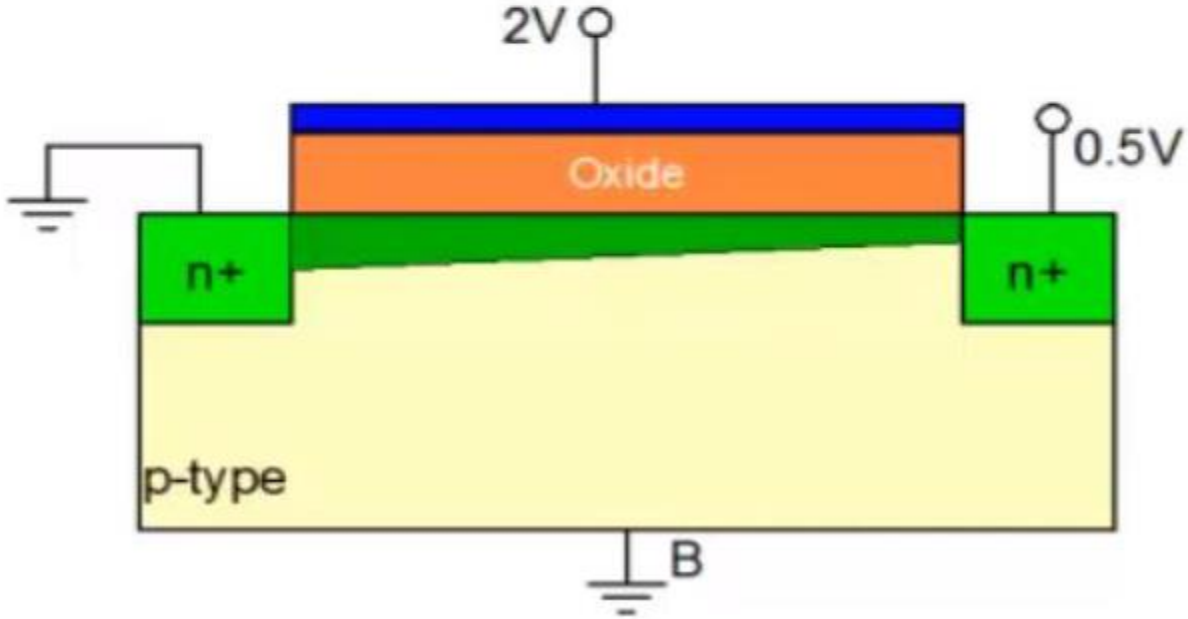
Inversion charge/area : $Q_{inv} = -C_{ox}(V_{GS} - V_{THN})$

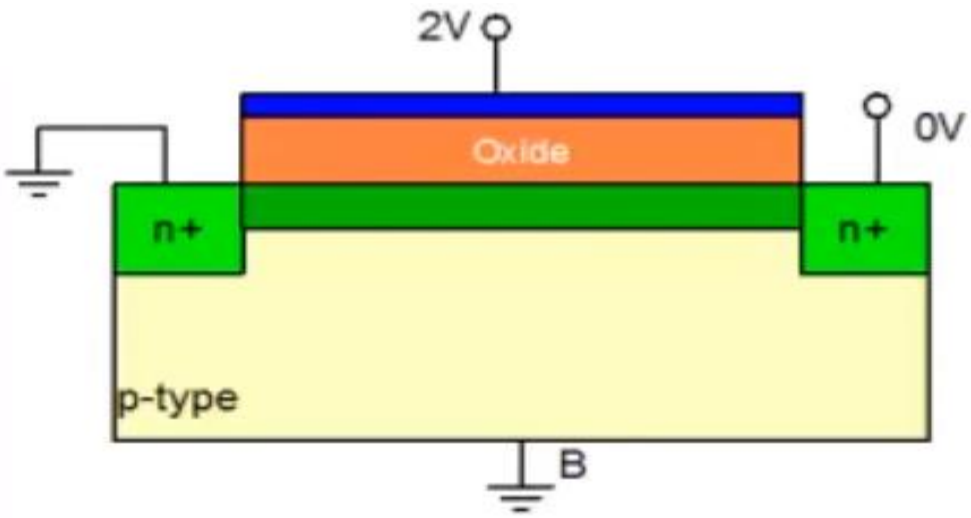
$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x))$$

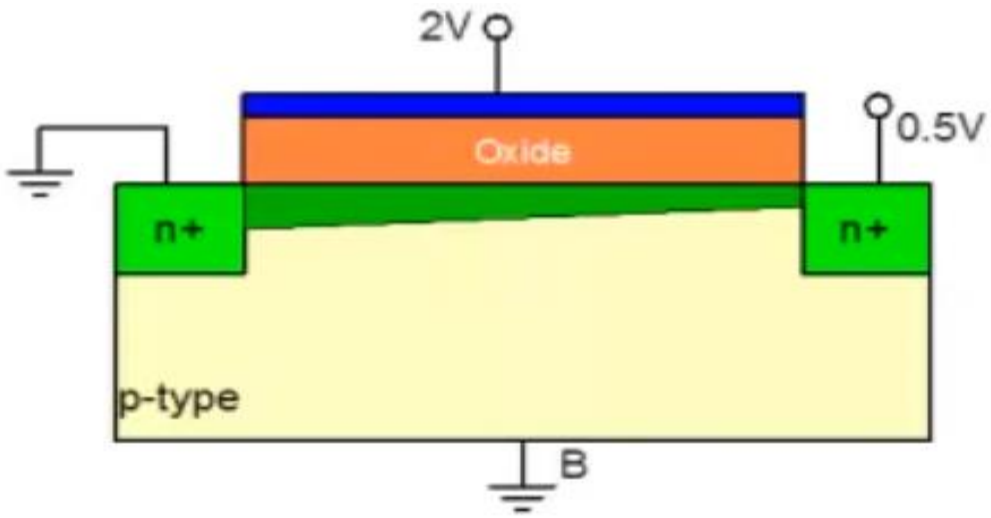


When a positive drain voltage is applied, current flows from drain to source and inversion charge density decreases from source to drain end.


2V
0V
Oxide
n+
n+
p-type
B


2V
0.5V
Oxide
n+
n+
p-type
B





$$dR_{ch} = \frac{1}{q\mu n(x)} \frac{dx}{W \times t}$$

$$R_{ch} \propto \frac{1}{\int Q_{inv} dx}$$

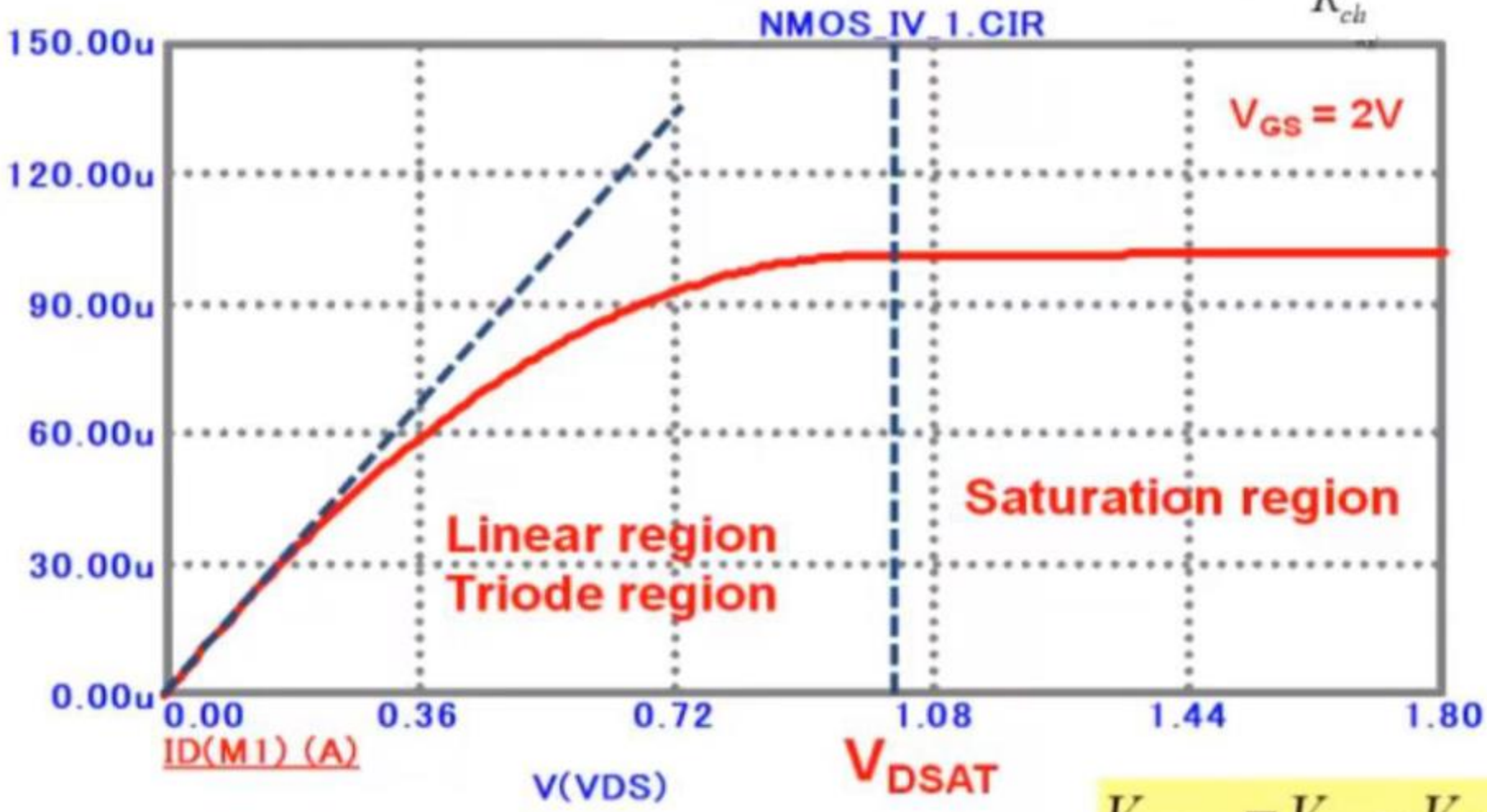
$$I_{DS} = \frac{V_{DS}}{R_{cho}} = 0$$

$$R_{ch} > R_{cho}$$

$$I_{DS} = \frac{V_{DS}}{R_{ch}} > 0$$

As drain voltage increases, channel resistance also increases causing drain current to depart from linear behavior

$$I_{DS} = \frac{V_{DS}}{R_{ch}} > 0$$

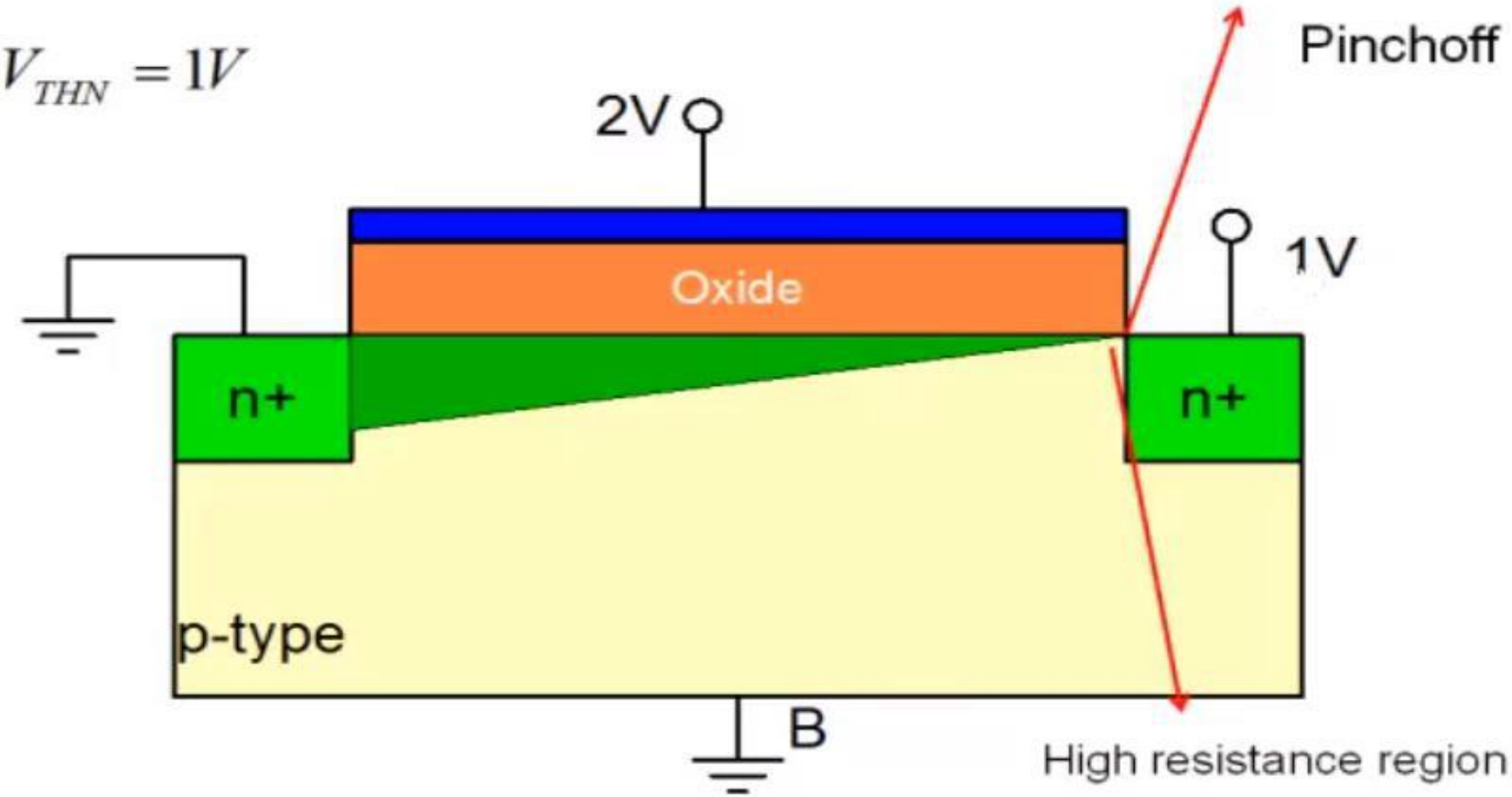


$$V_{DSAT} = V_{GS} - V_{THN}$$

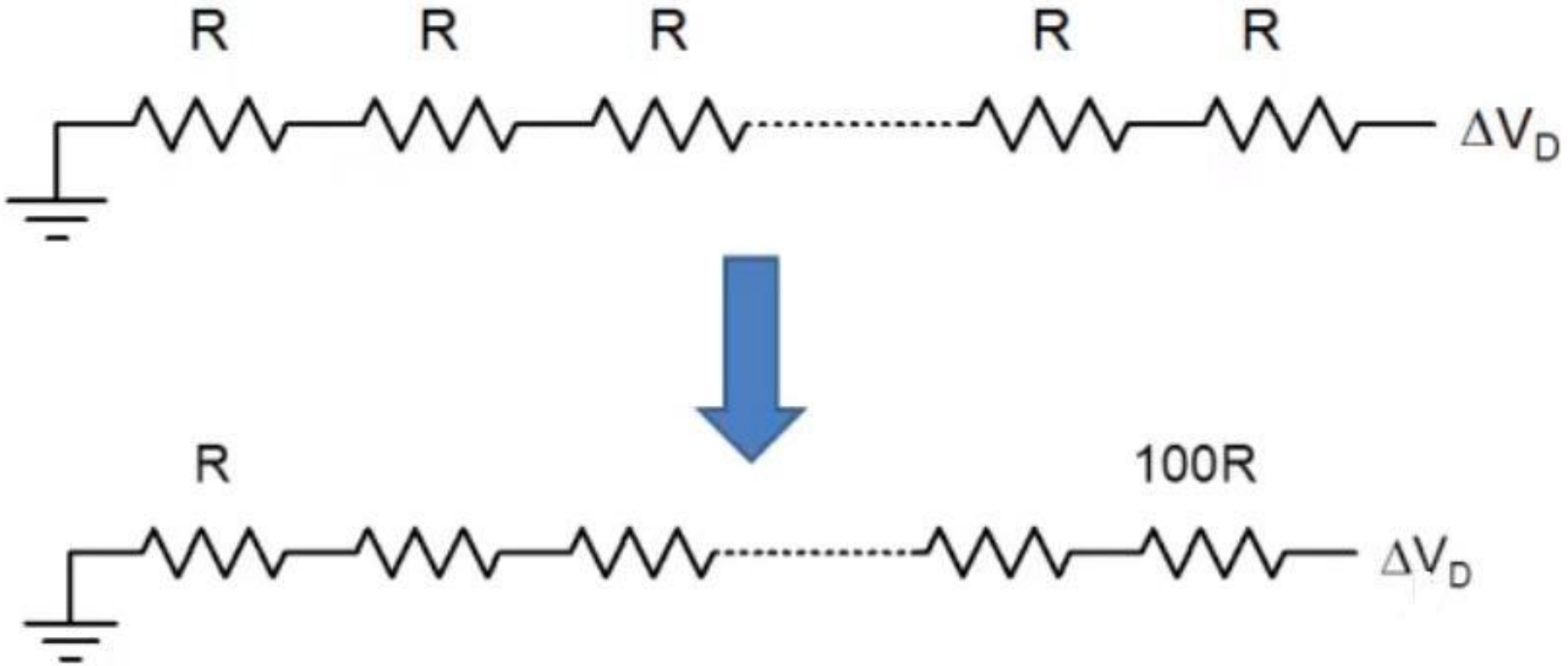
Note that **Saturation in MOSFET is analogous to forward active mode in BJT** and linear region is analogous to saturation in BJT.

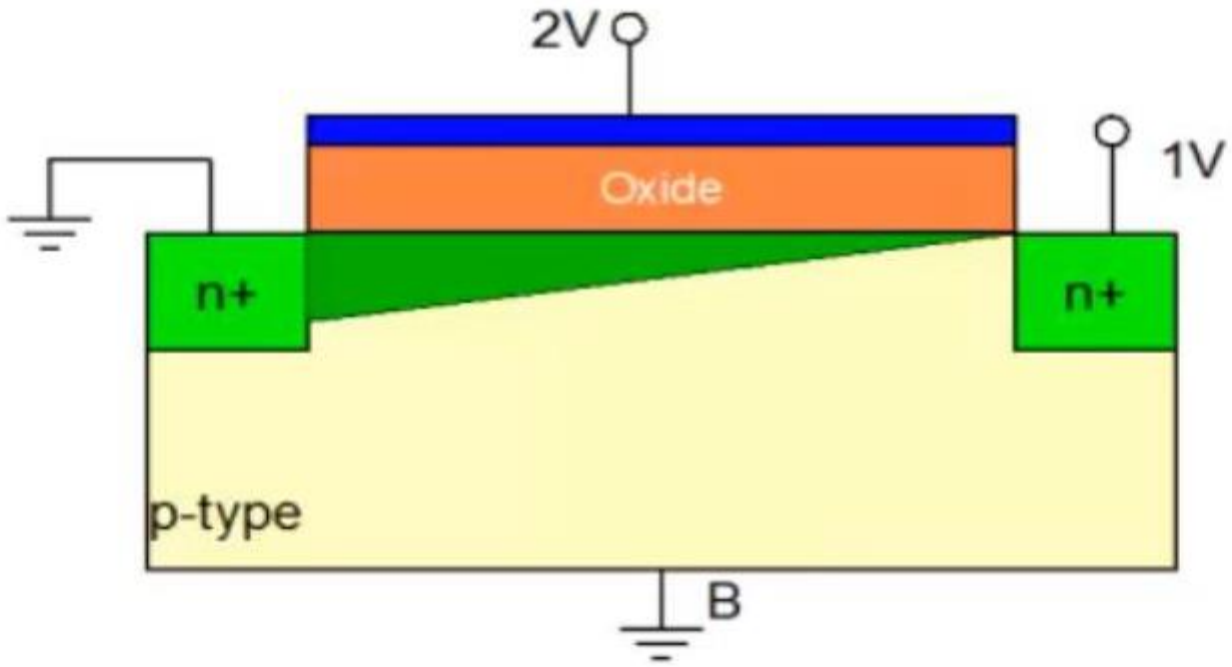
$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x)) \cong -C_{ox}(2-1-1) = 0$$

$$V_{THN} = 1V$$

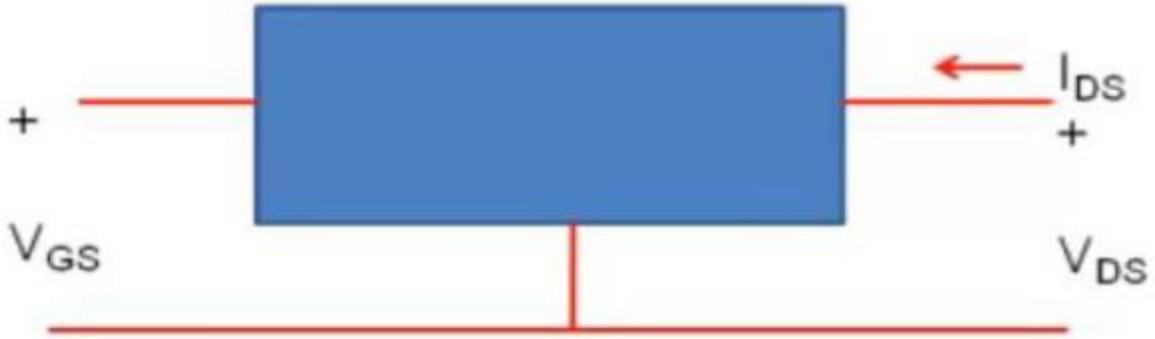


Any further increase in drain bias is absorbed in a small region next to the drain and rest of channel is not much affected and thus current becomes constant.


R
R
R
R
R
ΔV_D
R
100R
ΔV_D

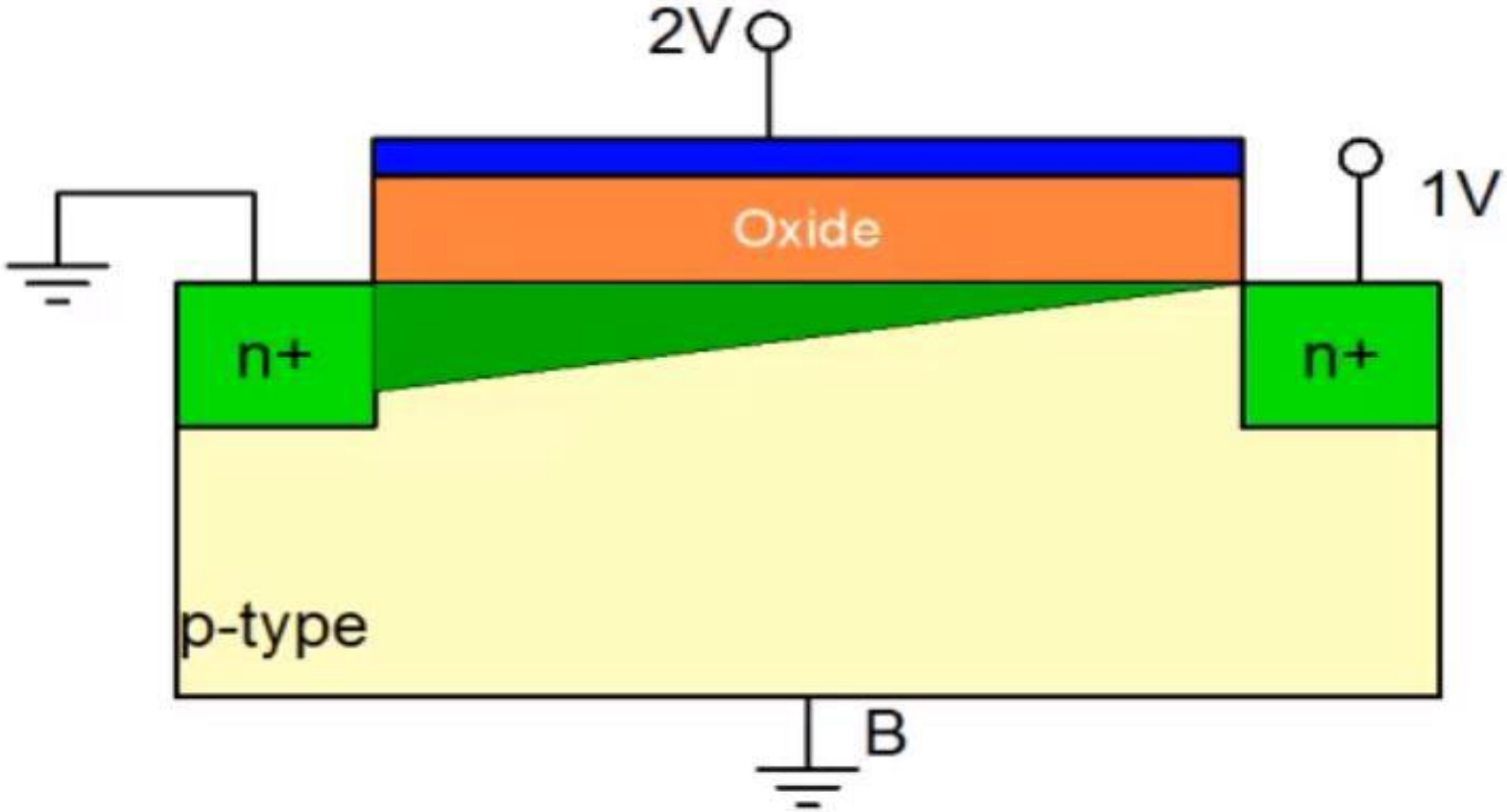


After pinchoff or saturation, drain current does not change much with drain voltage but is still very sensitive to gate voltage. MOSFET can now **AMPLIFY** signals



$$\frac{\partial I_{DS}}{\partial V_{GS}} >> \frac{\partial I_{DS}}{\partial V_{DS}}$$

The voltage at which pinchoff occurs is the drain-saturation voltage V_{DSAT}



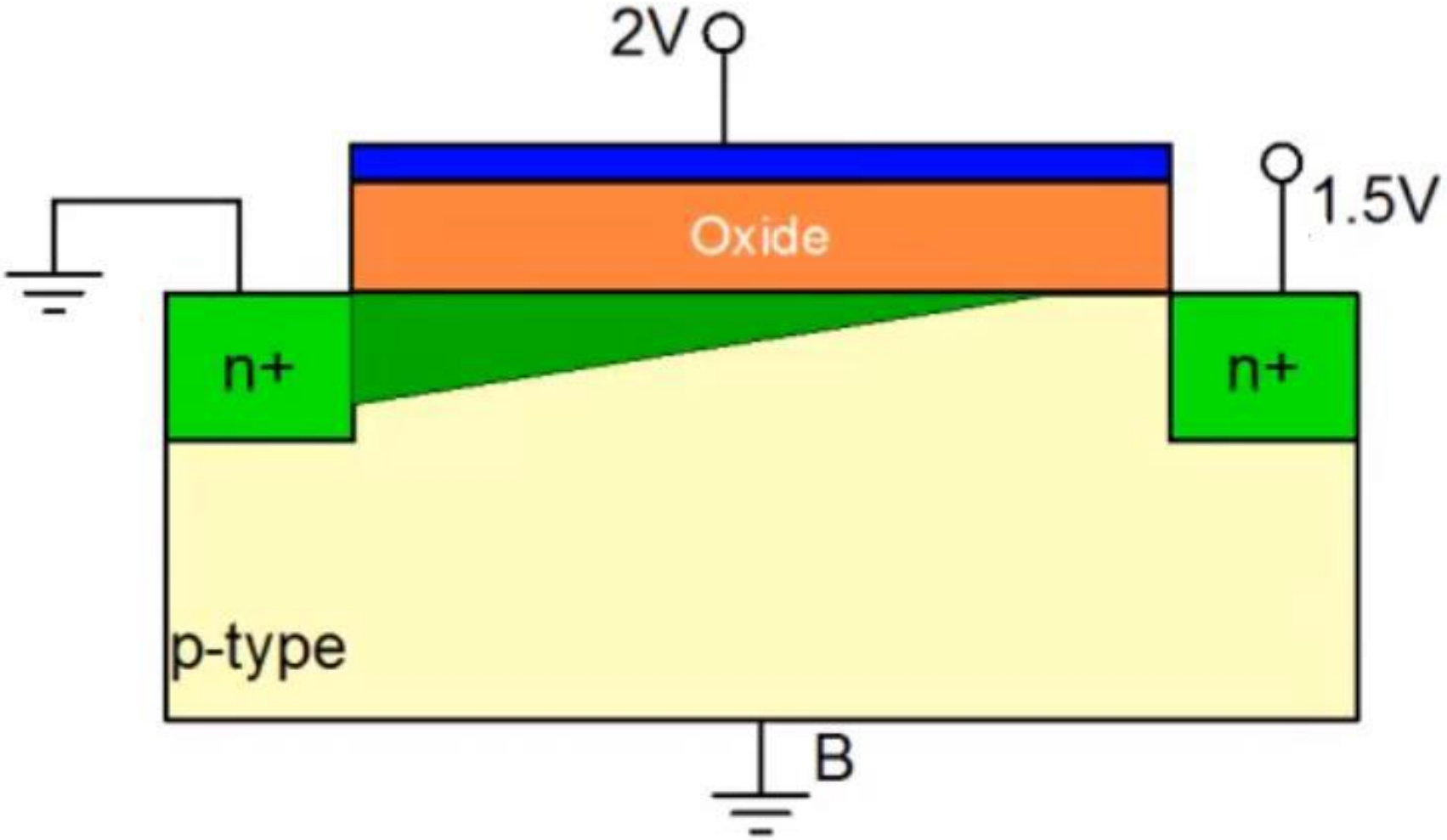
$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V_{DSAT}) \cong 0$$

$$V_{DSAT} = V_{GS} - V_{THN}$$

This is a very simple picture. In short channel MOSFETs especially, saturation is a more complicated phenomenon.,

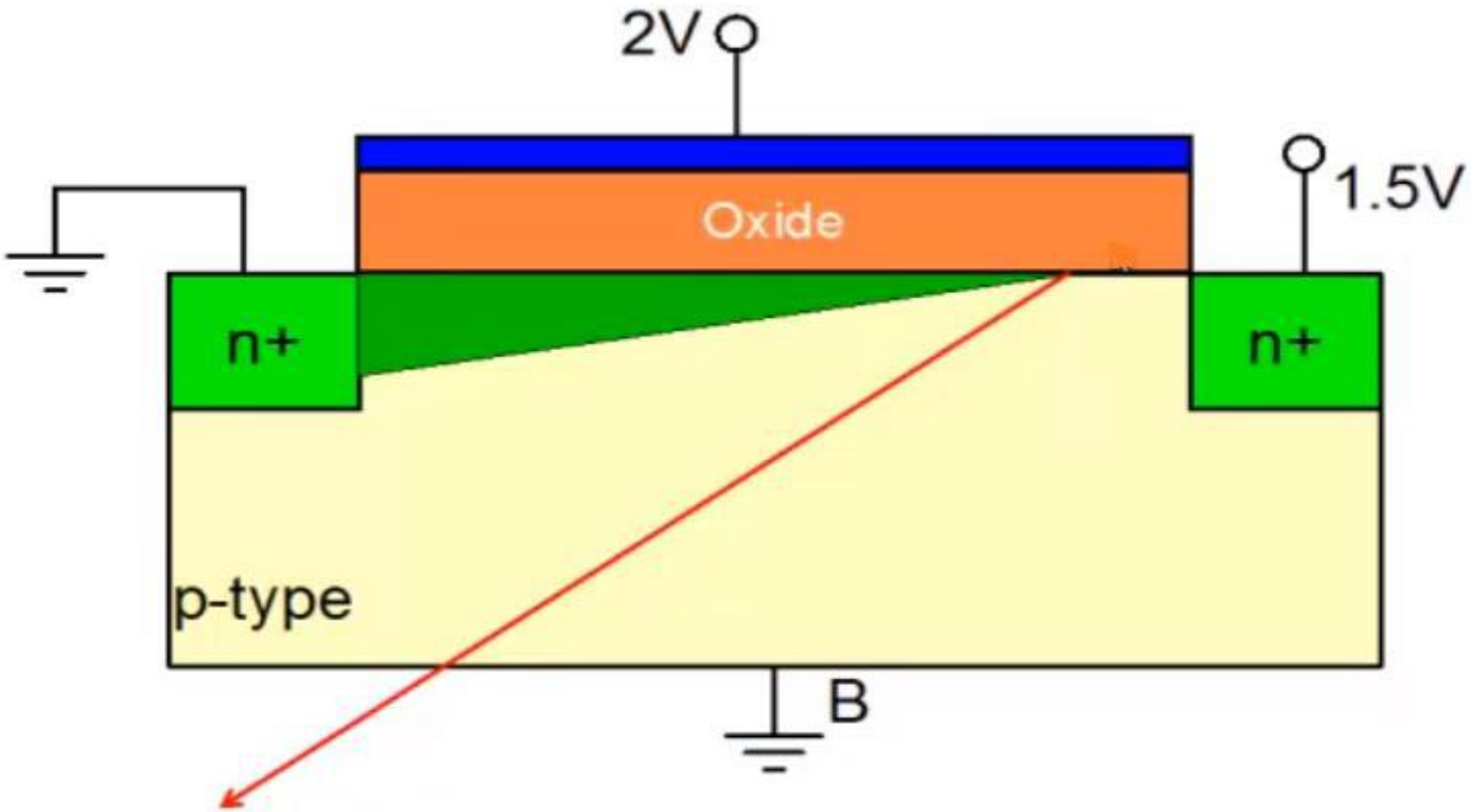
For voltages larger than saturation voltage

$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x)) \cong -C_{ox}(2-1-1) = 0$$



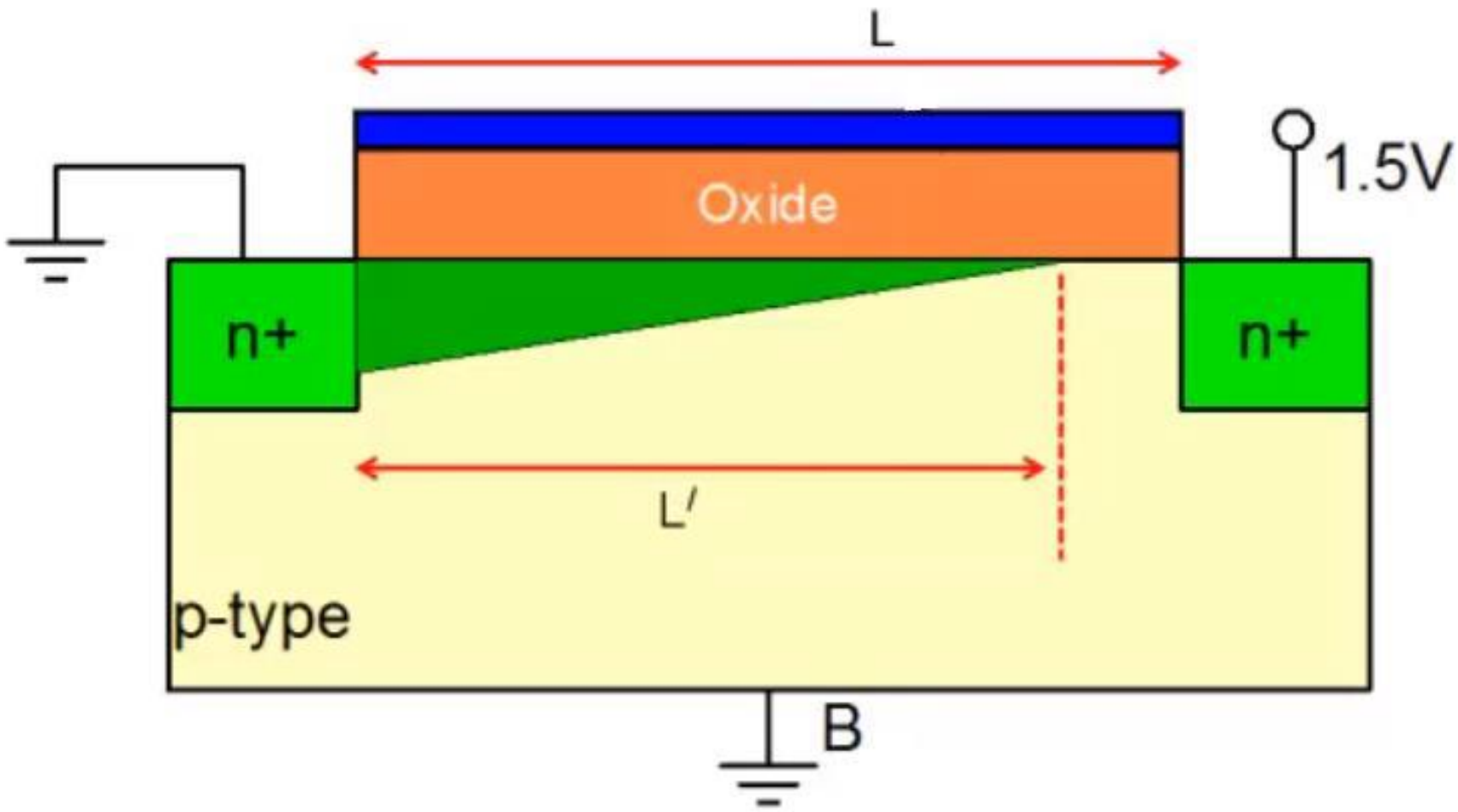
For voltages larger than saturation voltage

$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x)) \cong -C_{ox}(2-1-1) = 0$$

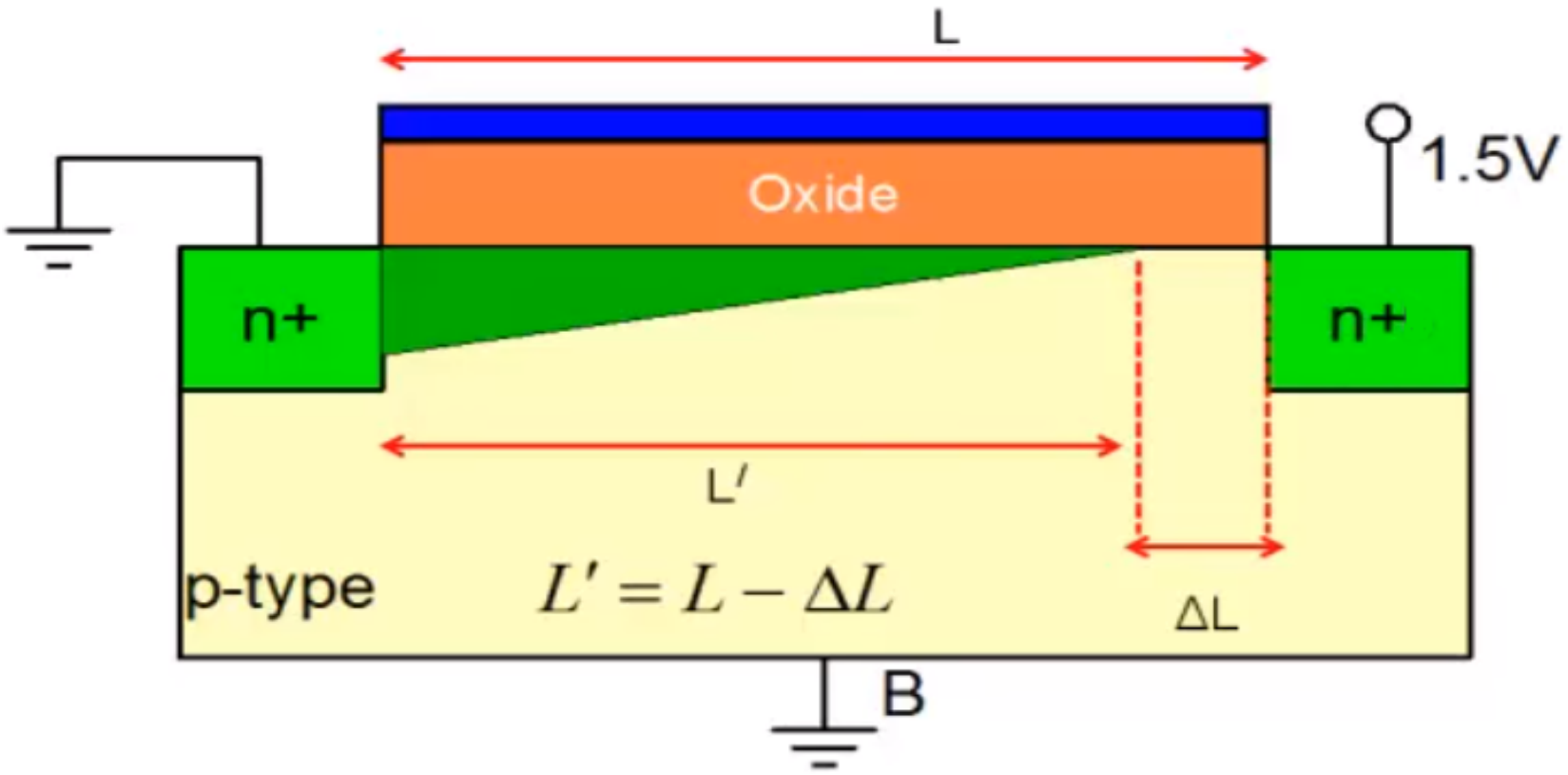


Pinchoff point moves left towards the source end. Voltage is V_{DSAT} = 1V

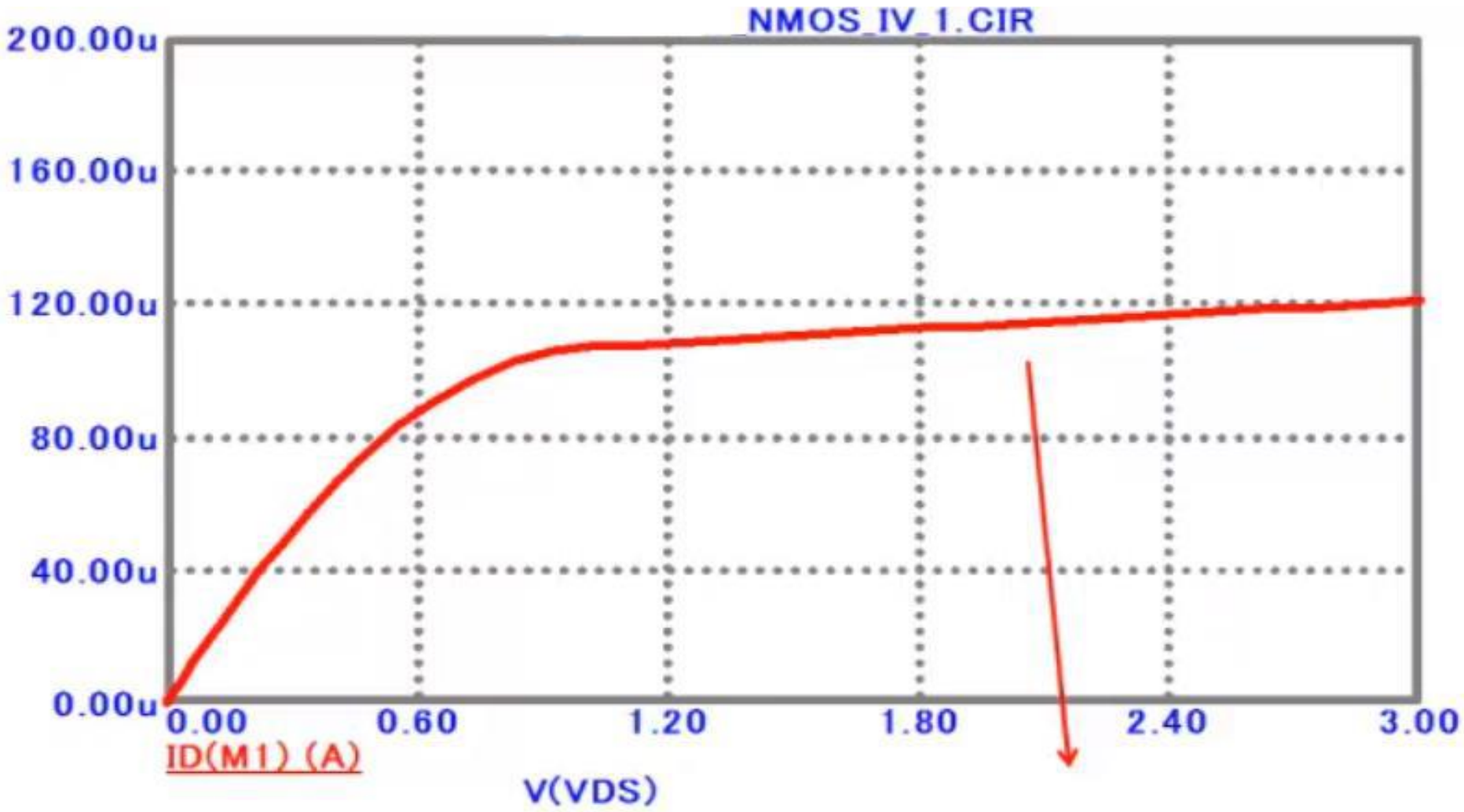
Channel Length Modulation



Channel Length Modulation

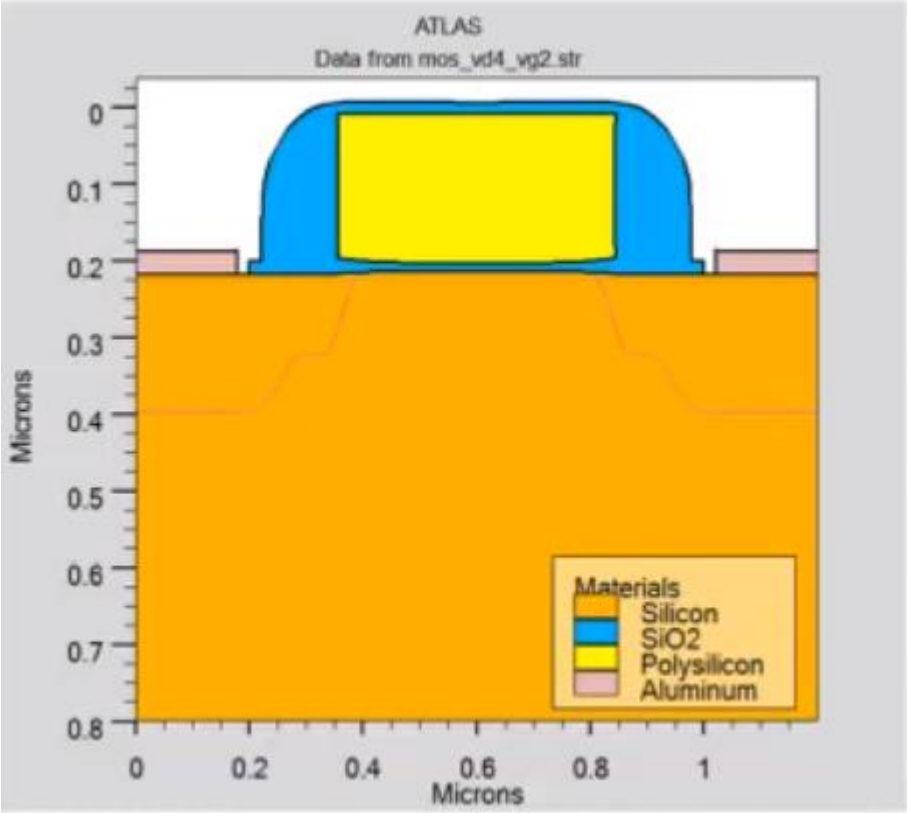


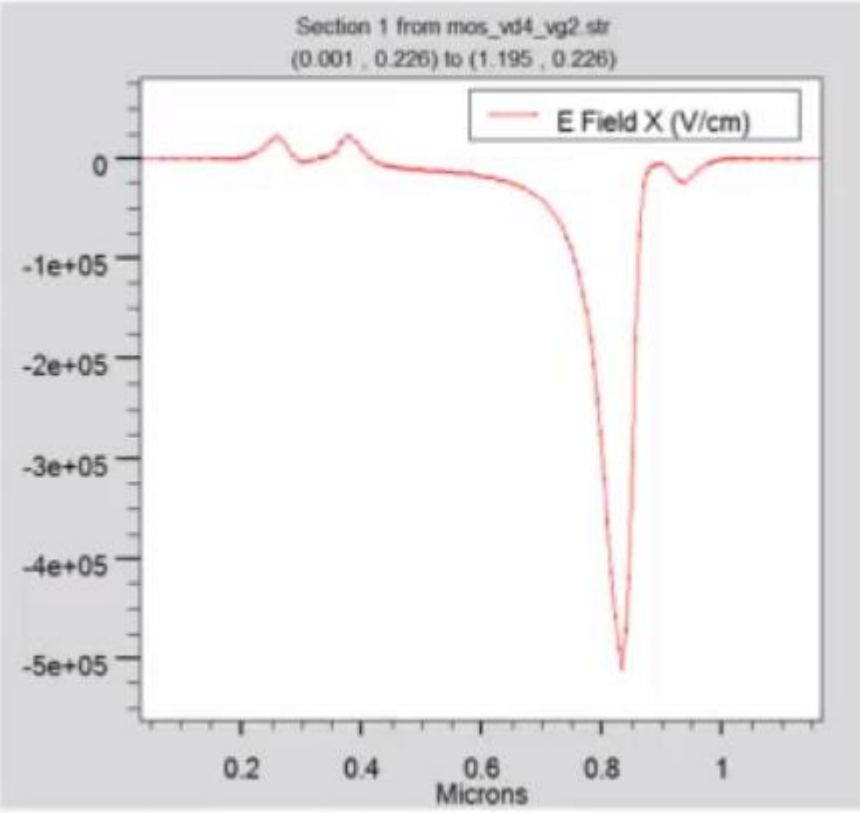
Effective channel length decreases as voltage increases beyond V_{DSAT}. As a result current increases a little with voltage



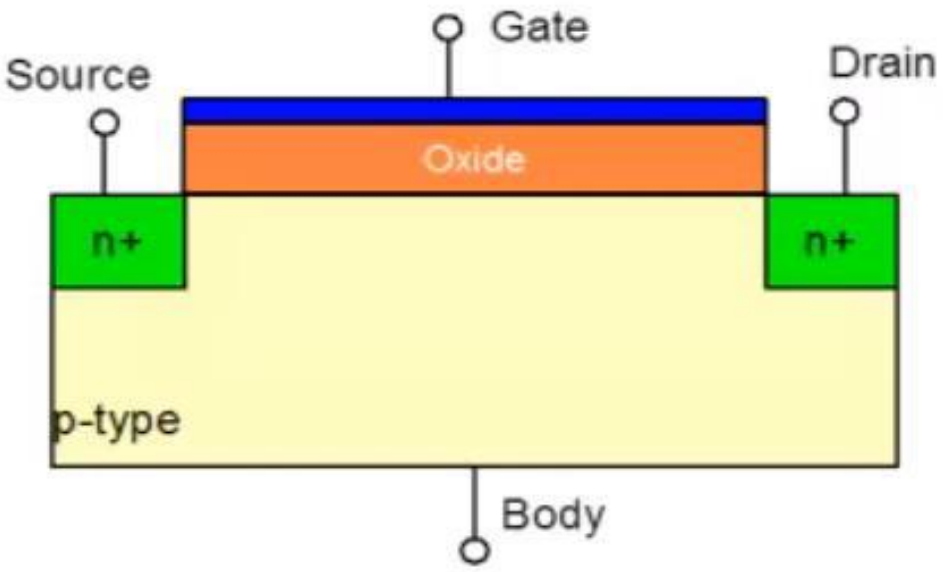
$$I_{DSAT} \times (1 + \lambda \times V_{DS})$$

λ: channel length modulation parameter


ATLAS
Data from mos_vd4_vg2.str
Microns
Microns
Materials
Silicon
SiO2
Polysilicon
Aluminum


Section 1 from mos_vd4_vg2.str
(0.001 , 0.226) to (1.195 , 0.226)
E Field X (V/cm)
Microns

Threshold Voltage



$$V_{THN} = V_{THN0} + \gamma(\sqrt{2\varphi_F + V_{SB}} - \sqrt{2\varphi_F})$$

$$V_{THNO} = 1V$$

$$\gamma = body\ parameter \quad Units : \sqrt{V}$$

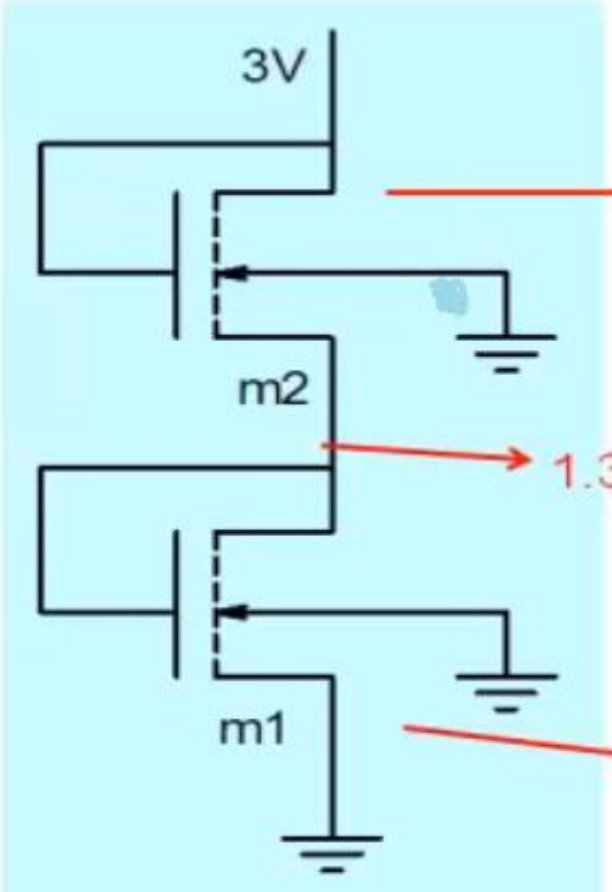
$$\gamma = 0.7\ V^{1/2}$$

Surface potential : $2\phi_F$

$$2\phi_F = 0.7V$$

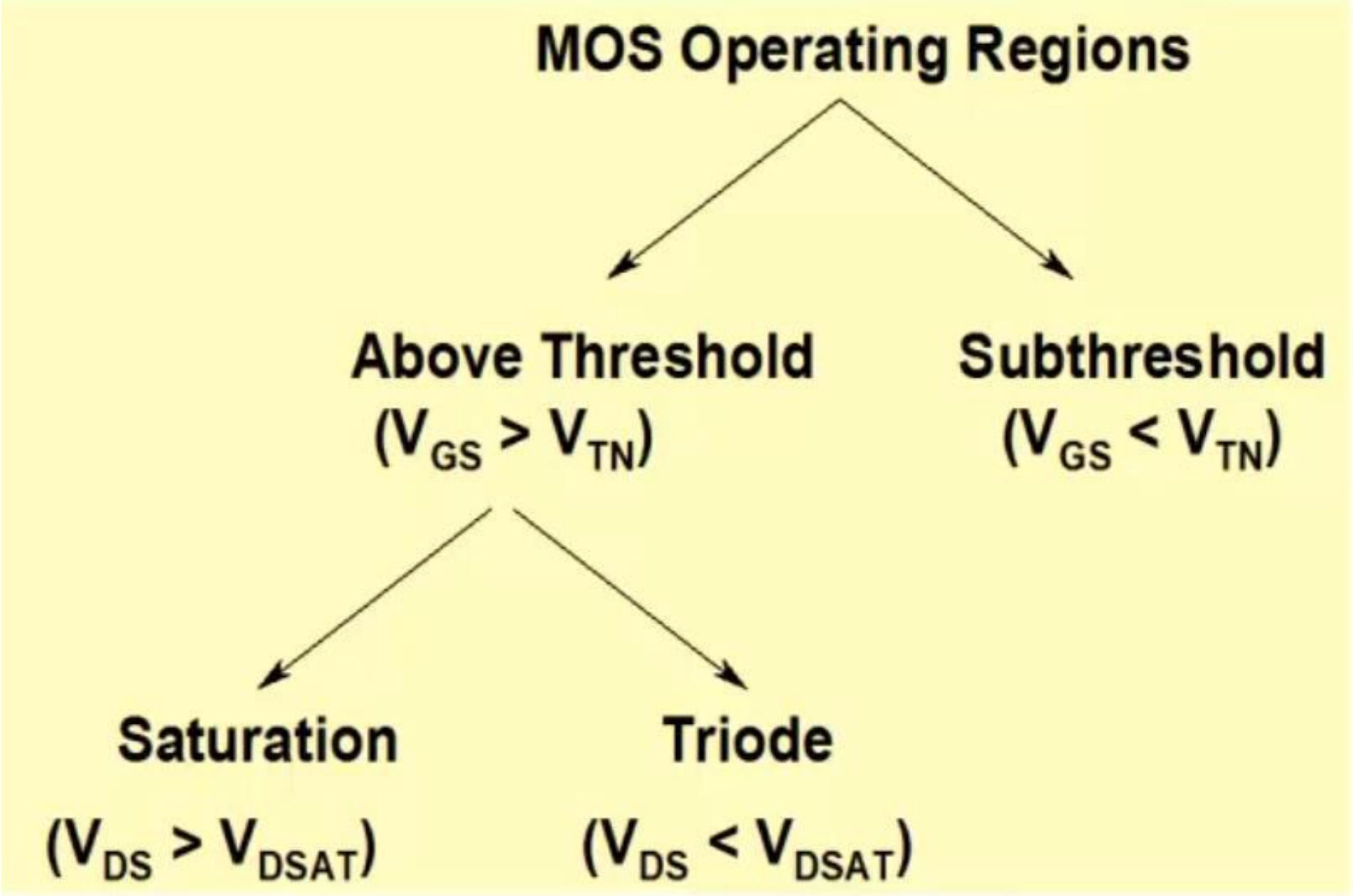
$$V_{THNO} = 1V; \gamma = 0.7\ V^{1/2}; 2\phi_F = 0.7V$$

$$V_{THN} = V_{THN0} + \gamma(\sqrt{2\varphi_F + V_{SB}} - \sqrt{2\varphi_F})$$

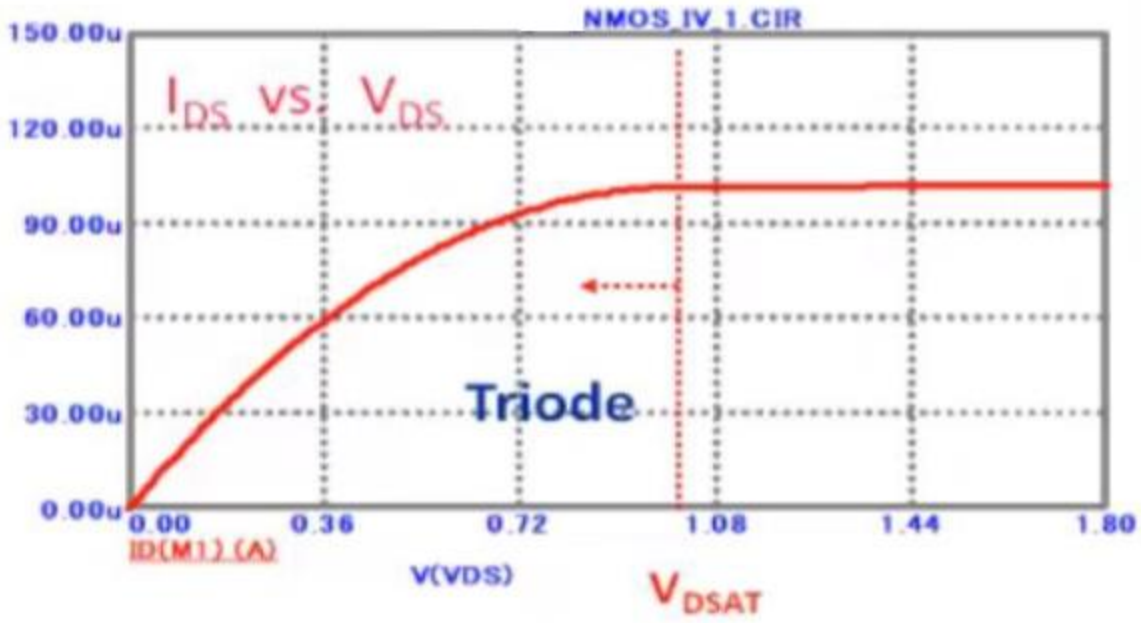


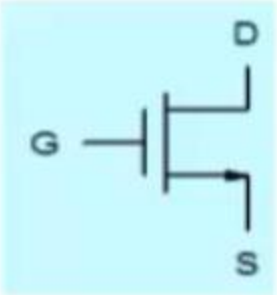
$$V_{SB2} = 1.3V; V_{THN2} = 1.4V$$

$$V_{THN1} = V_{THN0} = 1V$$


MOS Operating Regions
Above Threshold
($V_{GS} > V_{TN}$)
Subthreshold
($V_{GS} < V_{TN}$)
Saturation
($V_{DS} > V_{DSAT}$)
Triode
($V_{DS} < V_{DSAT}$)

dc Model: Triode (or Linear)





$$V_{GS} > V_{TN}$$

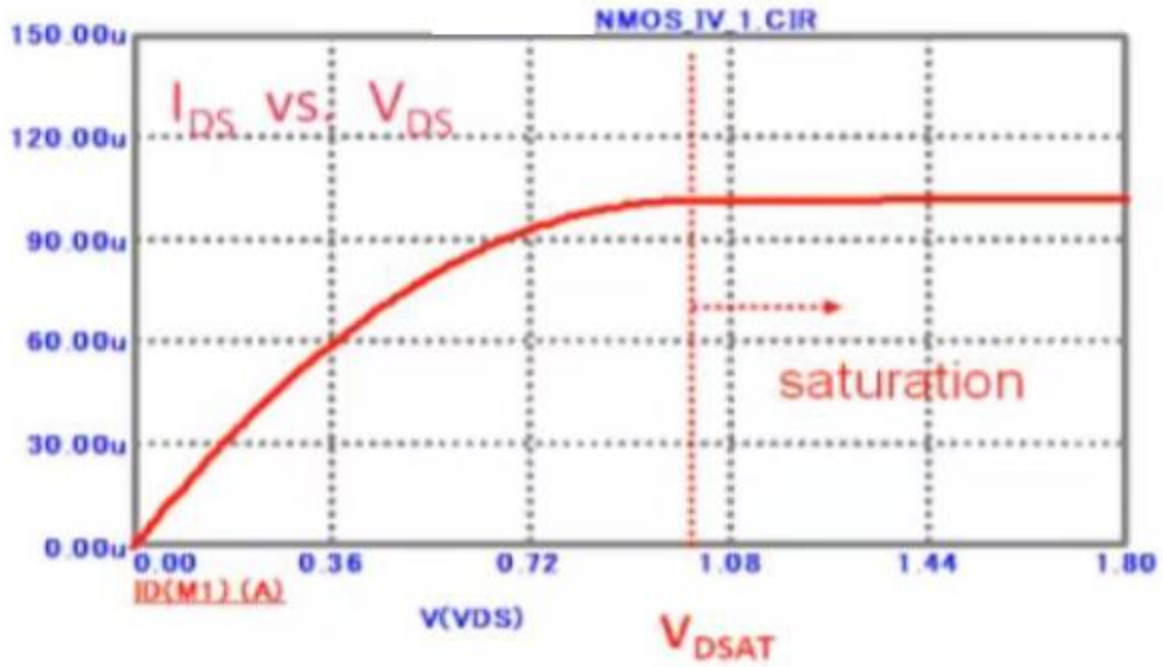
$$V_{DS} < V_{Dsat} = V_{GS} - V_{TN}$$

$$I_{DS} = \beta_N \left\{ (V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right\}$$

$$\beta_N = kP_N . \frac{W}{L}$$

$$kP_N = \mu_n C_{ox'} \ : (TransConductance\ parameter\ \frac{\mu A}{V^2})$$

DC Model: Saturation Region



$$V_{GS} > V_{THN}$$

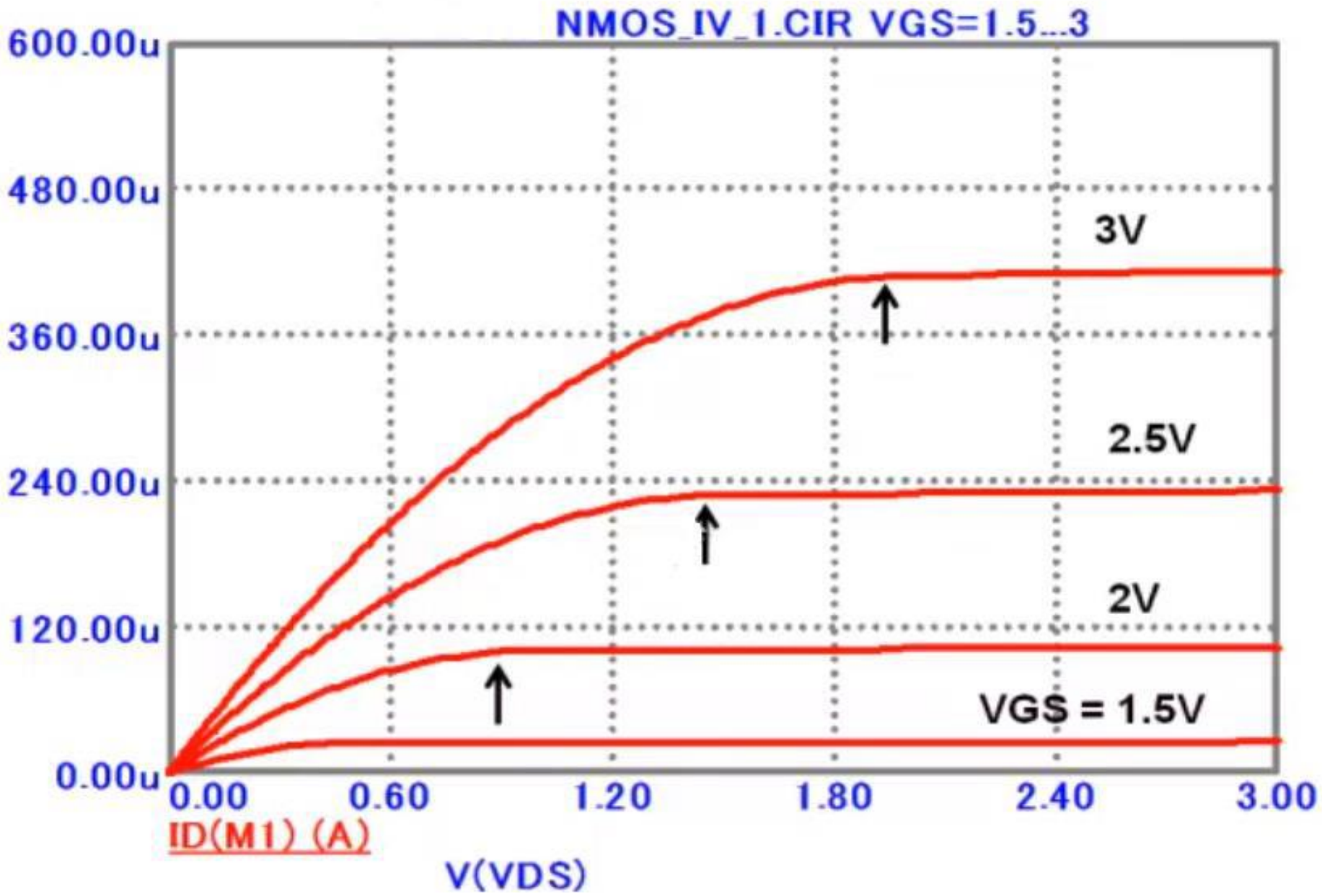
$$V_{DS} \geq V_{GS} - V_{THN}$$

$$I_{DS} = \frac{\beta_N}{2}(V_{GS} - V_{THN})^2[1 + \lambda_n V_{DS}]$$

λ_N is the channel length modulation parameter

Note that unlike BJT, VDSAT is not only larger but also dependent on applied gate-source voltage

Output Characteristics of MOSFET



dc model parameters

$$\text{Linear}: \; I_{DS} = \beta_N \left\{ (V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^{\;2}}{2} \right\}$$

$$\text{Saturation}: \; I_{DS} = \frac{\beta_N}{2} (V_{GS} - V_{THN})^2 [1 + \lambda_n V_{DS}]$$

$$\beta_N = kP_N \cdot \frac{W}{L}$$

$$\lambda_N$$

$$V_{THN} = V_{THN0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$

$$V_{THNO} = 1V; \gamma = 0.7\, V^{1/2}; 2\phi_F = 0.7V;$$

$$KP_N = 100\mu A / V^2; L = 1\mu m; \lambda = 0.01V^{-1}$$

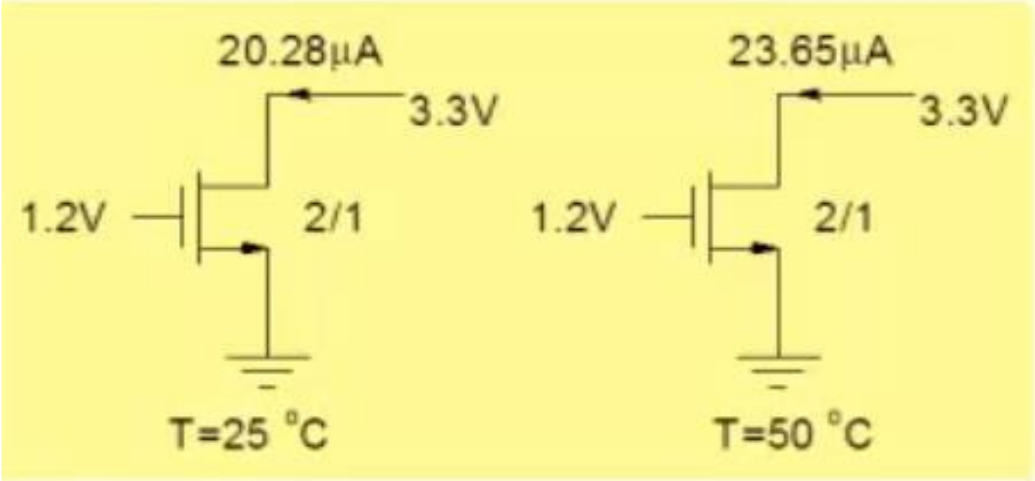
L is usually fixed, W is determined by designer

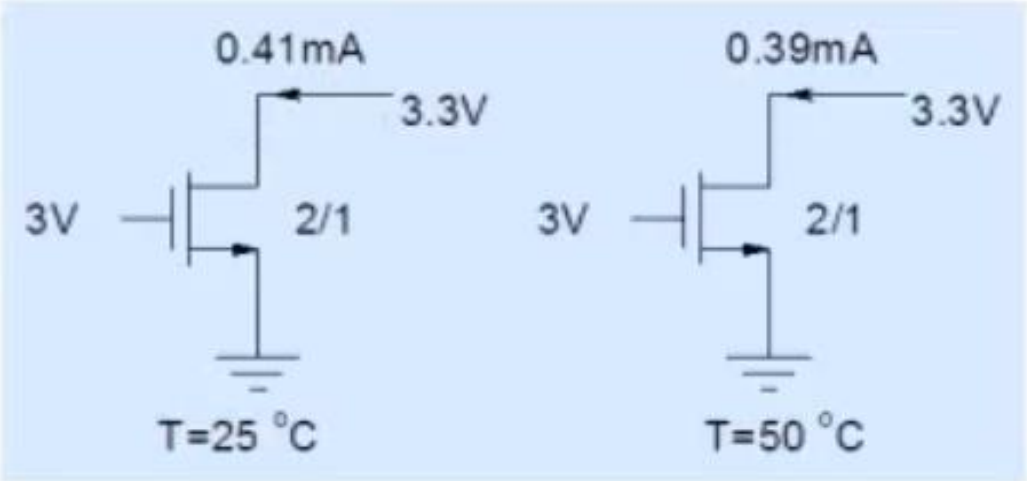
Temperature dependence

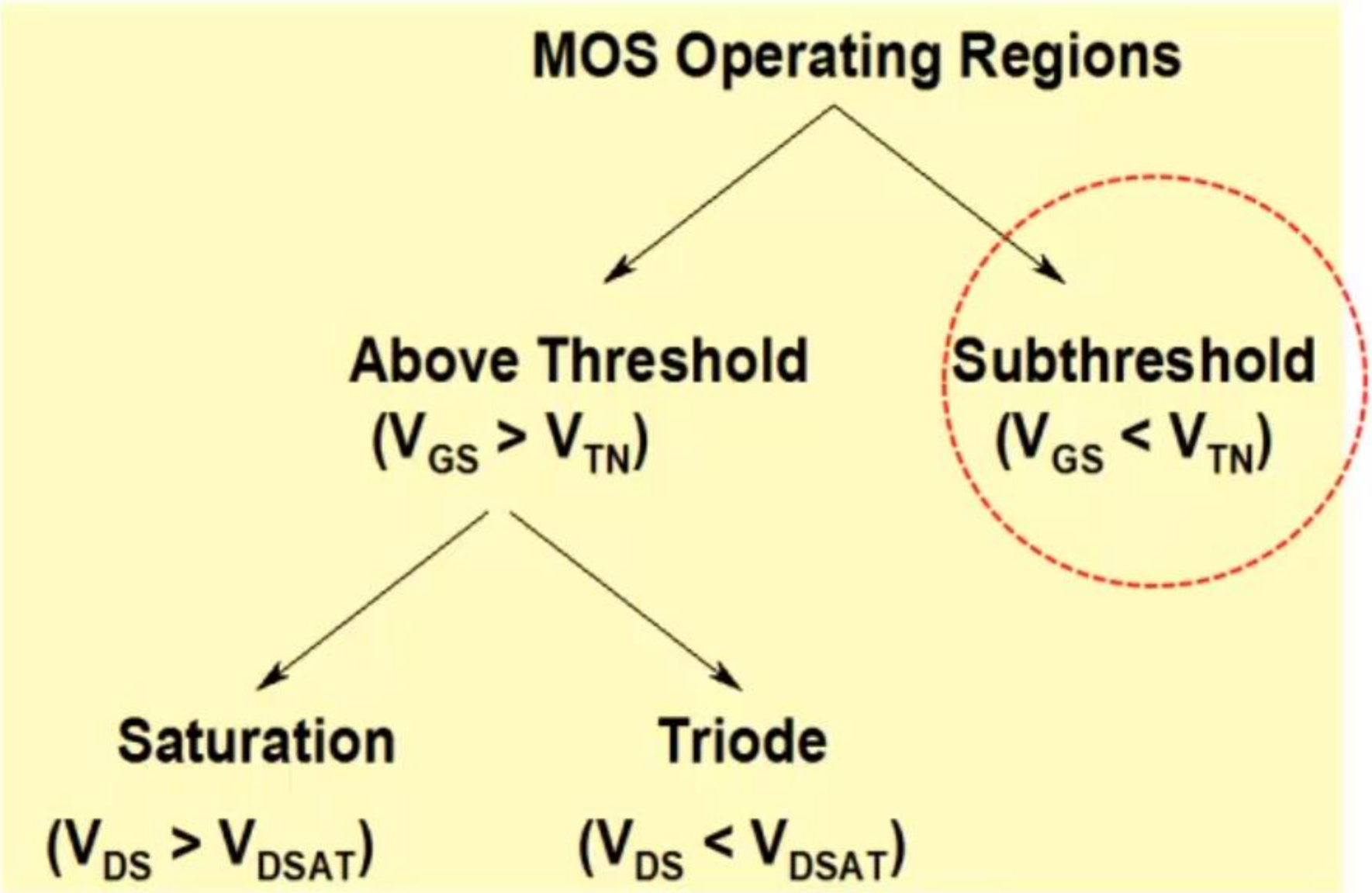
$$I_{DS} = \frac{KP_N}{2} \times \frac{W}{L} \times (V_{GS} - V_{THN})^2$$

Increase in temperature causes both transconductance parameter KP_N and threshold voltage V_{THN} to decrease

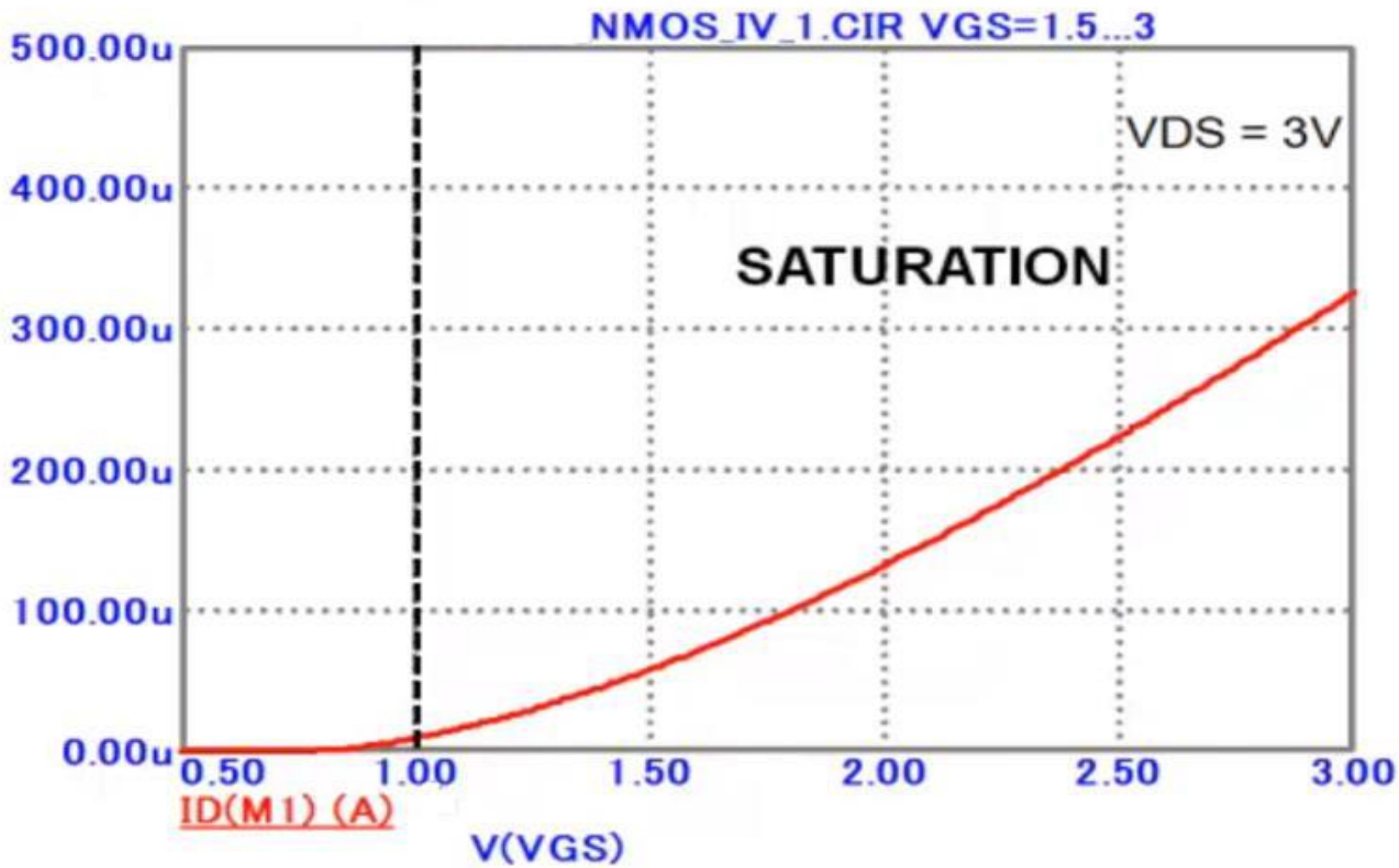
Although both K_{PN} and V_{THN} and decrease with temperature, the former causes a decrease in current while the latter causes an increase in current.m



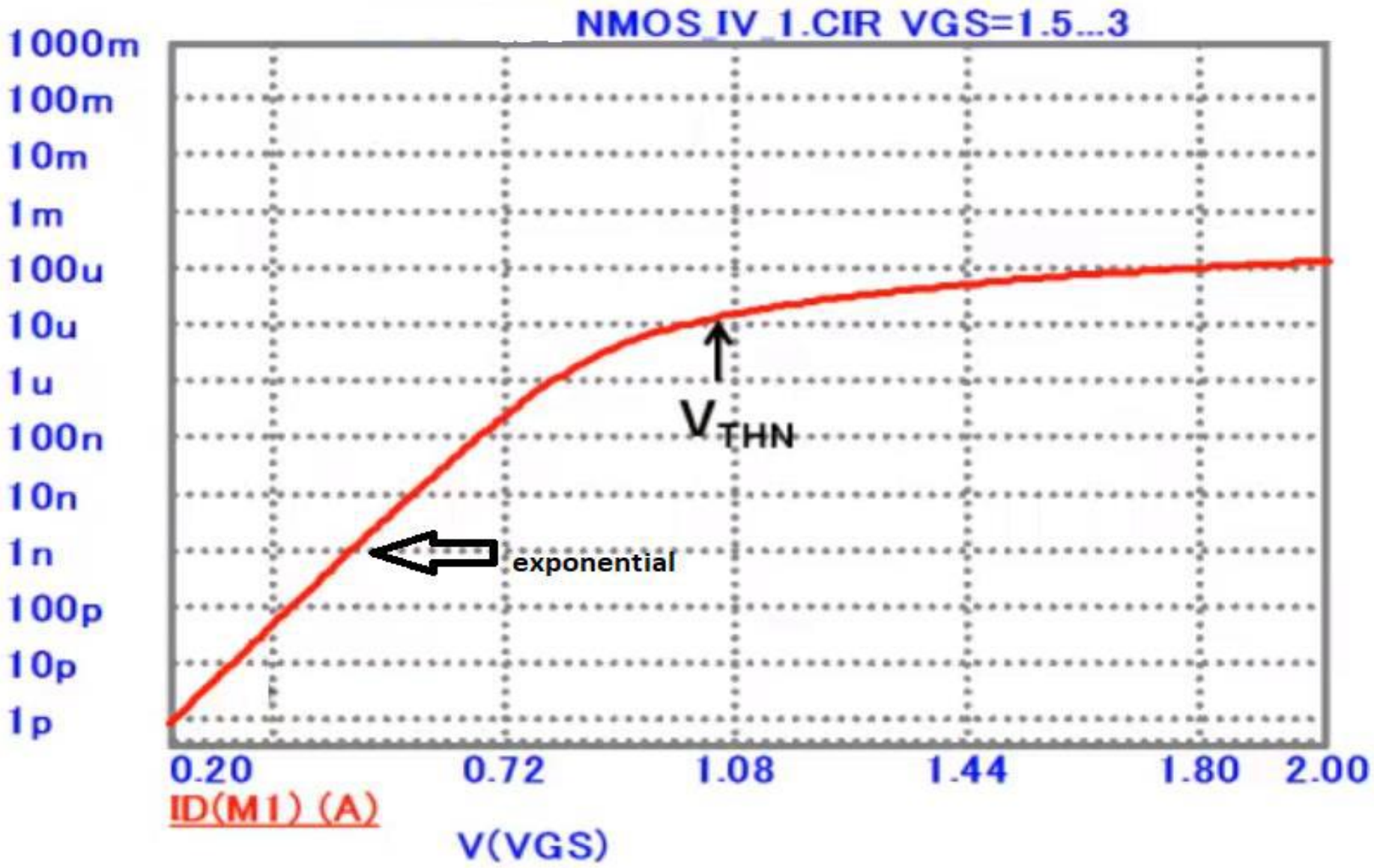



MOS Operating Regions
Above Threshold
($V_{GS} > V_{TN}$)
Subthreshold
($V_{GS} < V_{TN}$)
Saturation
($V_{DS} > V_{DSAT}$)
Triode
($V_{DS} < V_{DSAT}$)

Transfer characteristics of NMOS



Current is very small until gate-source voltage **exceeds threshold voltage** V_{THN}



-Logscale
-Ignoring leakages

$$I_D \propto e^{\frac{qV_{GS}}{N'kT}}$$

$$g_m = \frac{\partial I_{DS}}{\partial Vgs} = \frac{I_{DS}}{nV_T}$$

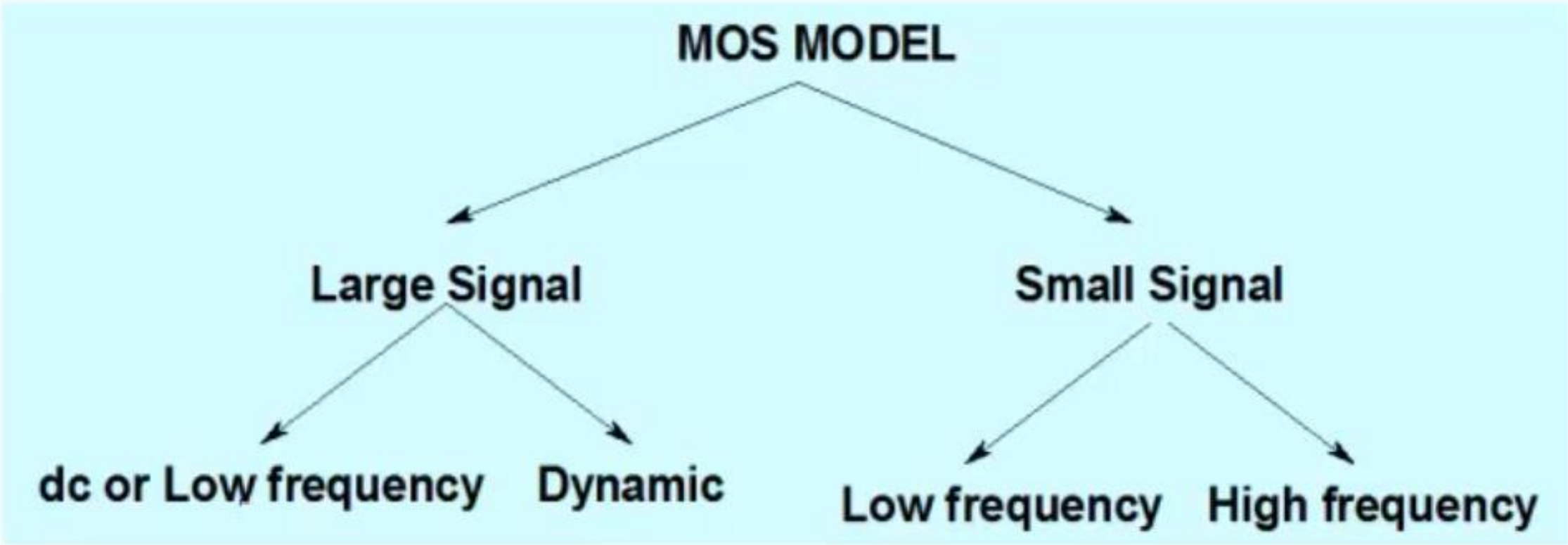
- In subthreshold region, MOS acts like a BJT

$$BJT: \qquad I_C = I_S e^{V_{BE}/V_T}$$

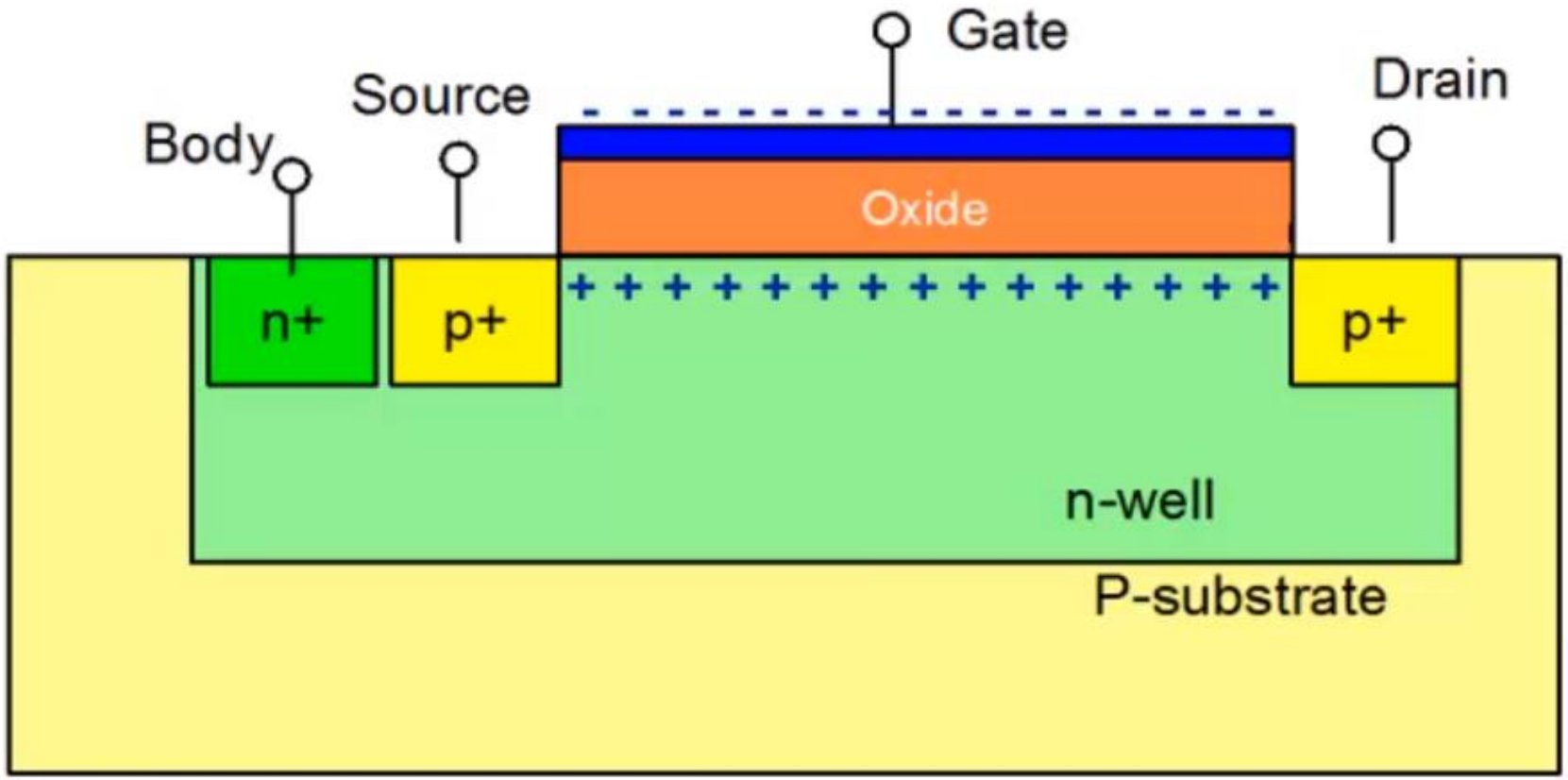
$$MOS: \quad I_{DS} = I_S e^{V_{GS}/\eta V_T}$$

- The advantage of MOS is that it offers almost infinite input impedance. Its disadvantage is that current levels are low.

MOS models : The classification of models can be done on the basis of magnitude and frequency of applied voltages

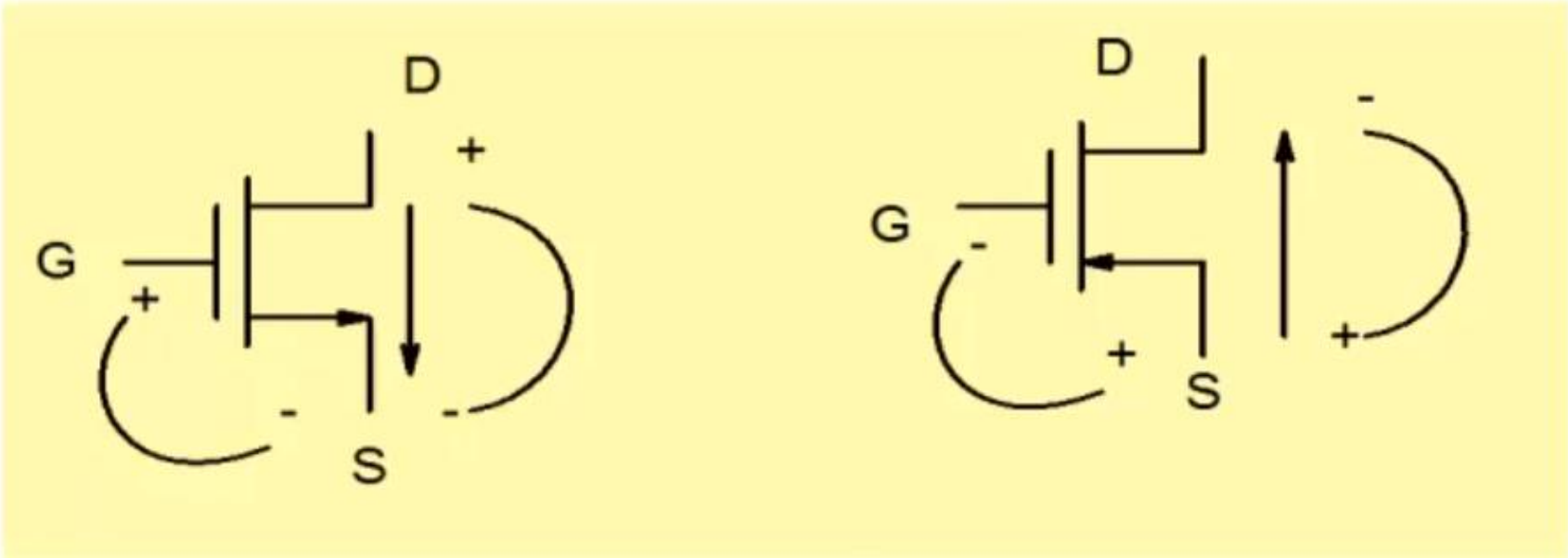


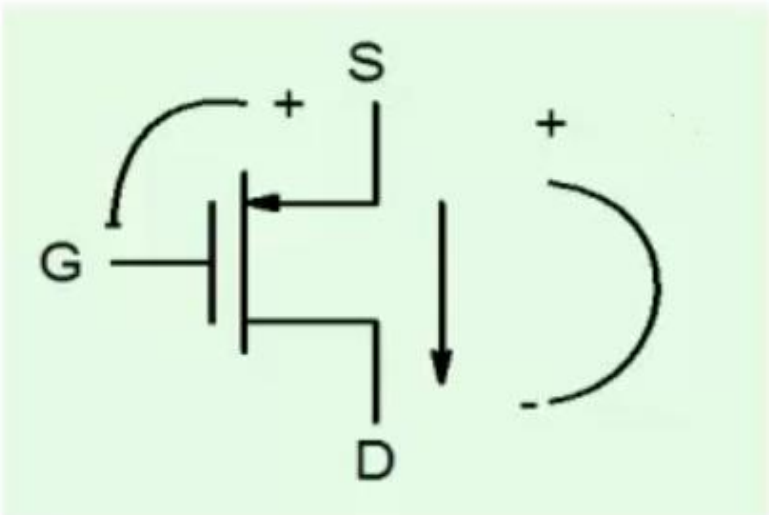
PMOS



V_{GS} is negative ; Threshold voltage V_{TP} is negative

V_{DS} is negative ; I_{DS} is negative





$$V_{GSN} \rightarrow V_{SGP}$$

$$I_{DSN} \rightarrow I_{SDP}$$

$$V_{DSN} \rightarrow V_{SDP}$$

Transformations

$$V_{GSN} \rightarrow V_{SGP} \qquad V_{DSN} \rightarrow V_{SDP} \qquad V_{BSN} \rightarrow V_{SBP}$$

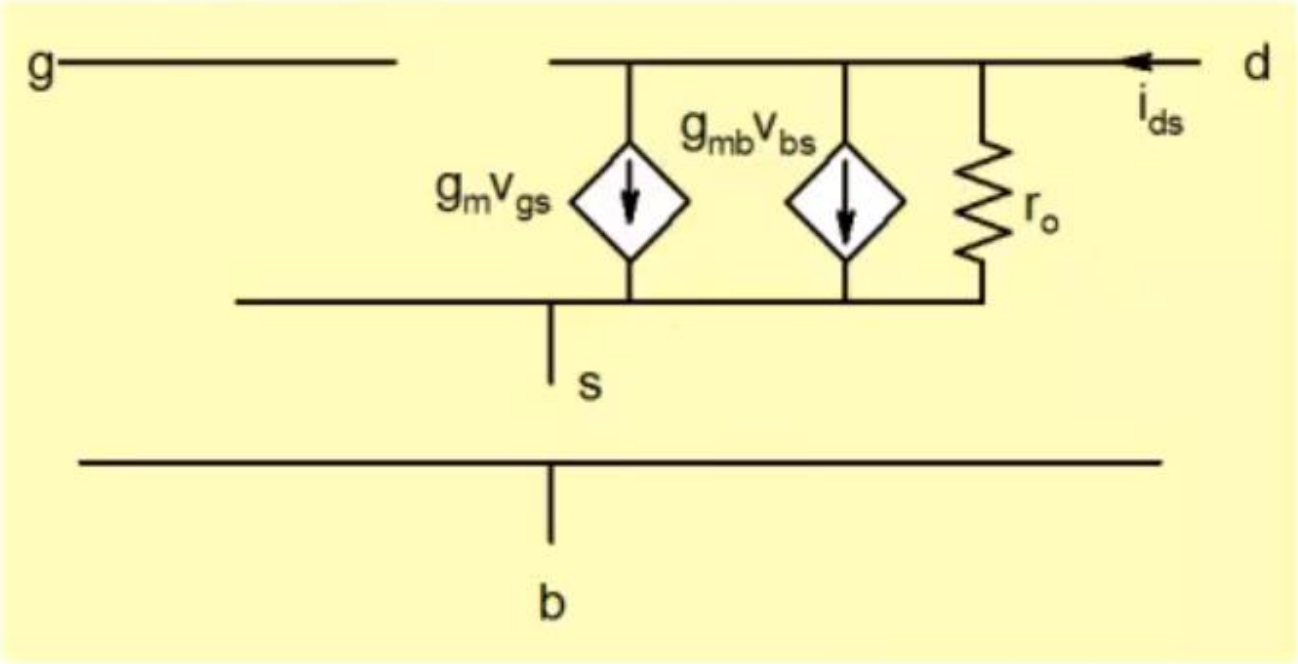
$$V_{THN} \rightarrow -V_{THP} \qquad I_{DSN} \rightarrow I_{SDP}$$

$$I_{DS} = \frac{\beta_N}{2}(V_{GS} - V_{THN})^2[1 + \lambda_n V_{DS}] \rightarrow$$

$$I_{SD} = \frac{\beta_P}{2}(V_{SG} + V_{THP})^2[1 + \lambda_p V_{SD}]$$

$$i_{sd} = g_m v_{sg} + g_{mb} v_{sb} + \frac{v_{sd}}{r_o} \qquad i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + \frac{v_{ds}}{r_o}$$ same as NMOS

Small Signal Model

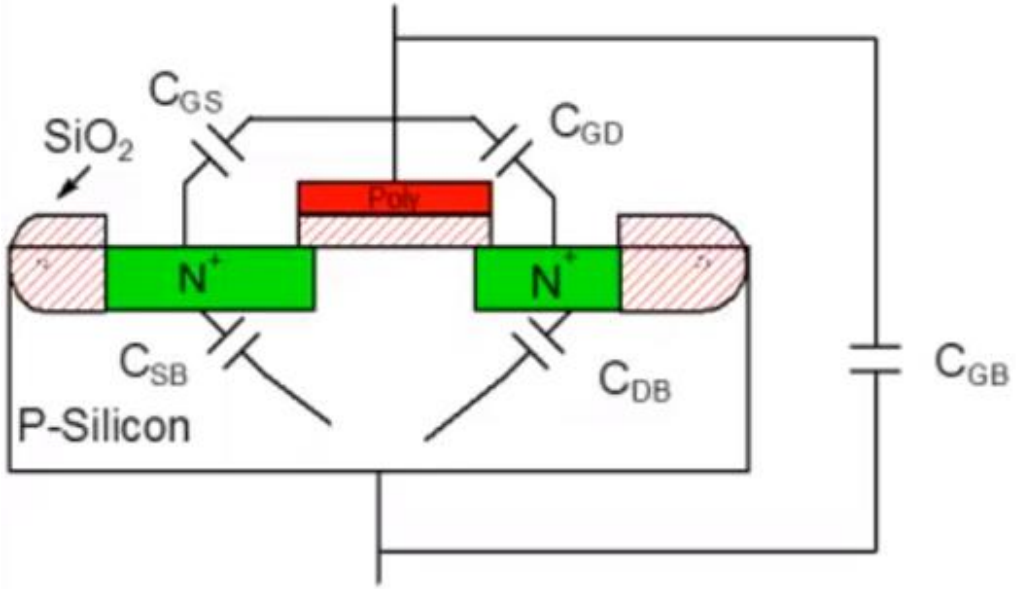


$$g_m = \frac{2I_{SDQ}}{V_{SGQ} + V_{THP}}$$

$$r_o = \frac{1}{\lambda_p I_{SDQ}}$$

Capacitance Model Saturation

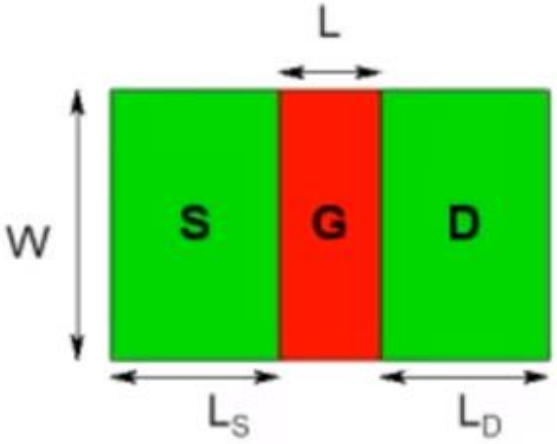
- There are five distinct components of capacitance as illustrated below



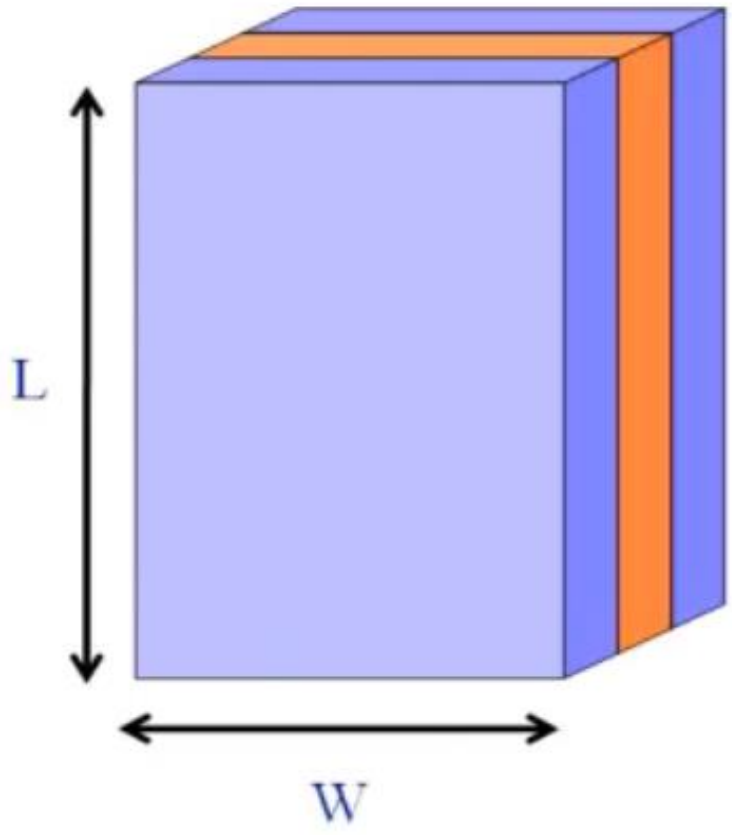
$$C_{gs} \cong \frac{2}{3} C_{ox'}.W.L + C_{gso}.W$$

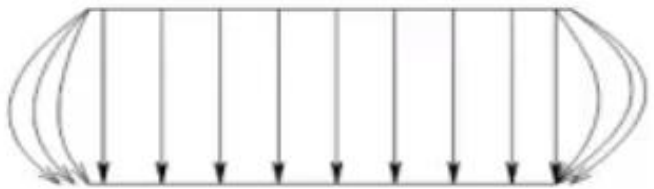
(Channel) (overlap)

$$C_{gd} = C_{GDO}.W$$

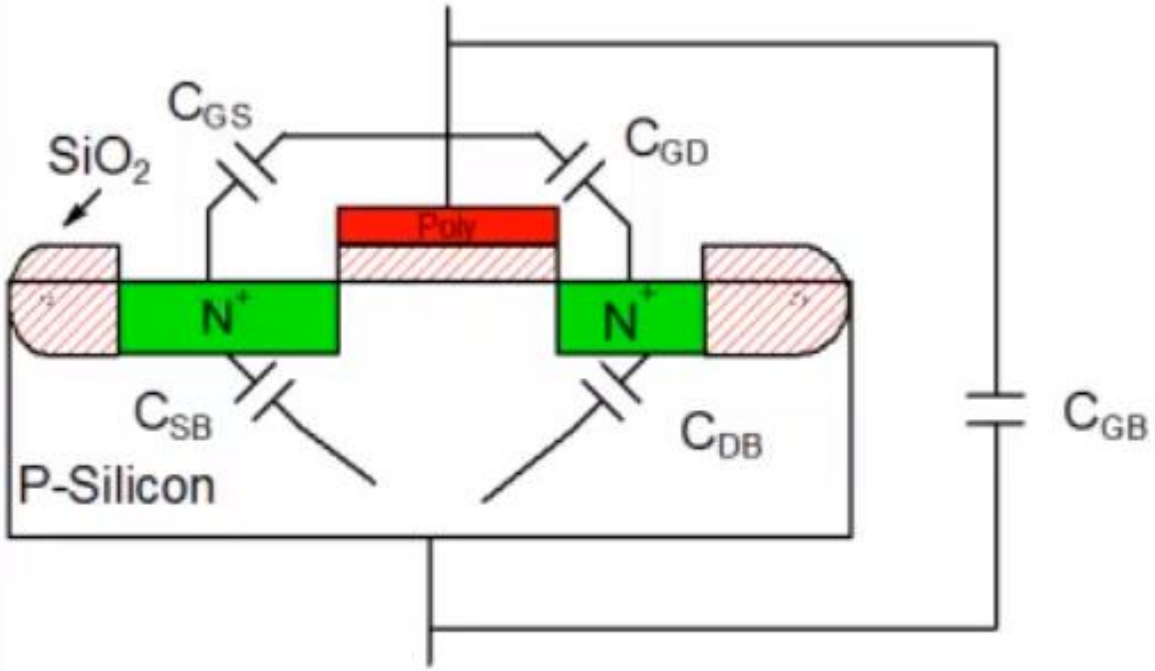


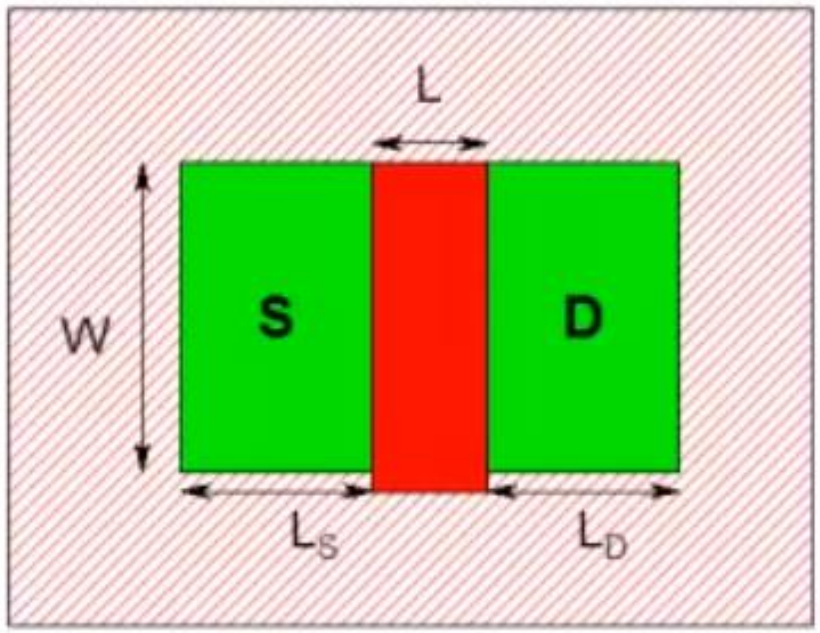
Capacitances: Area and Perimeter Components





$$C = \frac{\varepsilon}{d} \times W \times L + C_p \times (2L + 2W)$$

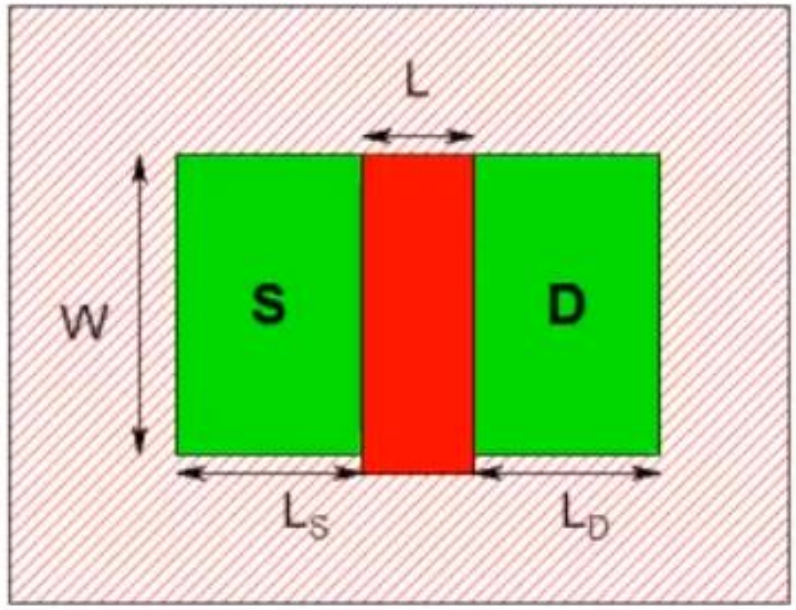




$$C_{sb} = \frac{C_j . A_s}{\left(1 + \frac{V_{SB}}{P_B}\right)^{M_j}} + \frac{C_{jsw} . P_S}{\left(1 + \frac{V_{SB}}{P_{BSW}}\right)^{M_{jsw}}}, \quad P_S = 2L_S + W \quad , \quad A_s = W . L_S$$

$$C_{db} = \frac{C_{jsw}.P_D}{\left(1+\frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}} + \frac{C_j.A_D}{\left(1+\frac{V_{DB}}{P_B}\right)^{M_j}} \qquad P_D = 2L_D + W$$

$$C_{gb} = C_{GBO}.L \sim \text{often negligible}$$



Triode/Linear Region

$$C_{gs} = \frac{1}{2} C_{ox'}.W.L + C_{GSO}.W$$

$$C_{gd} = \frac{1}{2} C_{ox'}.W.L + C_{GDO}.W$$

$$C_{sb} = same\,as\,before$$

$$C_{db} = same\,as\,before$$

$$C_{gb} = same\,as\,before$$

Assuming $V_{DS} \sim 0$

Cutoff Region

$$C_{gs} = C_{GSO}.W$$

$$C_{gd} = C_{GDO}.W$$

$$C_{sb} = same\,as\,before$$

$$C_{db} = same\,as\,before$$

$$C_{gb} = C_{GBO}.L + C_{ox'}.W.L$$

Assuming Tr. is in accumulation

Summary

$$C_{gs} \cong \frac{2}{3} C_{ox'}.W.L + C_{gso}.W \qquad C_{gd} = C_{GDO}.W$$

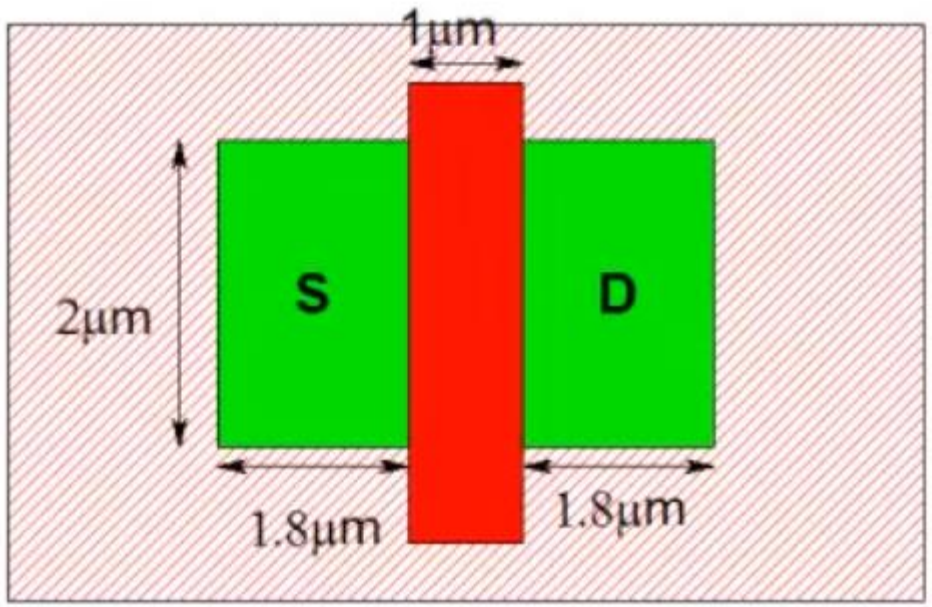
$$C_{sb} = \frac{C_j.A_s}{\left(1+\frac{V_{SB}}{P_B}\right)^{M_j}} + \frac{C_{jsw}.P_S}{\left(1+\frac{V_{SB}}{P_{BSW}}\right)^{M_{jsw}}}, \quad P_S = 2L_S + W \quad , \quad A_s = W.L_S$$

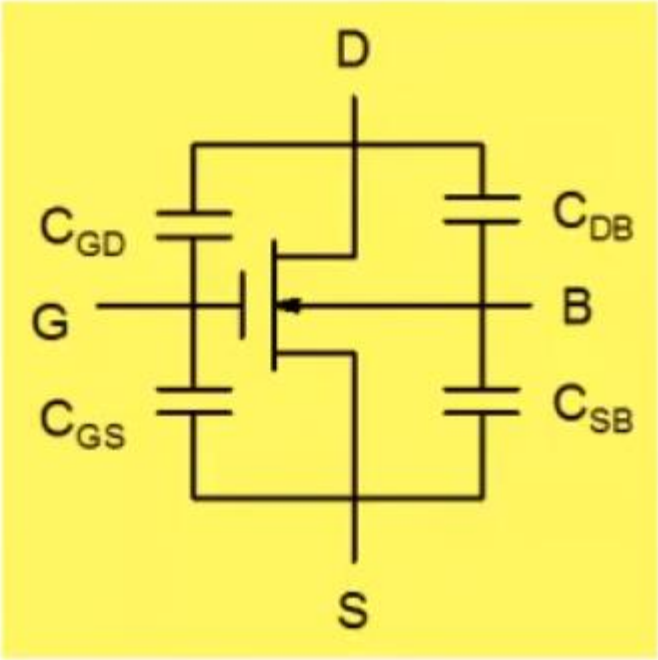
$$C_{db} = \frac{C_{jsw}.P_D}{\left(1+\frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}} + \frac{C_j.A_D}{\left(1+\frac{V_{DB}}{P_B}\right)^{M_j}} \quad P_D = 2L_D + W$$

The capacitance model presented herein requires 10 parameters:

$$C_{GSO}, C_{GDO}, C_{GBO}, C'_{OX}, C_J, PB, M_J, C_{JSW}, P_{BSW}, M_{JSW}$$

Typical Values of Capacitances





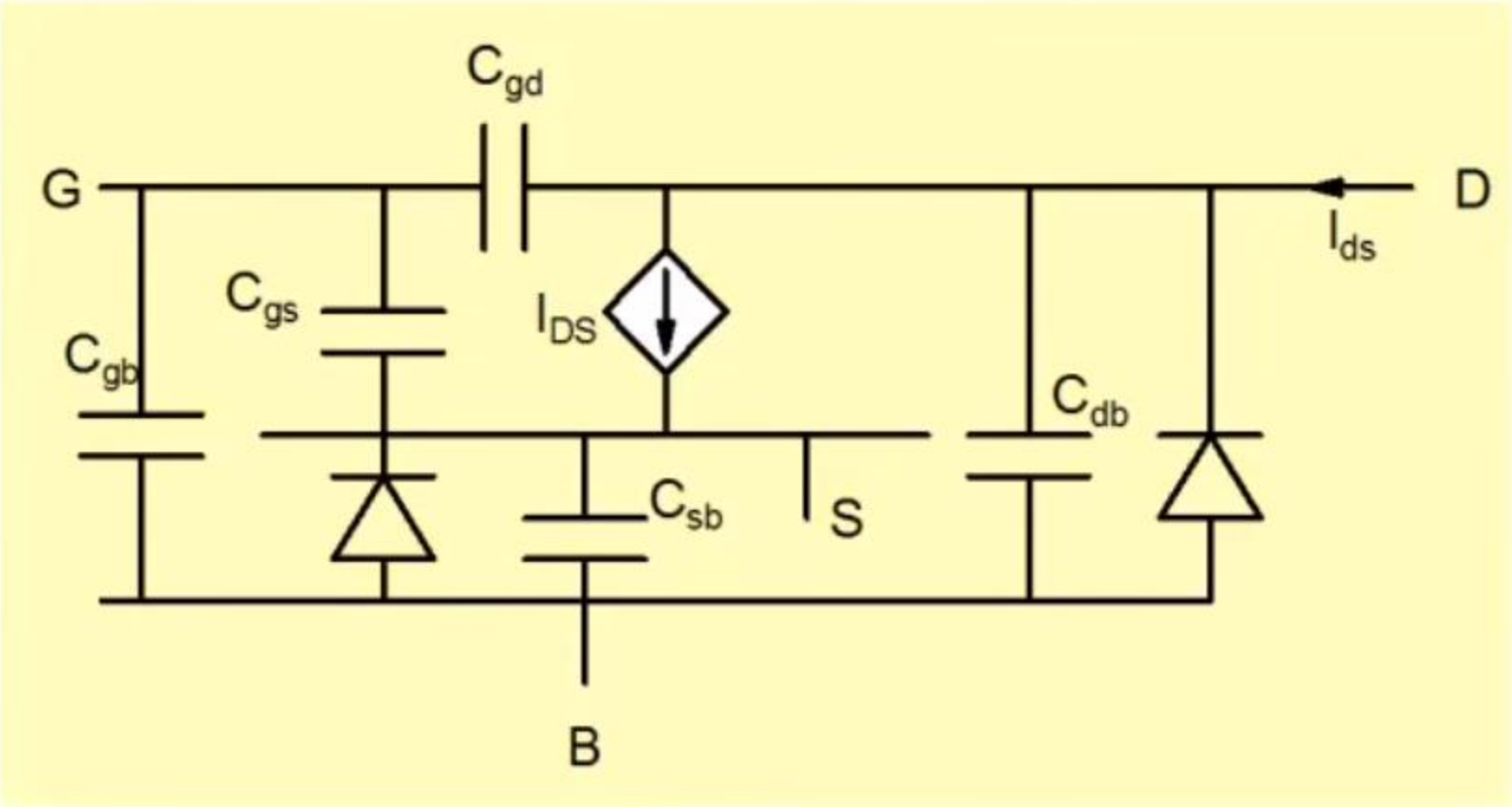
$C_{gs} = 4.1\,fF$; $C_{gd} = 0.43\,fF$

$C_{sb} = 4.47\,fF$

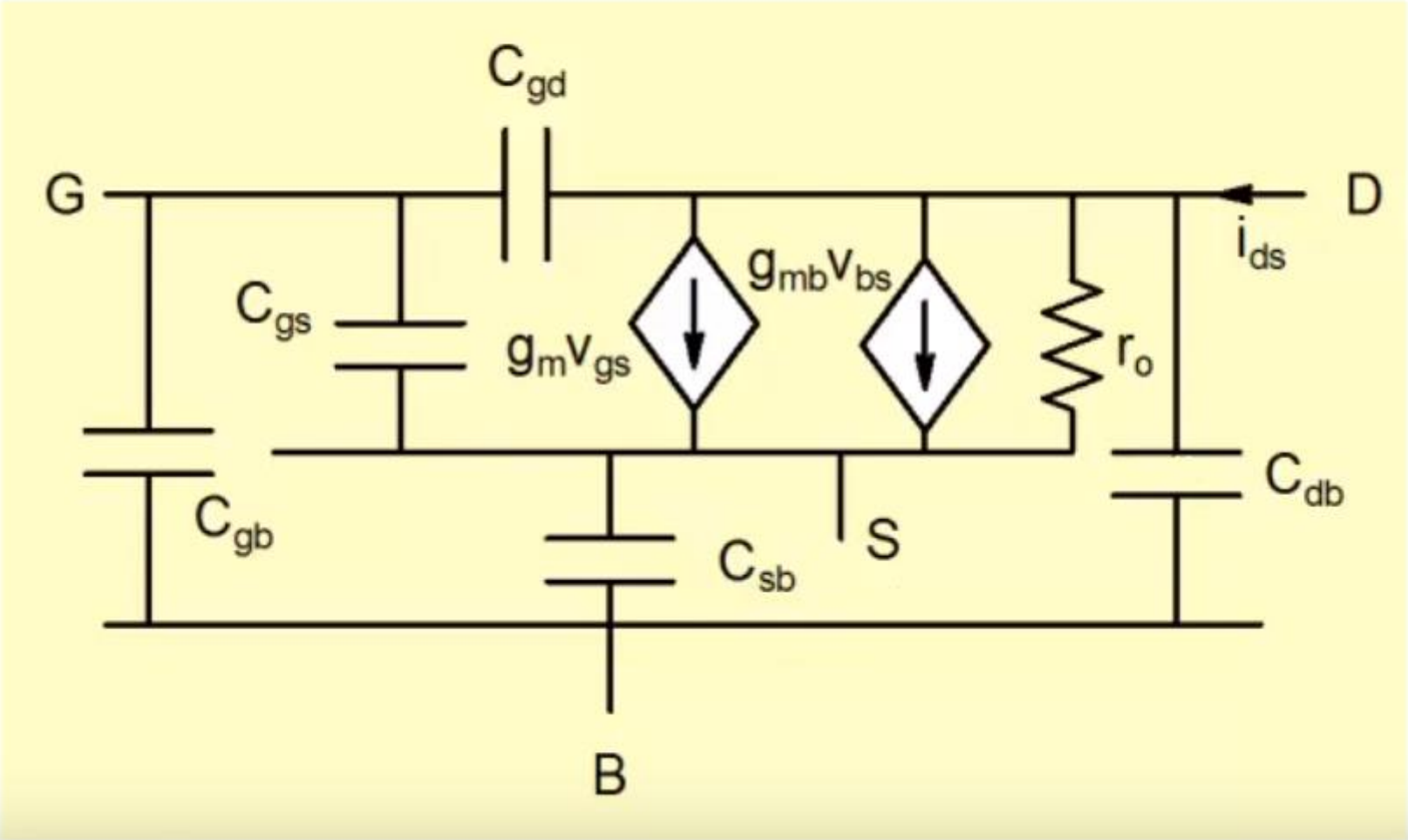
$C_{db} = 2.75\,fF$

$V_{SB} = 0$; $V_{DS} = 2V$

Complete Large Signal Model



High Frequency Small Signal Model



- We have so far discussed simple MOS models which are suitable for 'hand-analysis' of circuits. For more accurate prediction of circuit characteristics using circuit simulation more accurate MOS models are required.

- SPICE and its various variants are the most popular circuit simulation tool. In SPICE, there are a number of MOS models that are available including Level-1, level-2, Level-3, BSIM1, BSIM2, BSIM3, BSIM4 etc.

- Level-1 model is the simplest and is basically similar to the large signal model that we have described earlier. A popular model for submicron devices is BSIM3 model.

*** SPICE- Simulation Program with Integrated Circuit Emphasis**

*** BSIM- Berkeley Short-channel IGFET Model**

BSIM3 : Berkeley Short Channel IGFET (Insulated gate Field Effect) Model

$$I_{ds} = \frac{I_{dso(Vdseff)}}{1 + \frac{R_{ds} I_{dso(Vdseff)}}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)\left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right)$$

$$I_{dso} = \frac{W_{eff}\mu_{eff}C_{ox}V_{gsteff}(1 - A_{bulk}\frac{V_{dseff}}{2(V_{gsteff} + 2v_t)})V_{dseff}}{L_{eff}[1 + V_{dseff} / (E_{sat}L_{eff})]}$$

$$V_A = V_{Asat} + (1 + \frac{P_{vag}V_{gsteff}}{E_{sat}L_{eff}})(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}})^{-1}$$

$$V_{ACLM} = \frac{A_{bulk}E_{sat}L_{eff} + V_{gsteff}}{P_{CLM}A_{bulk}E_{sat}\, litl}(V_{ds} - V_{dseff})$$

Predictive Technology Model

Introduction

Latest Models

Nano-CMOS

Post-Silicon

Interconnect

Reliability

Contact

LATEST MODELS

Typical SPICE model files for each future generation are available here.

Attention: By using a **PTM** file, you agree to acknowledge both the URL of **PTM**: http://ptm.asu.edu/ **and the related publications** in all documents and publications involving its usage.

New!

June 01, 2012:

PTM releases a new set of models for multi-gate transistors (**PTM-MG**), for both HP and LSTP applications. It is based on BSIM-CMG, a dedicated model for multi-gate devices.

Acknowledgement: PTM-MG is developed in collaboration with ARM.

Please start from models and param.inc.

- 7nm PTM-MG HP NMOS, HP PMOS, LSTP NMOS, LSTP PMOS
- 10nm PTM-MG HP NMOS, HP PMOS, LSTP NMOS, LSTP PMOS
- 14nm PTM-MG HP NMOS, HP PMOS, LSTP NMOS, LSTP PMOS
- 16nm PTM-MG HP NMOS, HP PMOS, LSTP NMOS, LSTP PMOS
- 20nm PTM-MG HP NMOS, HP PMOS, LSTP NMOS, LSTP PMOS

The entire package is also available here: PTM-MG

November 15, 2008:

PTM releases a new set of models for low-power applications (PTM LP), incorporating high-k/metal gate and stress effect.

- 16nm PTM LP model: V2.1
- 22nm PTM LP model: V2.1
- 32nm PTM LP model: V2.1
- 45nm PTM LP model: V2.1

September 30, 2008:

PTM releases a new set of models for high-performance applications (PTM HP), incorporating high-k/metal gate and stress effect.

- 16nm PTM HP model: V2.1
- 22nm PTM HP model: V2.1

https://bsim.berkeley.edu/models/bsim4/

BSIM Group | About | News | Models | Publications | Members | Links

- BSIM-CMG
- BSIM-IMG
- BSIM-SOI
- BSIM-BULK
- BSIM4

el

BSIM4, as the extension of BSIM3 model, ysical effects into sub-100nm regime. It is a physics-based, accurate, scalable, robust SPICE model for circuit simulation and CMOS technology development. It is developed by the BSIM Research Group in the Department of Electrical Engineering and Computer Sciences (EECS) at the University of California, Berkeley. All suggestions for model improvements are charted by the Compact Model Coalition (CMC).

BSIM4 has been used for the 0.13 um, 90 nm, 65 nm, 45/40 nm, 23/28 nm, and 22/20nm technology nodes.

See BSIM3, a predecessor of BSIM4, here.

Latest Release

BSIM4 4.8.1 was released on Feb. 15, 2017.

We would like to thank CMC members for testing beta models and providing valuable feedbacks during model development.

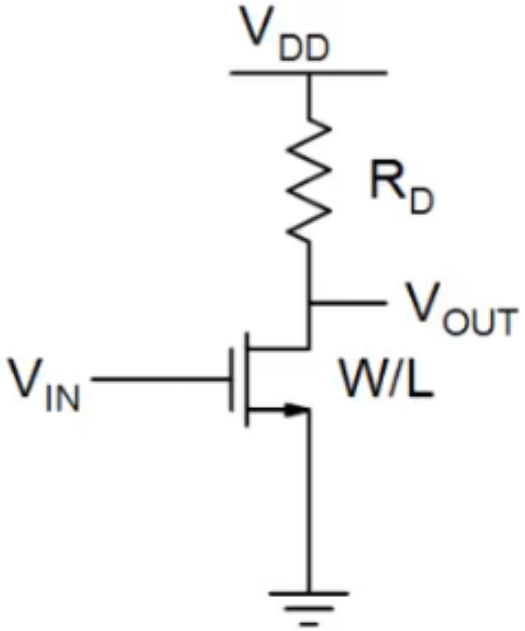
Download BSIM4 4.8.1 model package, including

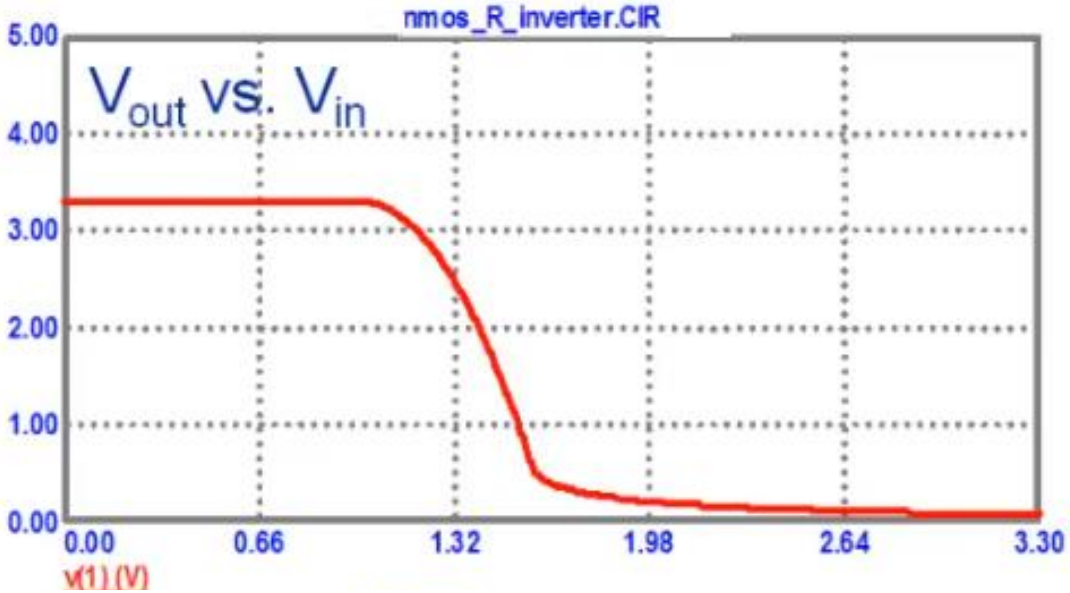
- Model code in C

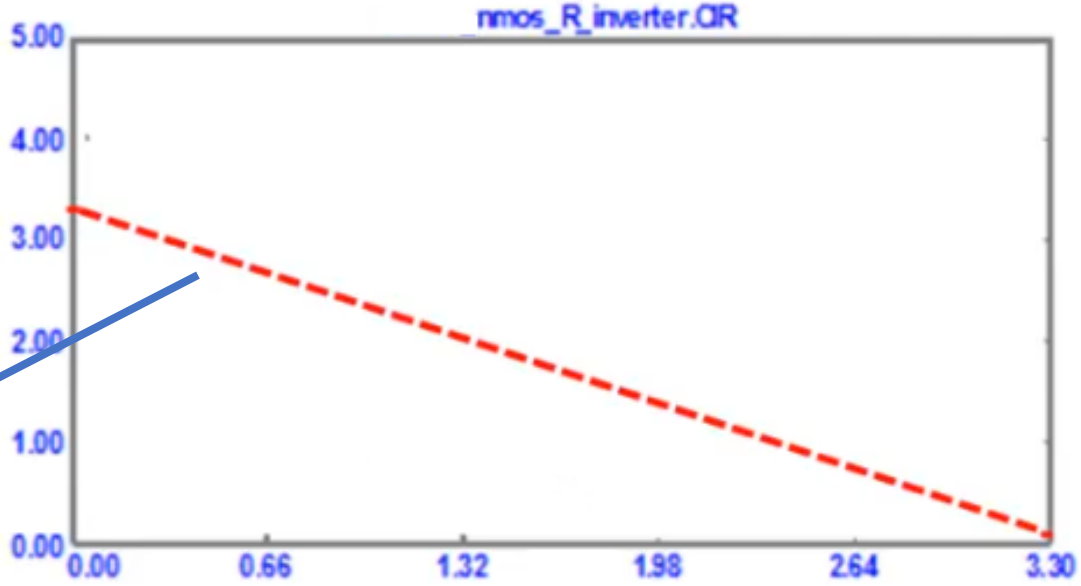
```
* PTM Low Power 16nm Metal Gate / High-K / Strained-Si
* nominal Vdd = 0.9V

.model  nmos  nmos  level = 54


+version = 4.0            binunit = 1              paramchk= 1              mobmod  = 0
+capmod  = 2              igcmod  = 1              igbmod  = 1              geomod  = 1
+diomod  = 1              rdsmod  = 0              rbodymod= 1              rgatemod= 1
+permod  = 1              acnqsmod= 0              trnqsmod= 0

+tnom    = 27             toxe    = 1.2e-009       toxp    = 9e-010         toxm    = 1.2e-009
+dtox    = 3e-010         epsrox  = 3.9            wint    = 5e-009         lint    = 0
+ll      = 0              wl      = 0              lln     = 1              wln     = 1
+lw      = 0              ww      = 0              lwn     = 1              wwn     = 1
+lwl     = 0              wwl     = 0              xpart   = 0              toxref  = 1.2e-009

+vth0    = 0.68191        k1      = 0.4            k2      = 0              k3      = 0
+k3b     = 0              w0      = 2.5e-006       dvt0    = 1              dvt1    = 2
+dvt2    = 0              dvt0w   = 0              dvt1w   = 0              dvt2w   = 0
+dsub    = 0.1            minv    = 0.05           voffl   = 0              dvtp0   = 1e-011
+dvtp1   = 0.1            lpe0    = 0              lpeb    = 0              xj      = 5e-009
+ngate   = 1e+023         ndep    = 7e+018         nsd     = 2e+020         phin    = 0
+cdsc    = 0              cdscb   = 0              cdscd   = 0              cit     = 0
+voff    = -0.1014        nfactor = 1.6            eta0    = 0.0095         etab    = 0
+vfb     = -0.55          u0      = 0.028          ua      = 6e-010         ub      = 1.2e-018
+uc      = 0              vsat    = 200000         a0      = 1              ags     = 0
+a1      = 0              a2      = 1              b0      = 0              b1      = 0
+keta    = 0.04           dwg     = 0              dwb     = 0              pclm    = 0.02
+pdiblc1 = 0.001          pdiblc2 = 0.001          pdiblcb = -0.005         drout   = 0.5
+pvag    = 1e-020         delta   = 0.01           pscbe1  = 8.14e+008      pscbe2  = 1e-007
+fprout  = 0.2            pdits   = 0.01           pditsd  = 0.23           pditsl  = 2300000
+rsh     = 5              rdsw    = 170            rsw     = 75             rdw     = 75
+rdswmin = 0              rdwmin  = 0              rswmin  = 0              prwg    = 0
+prwb    = 0              wr      = 1              alpha0  = 0.074          alpha1  = 0.005
+beta0   = 30             agidl   = 0.0002         bgidl   = 2.1e+009       cgidl   = 0.0002
+egidl   = 0.8            aigbacc = 0.012          bigbacc = 0.0028         cigbacc = 0.002
```

Circuit Design

Inverter with Resistive Load

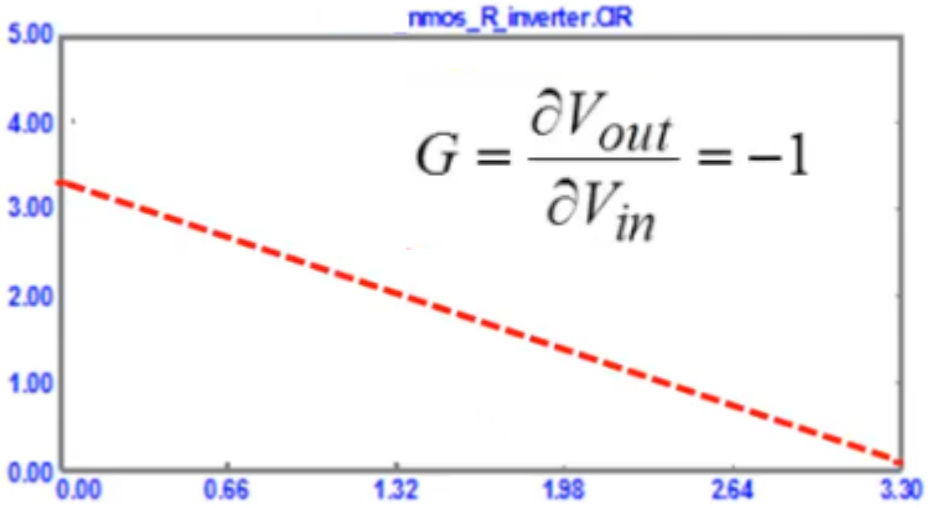


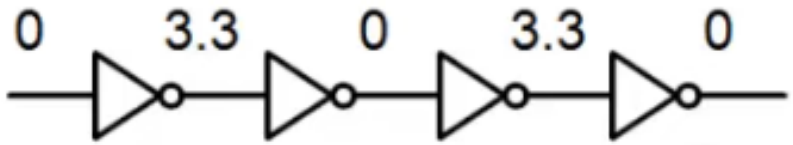


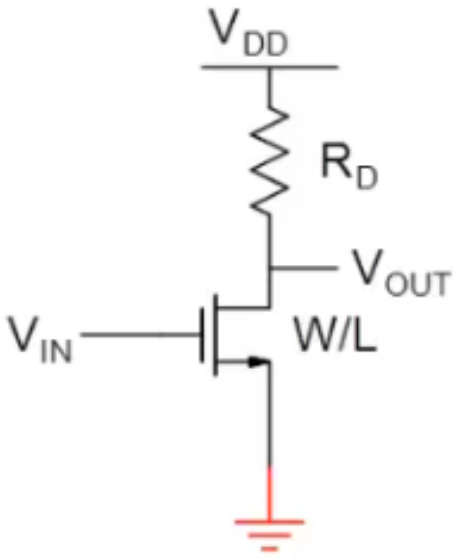


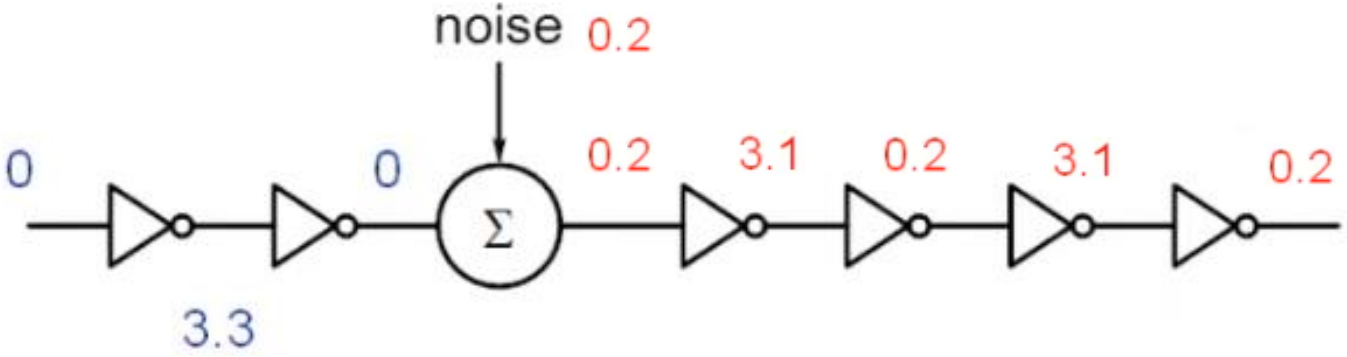
1. Area
2. Delay
3. Power
4. …

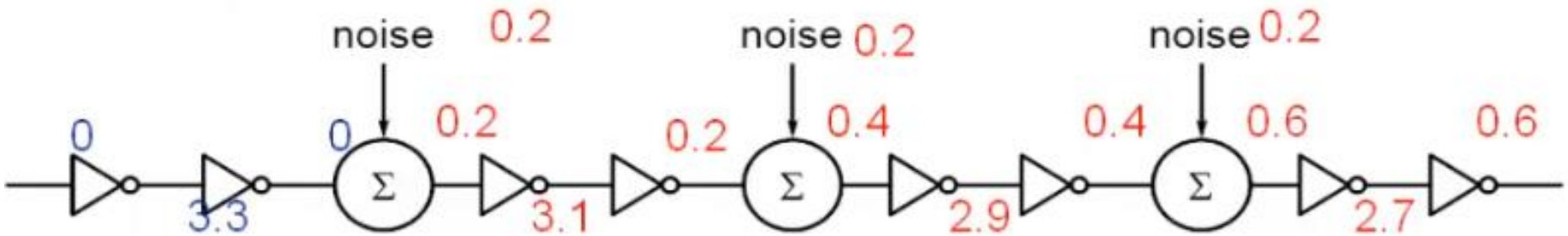
Is this a good inverter ?


nmos_R_inverter.DR
5.00
4.00
3.00
2.00
1.00
0.00
0.00
0.66
1.32
1.98
2.64
3.30
$G = \frac{\partial V_{out}}{\partial V_{in}} = -1$

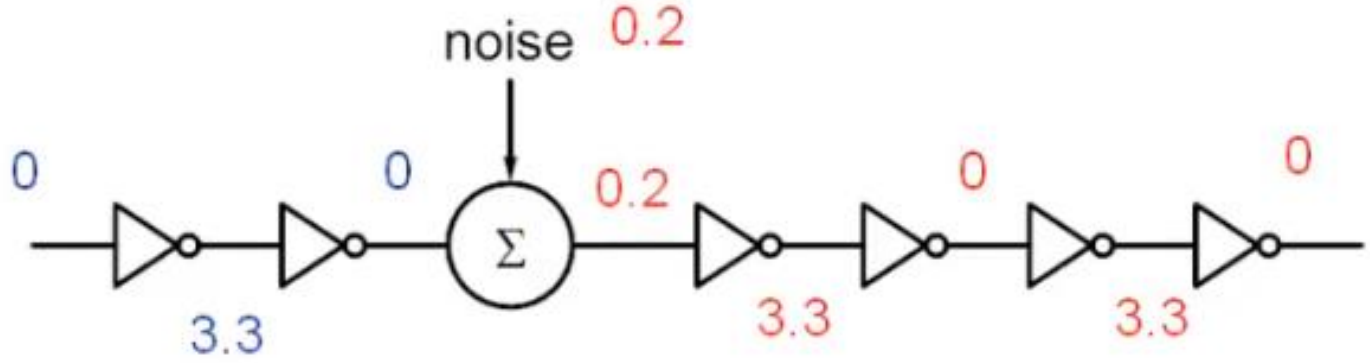

0
3.3
0
3.3
0

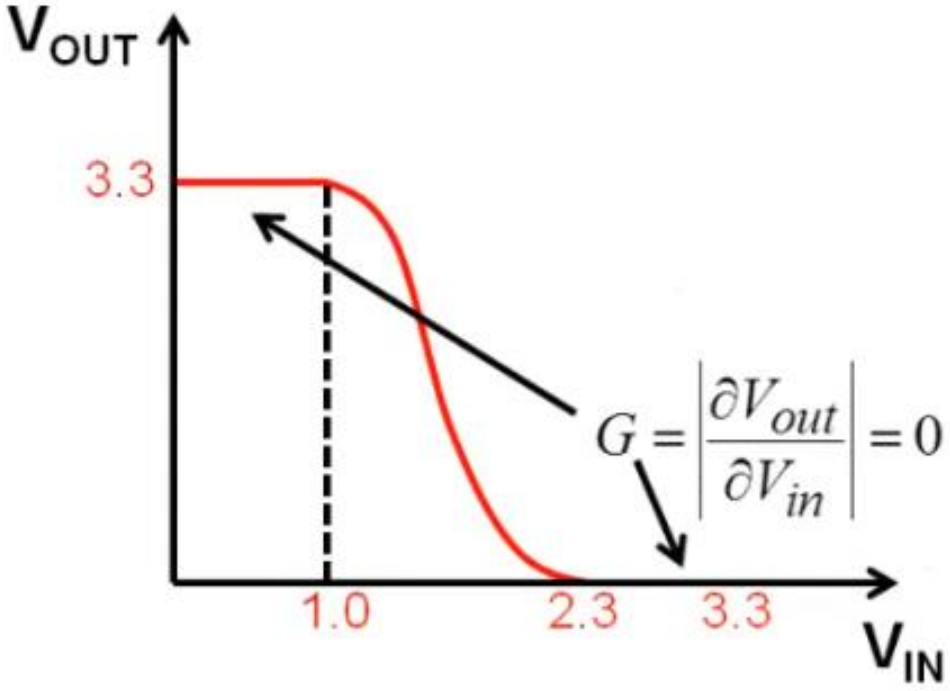

V_{DD}
R_D
V_{OUT}
V_{IN}
W/L

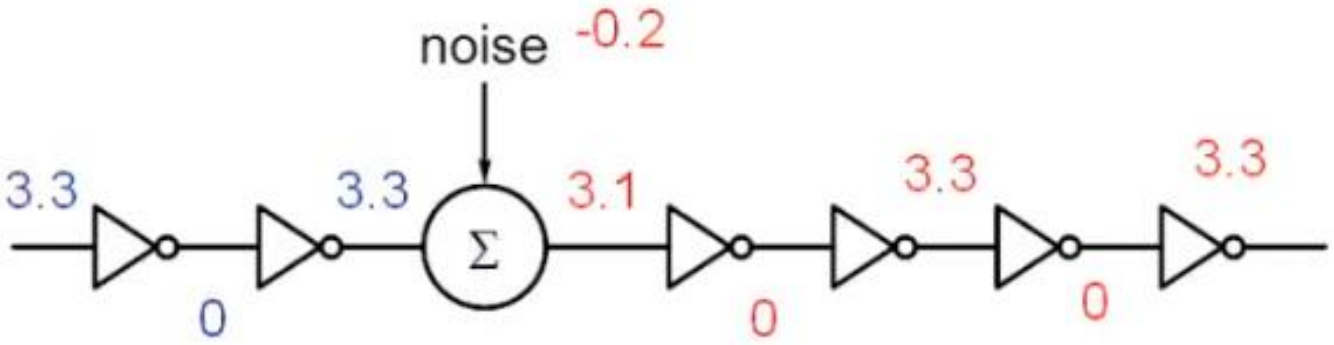

noise 0.2
0
0
Σ
0.2
3.1
0.2
3.1
0.2
3.3

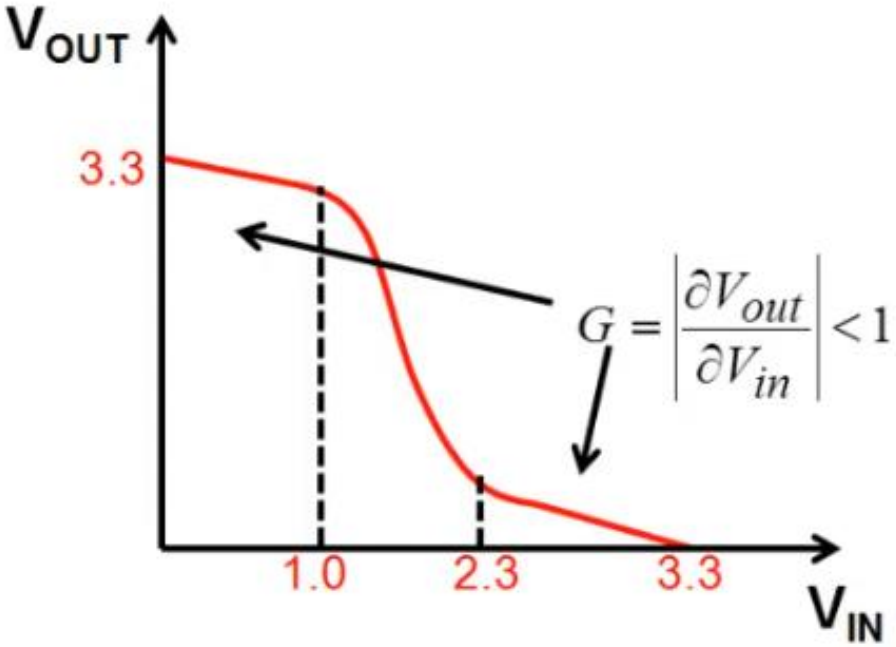

noise 0.2
noise 0.2
noise 0.2
0
0
Σ
0.2
3.3
3.1
0.2
Σ
0.4
2.9
0.4
Σ
0.6
2.7
0.6

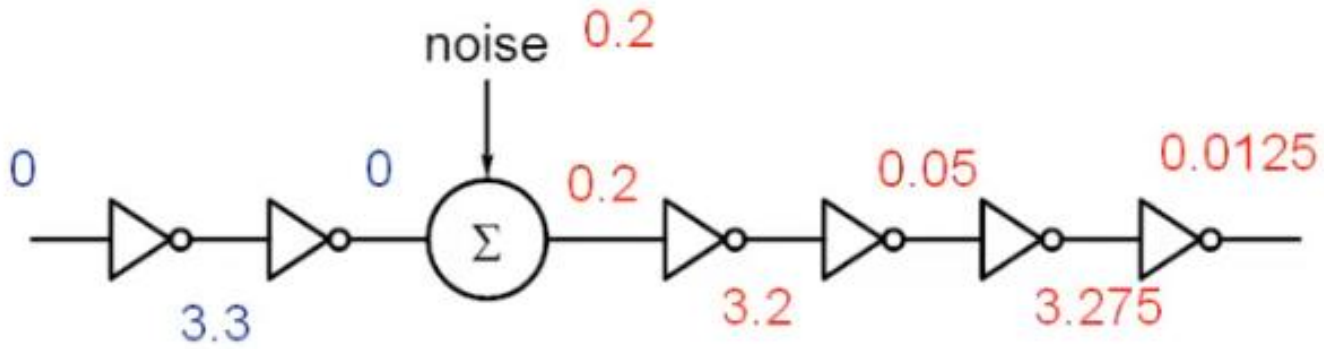
Systems that we design should be robust in presence of noise





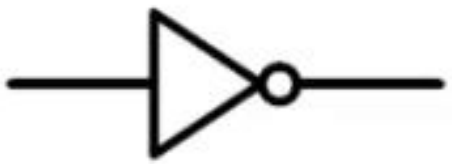




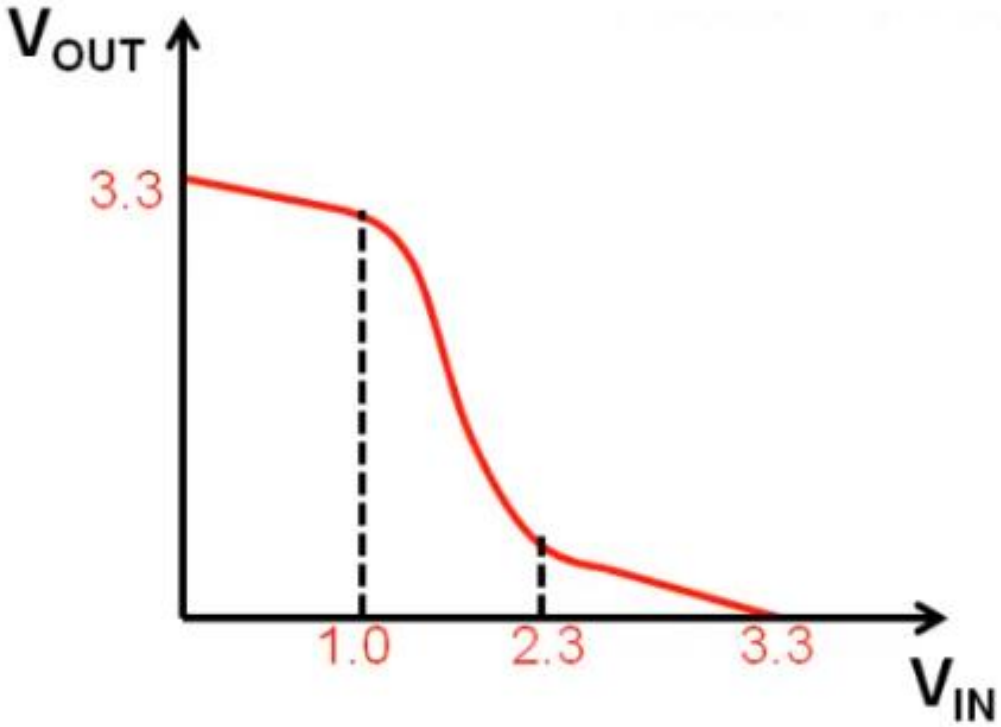


There must be a region with Gain greater than unity

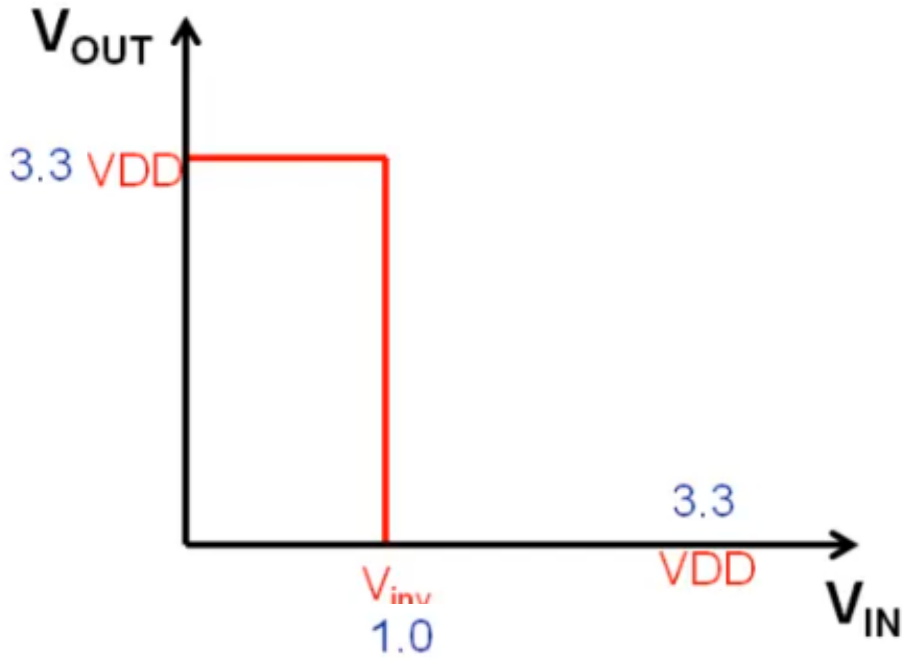
To build an inverter, we need an element that can provide gain

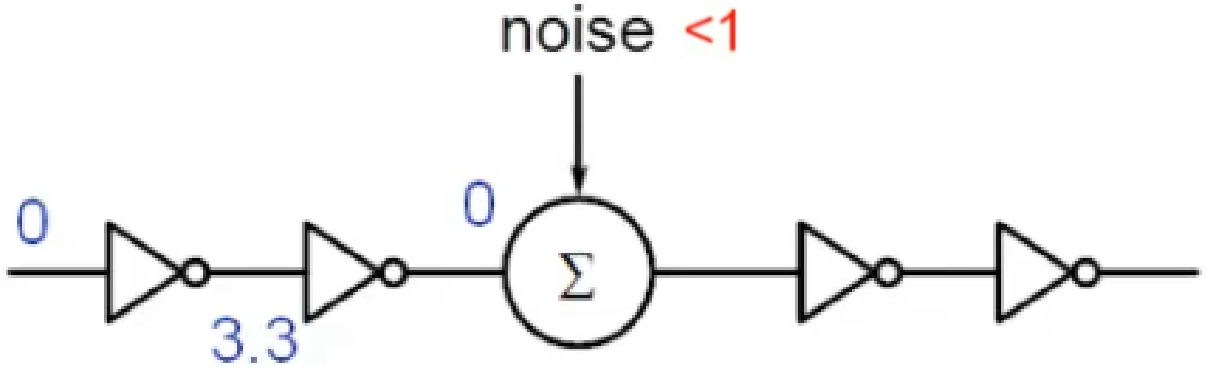


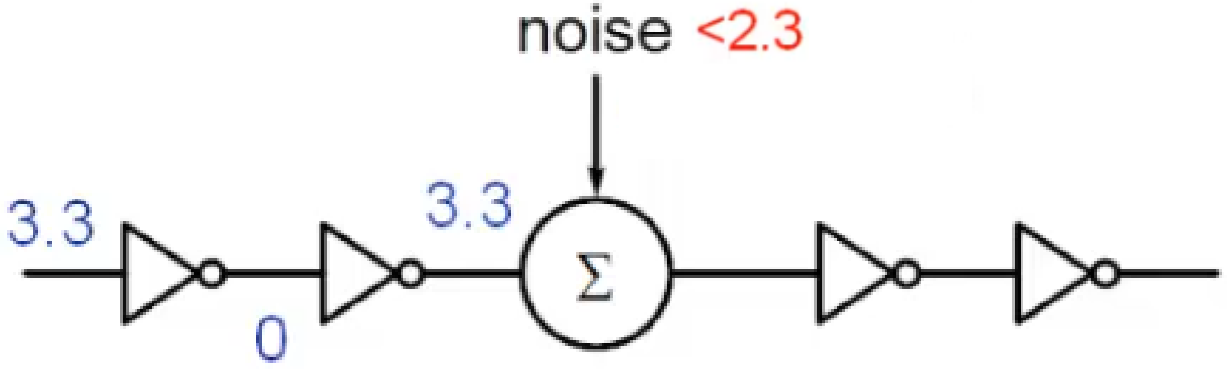
1. Area
2. Delay
3. Power
4. Noise margin



Inverter Threshold Voltage

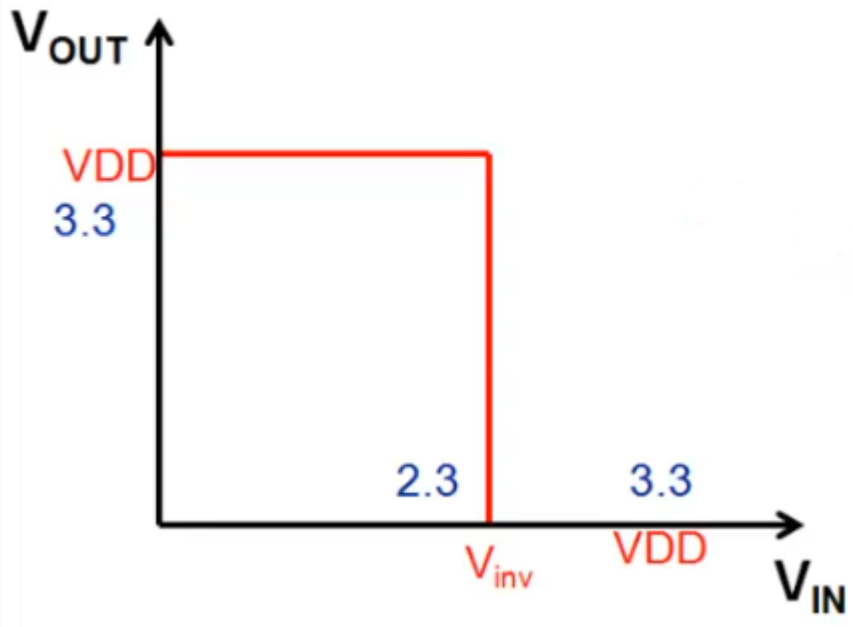


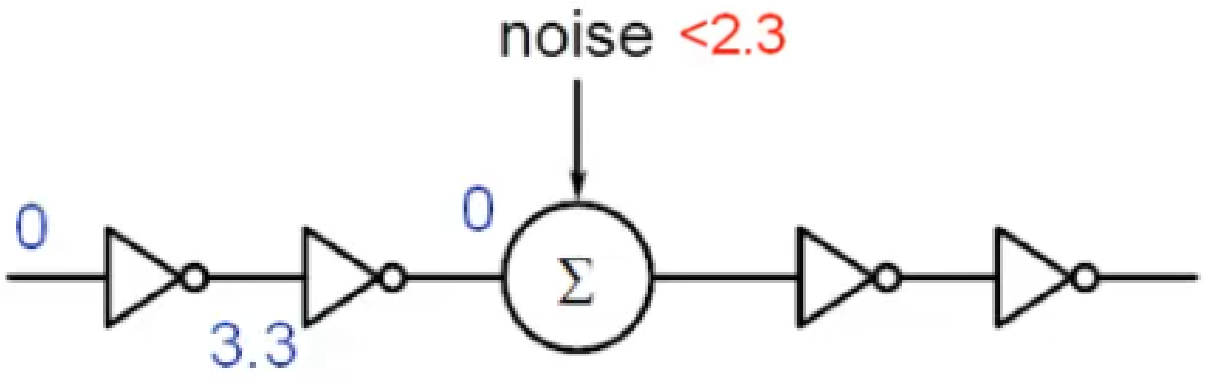


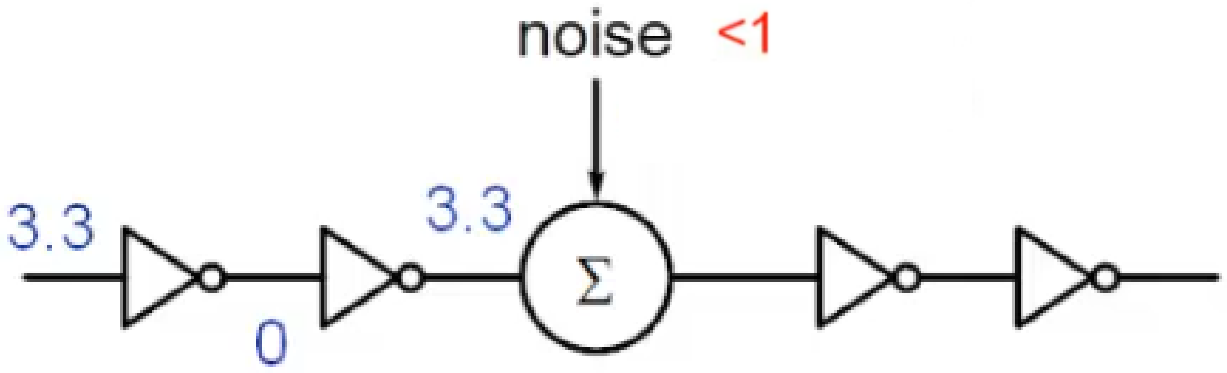


Asymmetrical characteristics

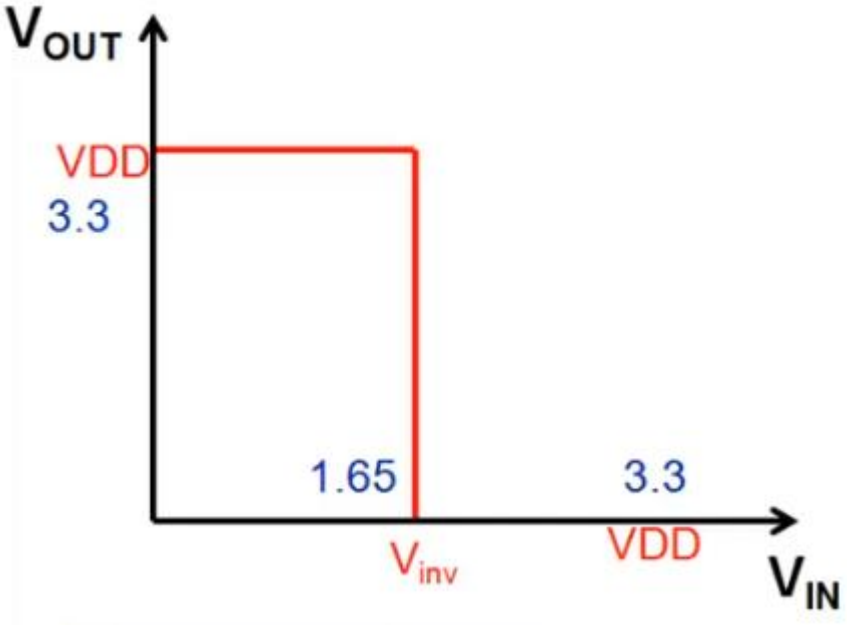
Inverter Threshold Voltage



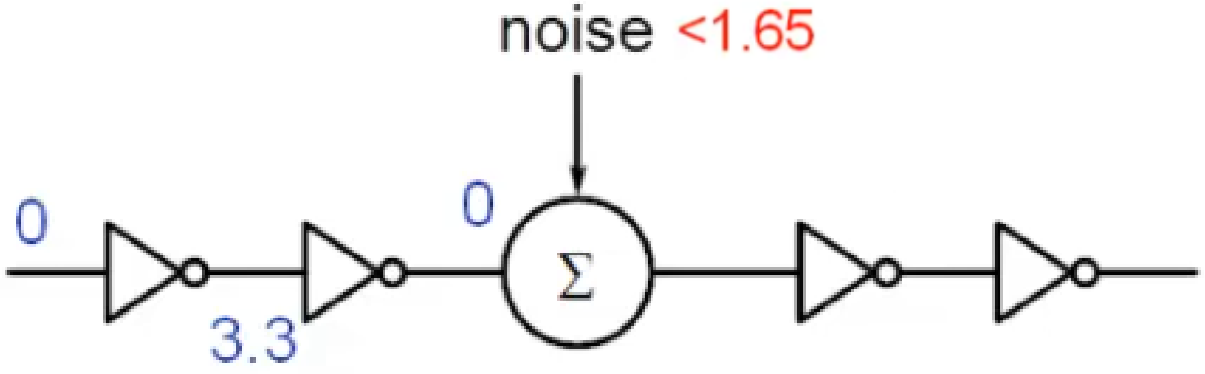


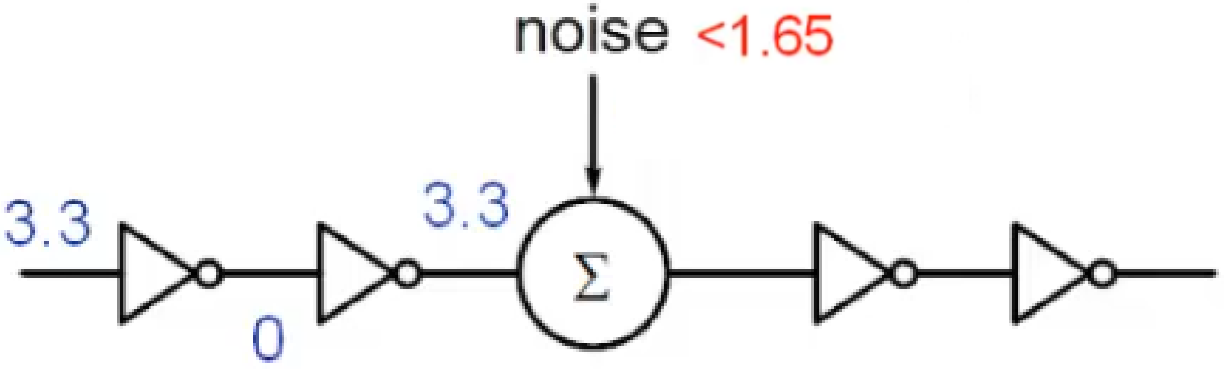


Asymmetrical characteristics



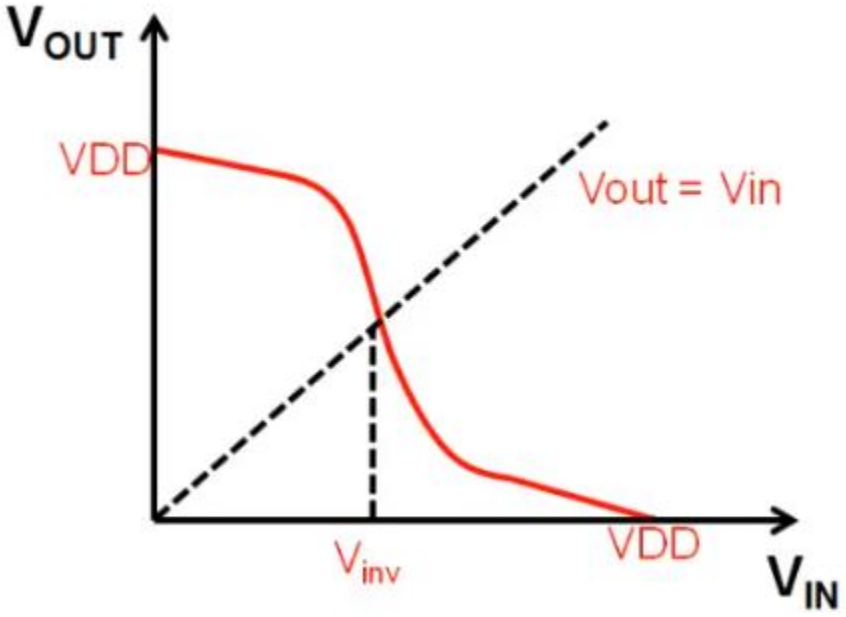
$$V_{inv} = 0.5V_{DD}$$





symmetrical characteristics

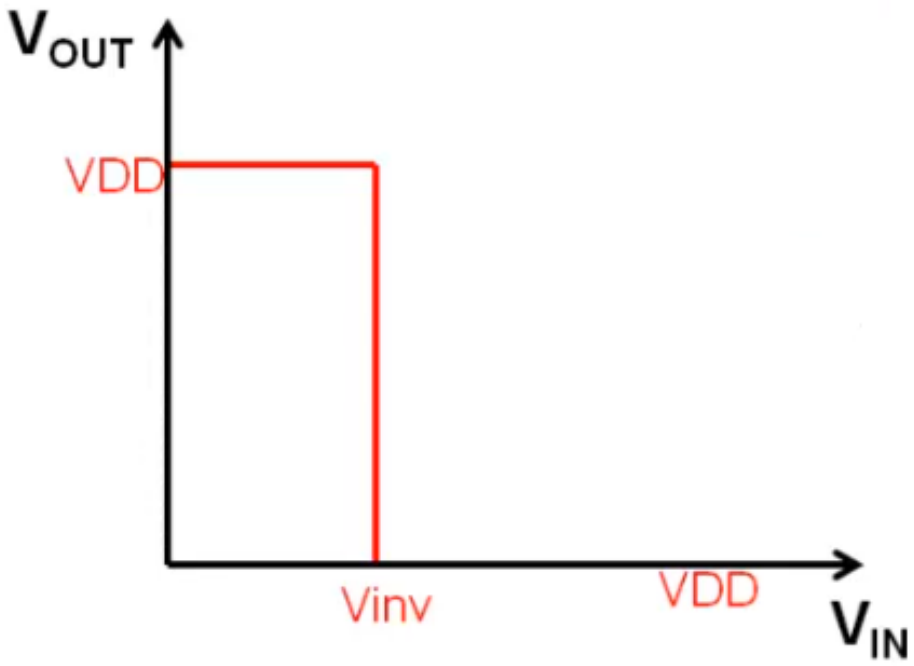
Inverter Threshold Voltage

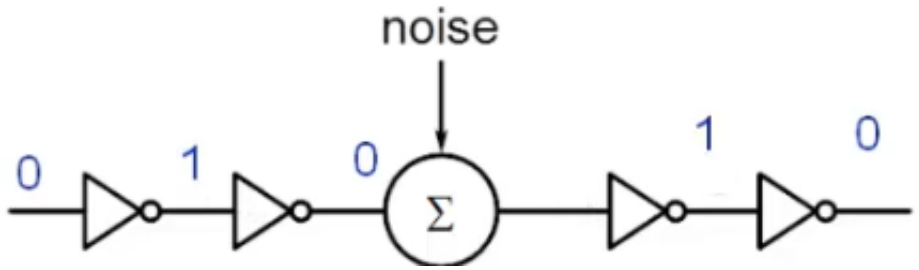


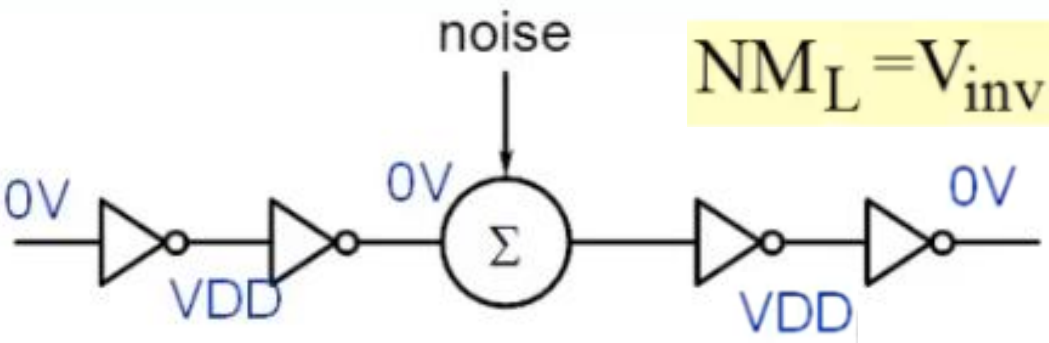
For $V_{in} > V_{inv}$, the output is closer to "0"

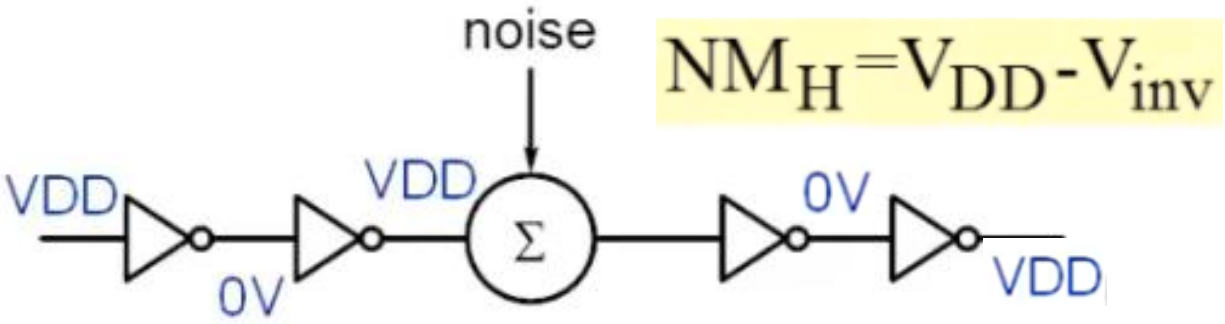
$$V_{inv} = 0.5V_{DD}$$

Noise Margins



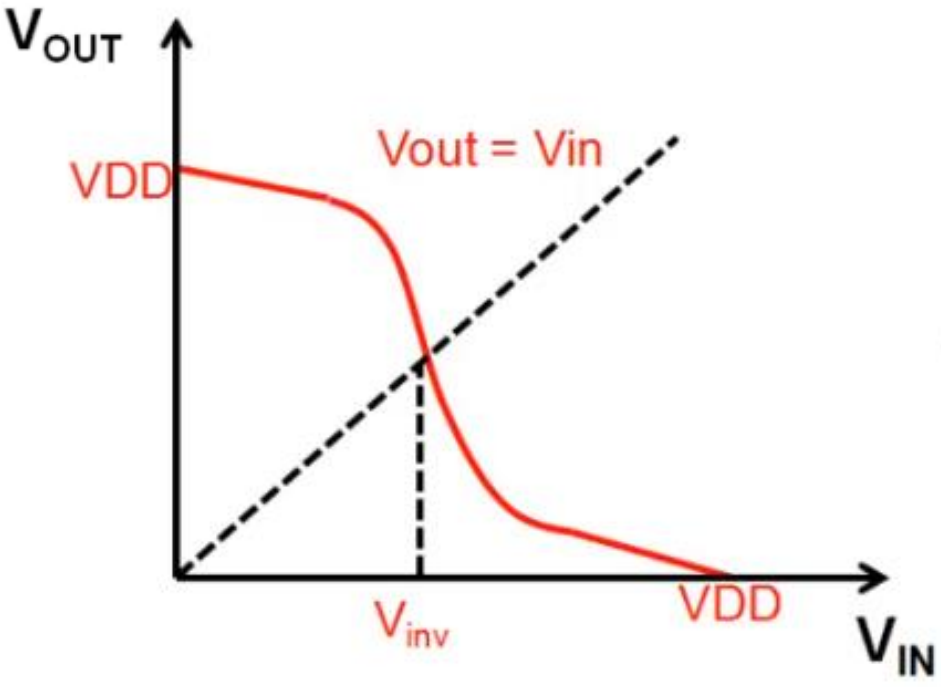


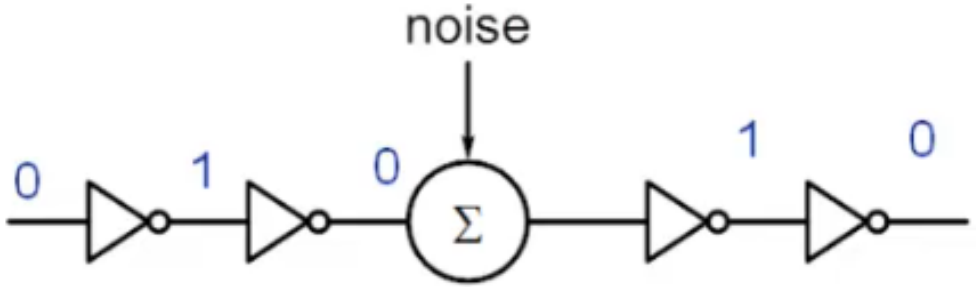


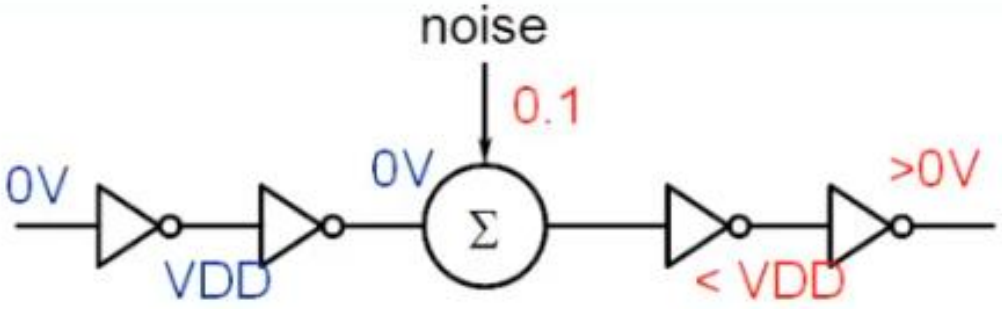


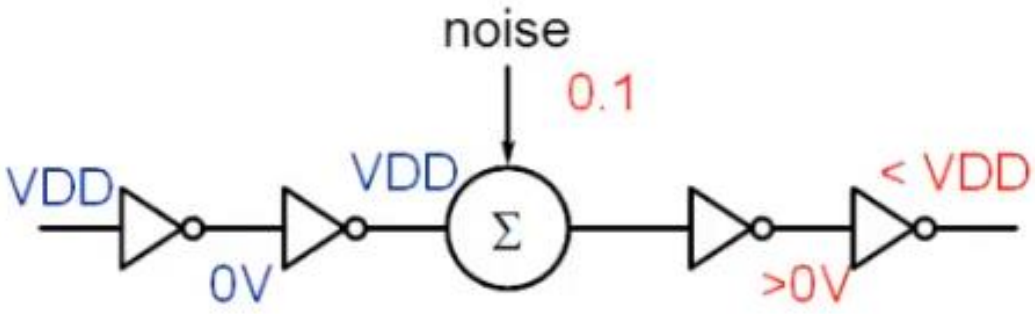
Logical correctness

Noise Margins

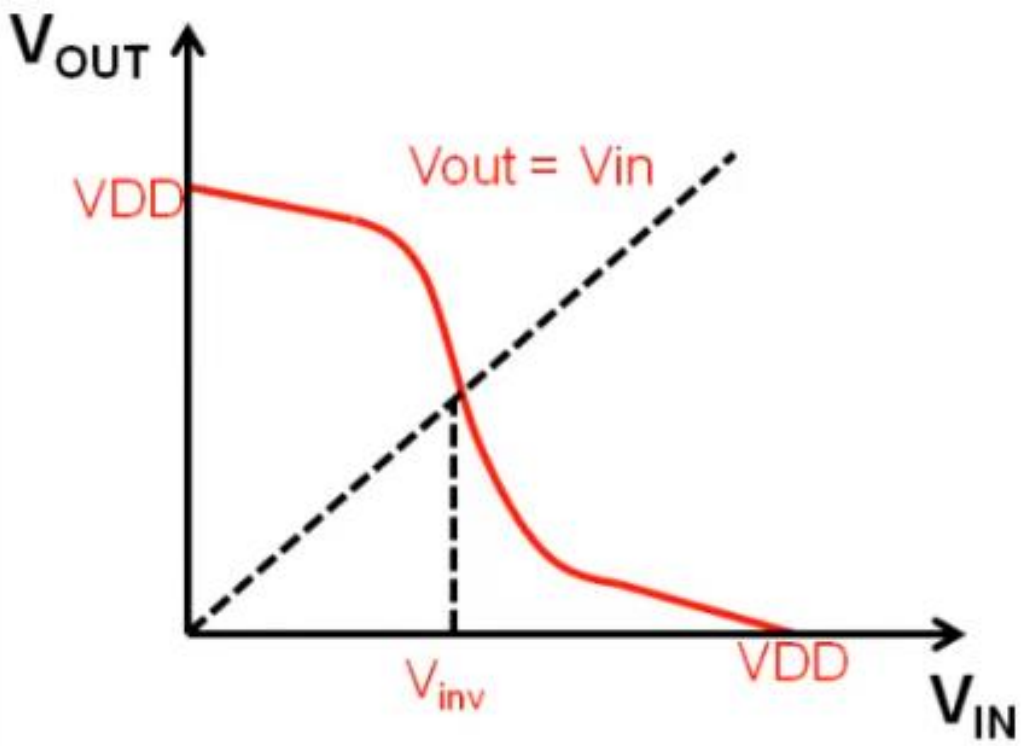


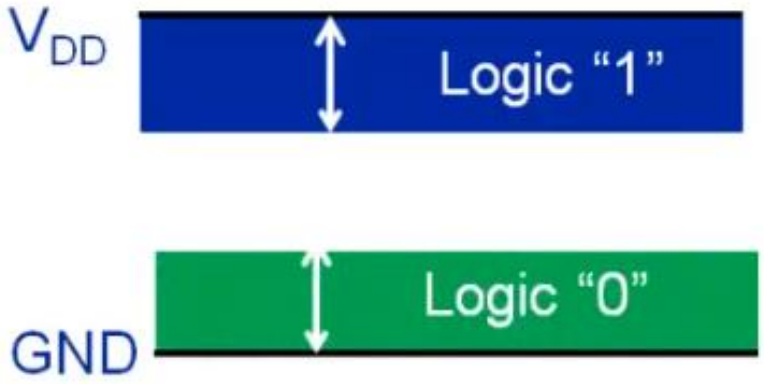


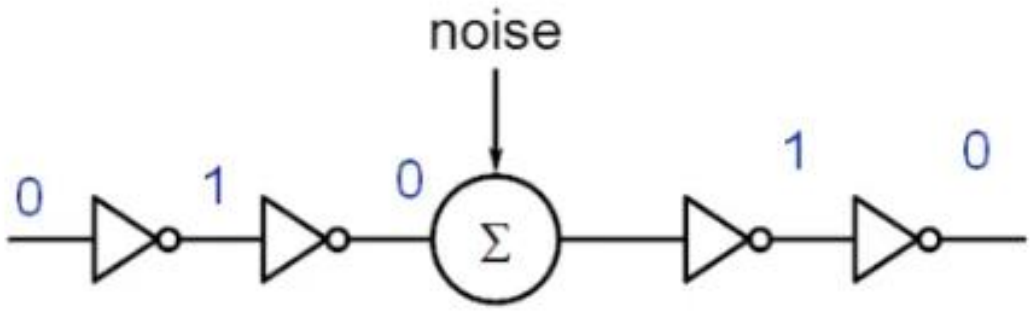


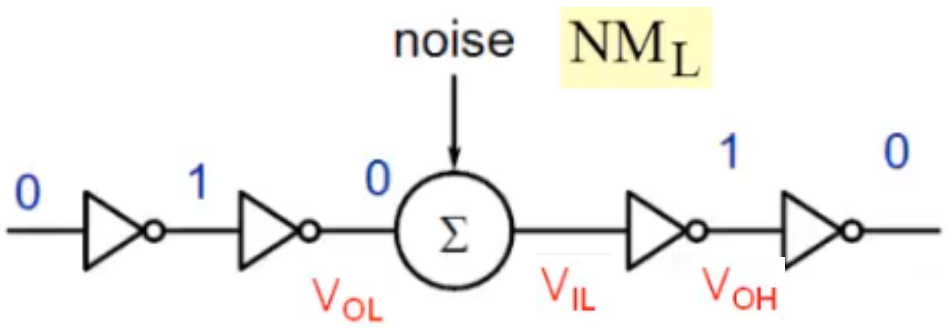


Need proper definition of logic levels in terms of voltages

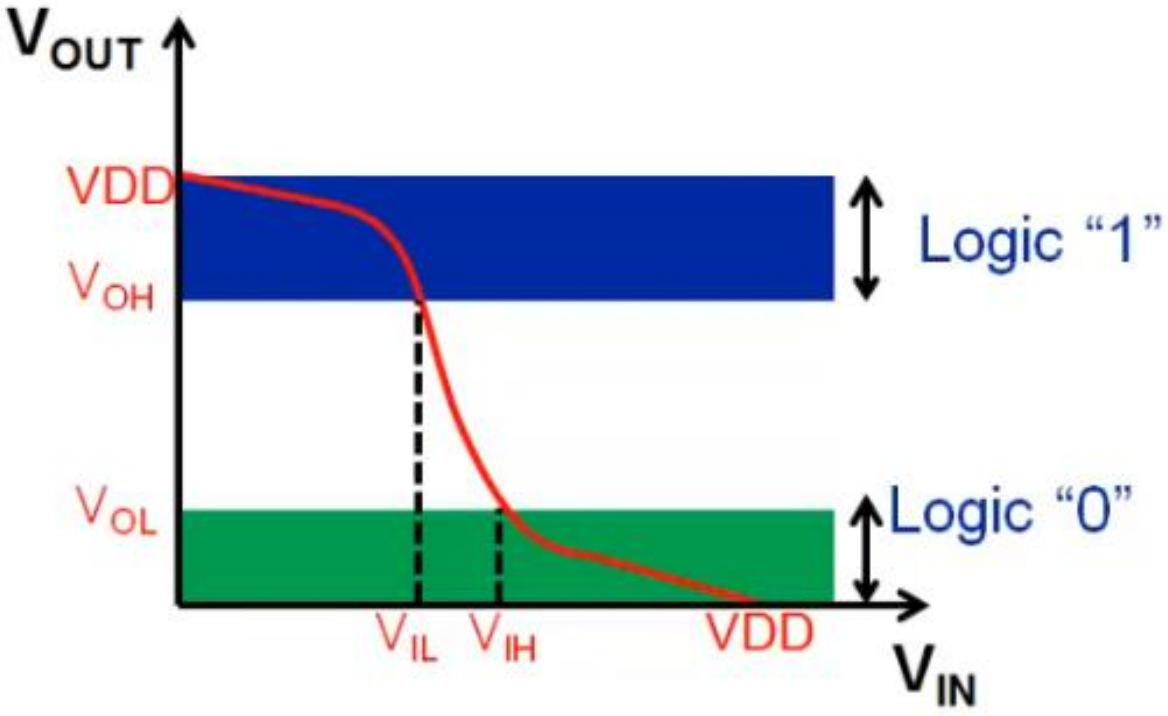

V_{OUT}
VDD
Vout = Vin
V_{inv}
VDD
V_{IN}


V_{DD}
Logic "1"
Logic "0"
GND

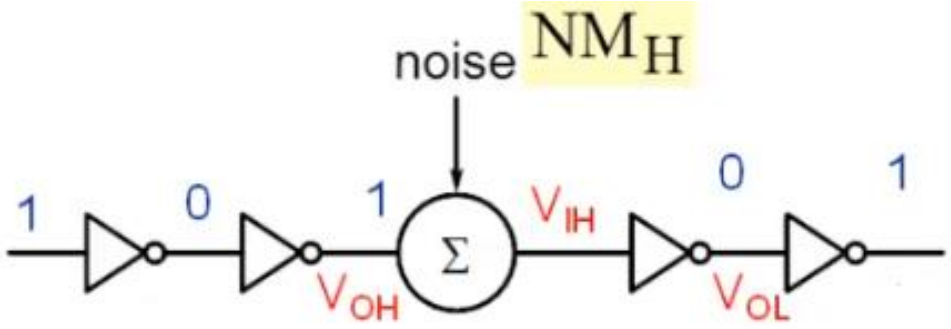

noise
0
1
0
Σ
1
0



$$NM_L = V_{IL} - V_{OL}$$

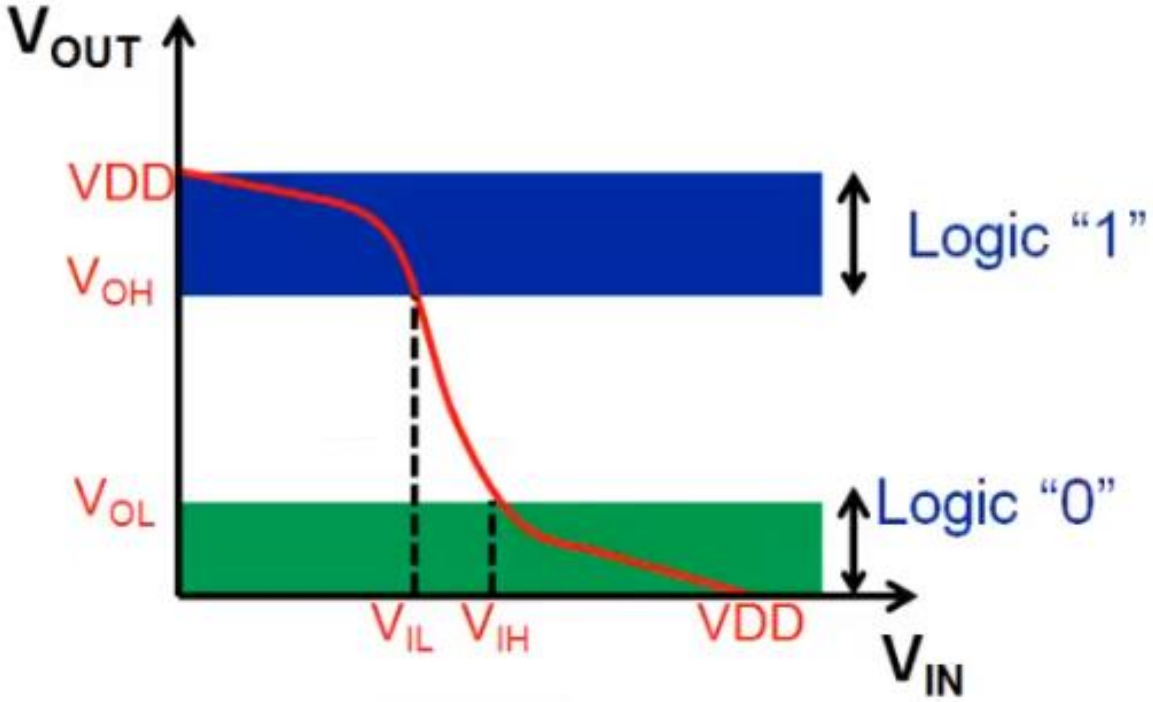


$$NM_H = V_{OH} - V_{IH}$$



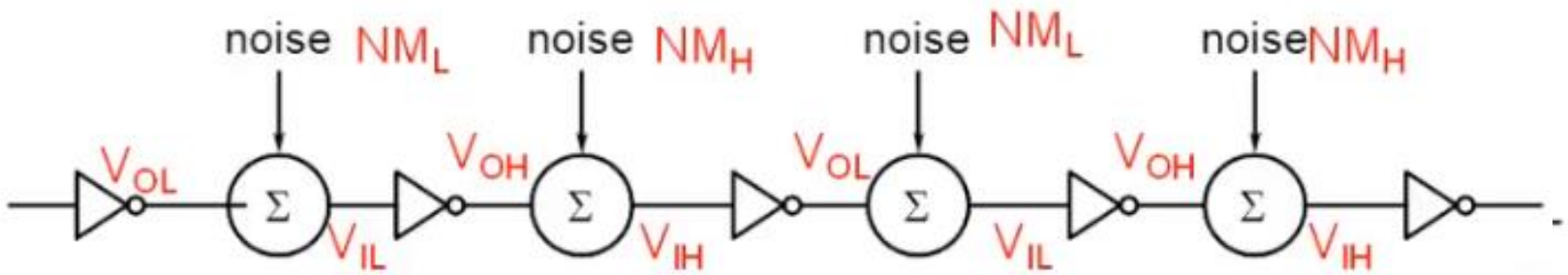
$$V_{DD} > V_{OH} > V_{IH} > V_{IL} > V_{OL} > 0$$

Noise Margins



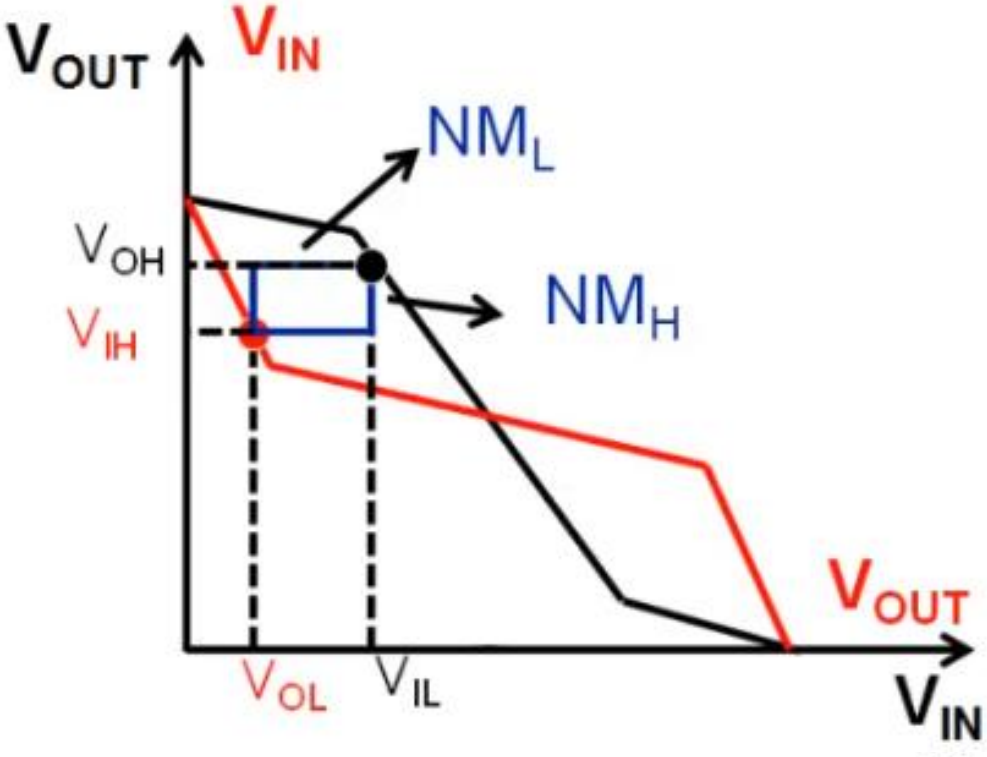
$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$



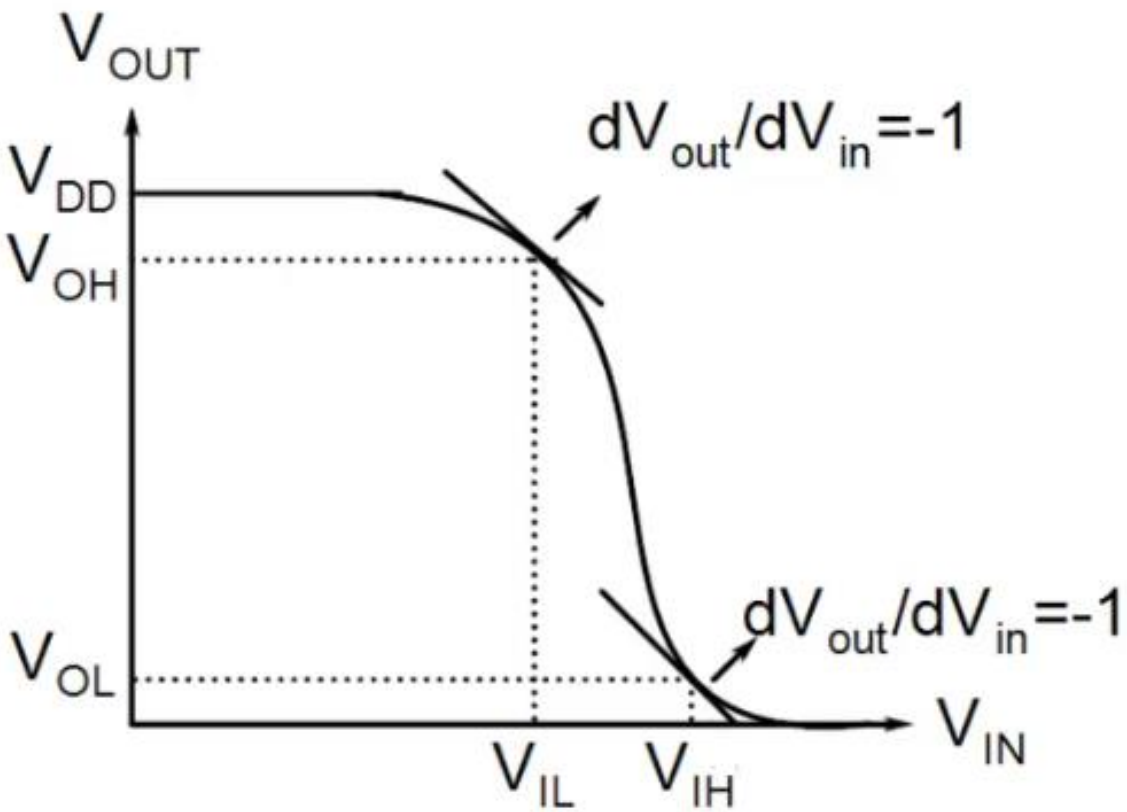
How do we find these threshold values?

Maximize $NM_L = V_{IL} - V_{OL}$ and $NM_H = V_{OH} - V_{IH}$



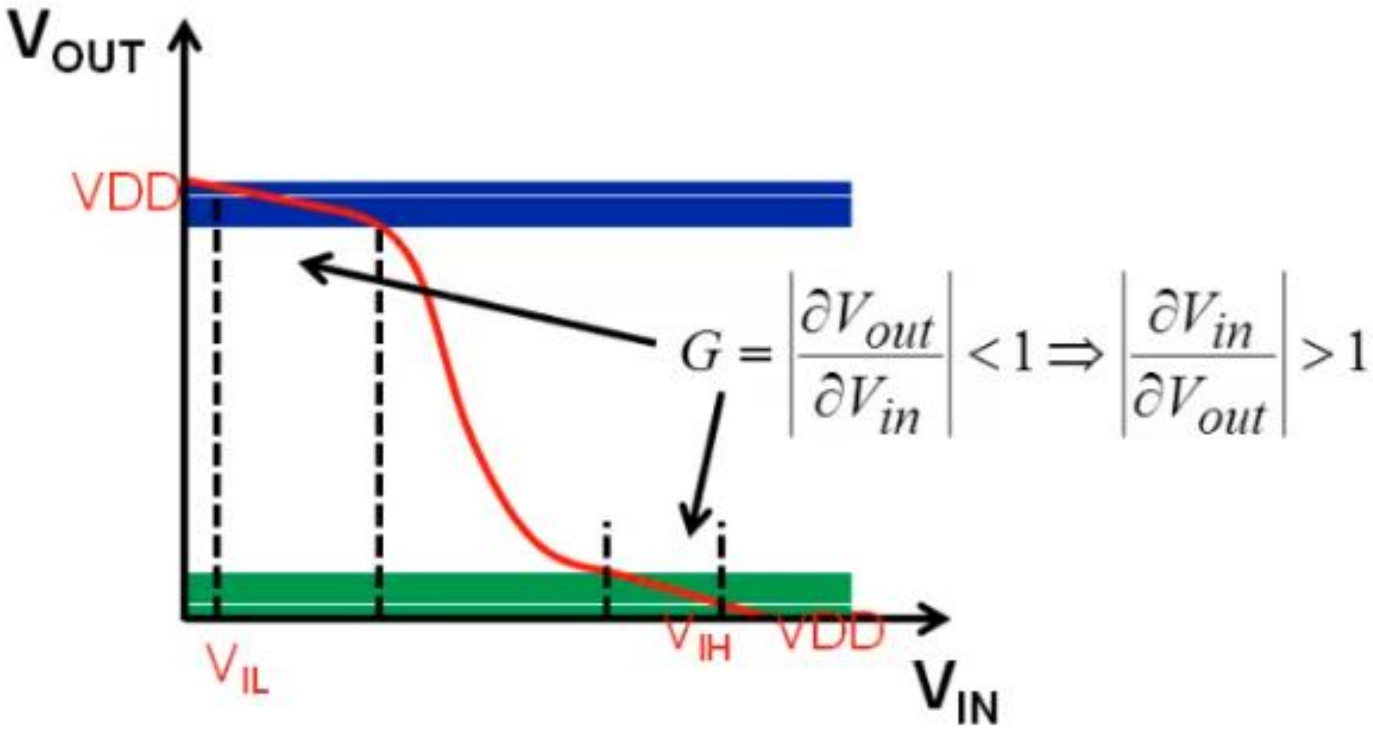
For NMH = NML, find the biggest square that can be accommodated

Alternative Method For finding threshold values?



-valid high and low logic levels should be defined as bands with one determined by the unity-Gain points on VTC

How do we find these threshold values?



$\uparrow NM_L = V_{IL} - V_{OL}$ $\uparrow NM_H = V_{OH} - V_{IH}$

$\uparrow$ $\uparrow$ $\downarrow$ $\downarrow$

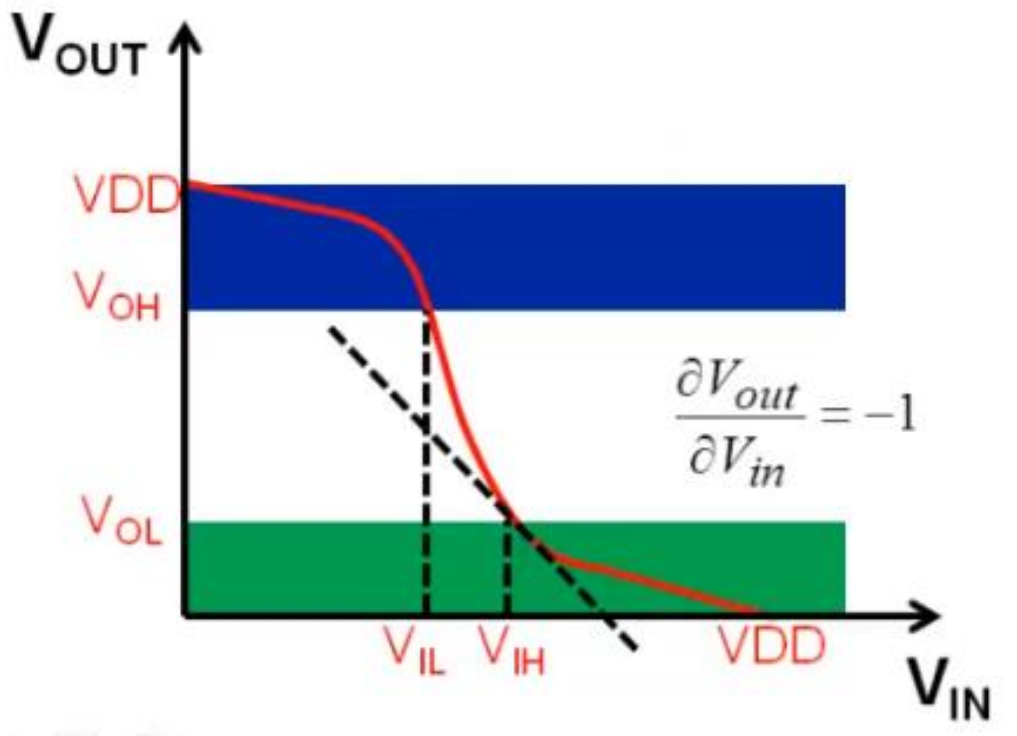
Both noise margins are very small

$NM_L = V_{IL} - V_{OL}$ increase $\delta V_{OL} = -\delta V_{OH}$ $\Rightarrow \delta V_{IL} = -\delta V_{IH}$

$$\delta(NM_L) = \delta V_{IL} - \delta V_{OL}$$

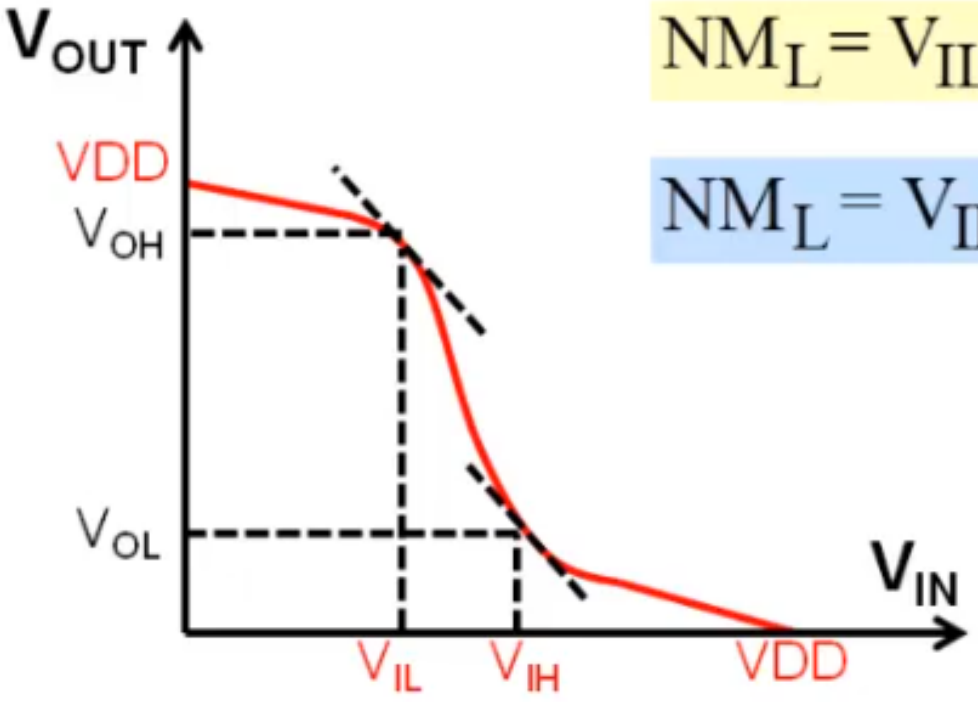
$$\delta(NM_L) = \left(\frac{\delta V_{IL}}{\delta V_{OL}} - 1\right) \times \delta V_{OL}$$

$$\frac{\delta(NM_L)}{\delta V_{OL}} = \left(\frac{1}{-\frac{\delta V_{OL}}{\delta V_{IH}}} - 1\right)$$



As long as $-\frac{\partial V_{out}}{\partial V_{in}} < 1$ NM_L improves

Noise Margins: Alternative definition

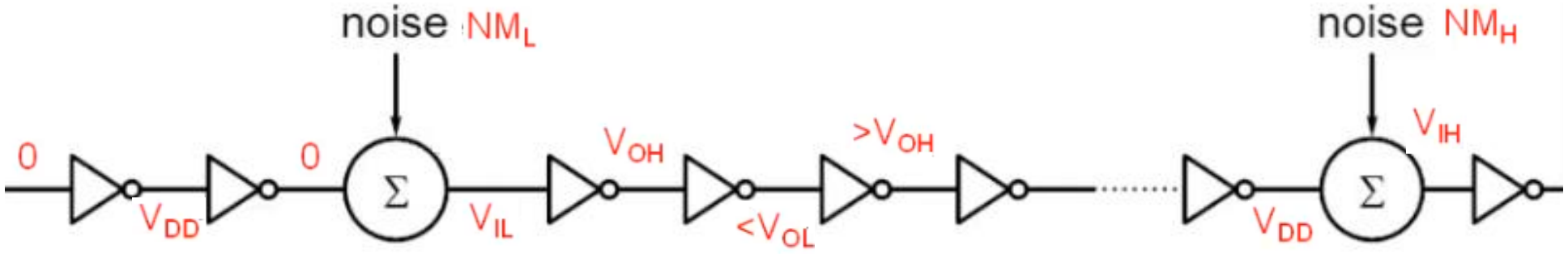


$NM_L = V_{IL} - V_{OL}$

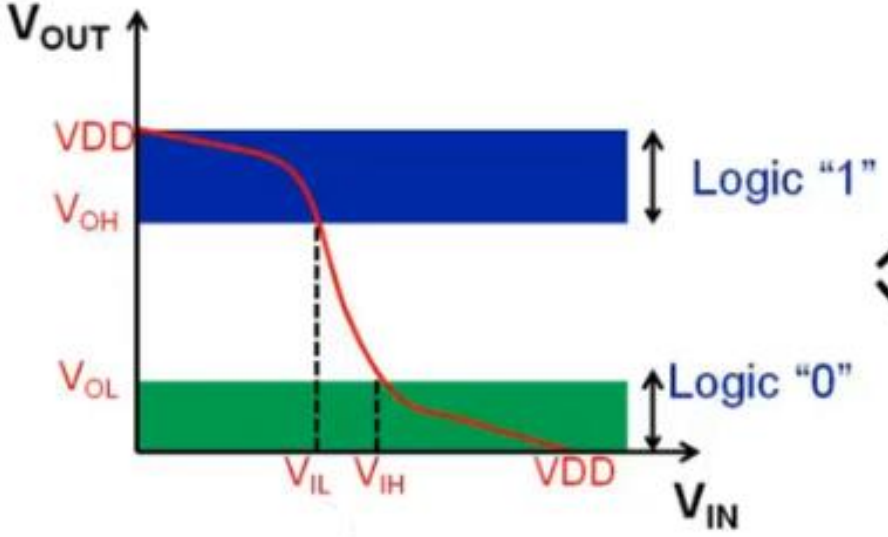
$NM_H = V_{OH} - V_{IH}$

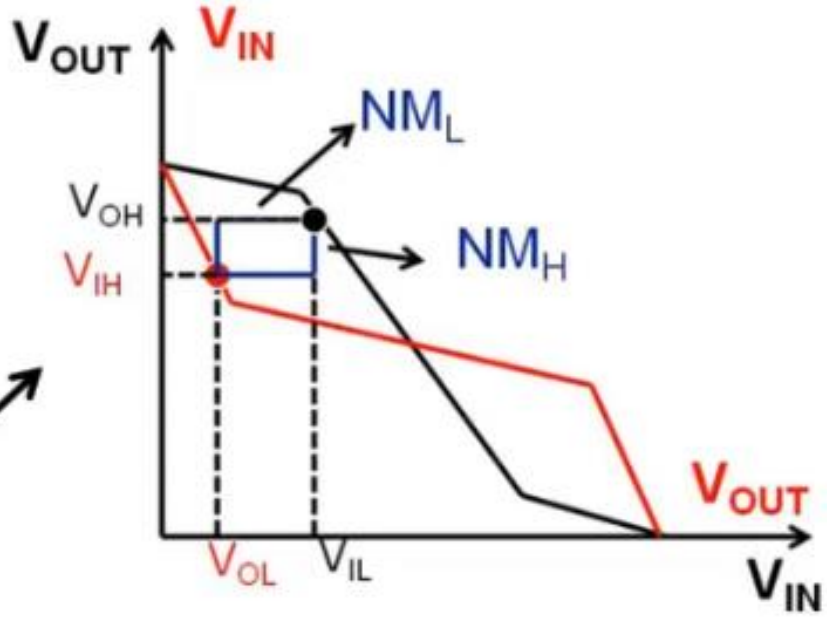
$NM_L = V_{IL} - 0$

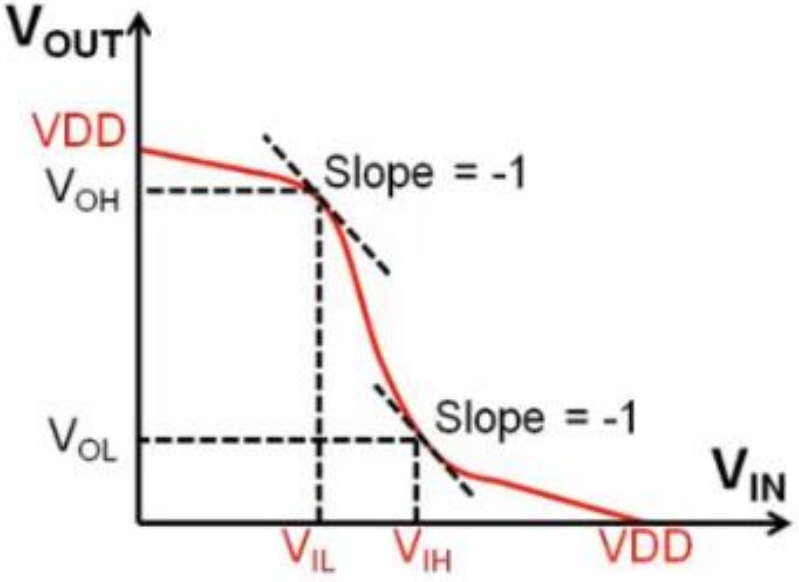
$NM_H = V_{DD} - V_{IH}$



Noise Margin: Summary

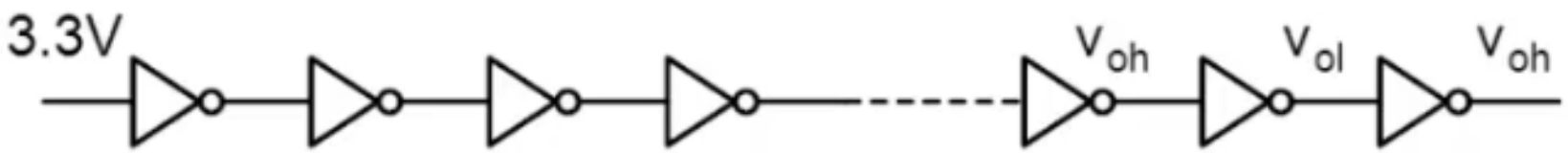


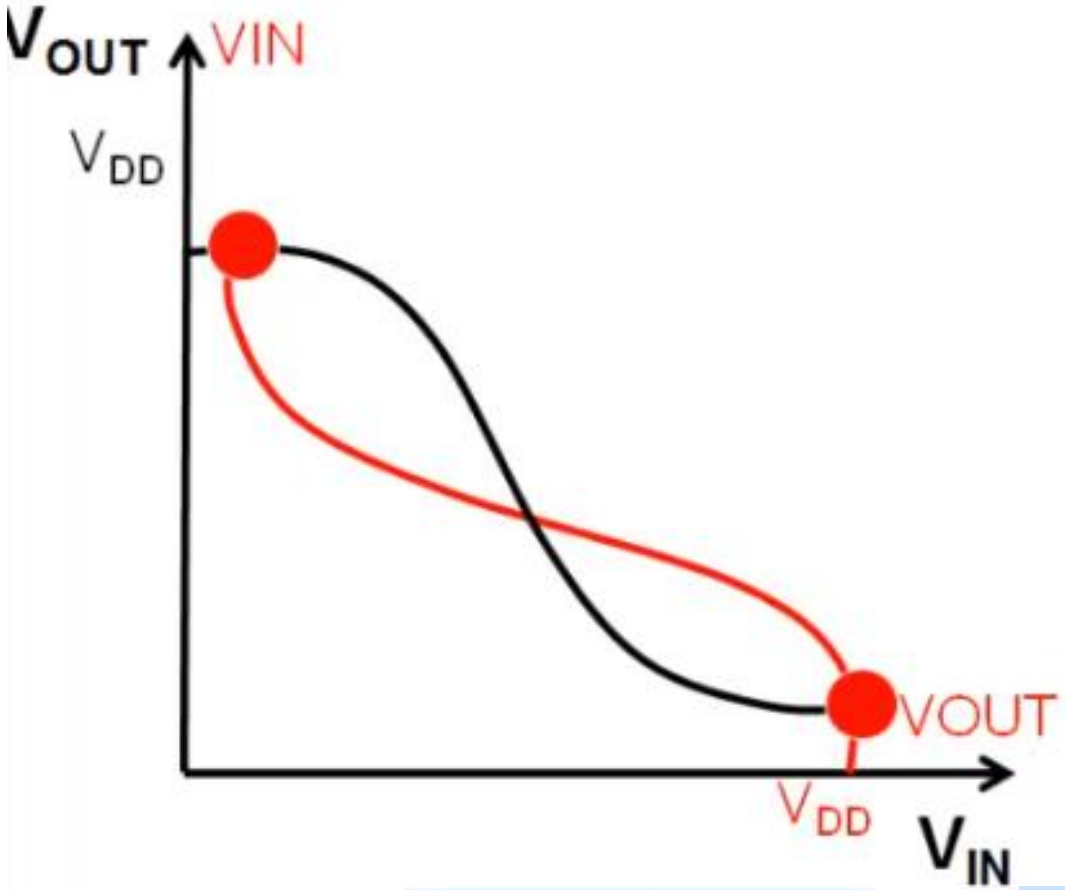


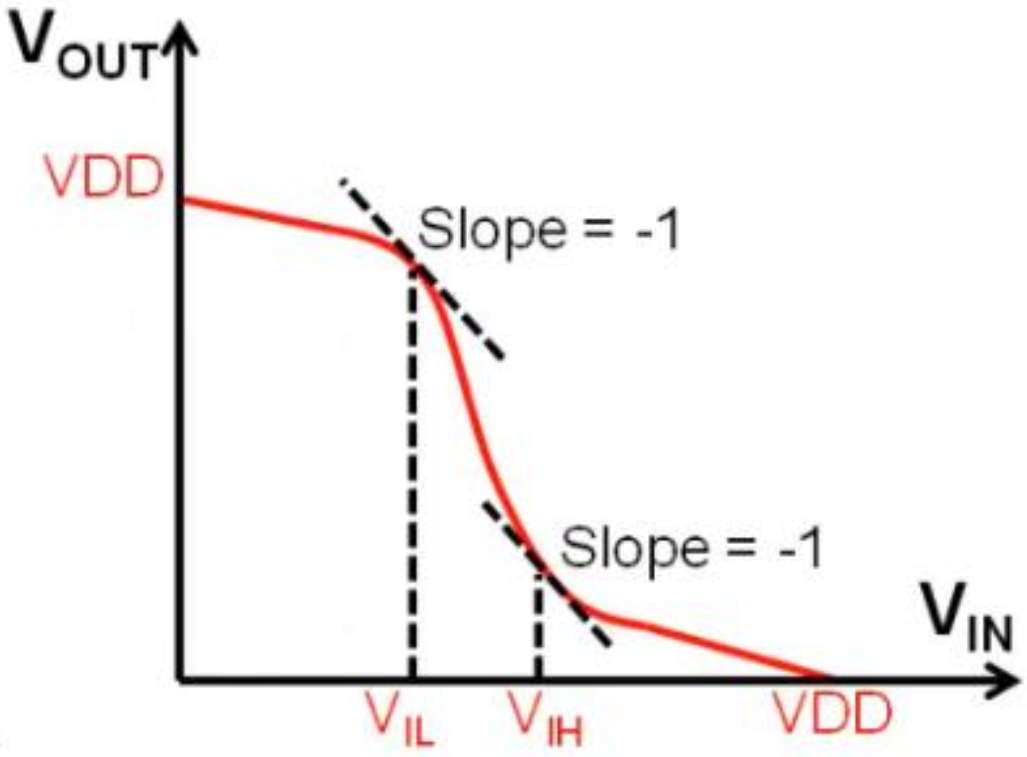


$NM_L = V_{IL} - V_{OL}$

$NM_H = V_{OH} - V_{IH}$





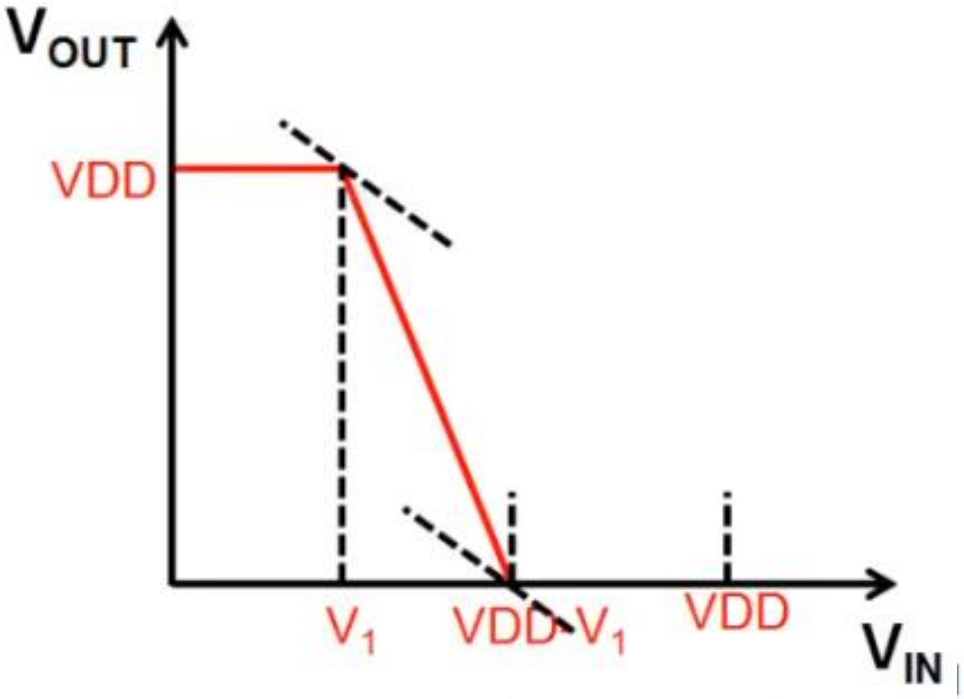


$NM_L = V_{IL}$-vol

$NM_H = v_{oh}$-V_{IH}

Example-1

$NM_L = V_{IL} - V_{OL}$ $NM_H = V_{OH} - V_{IH}$



$V_{OH} = V_{DD}$; $V_{IL} = V_1$

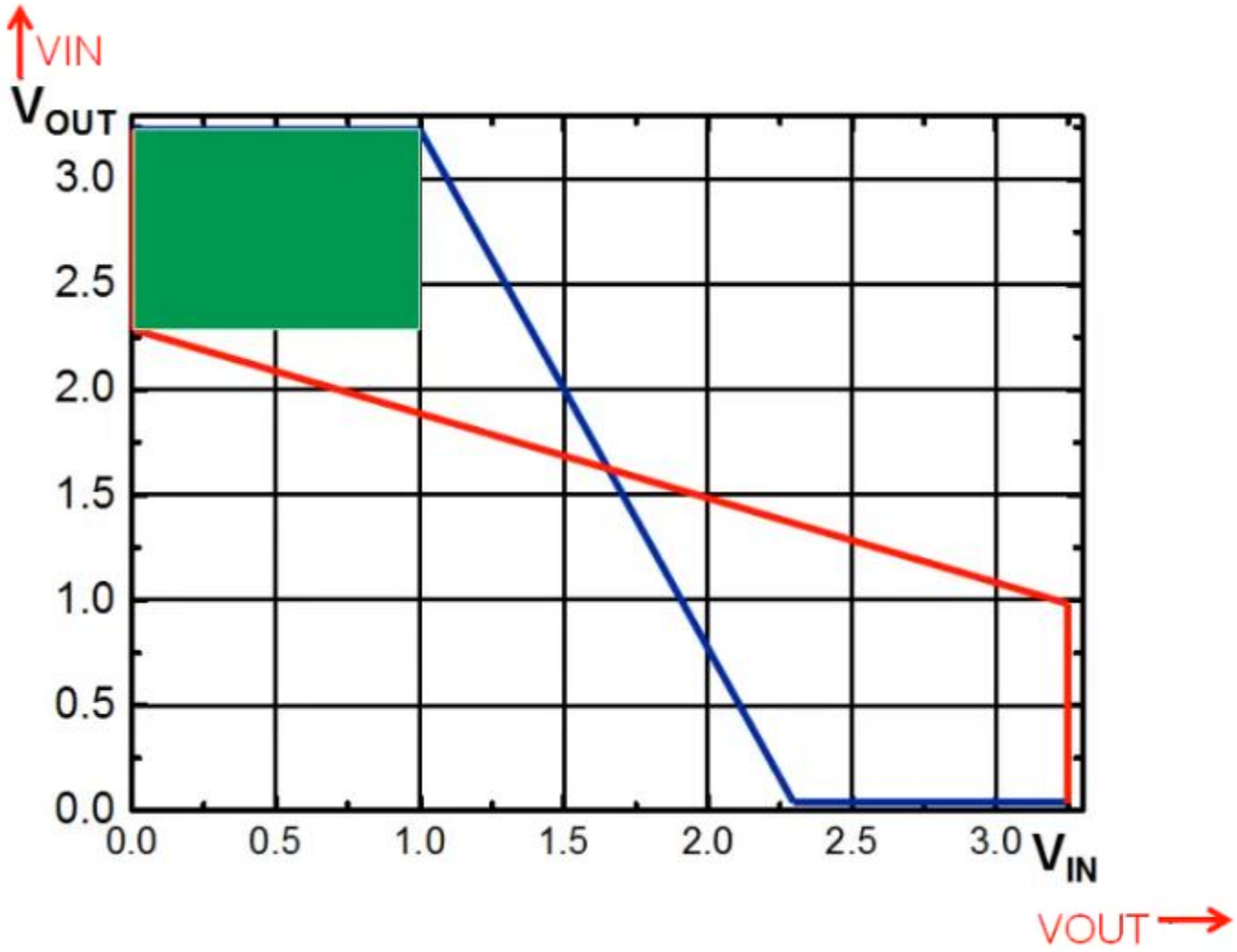
$V_{OL} = 0$; $V_{IH} = V_{DD} - V_1$

$NM_H = NM_L = V_1$

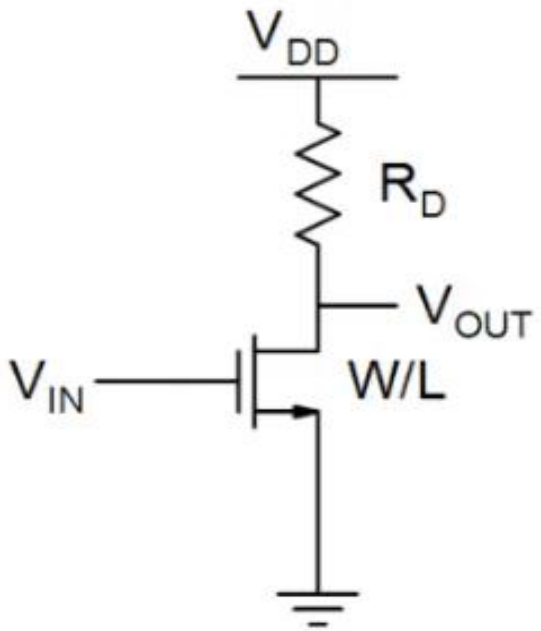
$$G_{max} = \left(\frac{V_{DD}}{V_{DD} - 2V_1} \right)$$

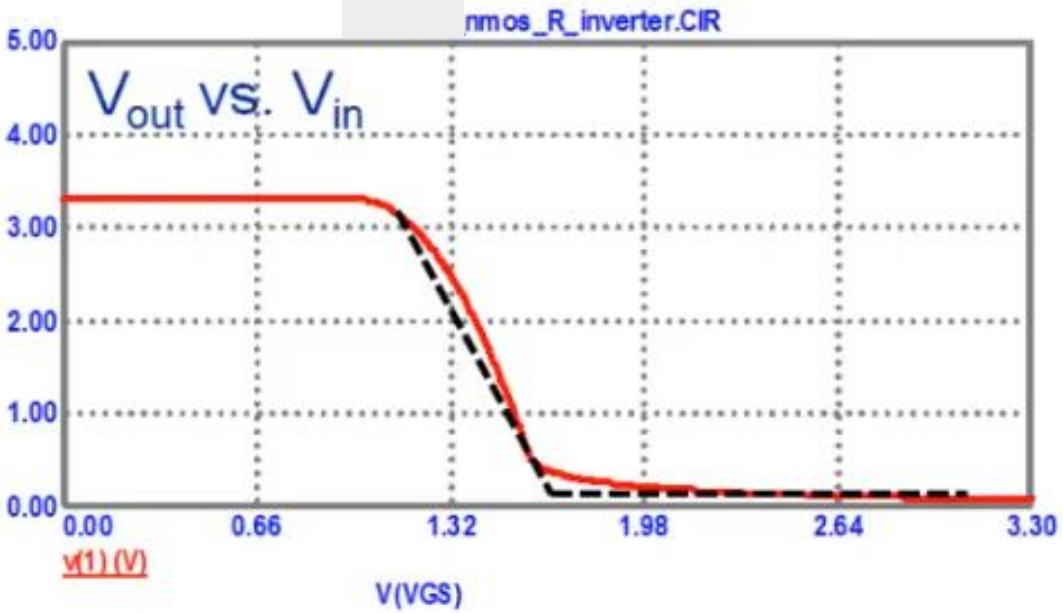
$$\frac{V_1}{V_{DD}} = 0.5\left(1 - \frac{1}{G_{max}}\right)$$

$$\frac{NM_H}{0.5V_{DD}} = \left(1 - \frac{1}{G_{max}}\right)$$


VIN
VOUT
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
0.5
1.0
1.5
2.0
2.5
3.0
VIN
VOUT

Inverter with Resistive Load





1. Area
2. Delay
3. Power
4. Noise Margins

$V_{OH} = V_{DD}; V_{OL} > 0$

$$I_{DS} \cong \frac{V_{DD}}{R_D} \cong \beta_N \times (V_{DD} - V_{THN}) \times V_{OL}$$

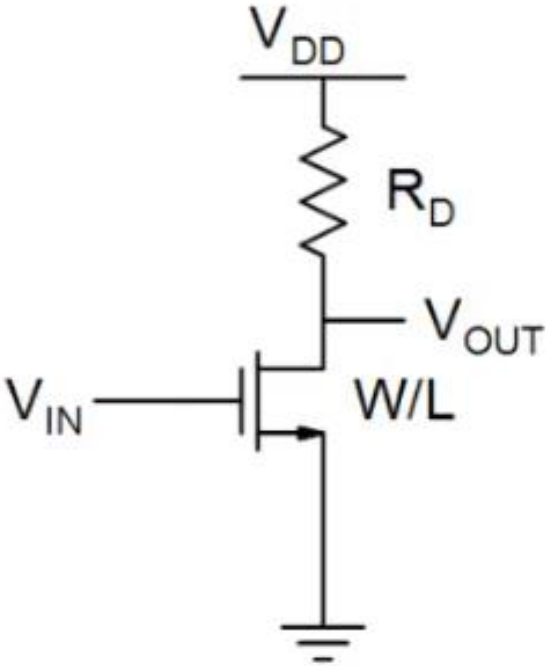
$$\Rightarrow V_{OL} = \left(\frac{V_{DD}}{V_{DD} - V_{THN}}\right) \times \frac{1}{KP_N} \times \frac{1}{(W/L) \times R_D}$$

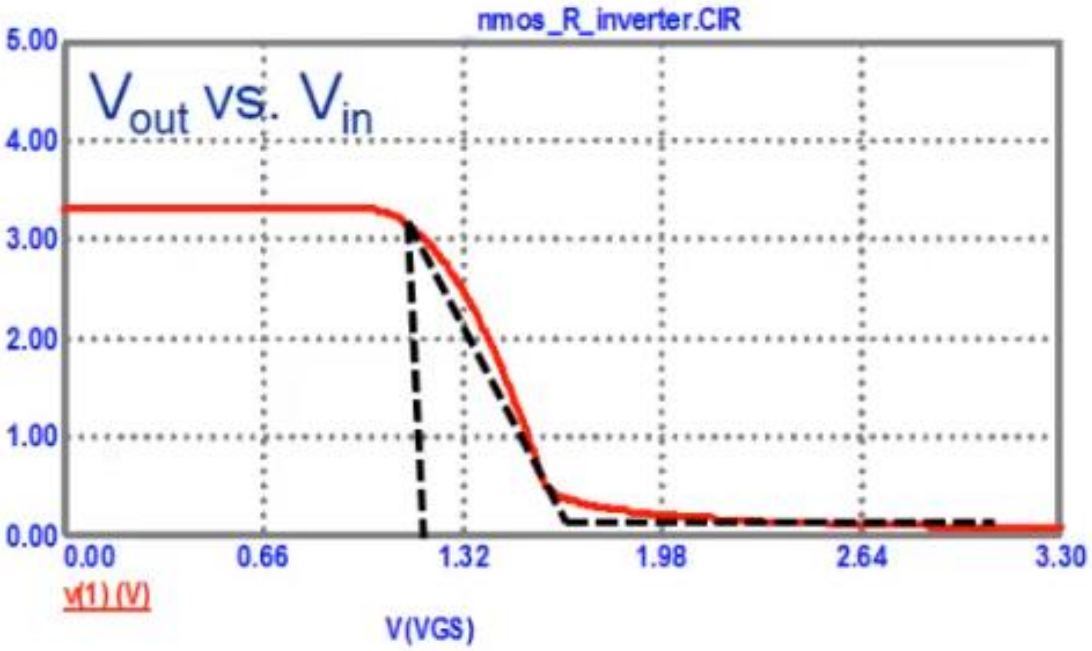
$$V_{DD} = 3.3V$$

$$KP_N = 100\mu A / V^2; V_{THN} = 1V$$

$$W/L = 4\lambda/2\lambda; R_D = 72k \Rightarrow V_{OL} \sim 0.1V$$

Inverter with Resistive Load





$KP_N = 100\mu A/V^2; V_{THN} = 1V$

$V_{DD} = 3.3V$

$W/L = 4\lambda/2\lambda; R_D = 72k \Rightarrow V_{OL} \sim 0.1V$

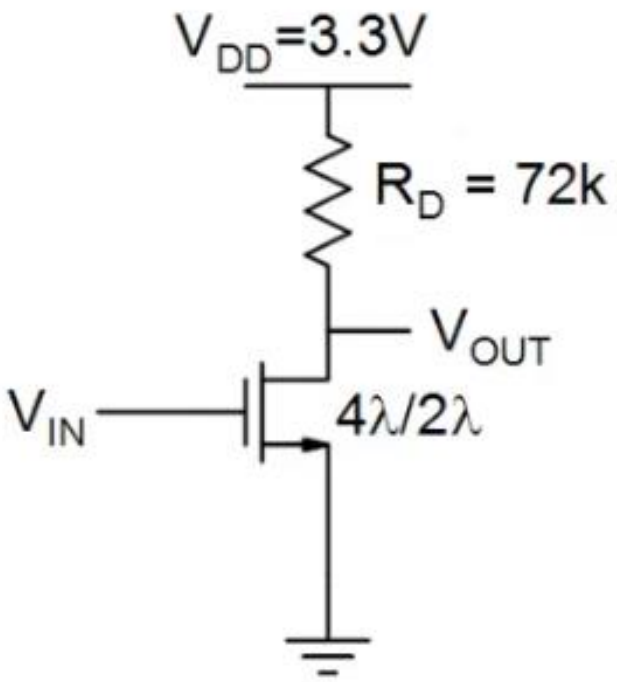
$V_{IL} \sim V_{THN} = 1V$

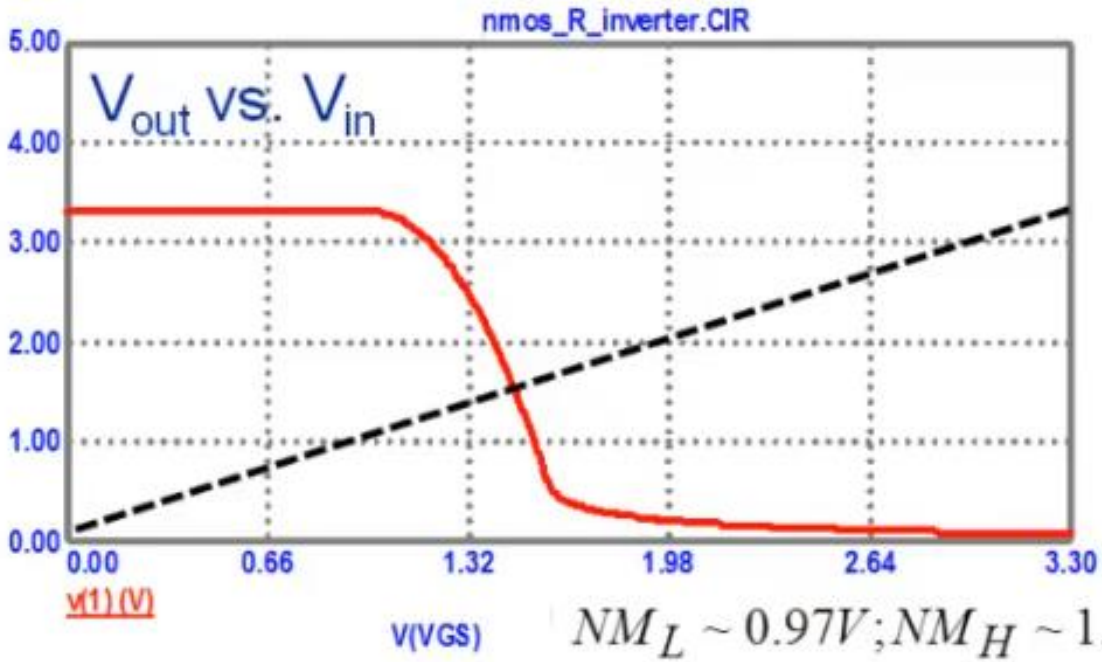
$$\frac{\partial V_{out}}{\partial V_{in}} = -1 \rightarrow V_{IL} \sim 1.07V$$

$$\boxed{NM_L = V_{IL} - V_{OL} \sim 0.97V}$$

$$\frac{NM_L}{0.5V_{DD}} = \frac{0.97}{1.65} = 0.59$$

$$\boxed{V_{IH} \sim 1.7 \Rightarrow NM_H = V_{DD} - V_{IH} \sim 1.6V}$$





$NM_L \sim 0.97V; NM_H \sim 1.6V$

$$V_{out} = V_{in}$$

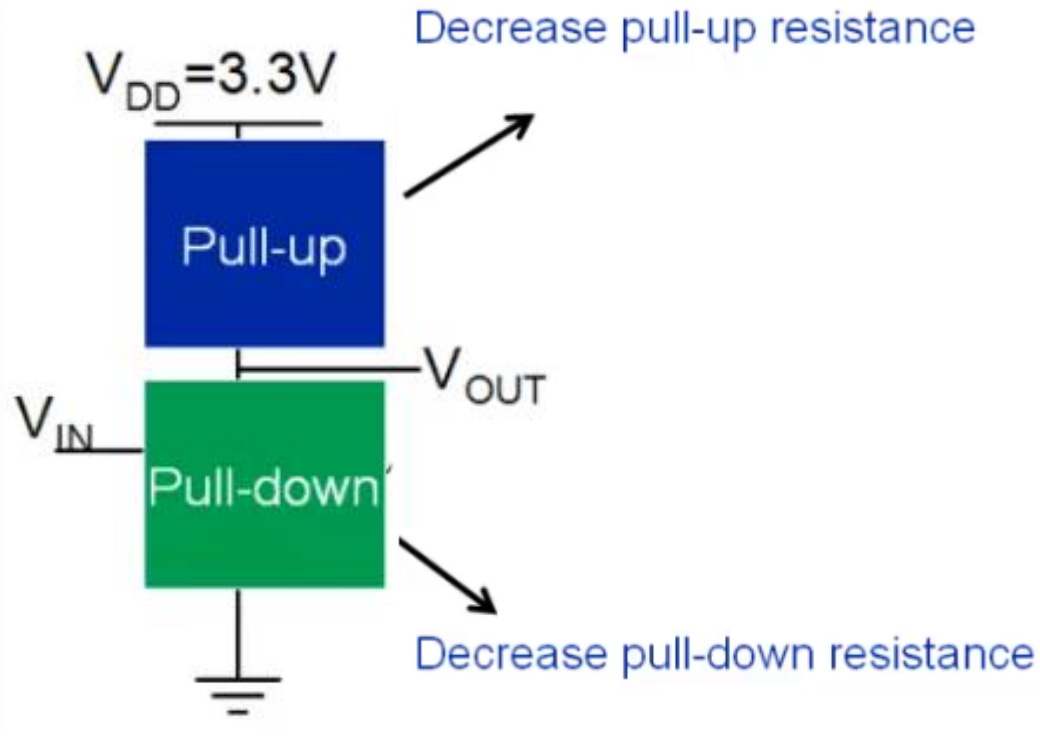
Transistor in saturation

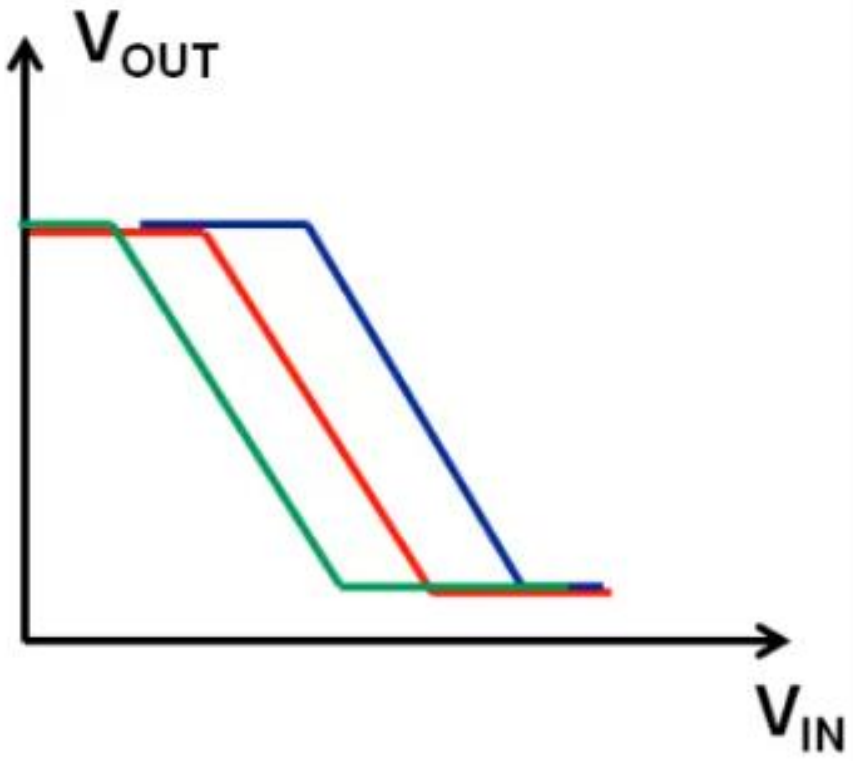
$$I_{DS} = \left(KP_N \times \frac{W}{L}\right) \times \frac{(V_{out} - V_{THN})^2}{2} = \frac{V_{DD} - V_{out}}{R_D}$$

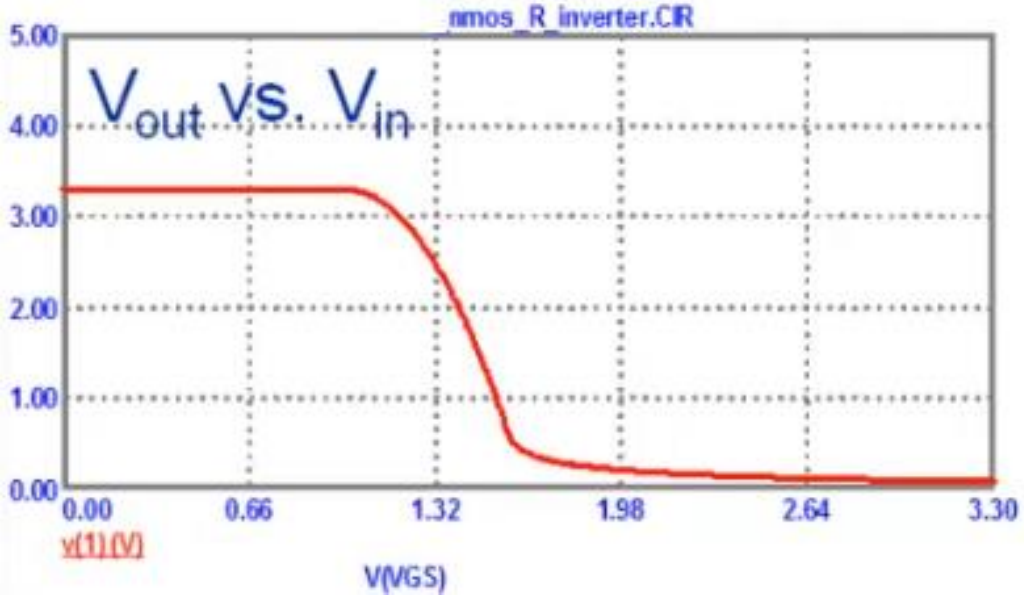
For $R_D = 72k$, $V_{out} = V_{in} = V_{inv} = 1.5V$

Shift characteristics to right to improve NM_L

1. Decrease R_D
2. Decrease W/L

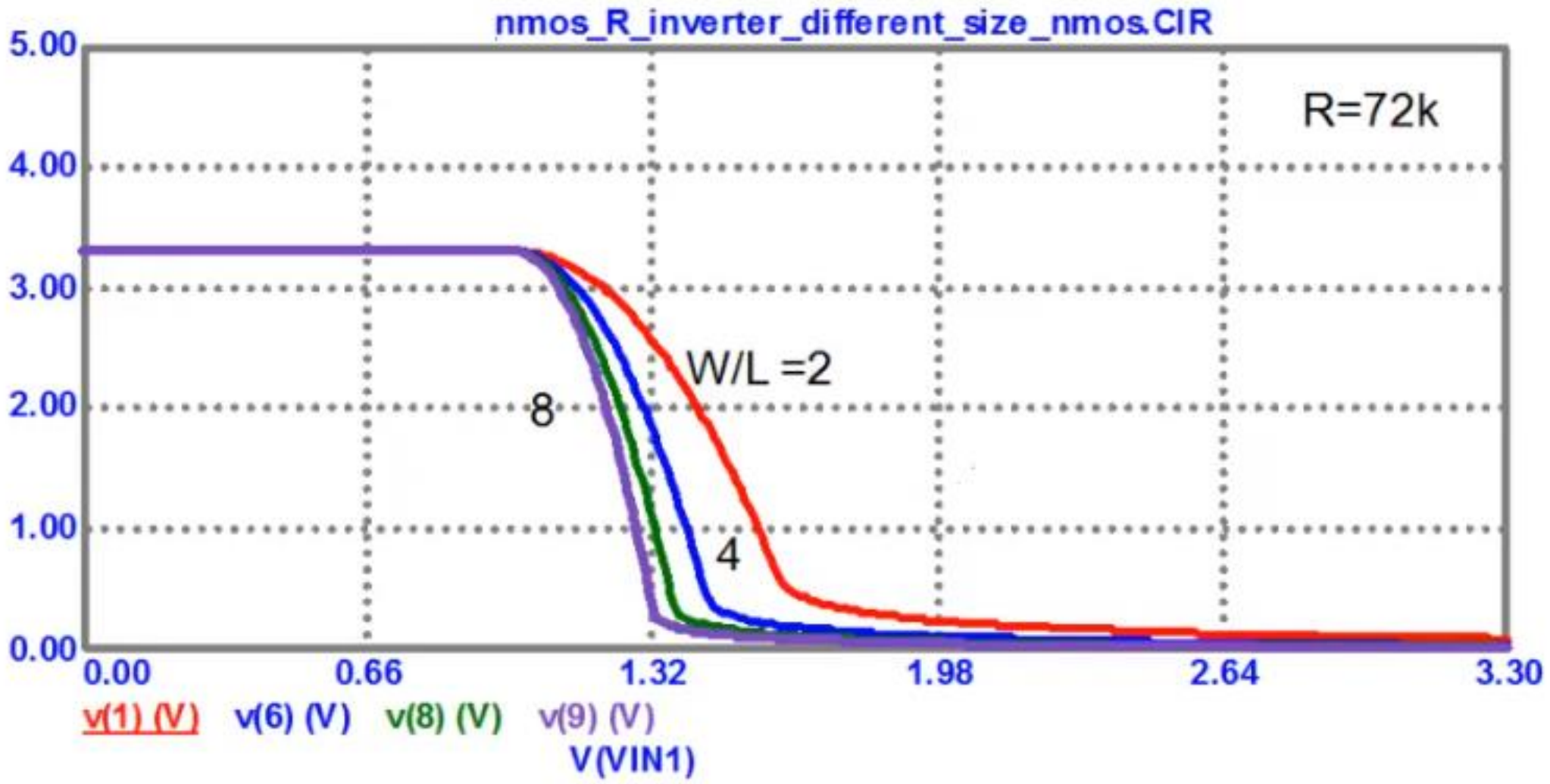




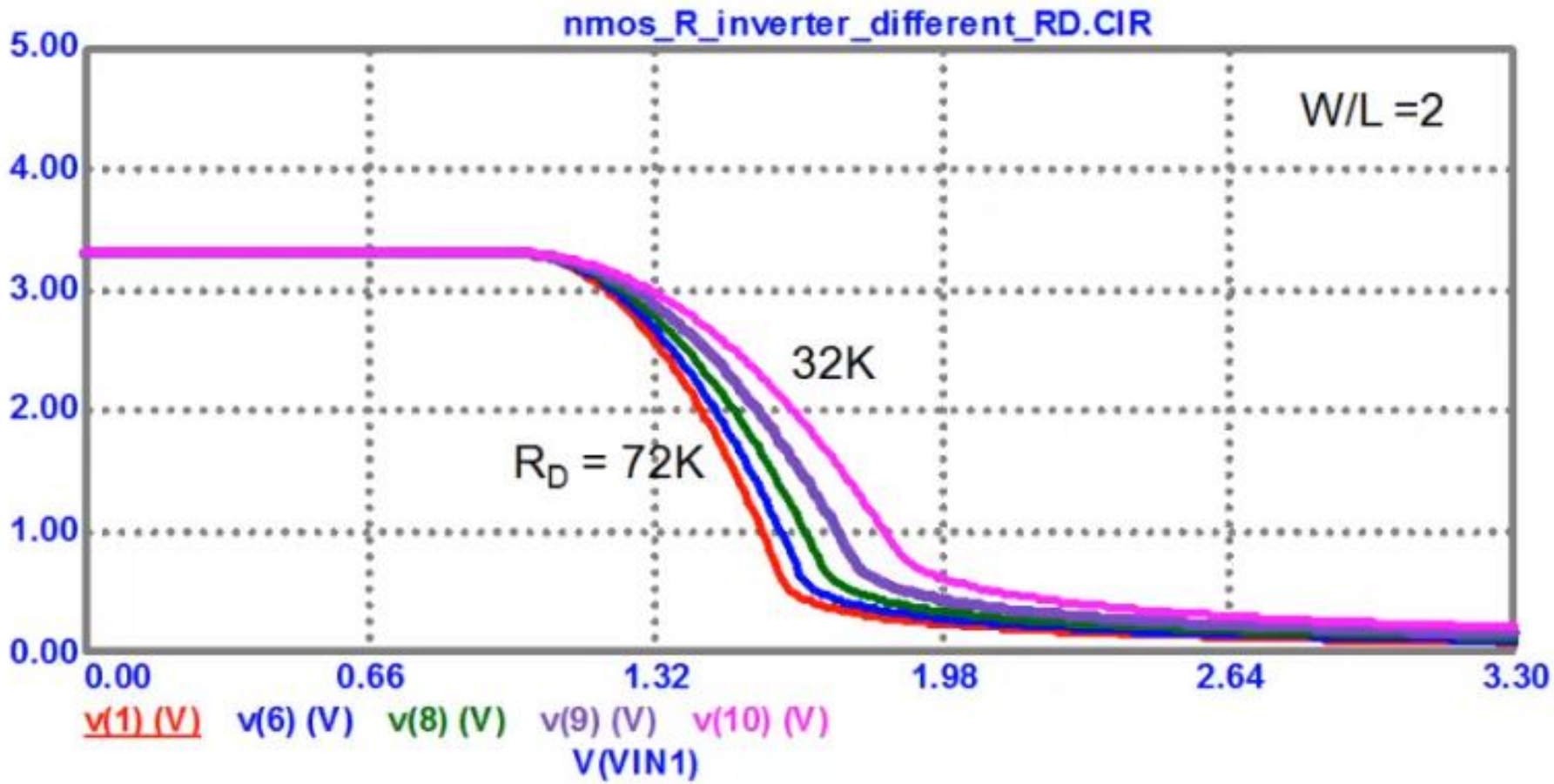


Shift characteristics to right to improve NM_L

1. Decrease R_D
2. Decrease W/L



Decreasing the pull down resistor shifts characteristics left



$R_D = 72k \Rightarrow V_{OL} = 0.1V; V_{OH} = 3.3V$

$V_{IL} = 1.07V; V_{IH} = 1.7V$

$NM_L \sim 0.97V; NM_H \sim 1.6V$

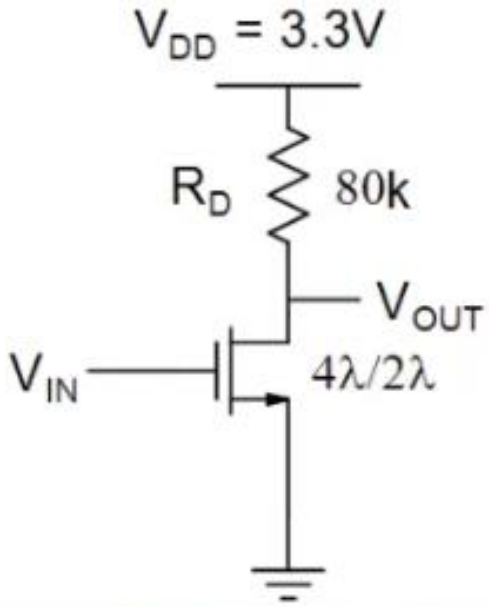
$V_{inv} = 1.5V$

$R_D = 32k \Rightarrow V_{OL} = 0.22V; V_{OH} = 3.3V$

$V_{IL} = 1.16V; V_{IH} = 2V$

$NM_L \sim 0.94V; NM_H \sim 1.3V$

$V_{inv} = 1.72V$



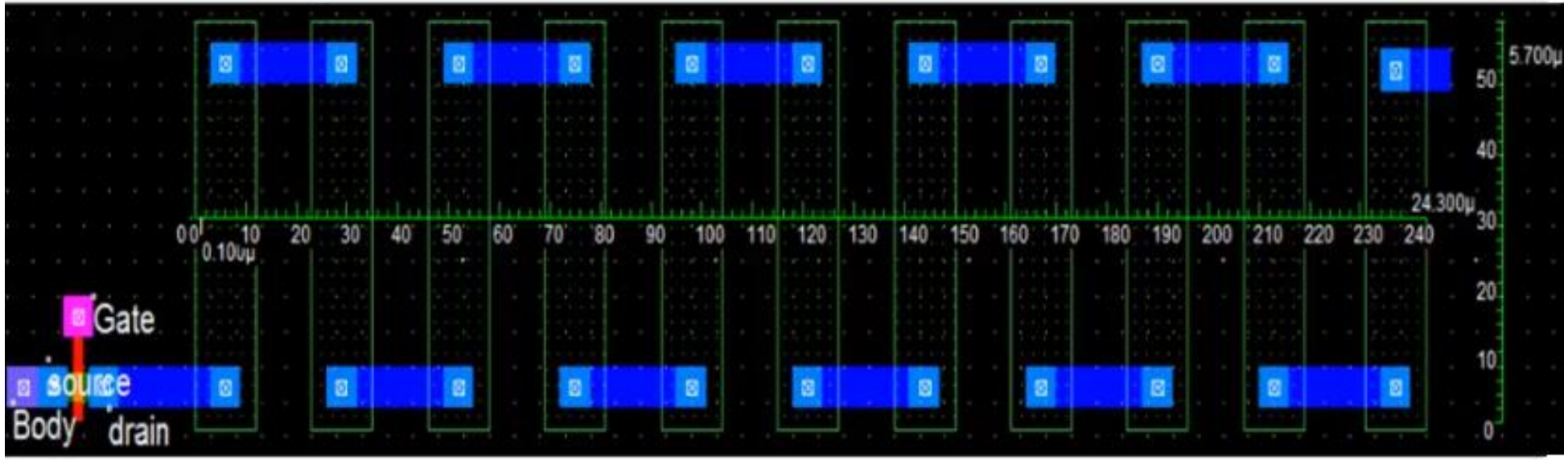
$$NM_L \sim 0.97V; NM_H \sim 1.6V$$

$$R_D = 10k$$

$$W/L = 4\lambda/2\lambda; R_D = 10k \Rightarrow V_{OL} \sim 0.72V$$

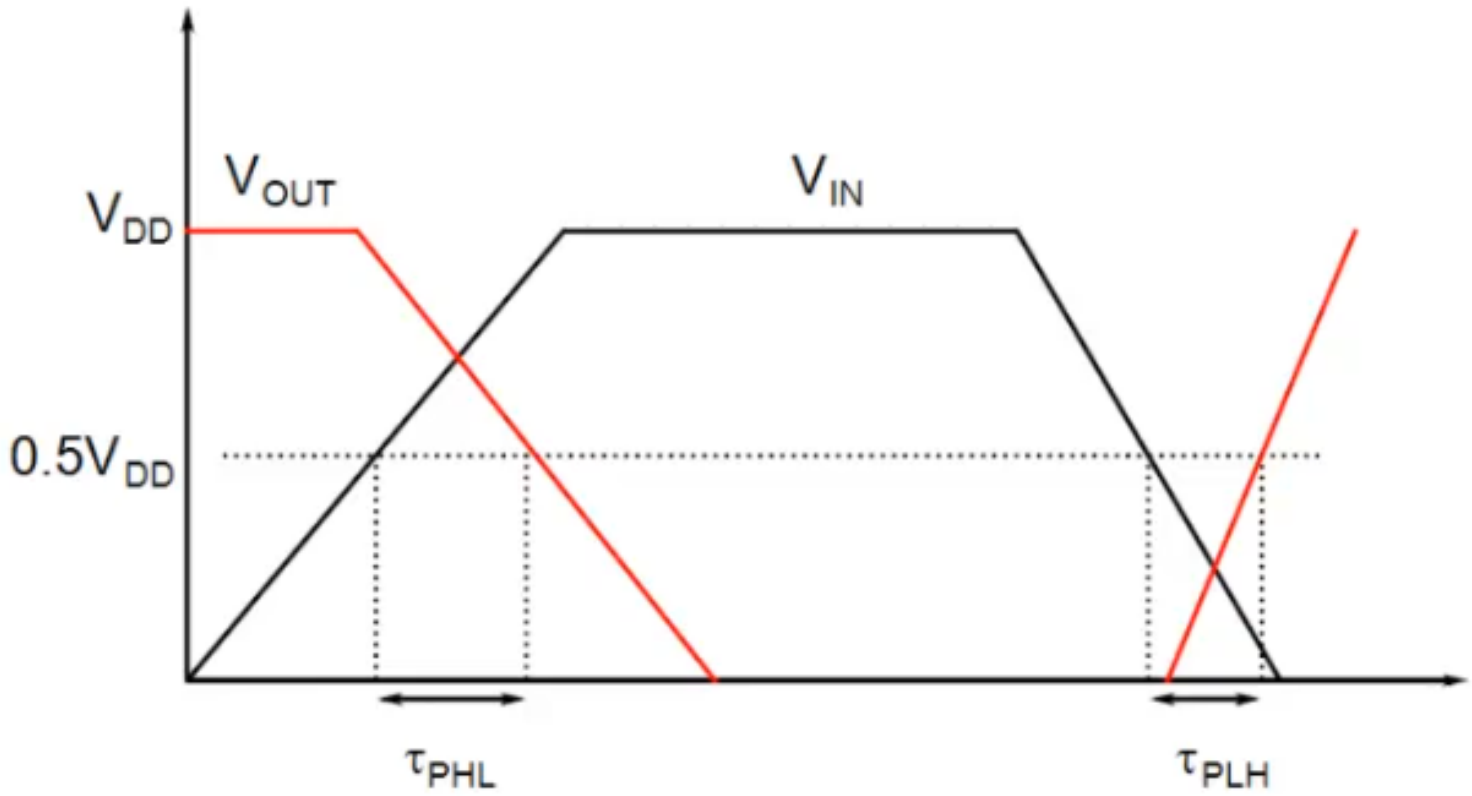
$$NM_L = V_{IL} - V_{OL} \sim 0.28V$$

1. Area
2. Delay
3. Power
4. Noise Margins

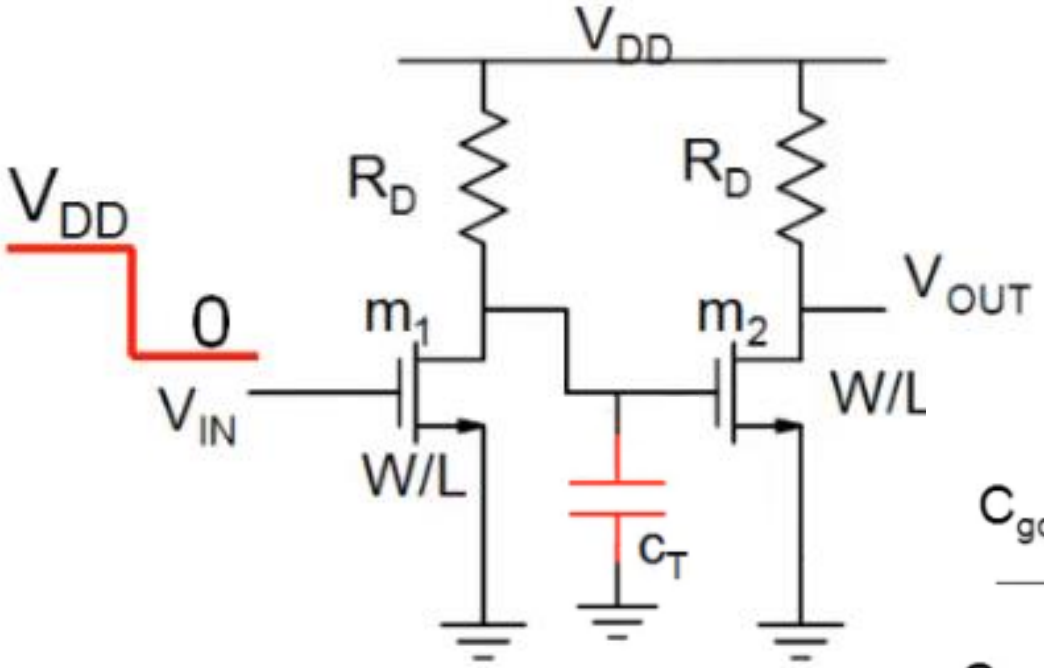


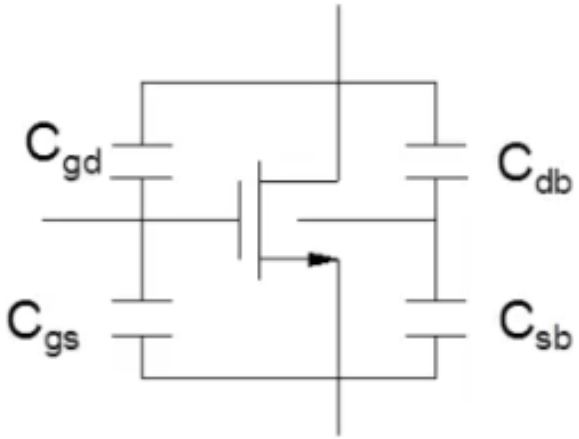
$$\frac{A_{RD}}{A_{tr1}} \sim 35$$

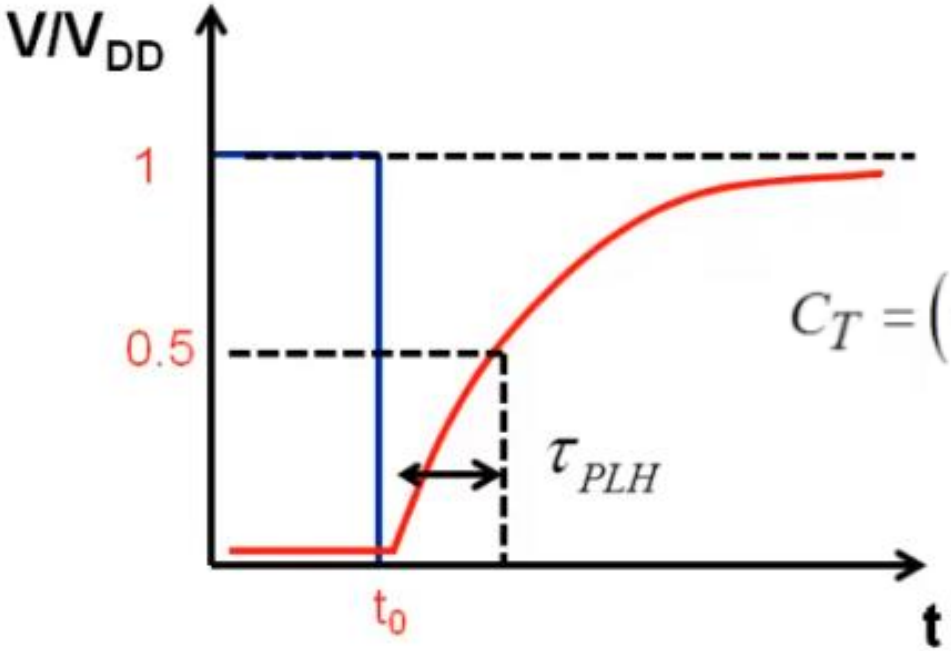
Propagation Delay



$$\tau_R \; ; \tau_F \; ; \tau_{PHL} \; ; \tau_{PLH}$$

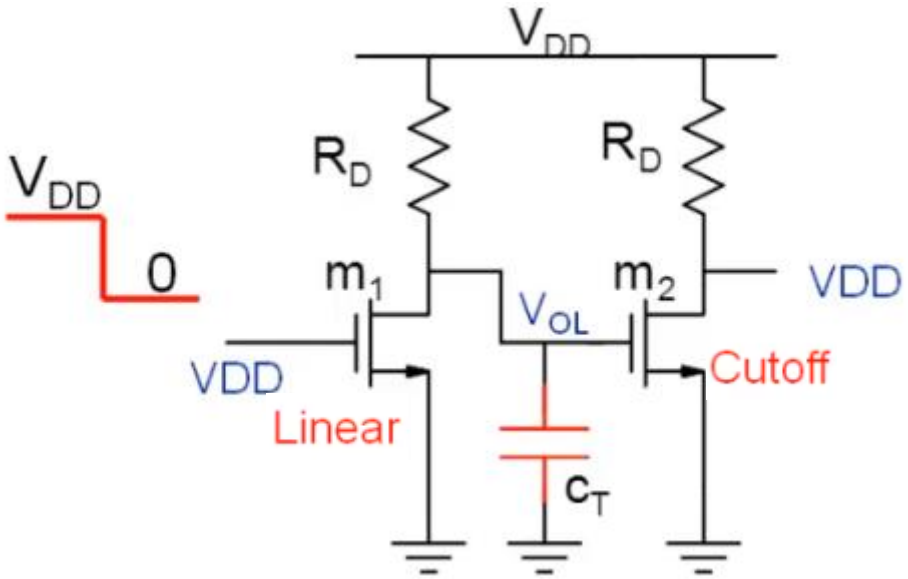


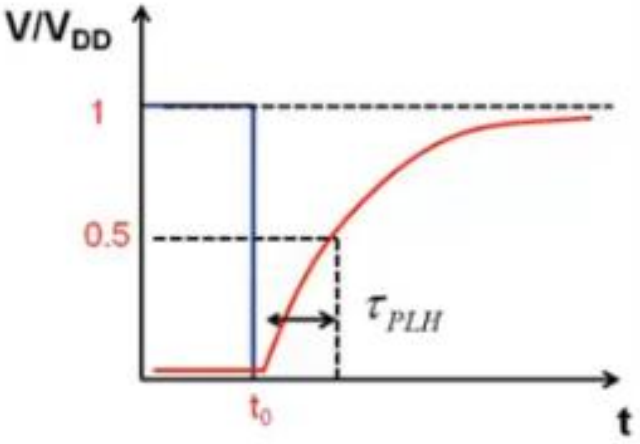


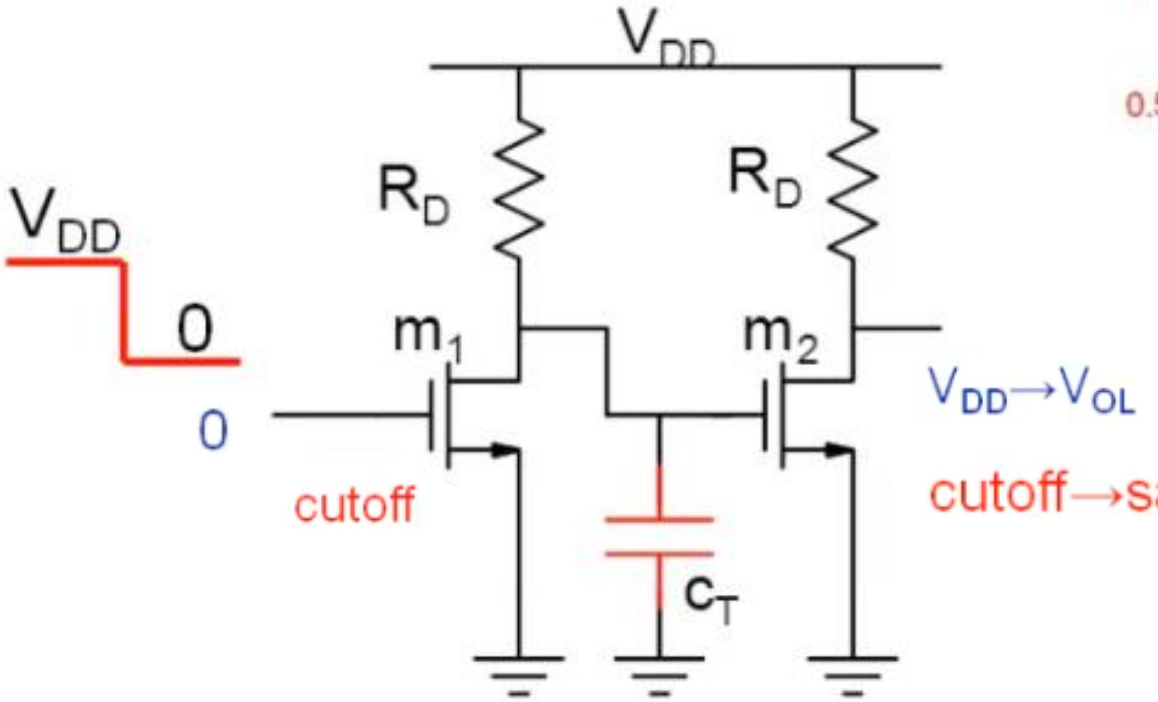


$$C_T = \left(C_{gd1} + C_{db1}\right) + \left(C_{gs2} + C_{gd2}\right)$$

Parameter	NMOS	PMOS
V_{THNO}(V)	0.69	-0.869
λ (for L = 1μm)	0.015	0.065
γ	0.696	0.456
KP (μA/V²)	100	40
CGSO (pF)	281	252
CGDO(pF/m)	281	252
CJ (μF/m²)	467.7	932
PB	0.9	0.92
MJ	0.5	0.466
CJSW(pF/m)	616.95	181
MJSW	0.235	0.5

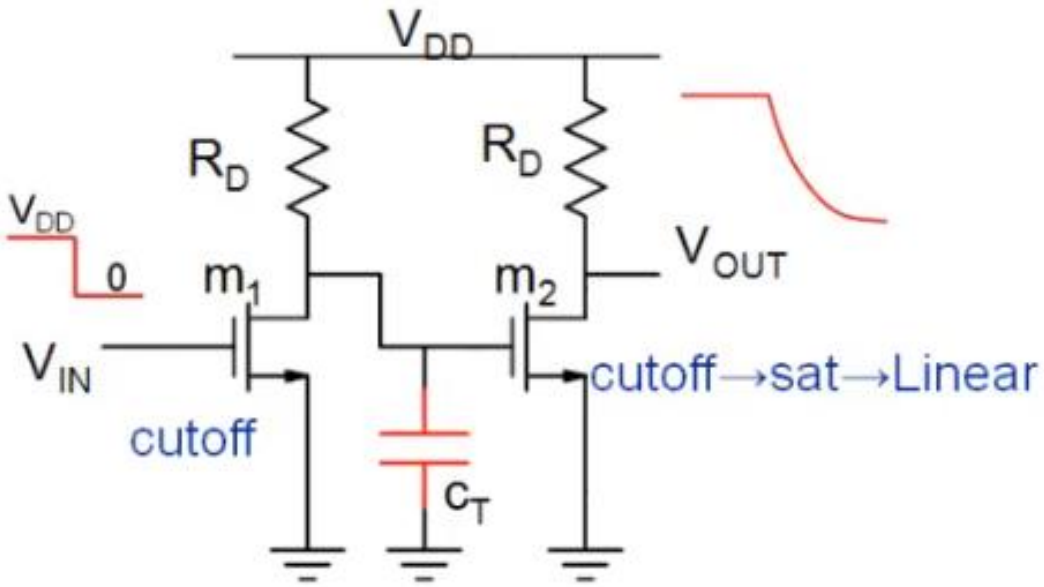


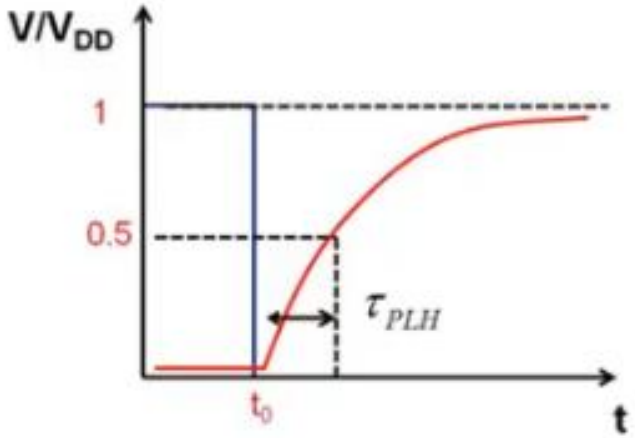


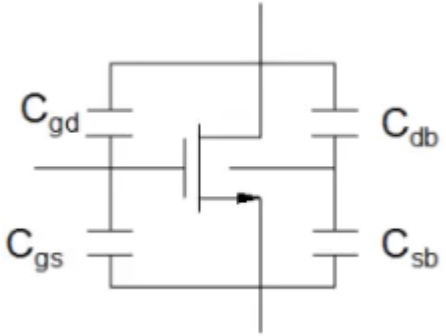


$V_{DD} \rightarrow V_{OL}$

cutoff→sat→Linear





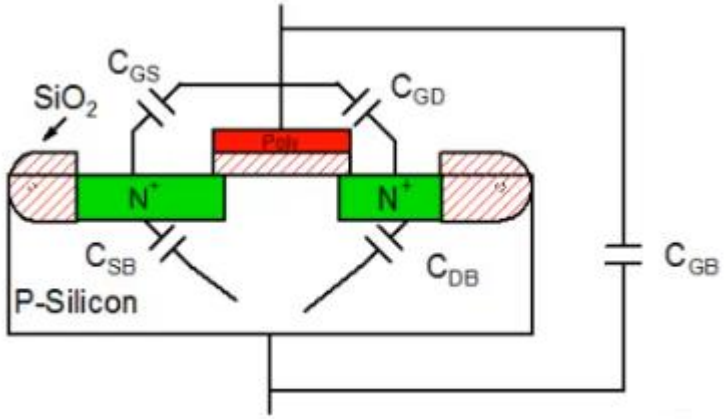


$$C_T = \left(C_{gd1} + C_{db1}\right) + \left(C_{gs2} + C_{gd2}\right)$$

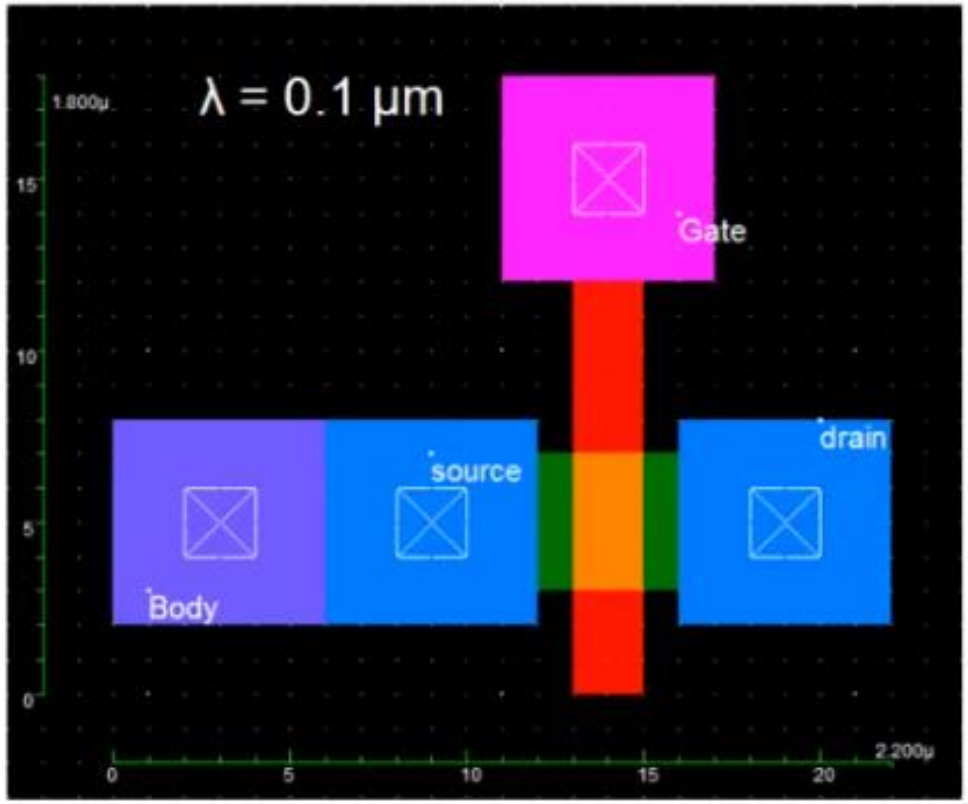
$$C_{gd1} = C_{GDO}.W_1 \qquad C_{gd2} = C_{GDO}.W_2$$

$$C_{db1} = \frac{C_{jsw}.P_D}{\left(1 + \frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}} + \frac{C_j.A_D}{\left(1 + \frac{V_{DB}}{P_B}\right)^{M_j}}$$

$V_{DB} = 0 \rightarrow 0.5VDD$



$$C_{gs1} \cong \left(C_{gso}.W\right) \rightarrow \frac{2}{3} C_{ox'}.W.L + C_{gso}.W$$



$$A_D = 4 \times 1 + 6 \times 6 = 40;$$

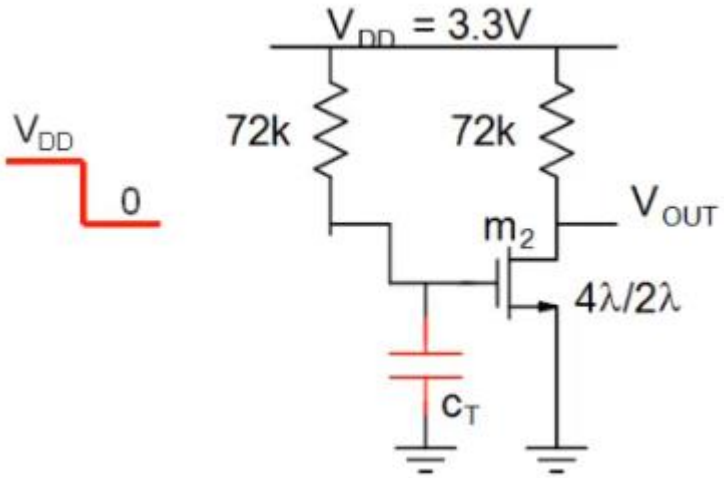
$$P_D = 2 \times (1 + 1 + 6) + 6 = 22$$

$V_{DB} = 0$

$$C_{db1} = \frac{C_{jsw}.P_D}{\left(1 + \frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}} + \frac{C_j.A_D}{\left(1 + \frac{V_{DB}}{P_B}\right)^{M_j}} = 5.7\,fF$$

~4fF

1.7fF

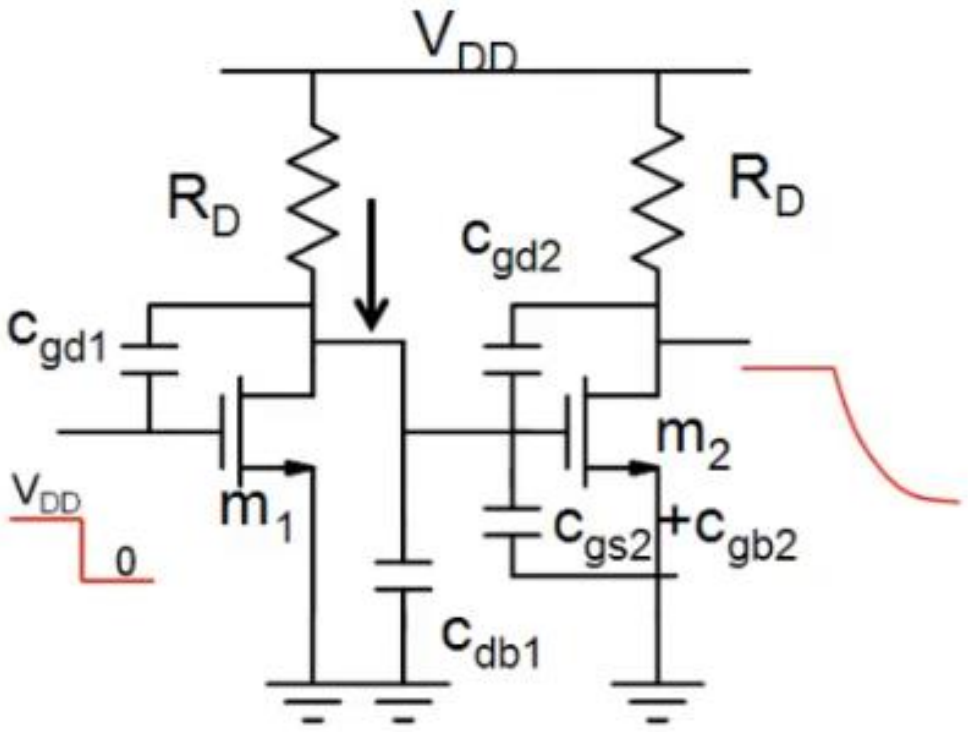


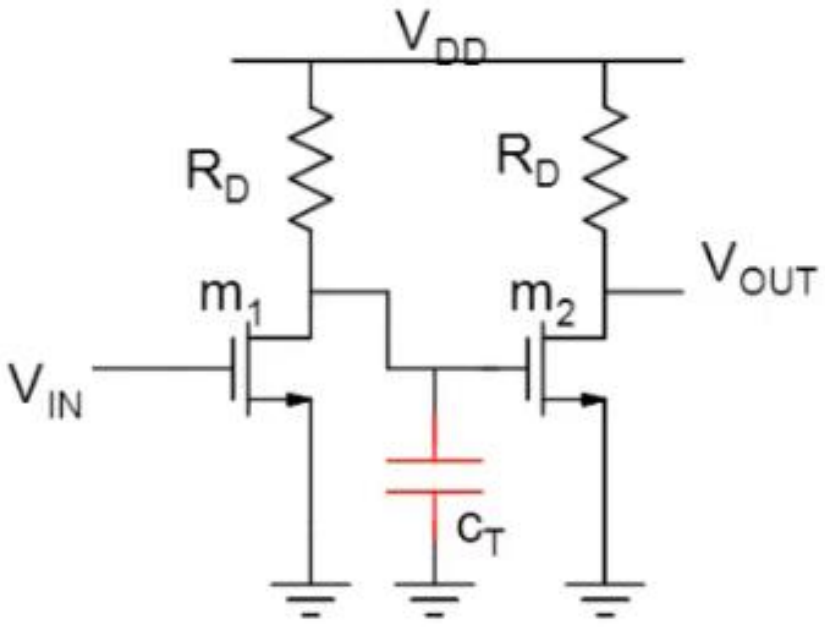
$$C_T = \left(C_{gd1} + C_{db1}\right) + \left(C_{gs2} + C_{gd2}\right)$$

$$C_{To} = 8.5\,fF$$

$$\tau_{PLH} \cong 0.693 \times R_D \times \tilde{C}_T$$
$$= 424\,ps$$

$\tau_{PLH} \cong 137\,ps$ if C_{db} is not considered





M1 : linear →cutoff

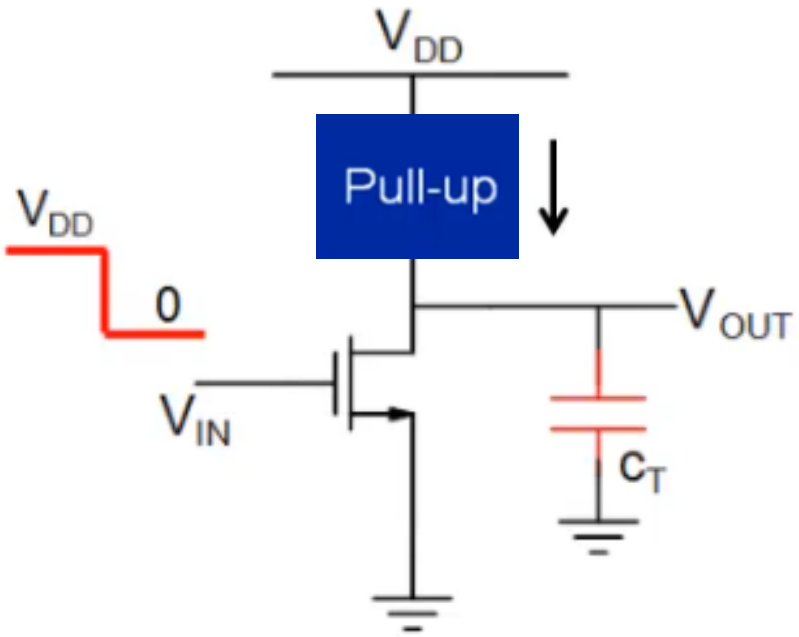
M2: cutoff→sat→Linear

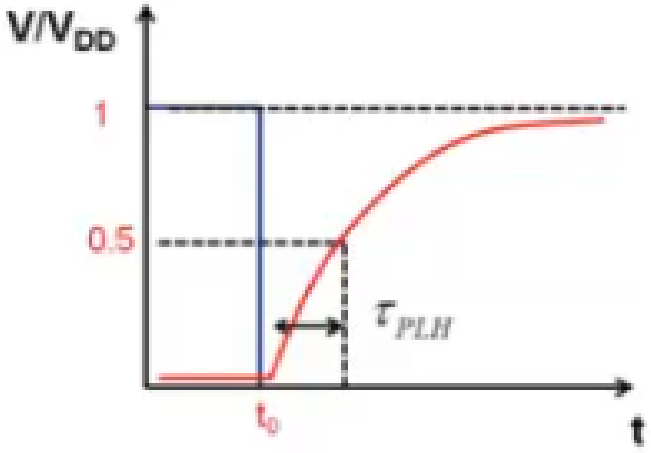
$$C_T = \left(C_{gd1} + C_{db1}\right) + \left(C_{gs2} + C_{gd2} + C_{gb2}\right)$$

$$I = \sum \frac{dQ_j}{dt}$$

$$I = C_{gd1} \times \frac{d\left(V_{D1} - V_{G1}\right)}{dt} + C_{gd2} \times \frac{d\left(V_{D1} - V_{D2}\right)}{dt} + C_{db1} \times \frac{dV_{D1}}{dt} + \left(C_{gs2} + C_{gb2}\right) \times \frac{dV_{D1}}{dt}$$

$$I = \left(C_{gd1} \times \left(1 - \overset{\sim -1}{\frac{dV_{G1}}{dV_{D1}}}\right) + C_{gd2} \times \left(1 - \overset{\sim -1}{\frac{dV_{D2}}{dV_{D1}}}\right) + C_{db1} + C_{gs2} + C_{gb2} \right) \times \frac{dV_{D1}}{dt}$$

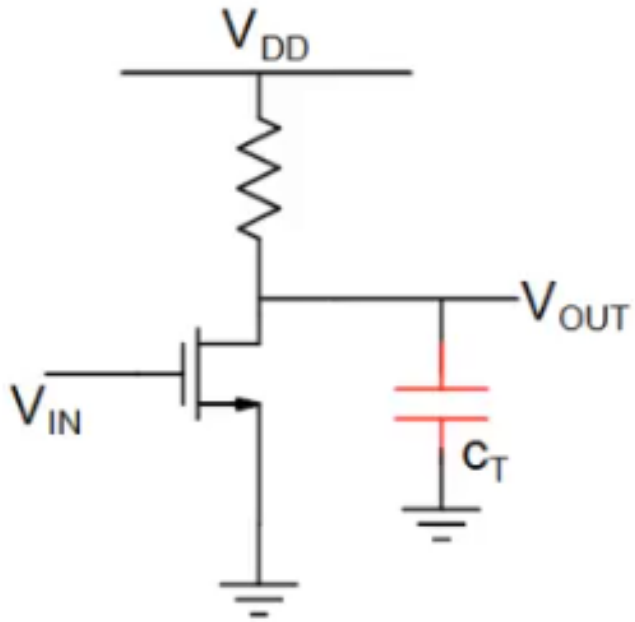




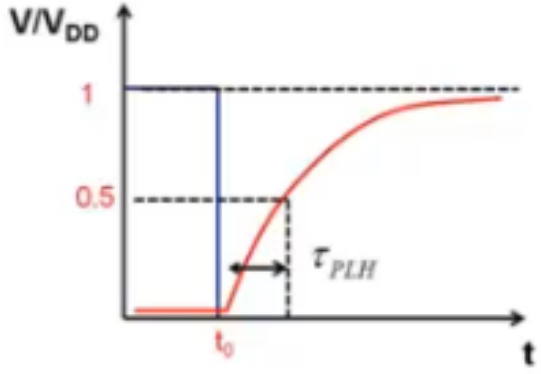
$$I_{pu} = C_T \times \frac{dV_{out}}{dt}$$

$$\tau_{plh} = \int_0^{0.5V_{DD}} \frac{C_T}{I_{pu}} \times dV_{out}$$

$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$$



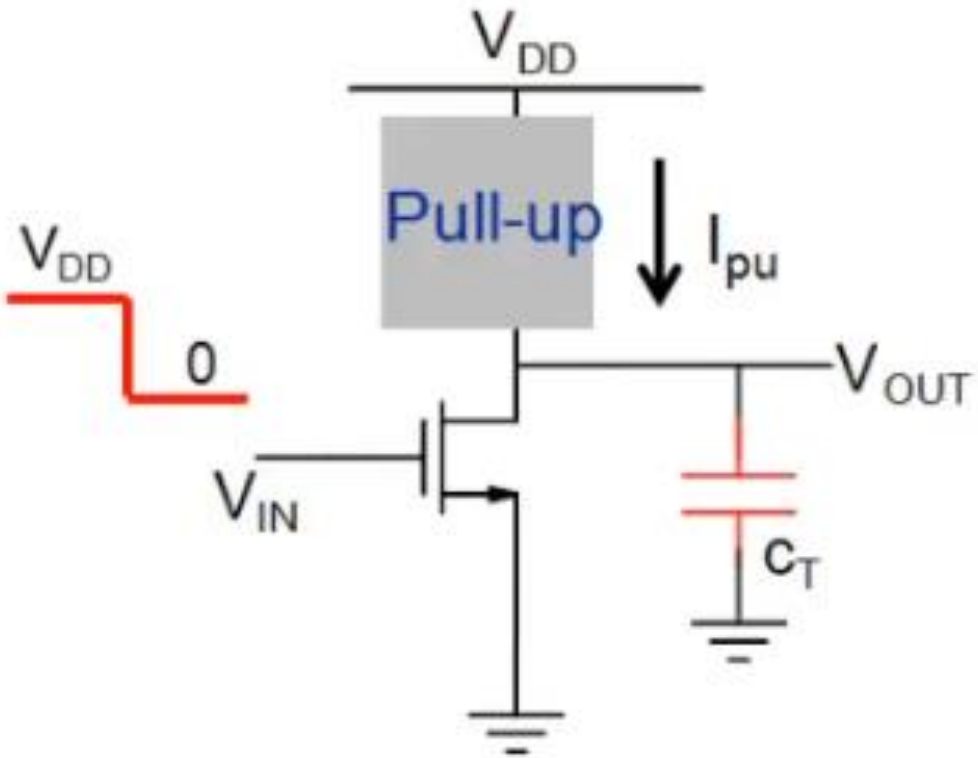
$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$$

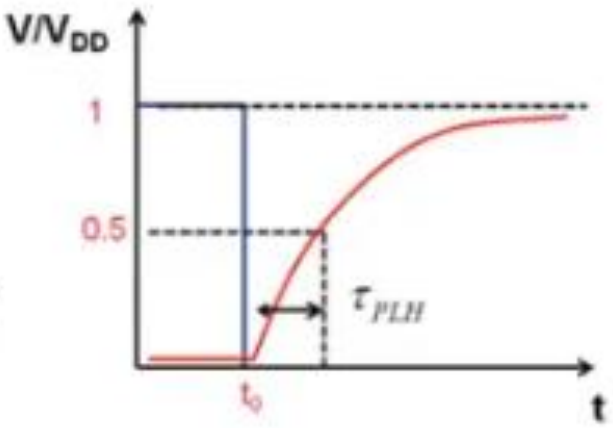


$$I_{pu} = \frac{V_{DD}}{R_D} \rightarrow \frac{0.5V_{DD}}{R_D}$$

$$\tilde{I}_{pu} \cong 0.75\frac{V_{DD}}{R_D}$$

$$\tau_{plh} \cong 0.67 \times R_D \tilde{C}_T$$



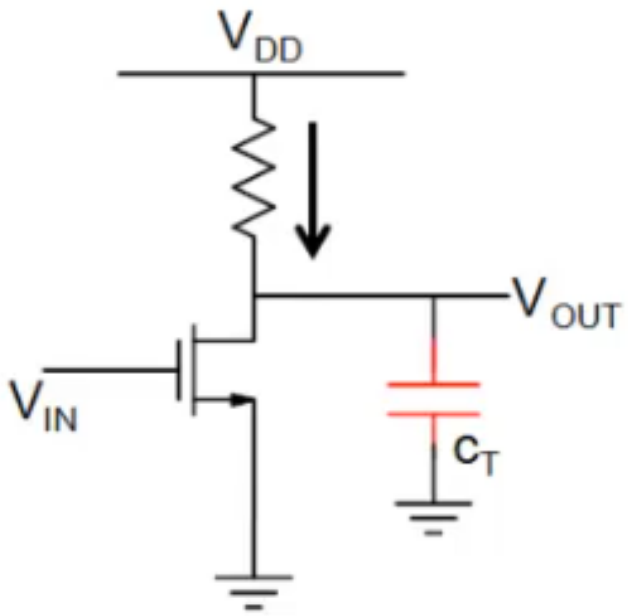


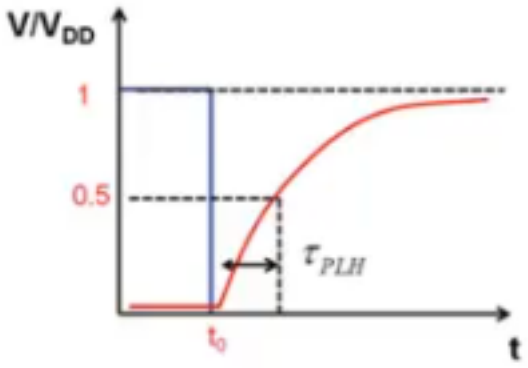
$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$$

$$I_{pu} \propto V_{DD}^{m}; m > 1 \qquad P_{diss} \propto V_{DD}$$

In general delay decreases with increase in supply voltage

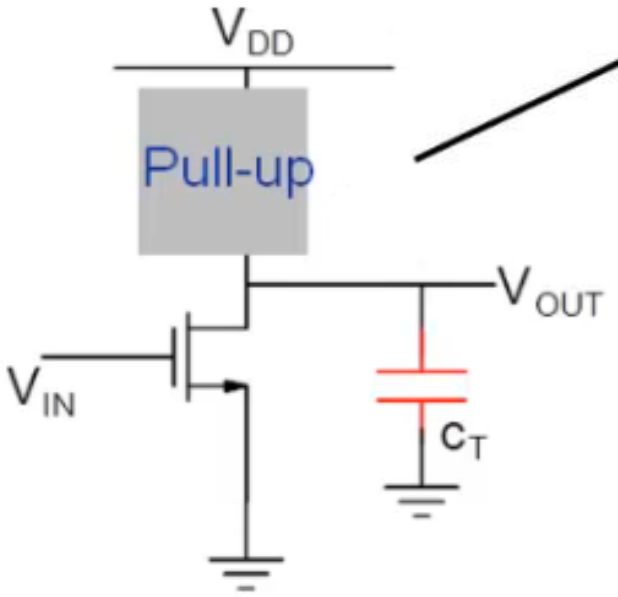
There is a power delay tradeoff





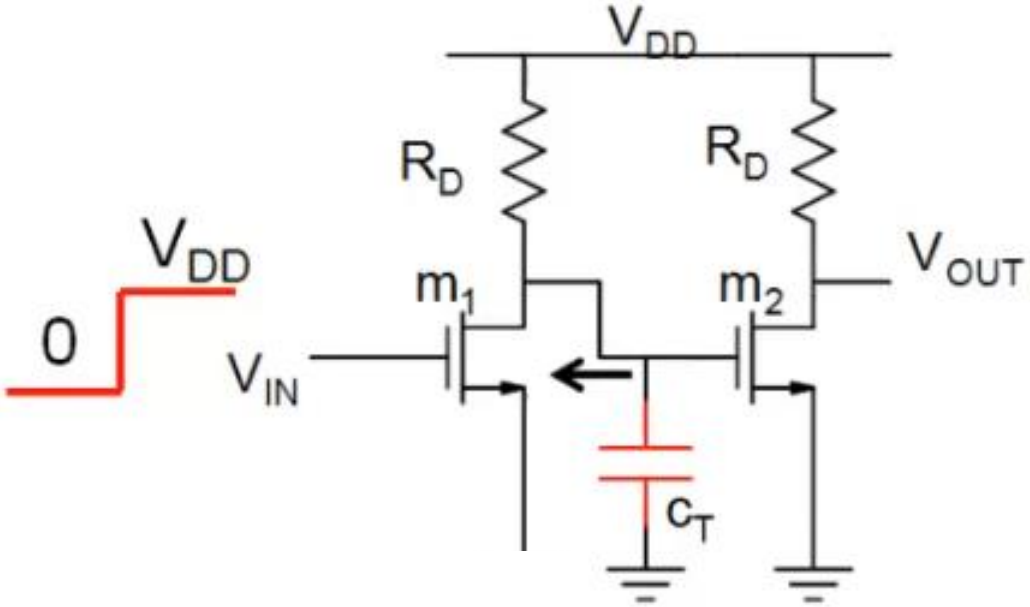
$$I_{pu} = \frac{V_{DD}}{R_D} \rightarrow \frac{0.5V_{DD}}{R_D}$$

$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$$



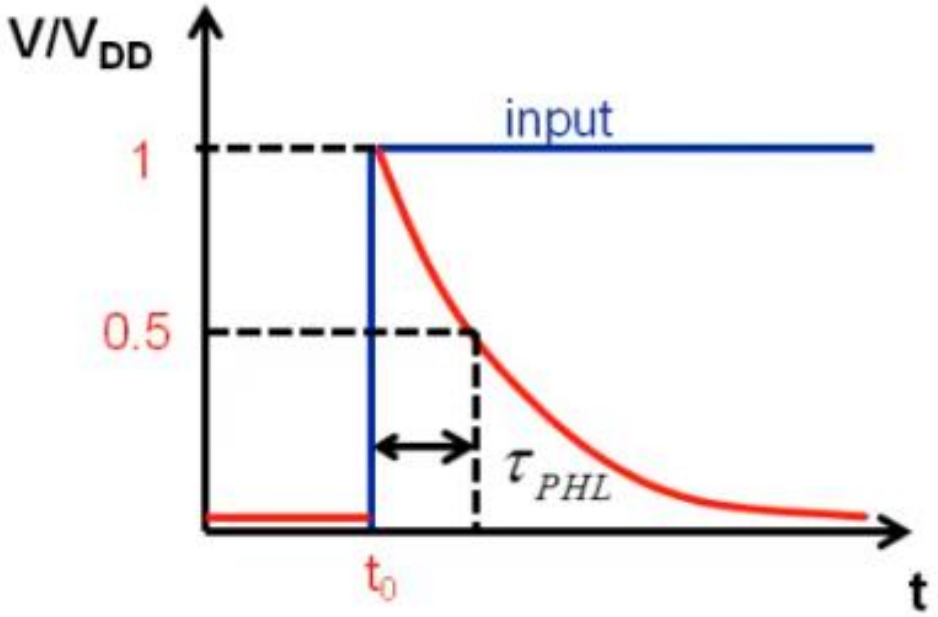
Ideally should be like a current source which switches on during charging.

High to Low delay propagation Delay



$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{dis.}}$$

$$I_{dis.} = I_{DS1} - \frac{V_{DD} - V_{D1}}{R_D}$$

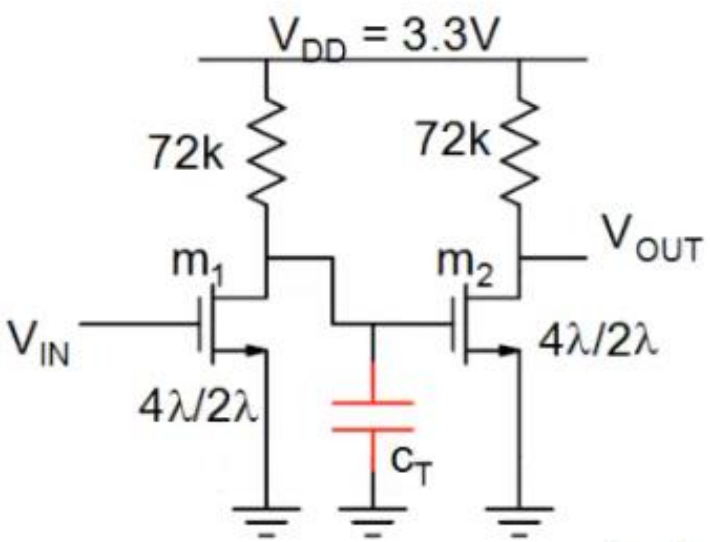


M1 : sat (3.3→2.3)
lin. (2.3→1.65)

$$I_{DS}(t=0) = \left(KP_N \times \frac{W}{L}\right) \times \frac{(V_{DD} - V_{THN})^2}{2}$$

$$I_{DS}(t=\tau_{phl}) = \left(KP_N \times \frac{W}{L}\right) \times \left((V_{DD} - V_{THN})\frac{V_{DD}}{2} - \frac{V_{DD}^2}{4}\right) - \frac{V_{DD}}{2R_D}$$

High to Low delay propagation Delay



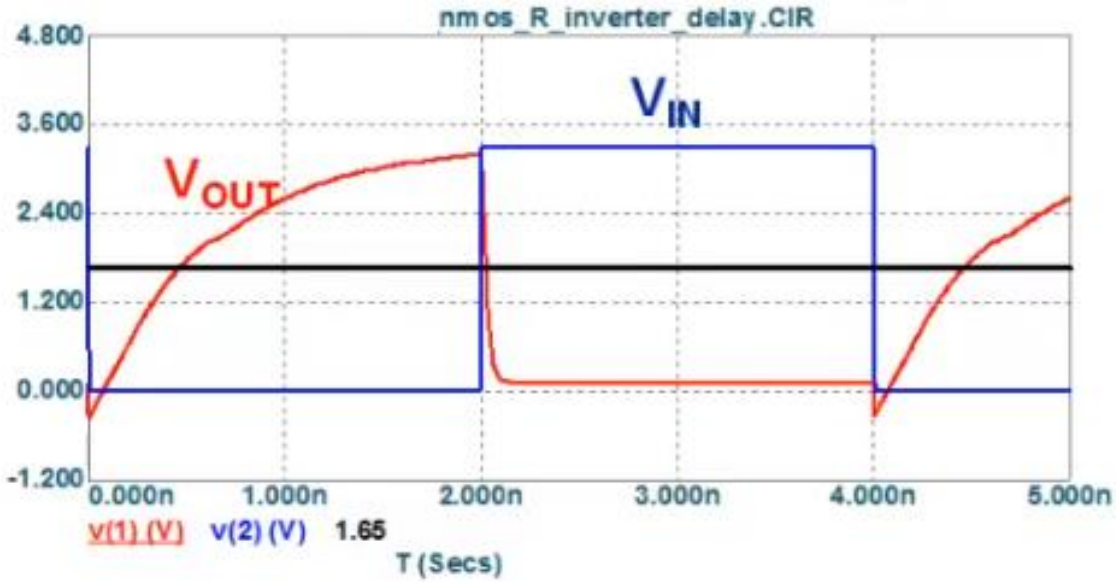
$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{dis.}}$$ ~39 ps

$$\tau_{PLH} \cong 424\,ps$$

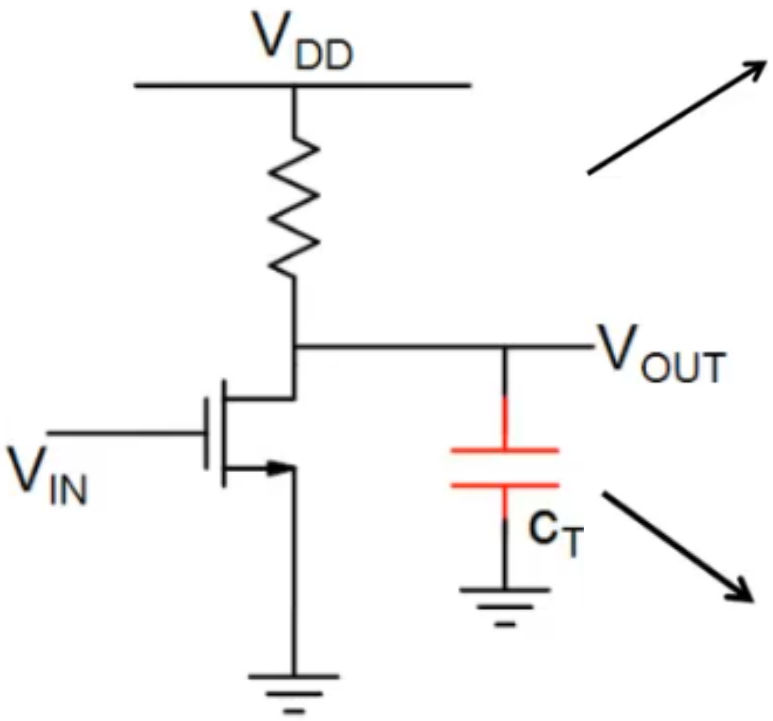
$$I_{dis.} = I_{DS1} - \frac{V_{DD} - V_{D1}}{R_D}$$

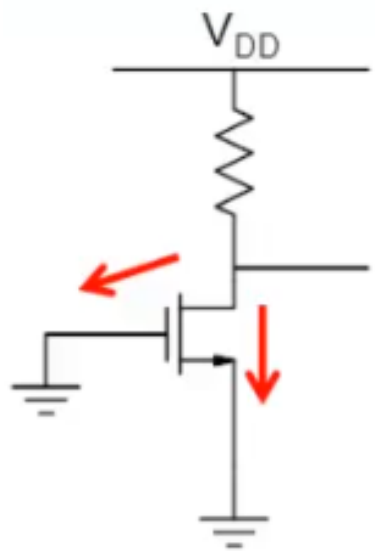
$$I_{DS}(t=0) = \left(KP_N \times \frac{W}{L}\right) \times \frac{(V_{DD} - V_{THN})^2}{2}$$ 0.53mA

$$I_{DS}(t=\tau_{phl}) = \left(KP_N \times \frac{W}{L}\right) \times \left((V_{DD} - V_{THN})\frac{V_{DD}}{2} - \frac{V_{DD}^2}{4}\right) - \frac{V_{DD}}{2R_D}$$ 0.19mA

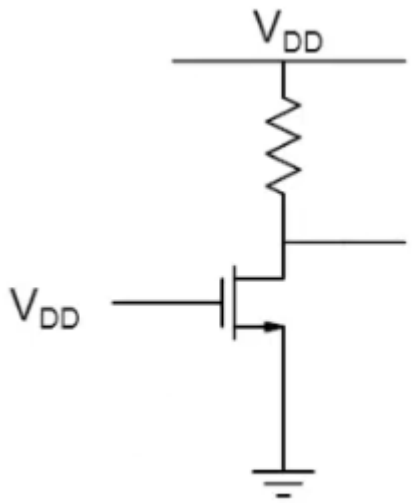


Power dissipation

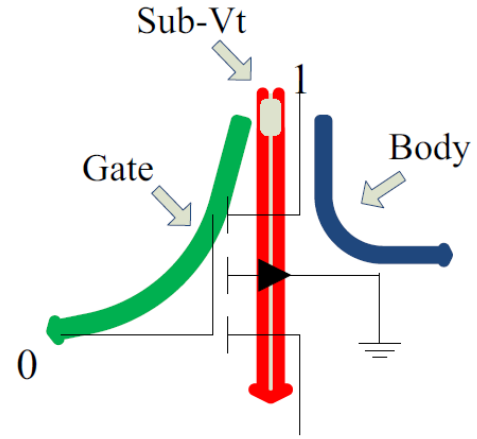


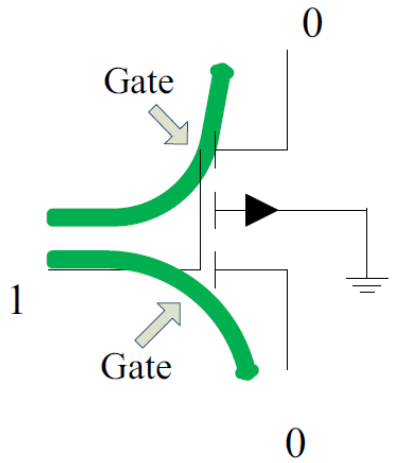


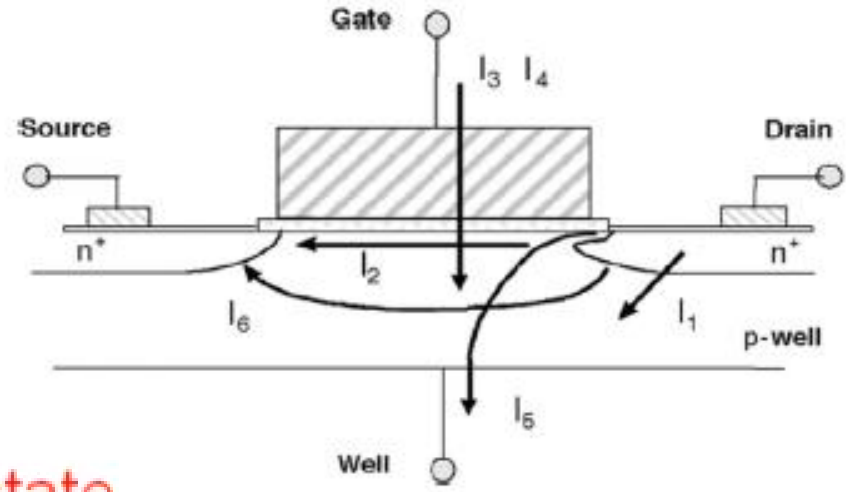
$$P = V_{DD} \times I_{leakage}$$



$$P \sim \frac{V_{DD}^2}{R_D}$$



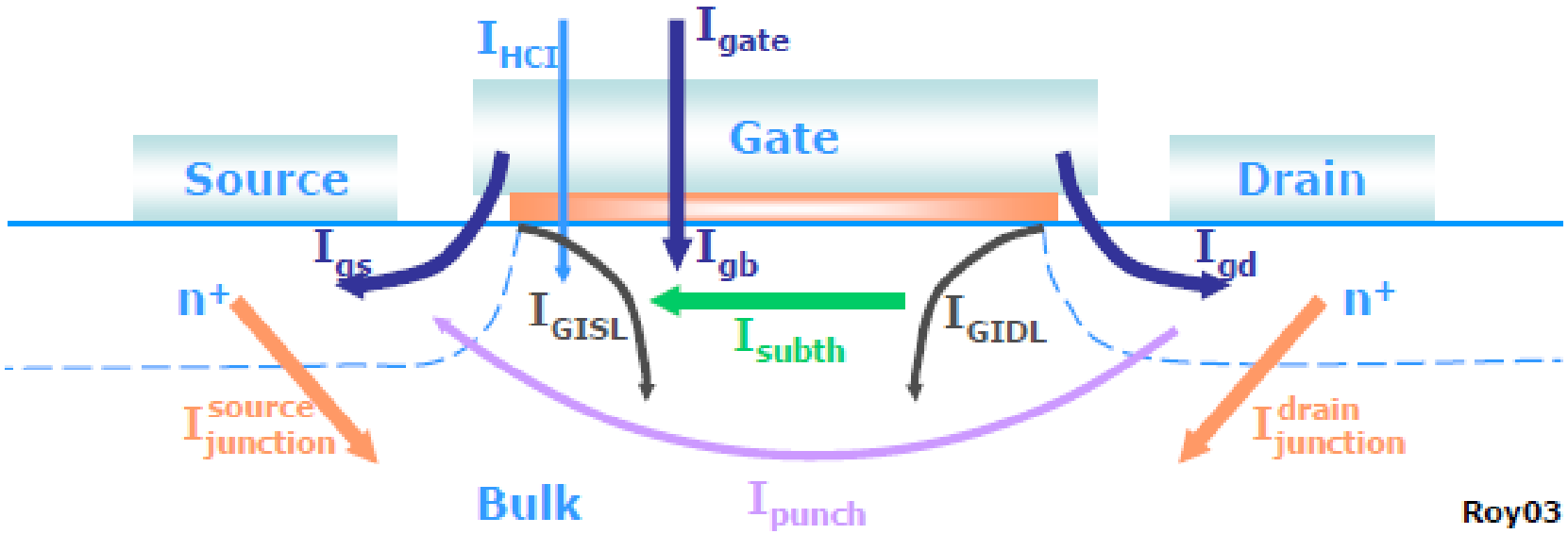




1. Static
2. Dynamic

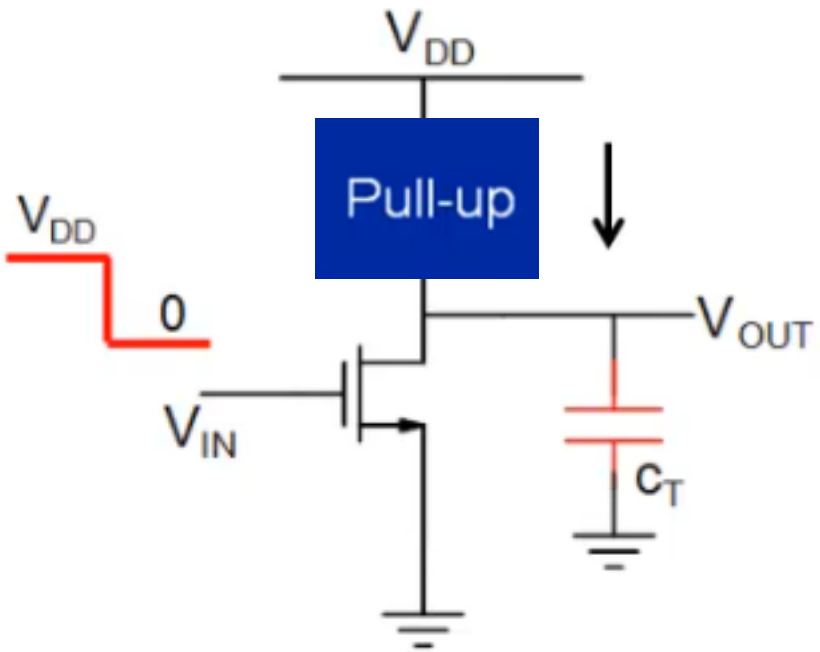
Energy should be drawn only to change the state

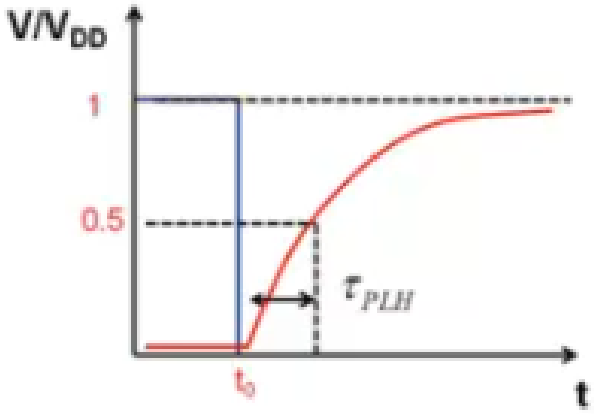
- **If channel is locking:**
  - subthreshold current (I_{subth}) ≤180nm
  - gate tunnelling to S/D (I_{gate}) ≤90nm
  - pn-junction leakage ($I_{junction}$) ≤65nm
  - gate induced drain leakage (I_{GIDL})
  - depletion punchthrough (I_{punch})
- **If channel is conducting:**
  - gate tunnelling (I_{gate})
  - pn-junction leakage ($I_{junction}$)
- **If channel is switching:**
  - hot carrier injection (I_{HCI})



Long Channels (L> 1μm) Leakages are very small.	→	Short Channels L > 180nm t_{ox} > 3nm Sub-threshold leakage	→	Very Short Channels L > 90nm t_{ox} > 2nm Sub-threshold leakage + Gate leakage	→	Nano scale Channels L < 90nm t_{ox} < 2nm Sub-threshold leakage + Gate leakage + Junction leakage / BTBT

Contribution of new leakage currents with scaled technologies

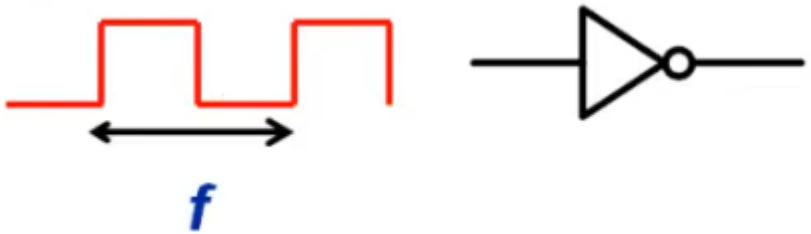




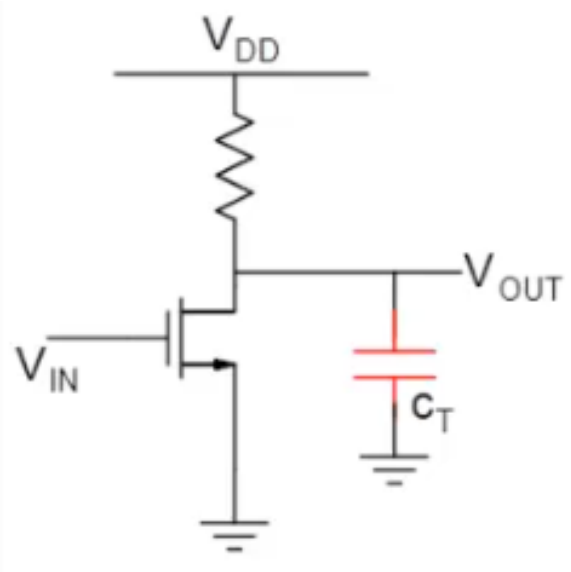
$$E_{supply} = \int V_{DD} \times I_{pu} dt = C_T \times V_{DD}^2$$

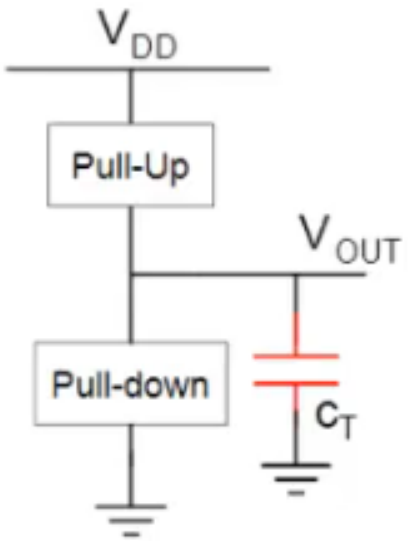
Half of it is dissipated in the resistor and the other half is stored in capacitor

When the inverter switches back to zero, the energy stored on capacitor is also dissipated

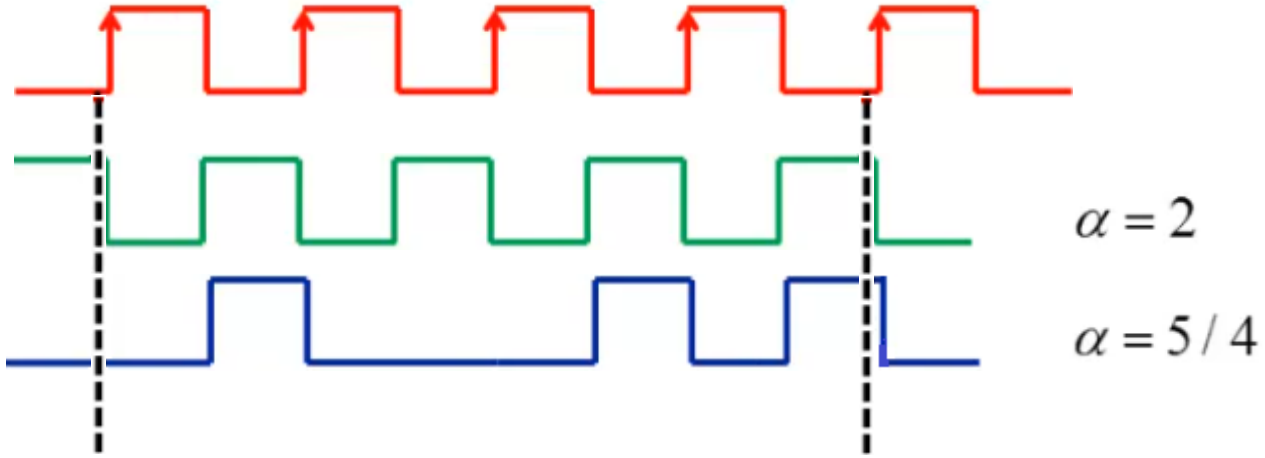


$$P_{dynamic} = \frac{0.5C_T \times V_{DD}^2 + 0.5C_T \times V_{DD}^2}{T} = C_T \times V_{DD}^2 \times f$$

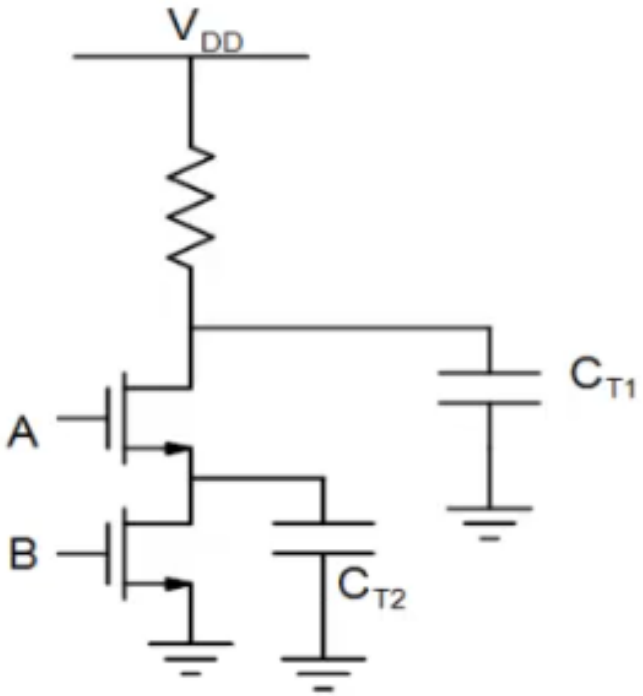




$$P_{dynamic} = C_T \times V_{DD}^2 \times f$$



$$P_{dynamic} = \sum \left(0.5 C_j \times V_j^2 \right) \times f \times \alpha_j$$



NAND gate

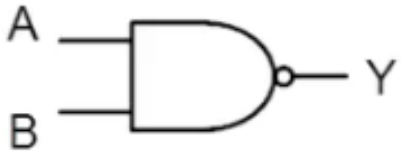
$$P_{dynamic} = \left(0.5C_{T1} \times V_{j1}^2\right) \times f \times \alpha_1 + \left(0.5C_{T2} \times V_{j2}^2\right) \times f \times \alpha_2$$

Suppose B= 1 and A switches with clock frequency

$$P_{dynamic} \cong \left(0.5C_{T1} \times V_{DD}^2\right) \times f \times 2$$

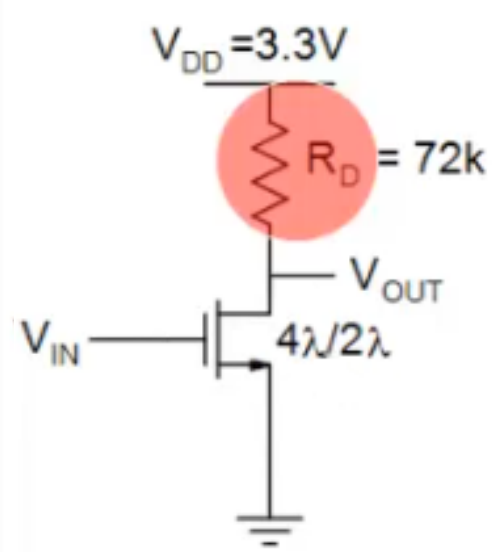
Suppose A= 1 and B switches with clock frequency

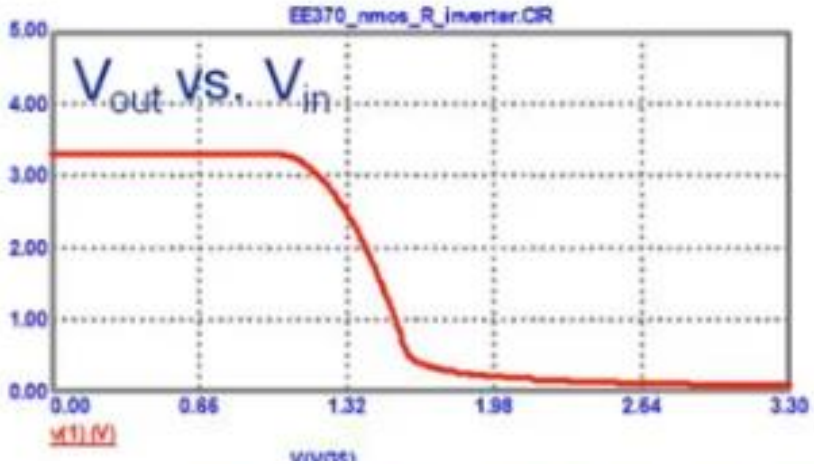
$$P_{dynamic} \cong \left(0.5C_{T1} \times V_{DD}^2\right) \times f \times 2 + \left(0.5C_{T2} \times V_{DD}^2\right) \times f \times 2$$



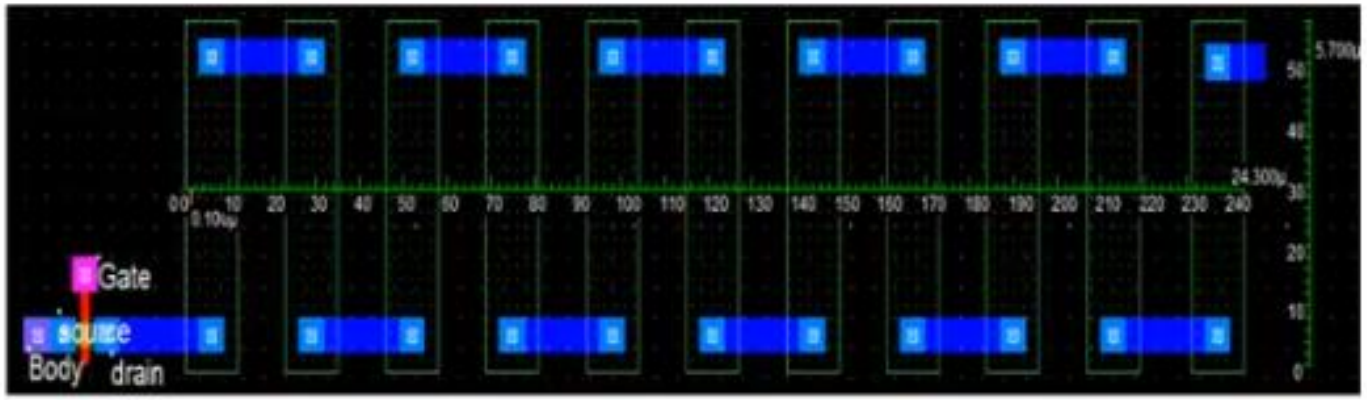
What about delays ?

Summary

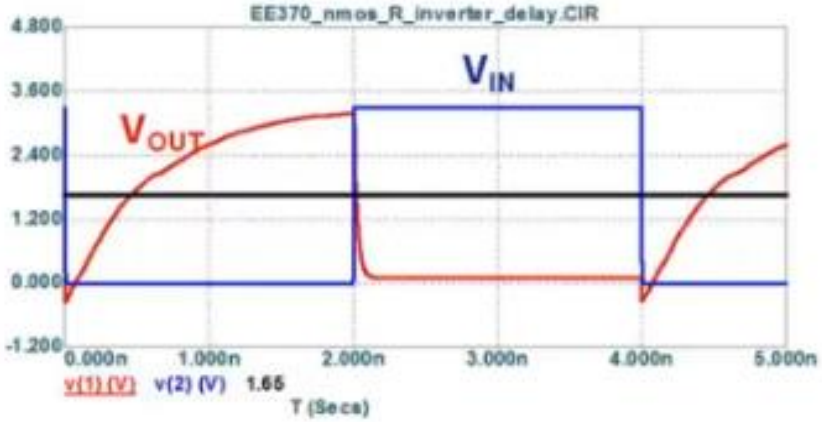




$$R_D = 72k \Rightarrow V_{OL} = 0.1V; V_{OH} = 3.3V$$
$$V_{IL} = 1.07V; V_{IH} = 1.7V$$
$$NM_L \sim 0.97V; NM_H \sim 1.6V$$
$$V_{inv} = 1.5V$$



1. Noise Margins
2. Area
3. Delay
4. Power

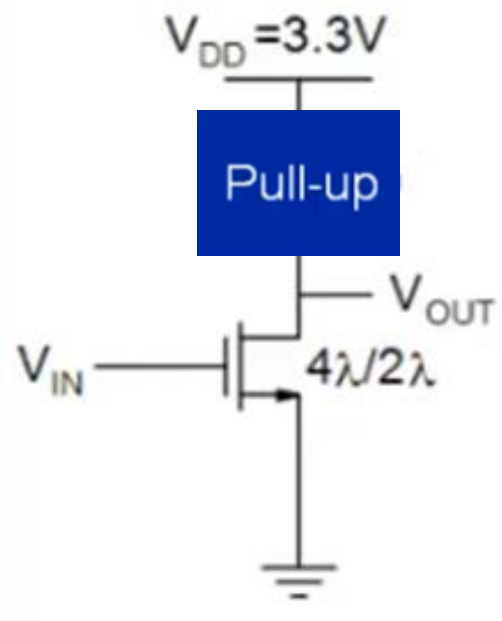


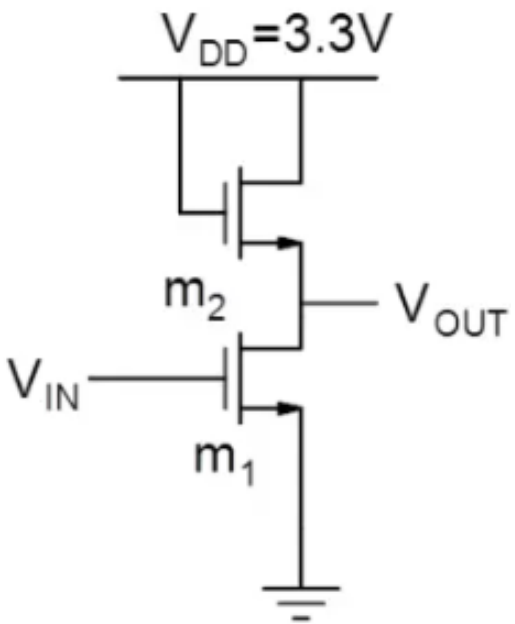
$$\tau_{PLH} \cong 424\,ps; \tau_{PHL} \sim 39\,ps$$

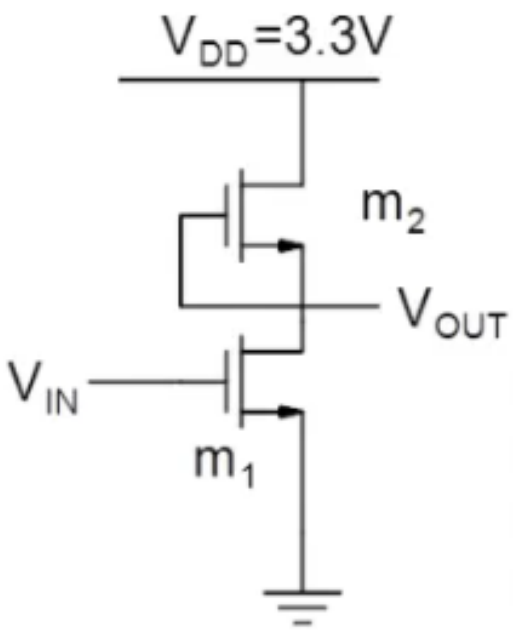
$$\tau_{PLH} \cong 0.693 \times R_D \times \tilde{C}_T$$

$$P_{static} \sim \frac{V_{DD}^2}{R_D}$$

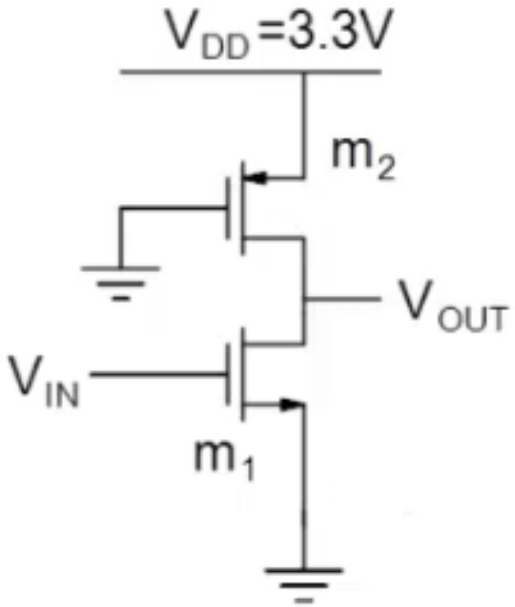
$$P_{dynamic} = C_T \times V_{DD}^2 \times f$$





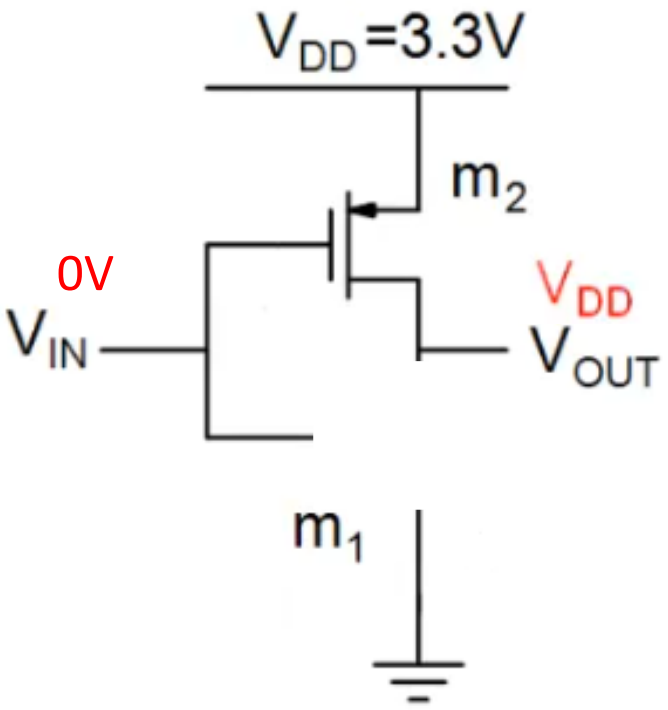


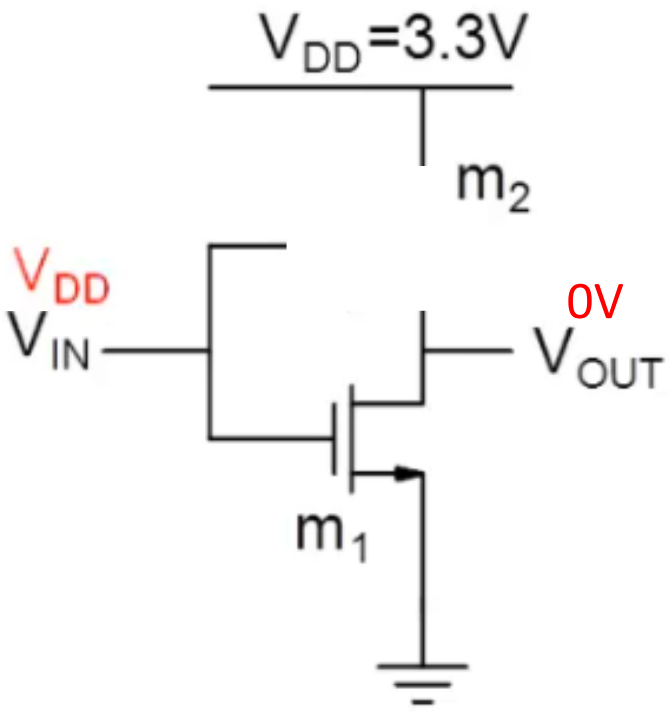
Make m2 depletion mode



They all have static power dissipation when output is low.

Pseudo-NMOS logic

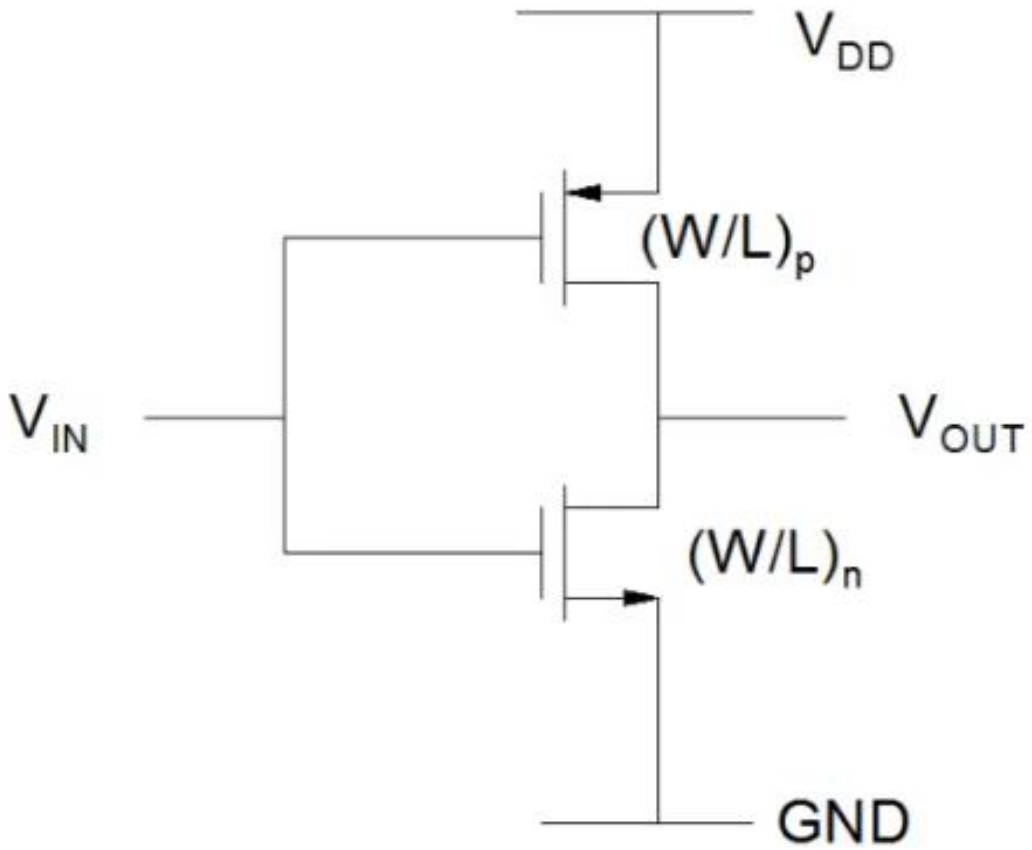




Logic "1" is VDD and "logic "0" is GND independent of size of transistors.

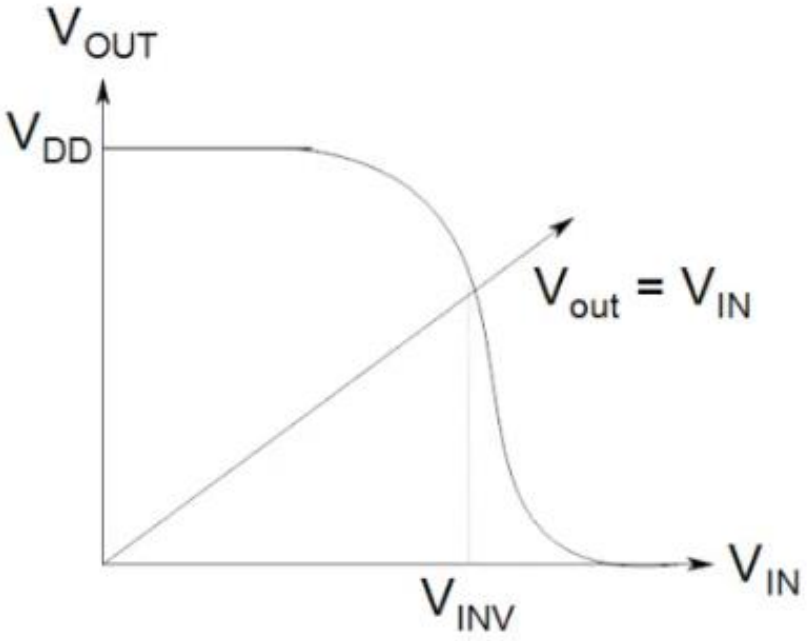
There is "no" static power dissipation in the circuit

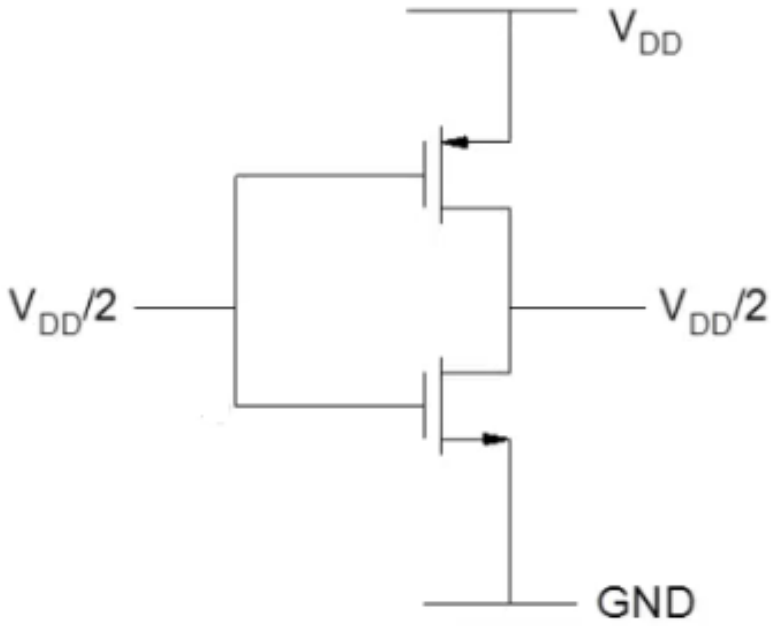
CMOS Inverter



How should we size to obtain symmetrical VTC ?

CMOS Inverter : VTC

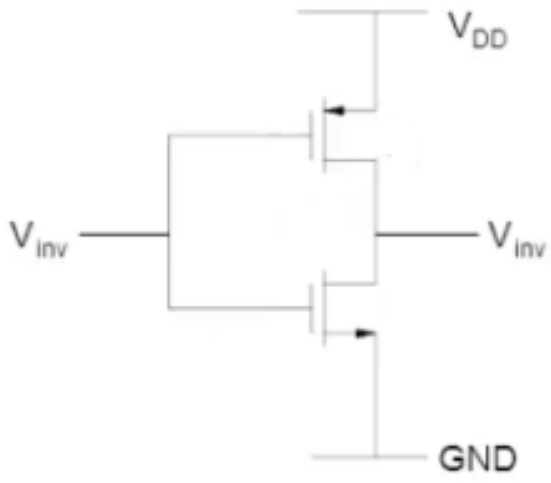




Both NMOS and PMOS are in saturation region

CMOS Inverter : VTC

$$I_{DSN} = I_{SDP}$$



$$\frac{\beta_N}{2}(V_{inv} - V_{THN})^2 = \frac{\beta_P}{2}(V_{SGP} + V_{THP})^2$$

$$V_{SGP} = V_{DD} - V_{inv}$$

$$\beta_N = W_N / L_N KP_N$$

$$\beta_P = W_p / L_P KP_P$$

$$V_{INV} = \frac{V_{THN} + \frac{1}{\sqrt{\beta_R}}(V_{DD} + V_{THP})}{1 + \frac{1}{\sqrt{\beta_R}}}$$

$$\beta_R = \frac{\beta_N}{\beta_P} = \left(\frac{W_N / L_N}{W_P / L_P}\right) \times \left(\frac{KP_N}{KP_P}\right)$$

CMOS Inverter : VTC

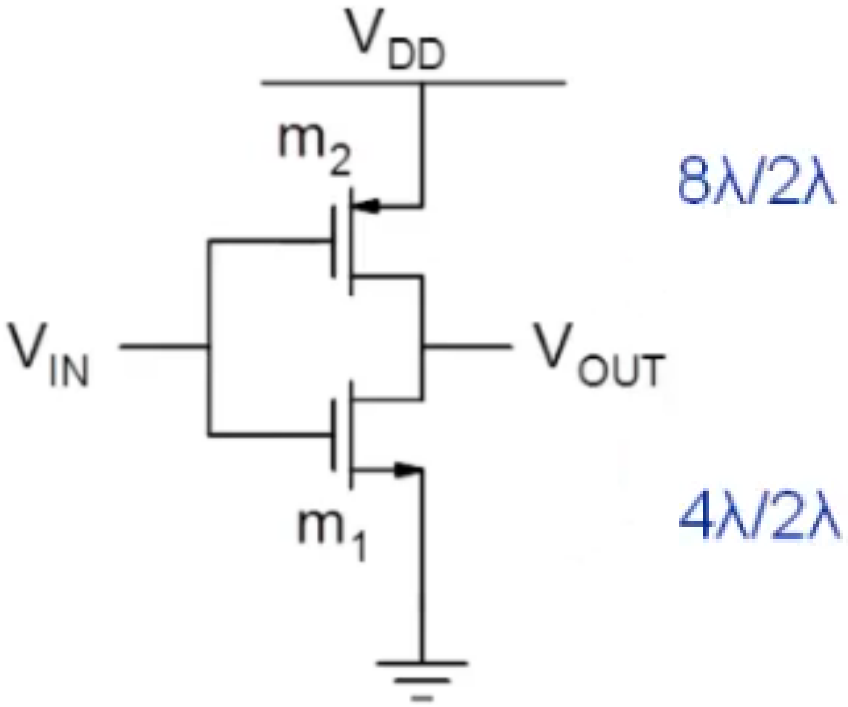
$$V_{INV} = \frac{V_{THN} + \frac{1}{\sqrt{\beta_R}}(V_{DD} + V_{THP})}{1 + \frac{1}{\sqrt{\beta_R}}}$$

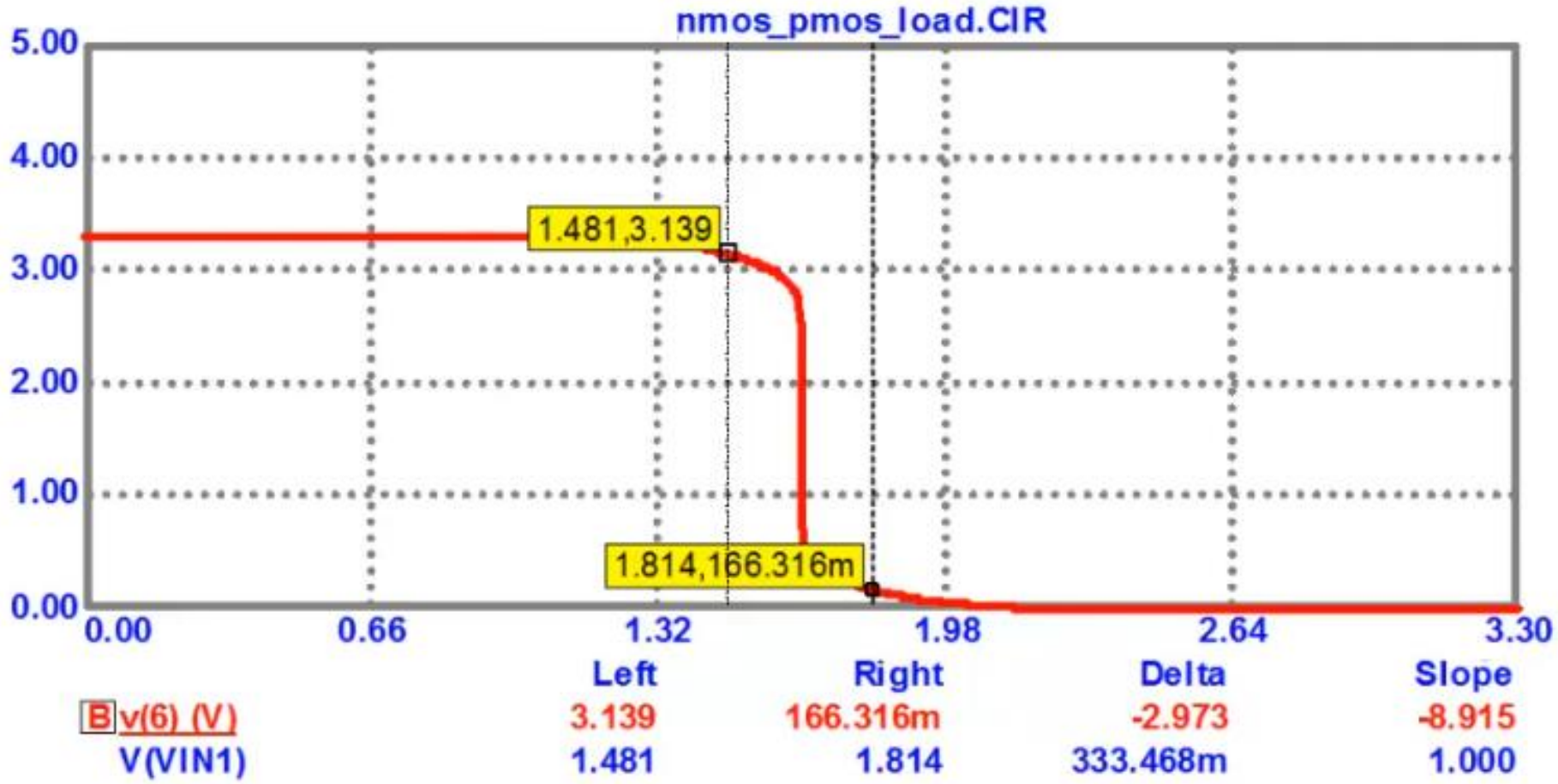
$$V_{INV} = 0.5V_{DD}$$

$$\beta_R = \frac{0.5V_{DD} + V_{THP}}{0.5V_{DD} - V_{THN}}$$

$$\Rightarrow \beta_R = 1$$

$$\frac{W_P/L_P}{W_N/L_N} = \frac{KP_N}{KP_P}$$ 2.0





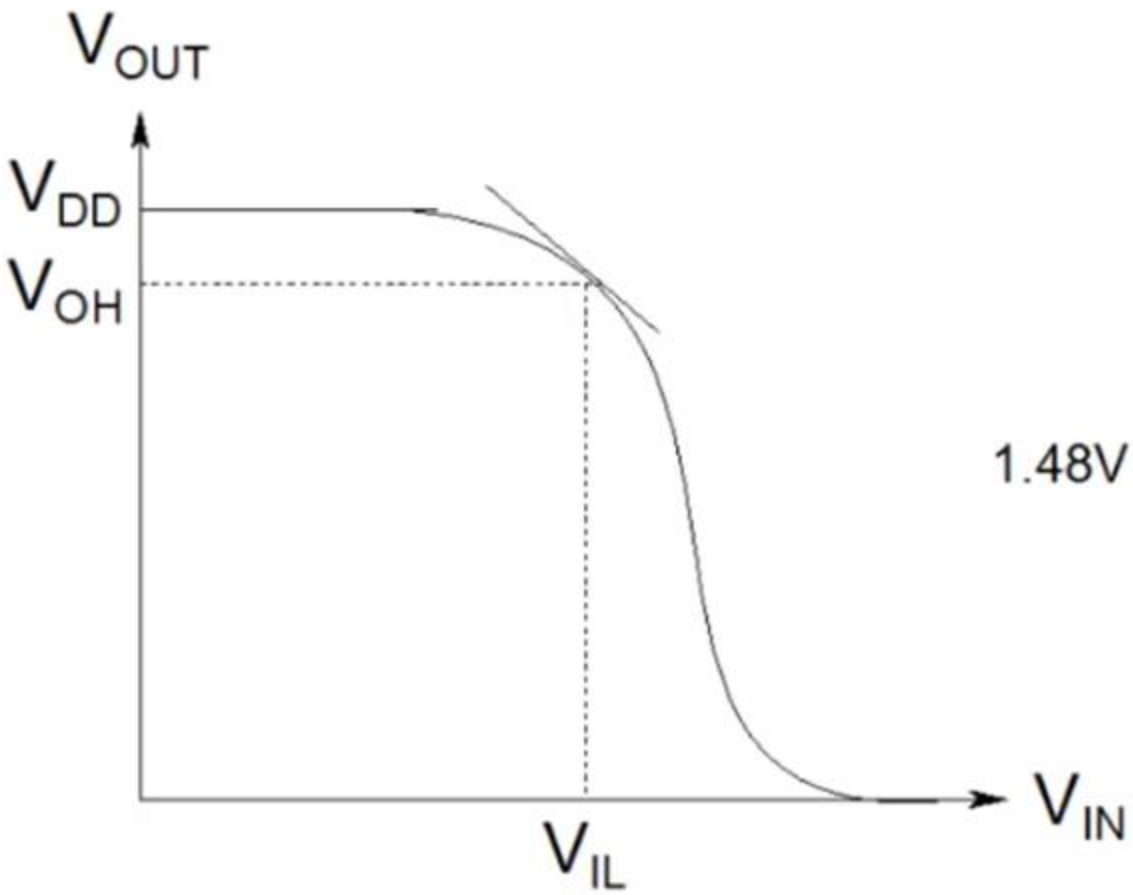
$$V_{IL} = 1.48V; v_{ol} = 0V$$

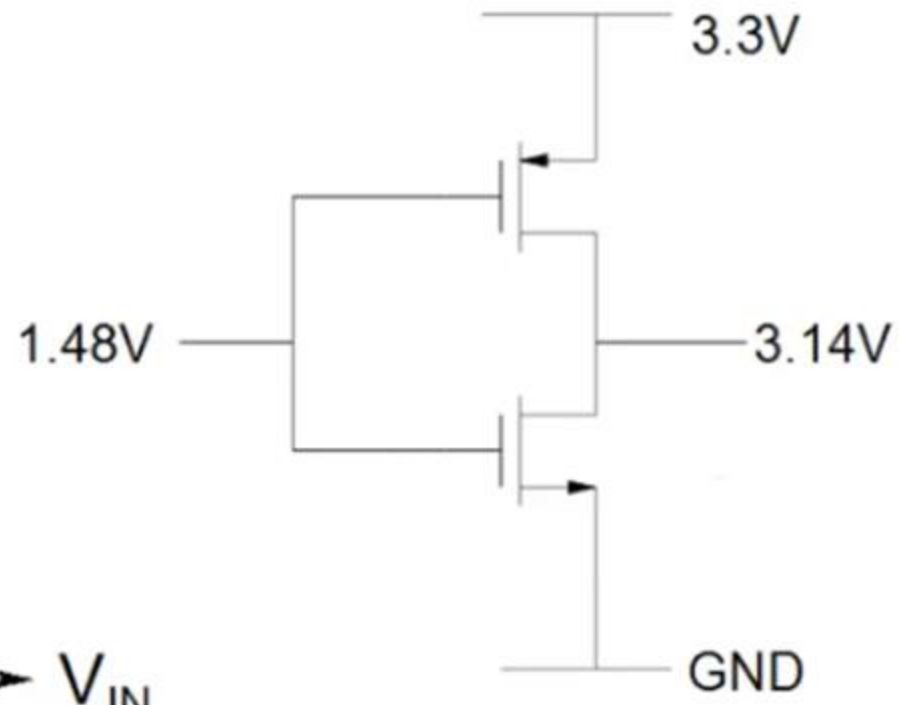
$$V_{IH} = 1.814V; v_{oh} = 3.3V$$

$$NM_H = 1.48V; NM_L = 1.48V$$

$$\frac{NM_H}{0.5V_{DD}} = 0.9$$

CMOS Inverter : V_{IH} ; V_{IL}





At V_{IL} , PMOS in Linear and NMOS in Saturation

CMOS Inverter : V_{IH} ; V_{IL}

W_P/W_N	V_{INV}	V_{IH}	V_{IL}	V_{OH}	V_{OL}
1	1.53	1.67	1.34	3.16	0.177
2	1.65	1.81	1.48	3.14	0.166
3	1.7	1.9	1.575	3.12	0.148

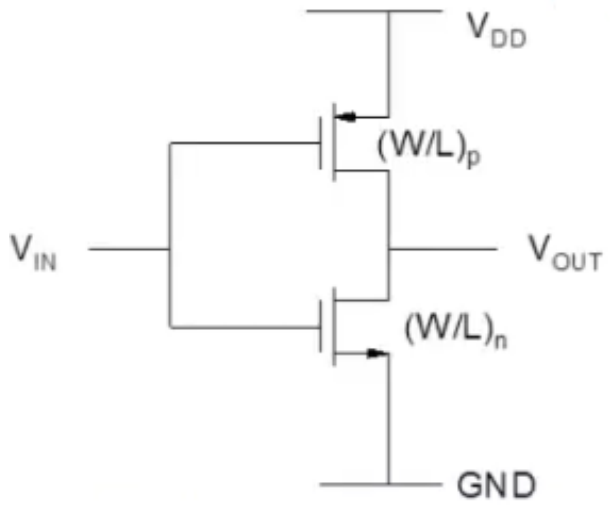
CMOS Inverter : V_{IL}

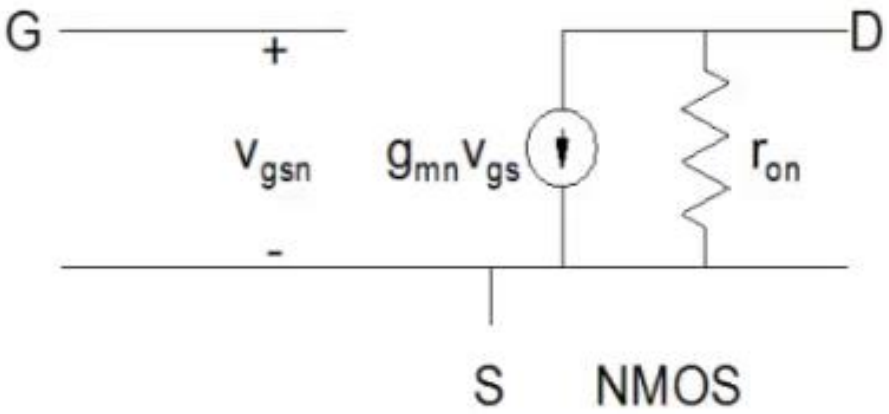
$$\frac{\beta_N}{2}(V_{IL} - V_{THN})^2 =$$

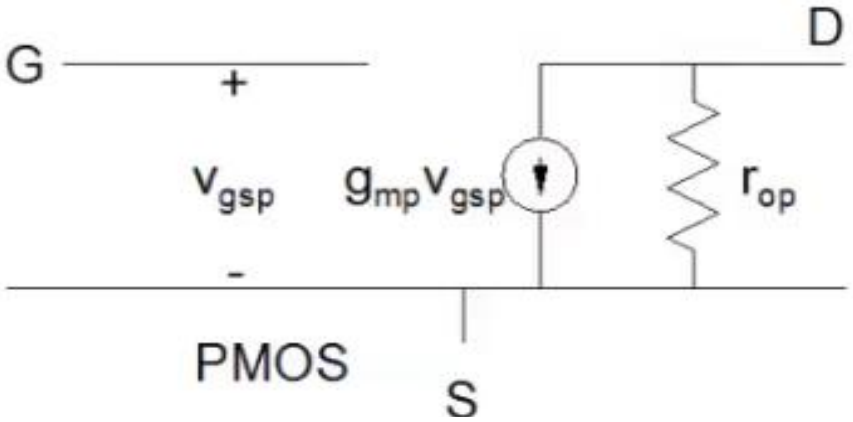
$$\beta_P((V_{DD} - V_{IL} + V_{THP})(V_{DD} - V_{OUT}) - 0.5(V_{DD} - V_{OUT})^2)$$

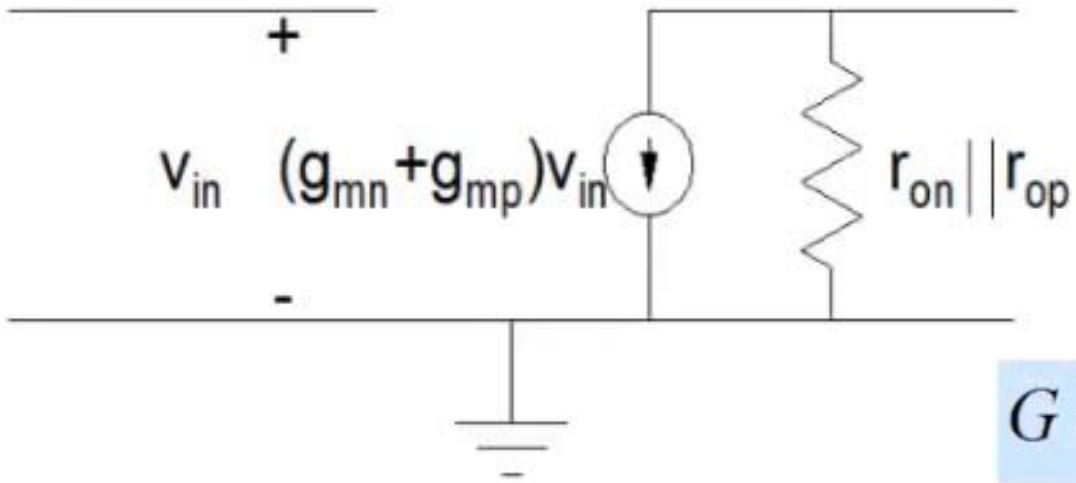
- Gain of inverter is Unity

CMOS Inverter : V_{IH} ; V_{IL}









$$G = -(g_{MN} + g_{MP}) \times r_{ON} \| r_{OP}$$

CMOS Inverter : V_{IL}

$$G = -(g_{MN} + g_{MP}) \times r_{ON} \| r_{OP} = -1$$

$$\Rightarrow (g_{MN} + g_{MP}) \times r_{OP} \cong 1$$

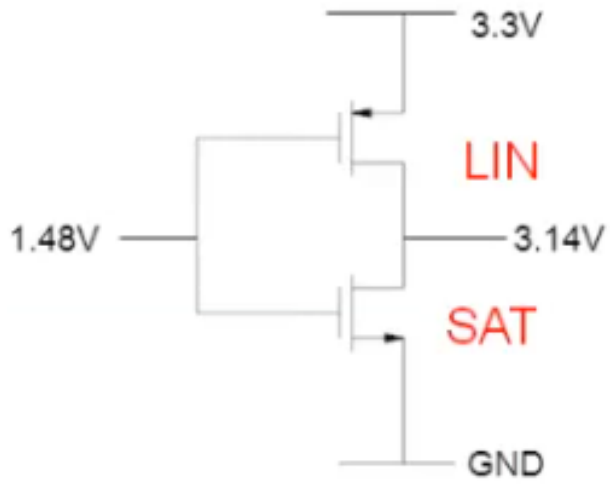
$$g_{mn} = \beta_N \times (V_{IL} - V_{THN})\ ;\ \ g_{mp} = \beta_P \times (V_{DD} - V_{OUT})$$

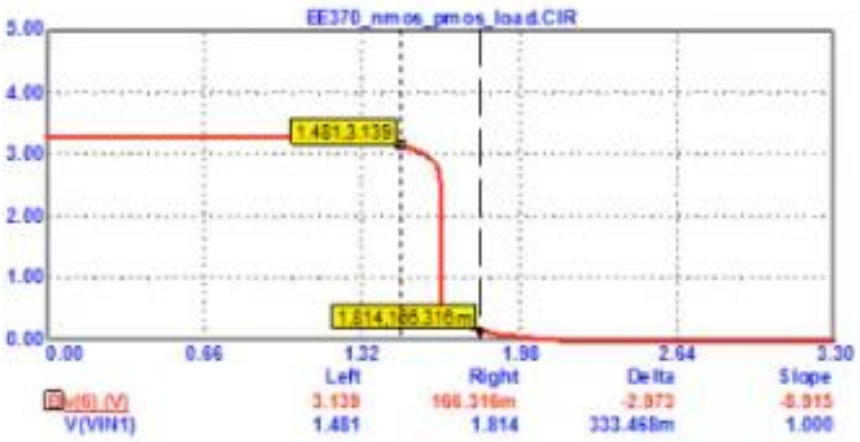
$$r_{op} = \frac{1}{\beta_P \times (V_{DD} - V_{IL} + V_{THP} + V_{DD} - V_{OUT})}$$

$$\frac{\beta_N}{2}(V_{IL} - V_{THN})^2 =$$

$$\beta_P((V_{DD} - V_{IL} + V_{THP})(V_{DD} - V_{OUT}) - 0.5(V_{DD} - V_{OUT})^2)$$

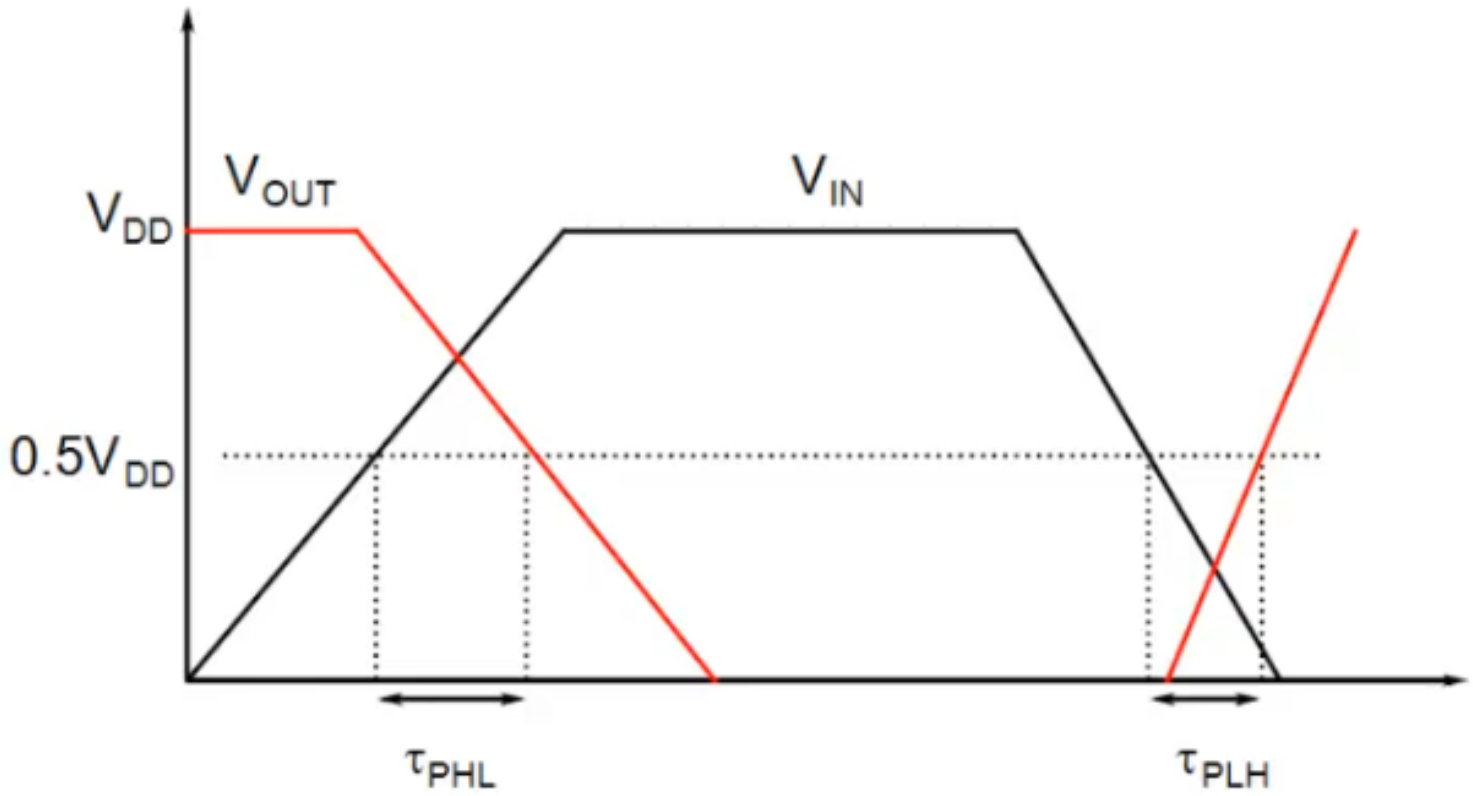
$$V_{IL} \sim V_{inv} - \delta V\ ;\ V_{IH} \sim V_{inv} + \delta V$$





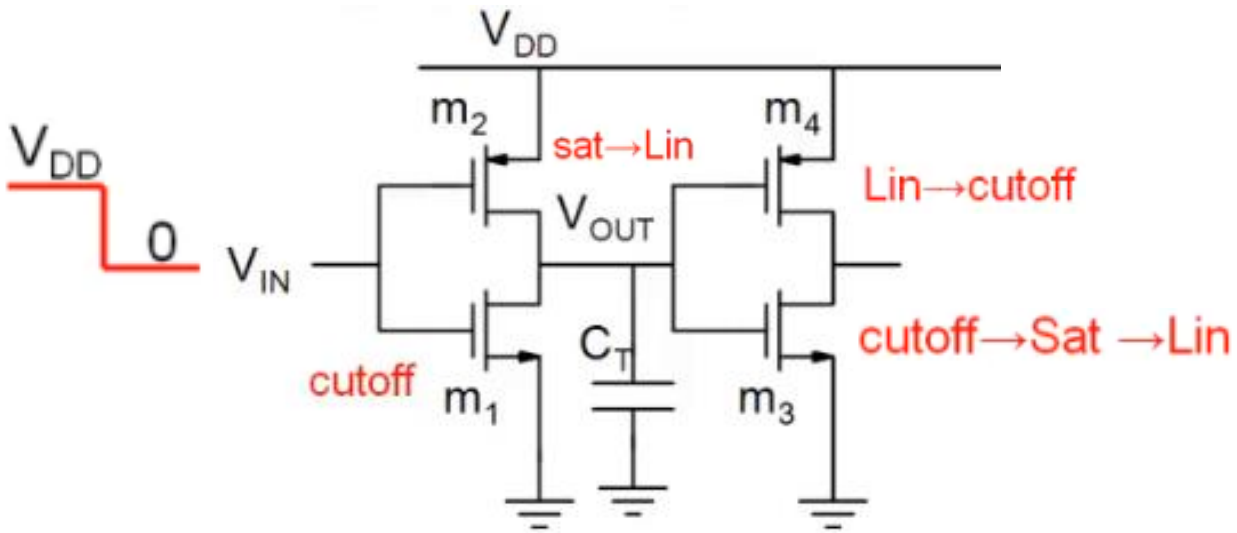
$$\delta V \sim 0.17V$$

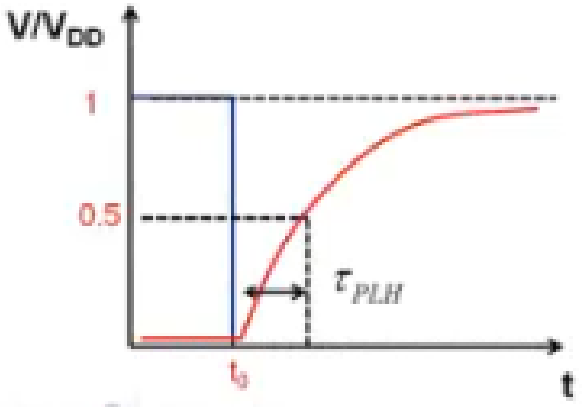
CMOS: Propagation Delay



$$\tau_R \; ; \tau_F \; ; \tau_{PHL} \; ; \tau_{PLH}$$

Low to high propagation delay

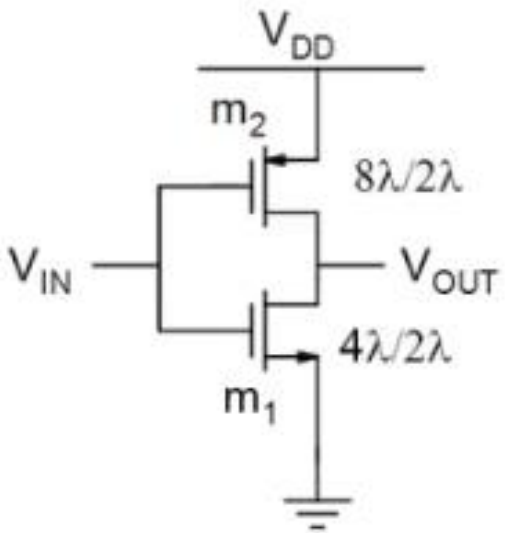




$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd}}$$

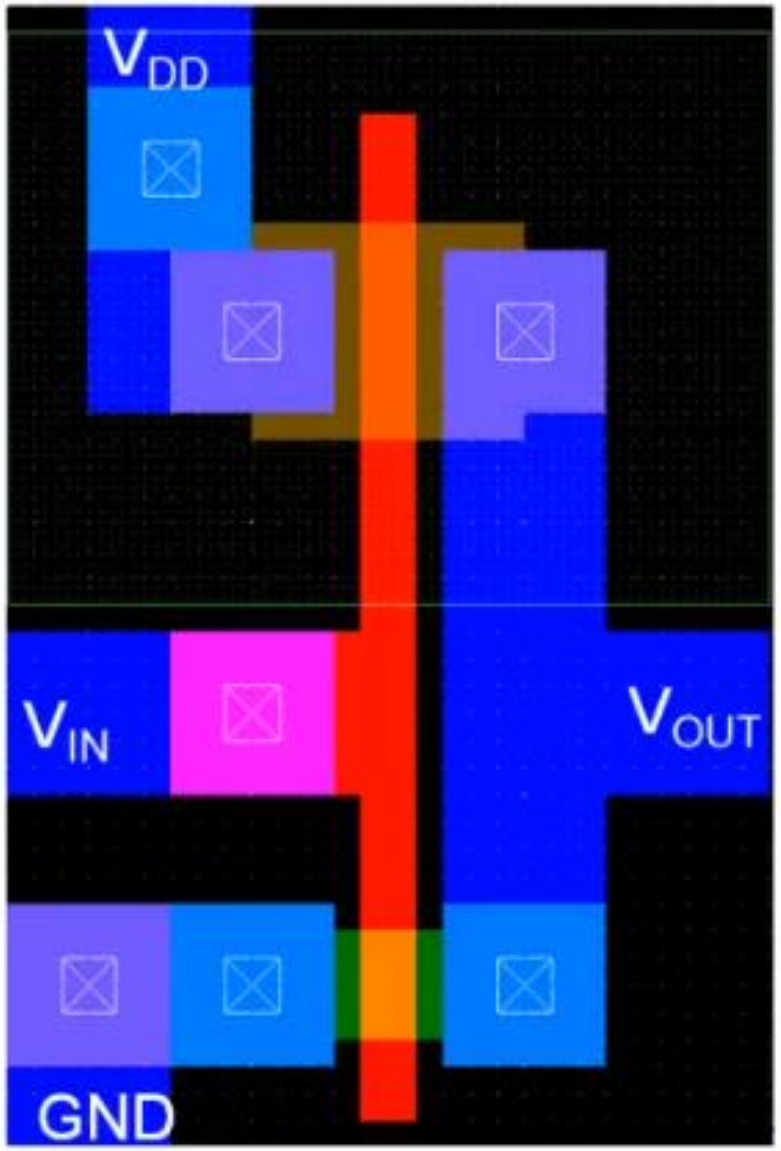
$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$$

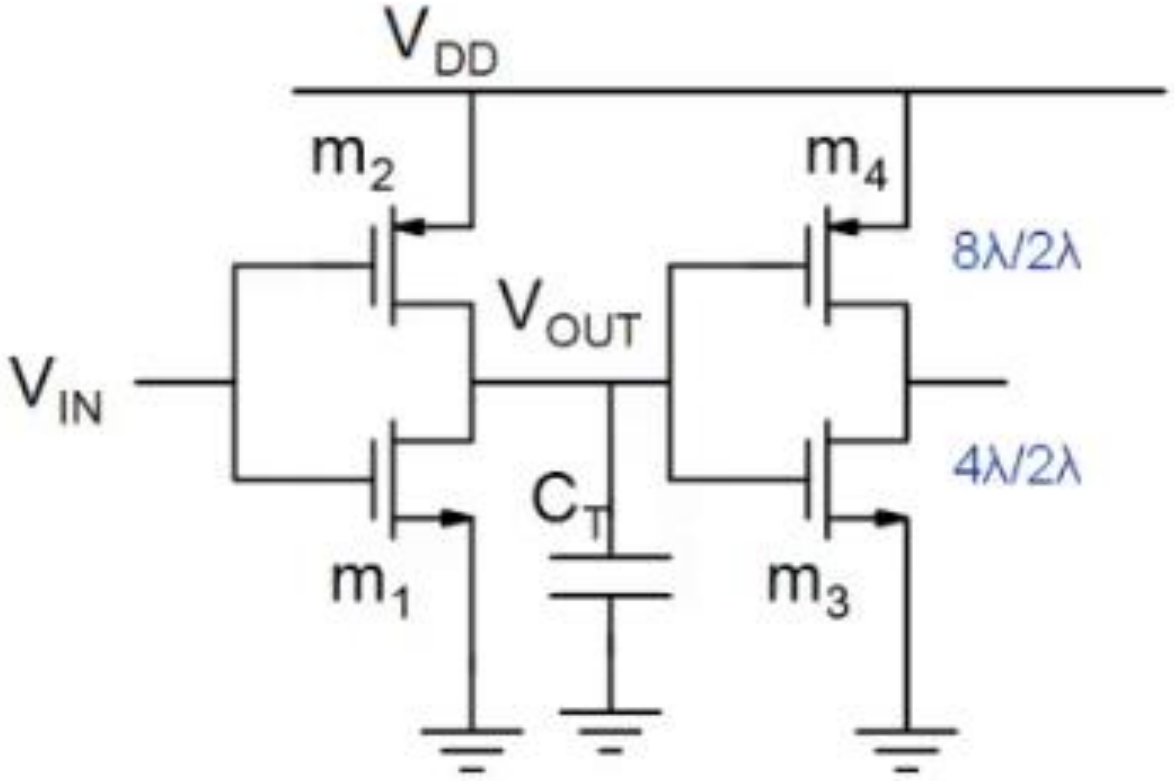
$$C_T = \left(C_{gdn1} + C_{dbn1} + C_{gdp2} + C_{dbp2}\right) +$$
$$\left(C_{gsn3} + C_{gdn3} + C_{gbn3} + C_{gsp4} + C_{gdp4} + C_{gbp4}\right)$$



$$A_{D1} = 4 \times 1 + 6 \times 6 = 40;$$
$$P_{D1} = (1 + 1 + 6) \times 2 + 6 = 22$$

$$A_{D2} = 8 \times 4 + 3 \times 6 = 50;$$
$$P_{D2} = (4 + 1 + 3) \times 2 + 6 = 22$$





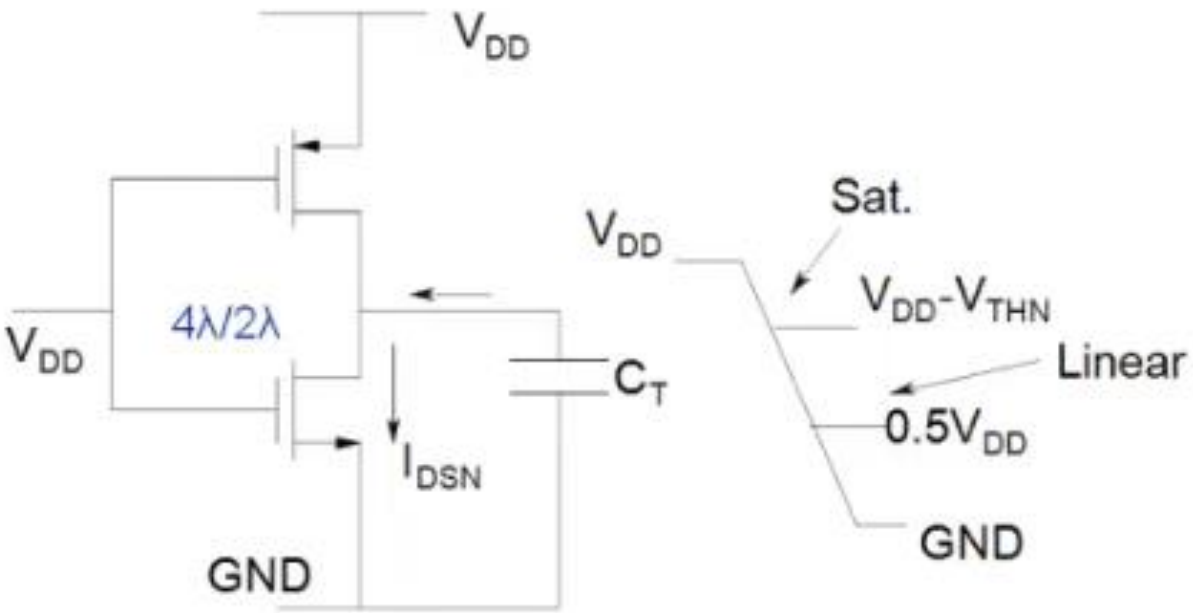
~0.3fF ~6fF ~0.6fF ~6fF

$$C_T = \left(C_{gdn1} + C_{dbn1} + C_{gdp2} + C_{dbp2}\right) +$$

~13+7fF

$$\left(\underbrace{C_{gsn3} + C_{gdn3}}_{\sim 2.0\text{fF}} + C_{gbn3} + \underbrace{C_{gsp4} + C_{gdp4}}_{\sim 5\text{fF}} + C_{gbp43}\right)$$

Delay Analysis：



$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}}$$

$\tau_{phl} \sim 65ps$

42+23

$$I_{DS}(t=0) = \left(KP_N \times \frac{W_N}{L_N}\right) \times \frac{(V_{DD} - V_{THN})^2}{2}$$

$$I_{DS}(t=\tau_{phl}) = \left(KP_N \times \frac{W_N}{L_N}\right) \times \left((V_{DD} - V_{THN})\frac{V_{DD}}{2} - \frac{V_{DD}^2}{8}\right)$$

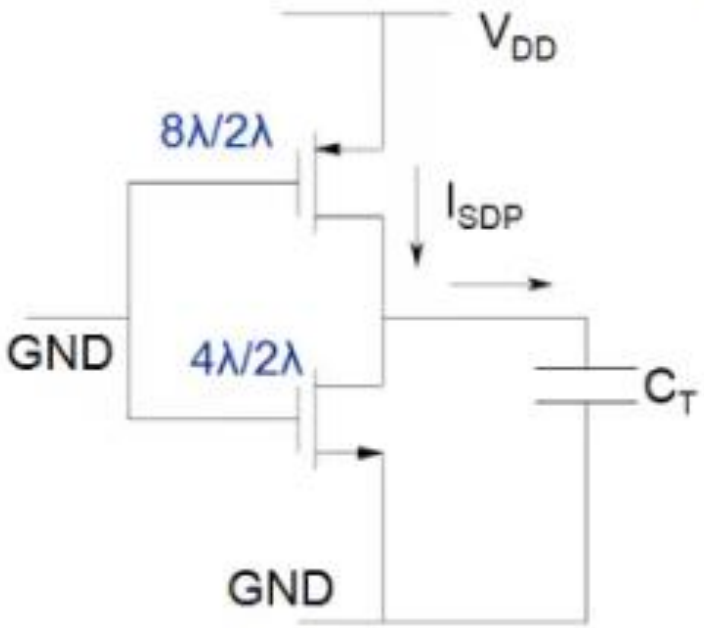
~0.53mA → $\tilde{I}_{pd} \sim 0.5mA$

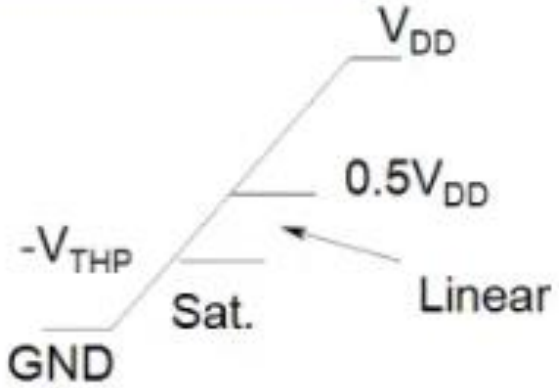
~0.487mA → $\tilde{I}_{pd} \sim 0.5mA$

Delay Analysis：

$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu.}}$$

$$\tau_{plh} \sim 65ps$$

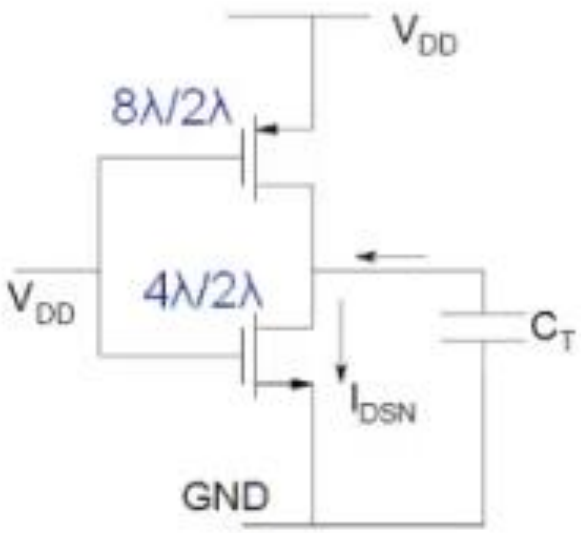




$$I_{SDP}(t=0) = \left(KP_P \times \frac{W_P}{L_P}\right) \times \frac{(V_{DD}+V_{THP})^2}{2}$$ ~0.53mA

$$\tilde{I}_{pu} \sim 0.5mA$$

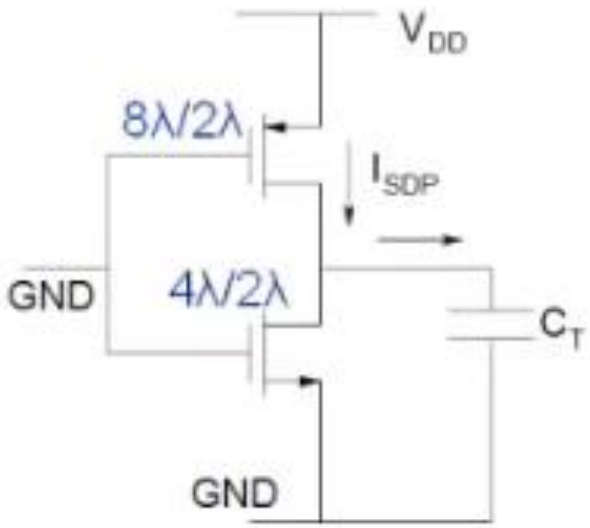
$$I_{SDP}(t=\tau_{plh}) = \left(KP_P \times \frac{W_P}{L_P}\right) \times \left((V_{DD}+V_{THP})\frac{V_{DD}}{2} - \frac{V_{DD}^2}{8}\right)$$ ~0.487mA



$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}}$$

$$I_{DS}(t=0) = \left(KP_N \times \frac{W_N}{L_N}\right) \times \frac{(V_{DD} - V_{THN})^2}{2}$$

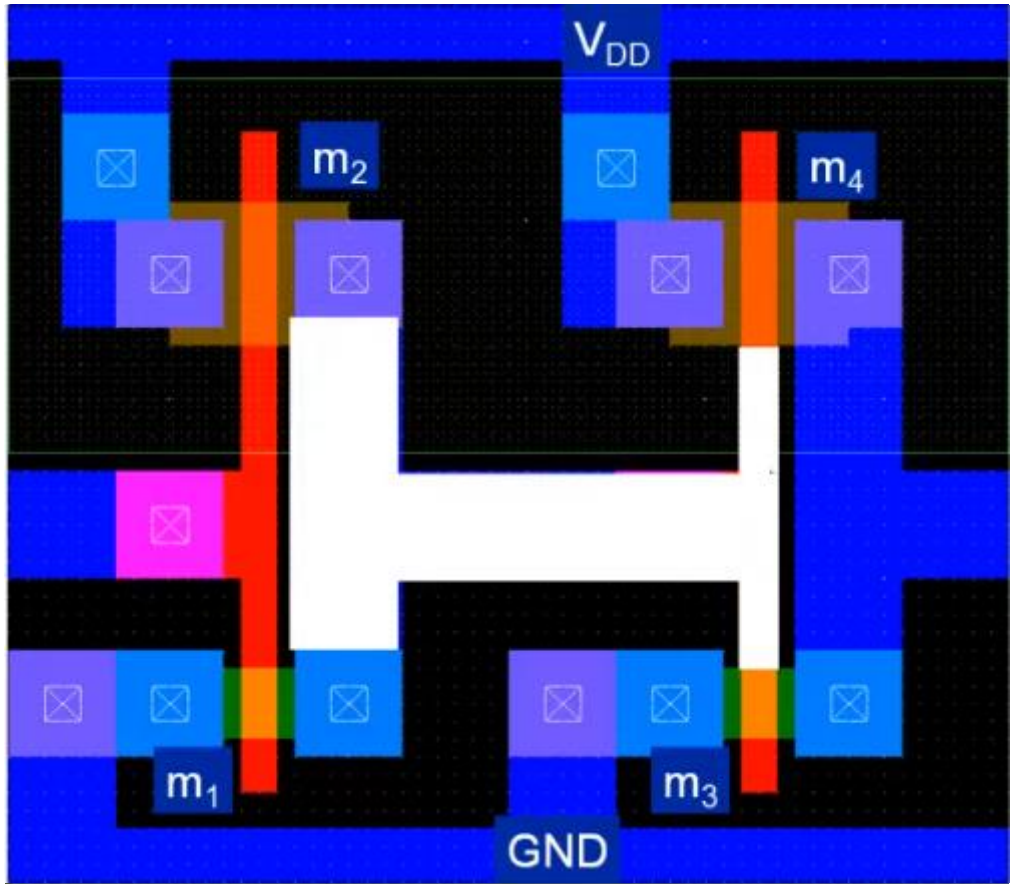
$$I_{DS}(t=\tau_{phl}) = \left(KP_N \times \frac{W_N}{L_N}\right) \times \left((V_{DD} - V_{THN})\frac{V_{DD}}{2} - \frac{V_{DD}^2}{8}\right)$$

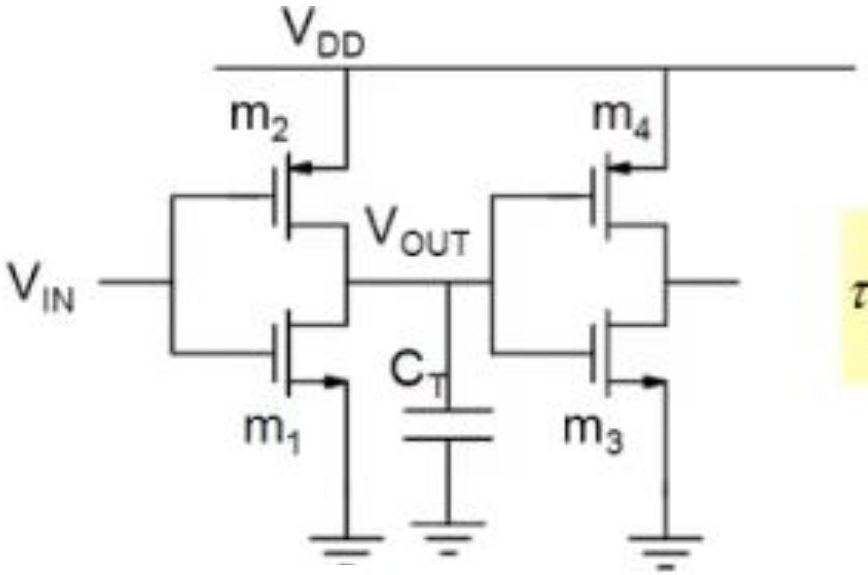


$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu.}}$$

$$I_{SDP}(t=0) = \left(KP_P \times \frac{W_P}{L_P}\right) \times \frac{(V_{DD} + V_{THP})^2}{2}$$

$$I_{SDP}(t=\tau_{plh}) = \left(KP_P \times \frac{W_P}{L_P}\right) \times \left((V_{DD} + V_{THP})\frac{V_{DD}}{2} - \frac{V_{DD}^2}{8}\right)$$


V_{DD}
m_2
m_4
m_1
m_3
GND



$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}}$$

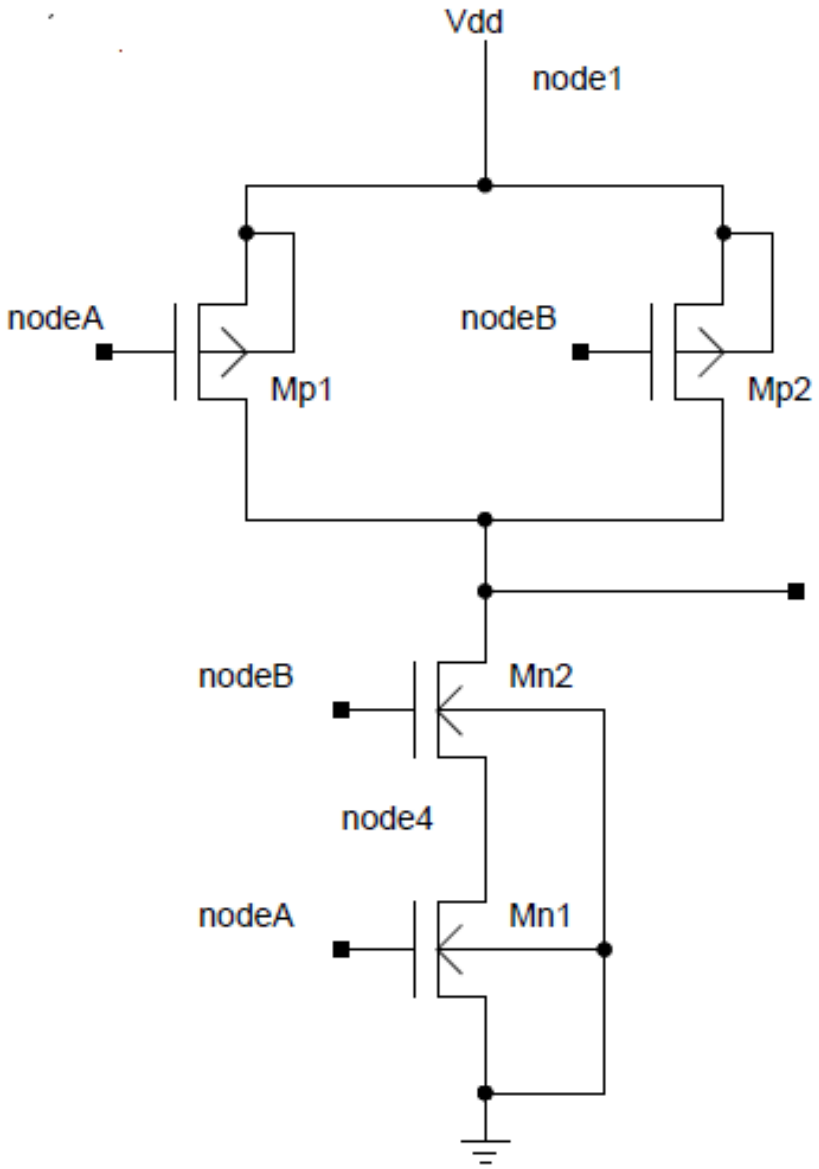
~13fF

~7fF

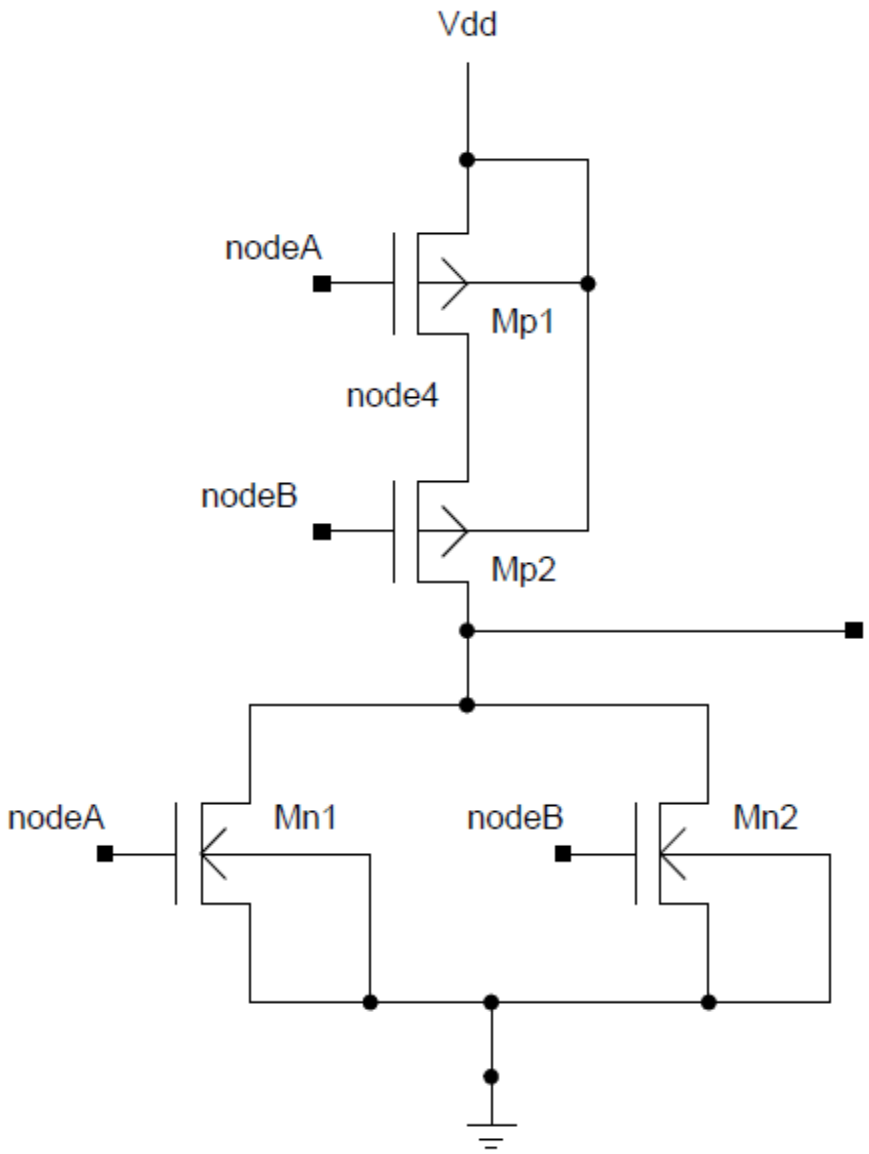
$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_{in} V_{DD}}{\tilde{I}_{pd.}} + 0.5 \times \frac{\tilde{C}_L V_{DD}}{\tilde{I}_{pd.}}$$

$$\tau_{phl}(ps) \cong 42 + a \times C_L(fF);\ a = 3.25$$

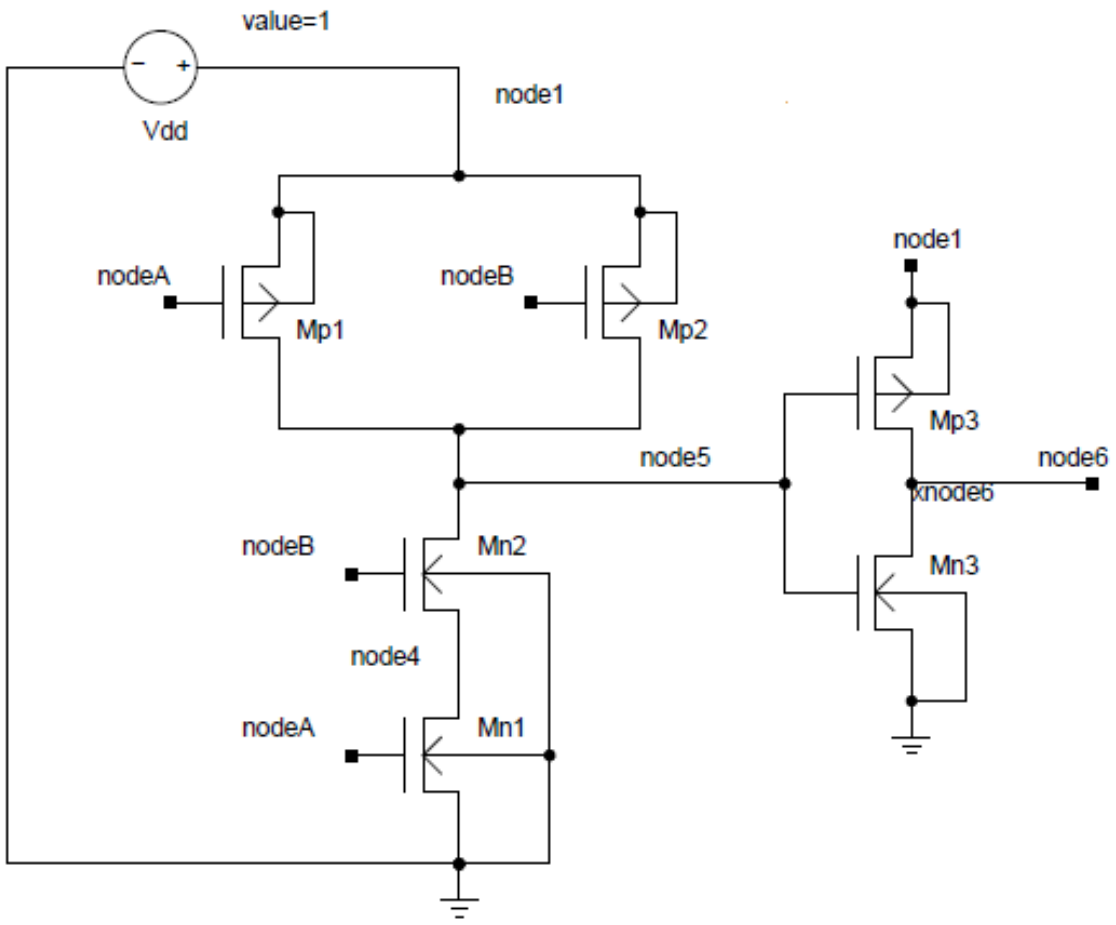
ps/fF or ns/pF


Vdd
node1
nodeA
Mp1
nodeB
Mp2
nodeB
Mn2
node4
nodeA
Mn1

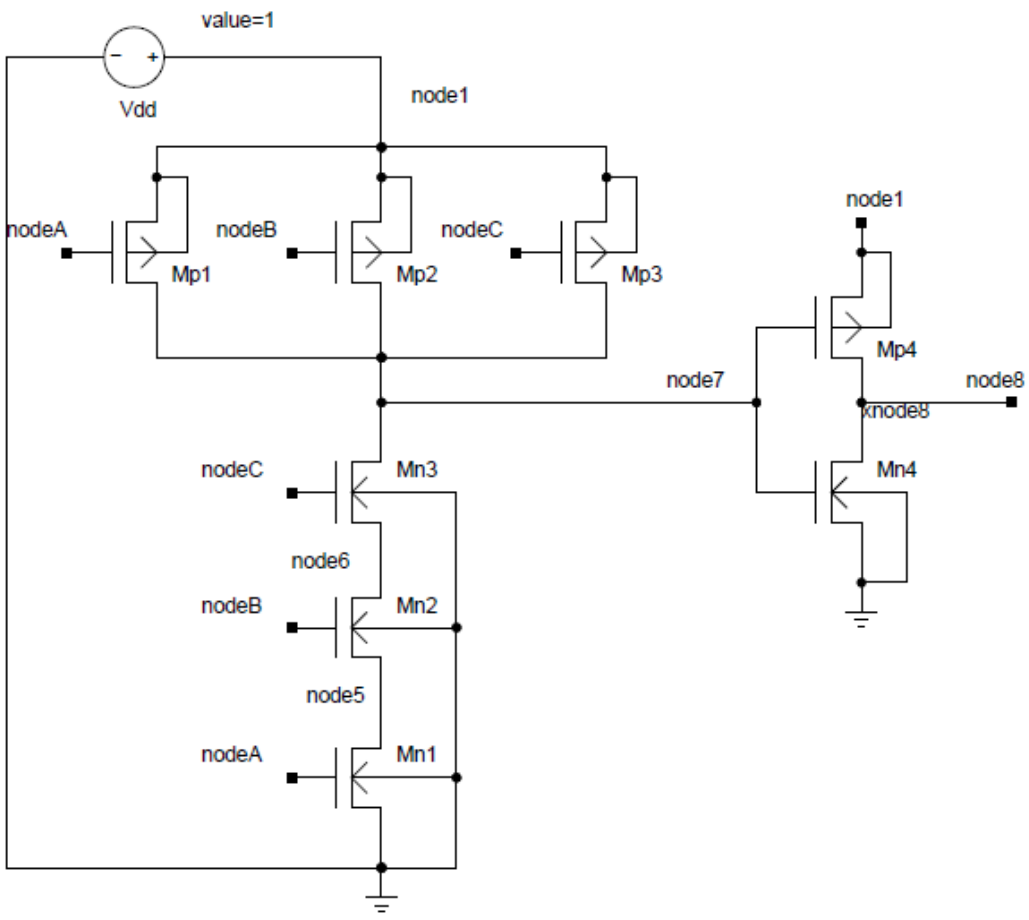
NAND2


Vdd
nodeA
Mp1
node4
nodeB
Mp2
nodeA
Mn1
nodeB
Mn2

NOR2

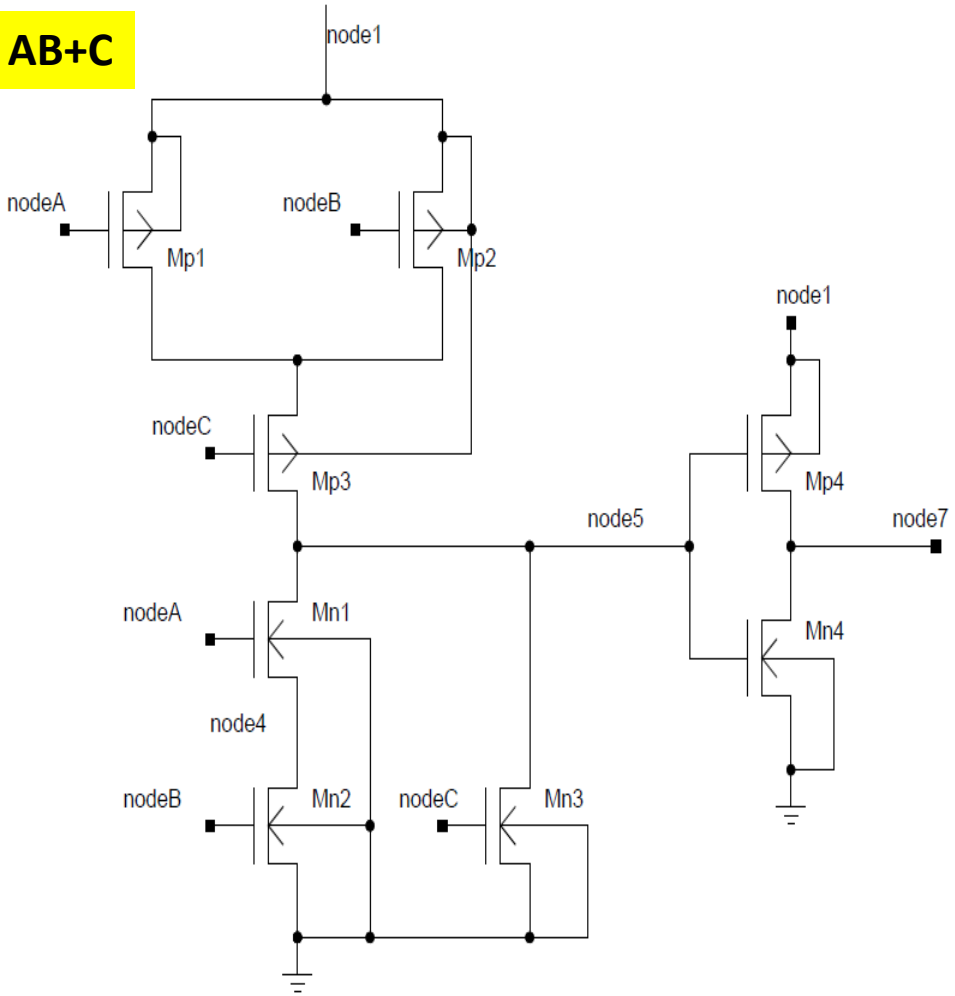

value=1
Vdd
node1
nodeA
Mp1
nodeB
Mp2
node1
Mp3
node5
node6
xnode6
nodeB
Mn2
Mn3
node4
nodeA
Mn1

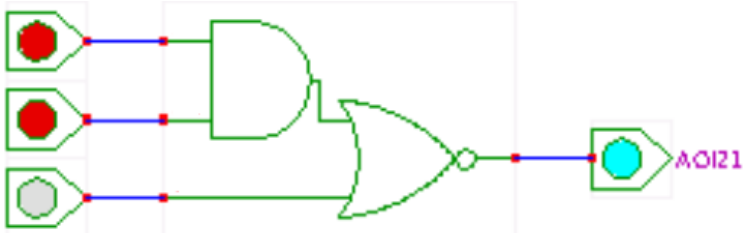
AND2


value=1
Vdd
node1
nodeA
Mp1
nodeB
Mp2
nodeC
Mp3
node1
Mp4
node7
node8
xnode8
nodeC
Mn3
Mn4
node6
nodeB
Mn2
node5
nodeA
Mn1

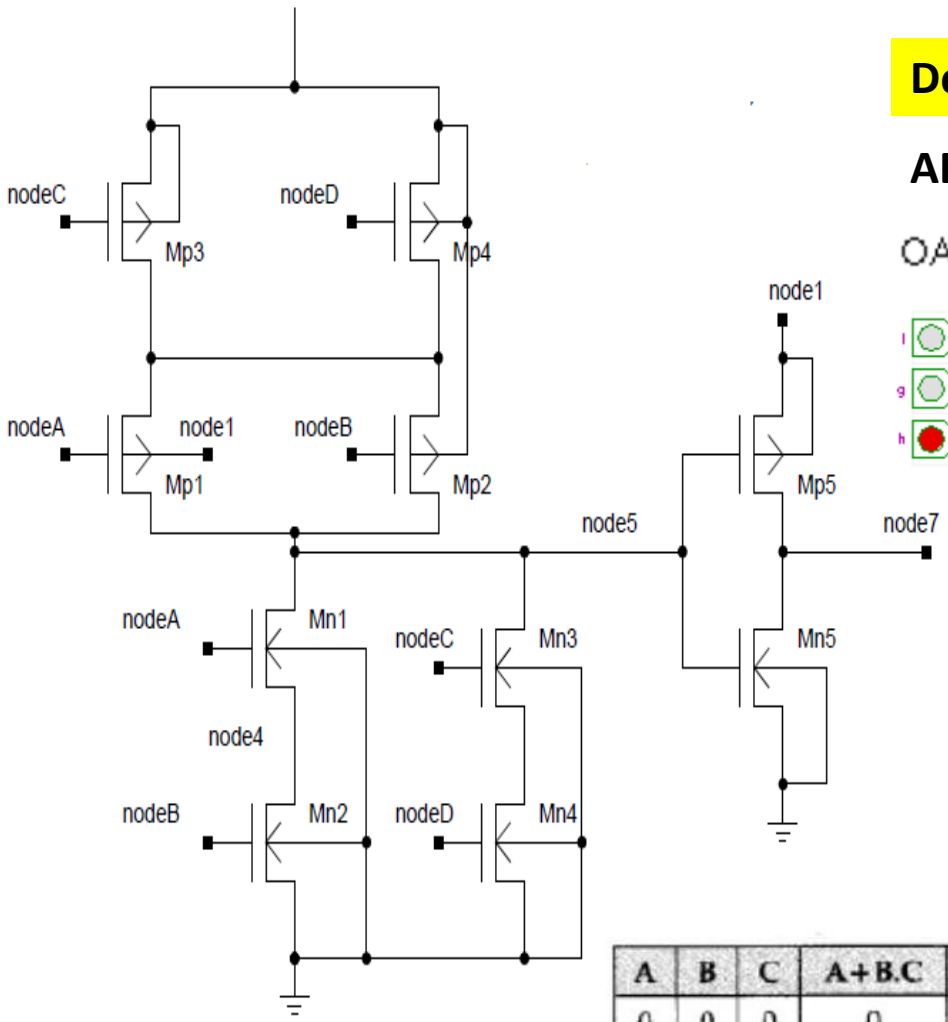
AND3

AB+C





AO12

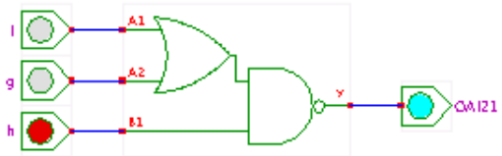


AO22

Design

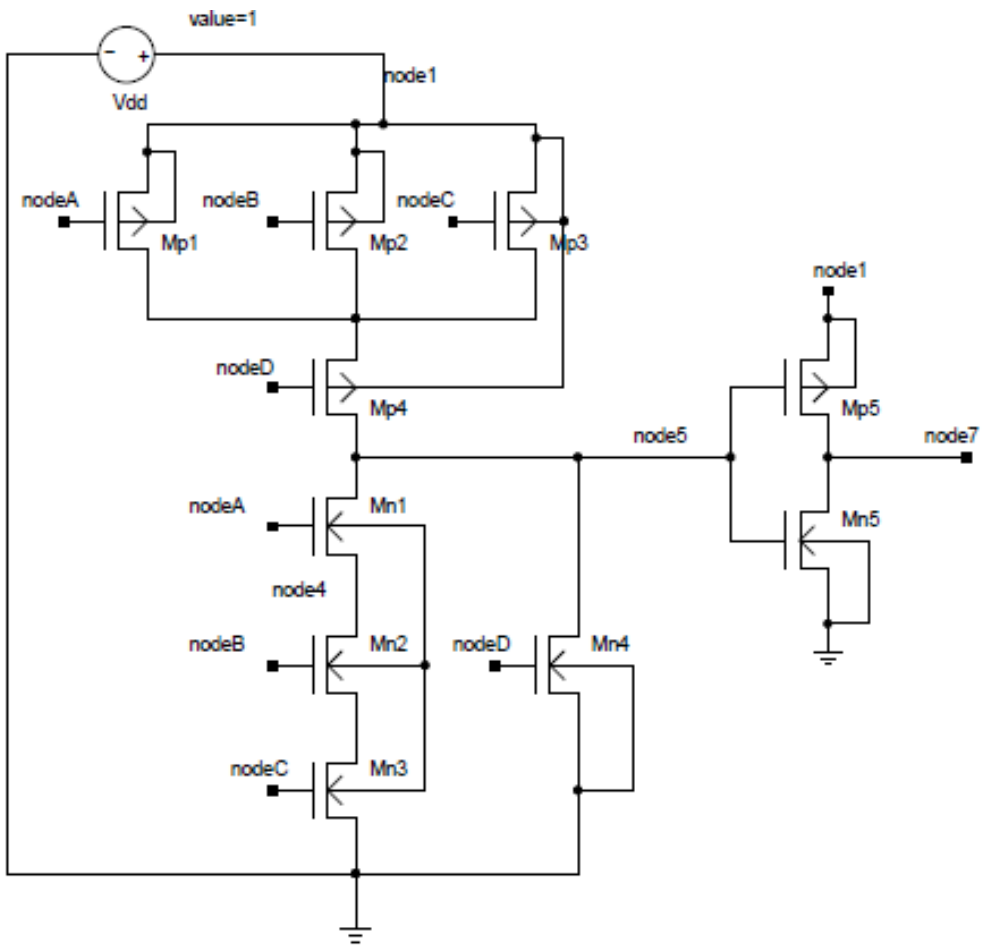
ABC+DE

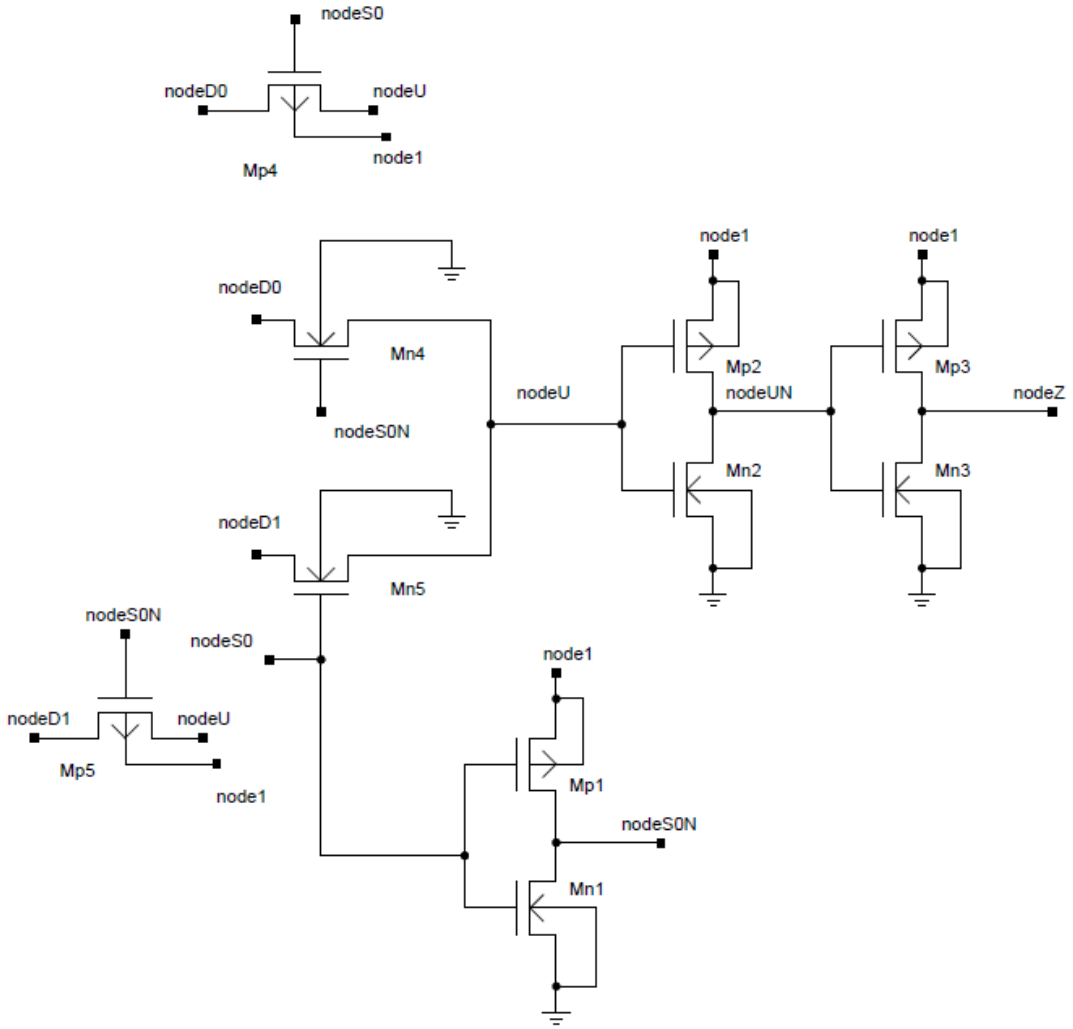
OAI21 (Or-And-Invert)



A	B	C	A+B.C	A+B	A+C	(A+B).(A+C)
0	0	0	0	0	0	0
0	0	1	0	0	1	0
0	1	0	0	1	0	0
0	1	1	1	1	1	1
1	0	0	1	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

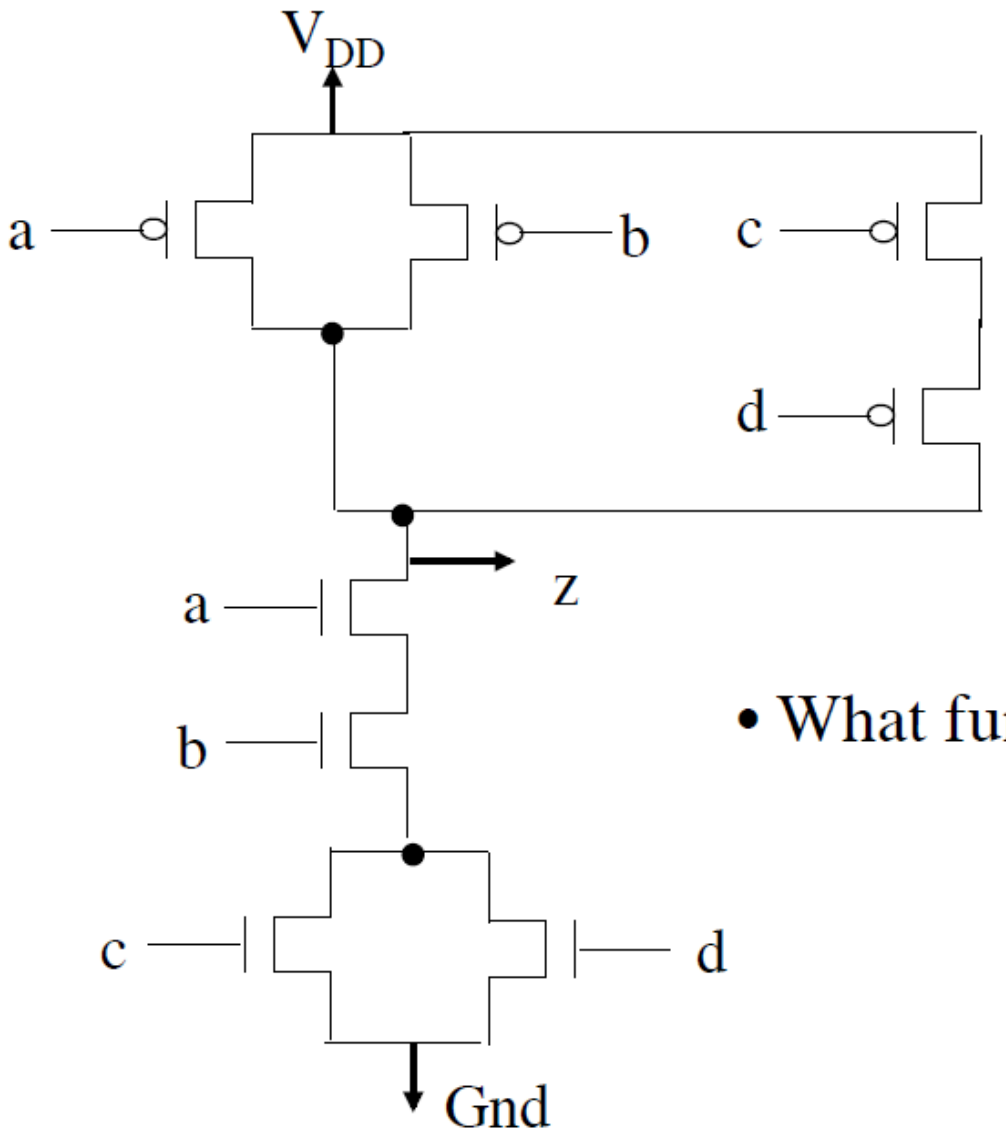
AO31





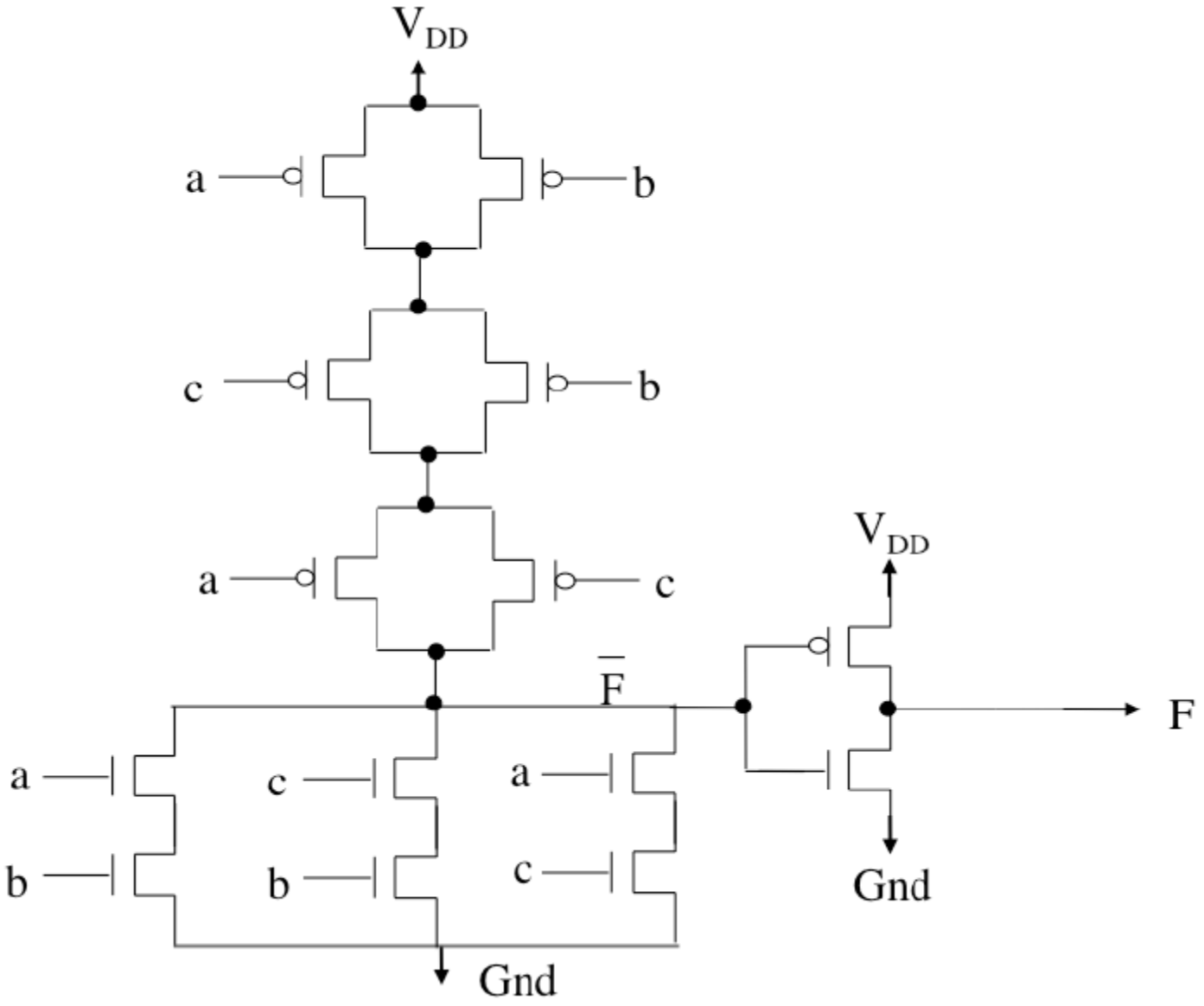
2:1 MUX

How to design? $Y = \overline{(A + B + C) \cdot D}$



- What function is implemented by this circuit?

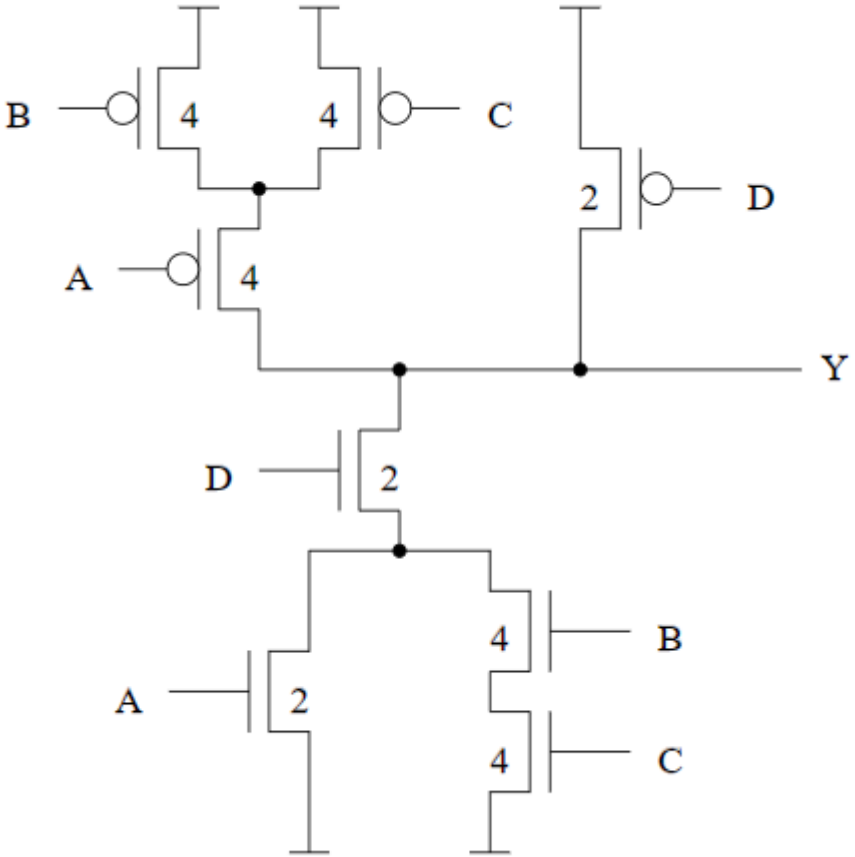
How to implement
$F = ab + bc + ca$?

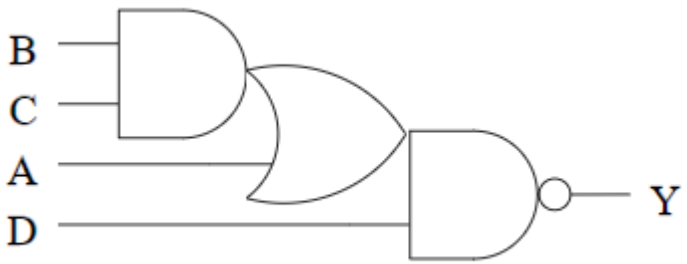


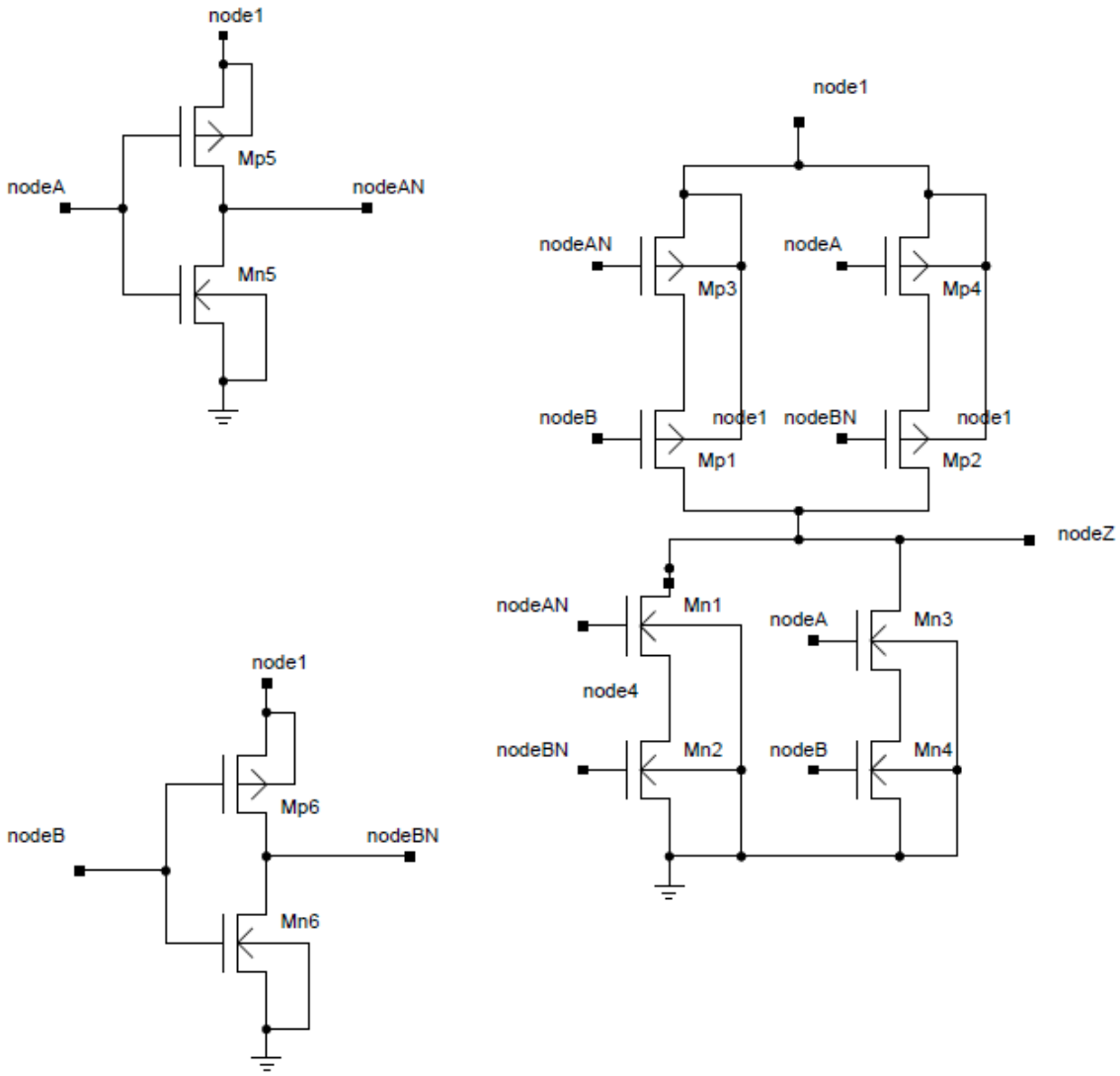
Besides the AOI and OAI gates for complemented two-level normal forms, we can design compound gates for multilevel expressions as well. For example, Boolean expression

$$Y = \overline{(A + BC) \cdot D}$$

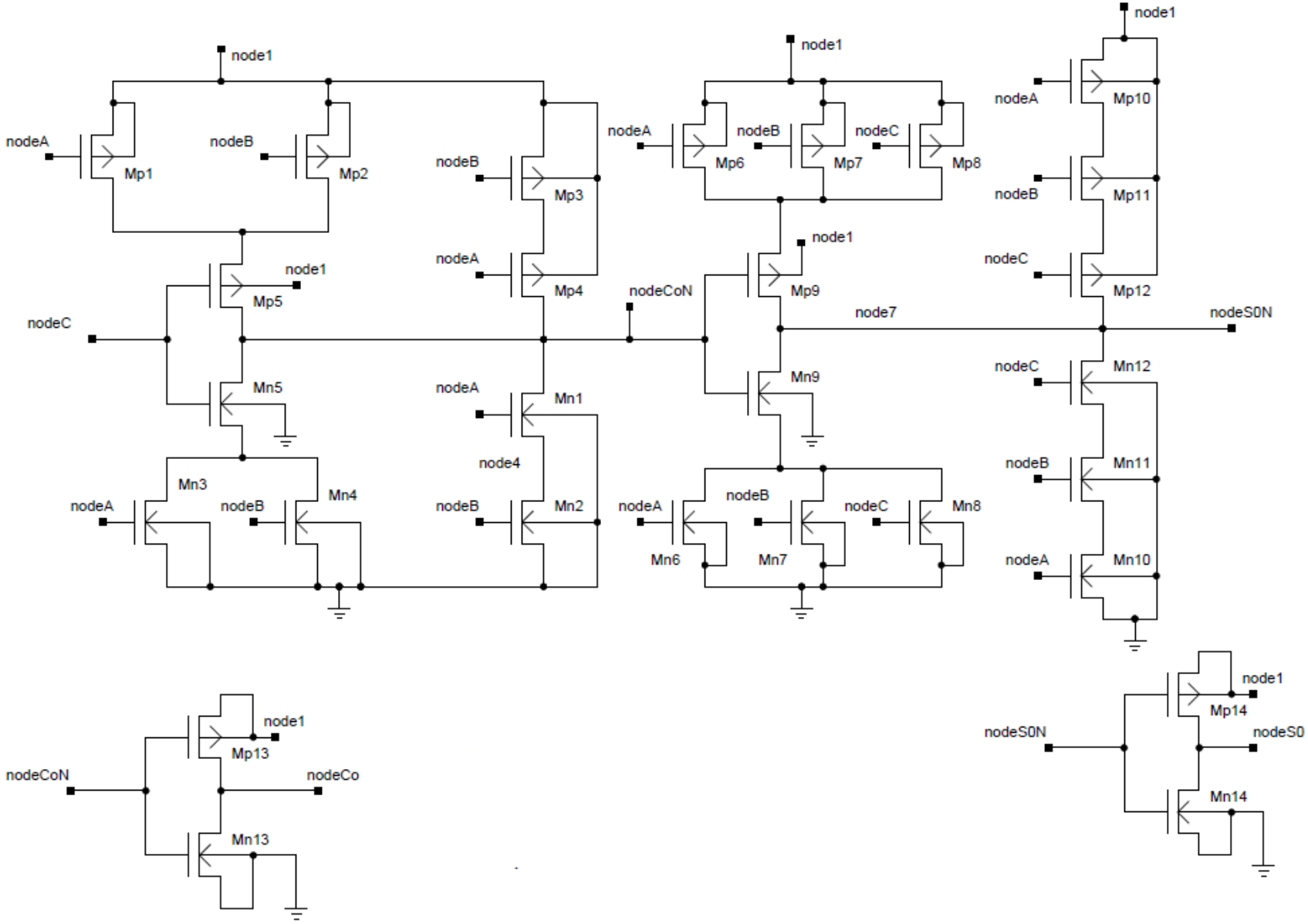
has a pull-down network consisting of a series composition of D and a parallel composition of A and a series composition of B and C.



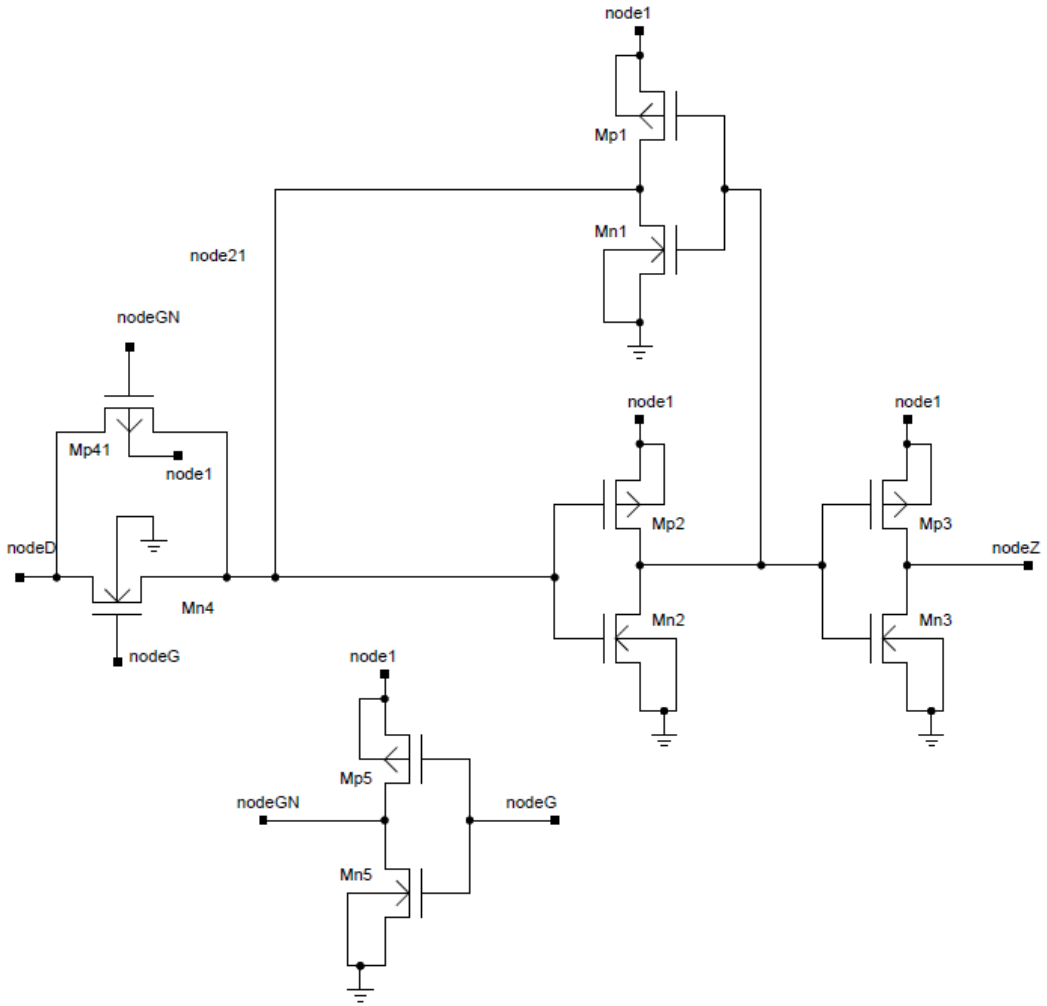



node1
Mp5
nodeA
nodeAN
Mn5
node1
nodeAN
nodeA
Mp3
Mp4
nodeB
node1
nodeBN
node1
Mp1
Mp2
nodeZ
nodeAN
Mn1
nodeA
Mn3
node4
nodeBN
Mn2
nodeB
Mn4
node1
Mp6
nodeB
nodeBN
Mn6

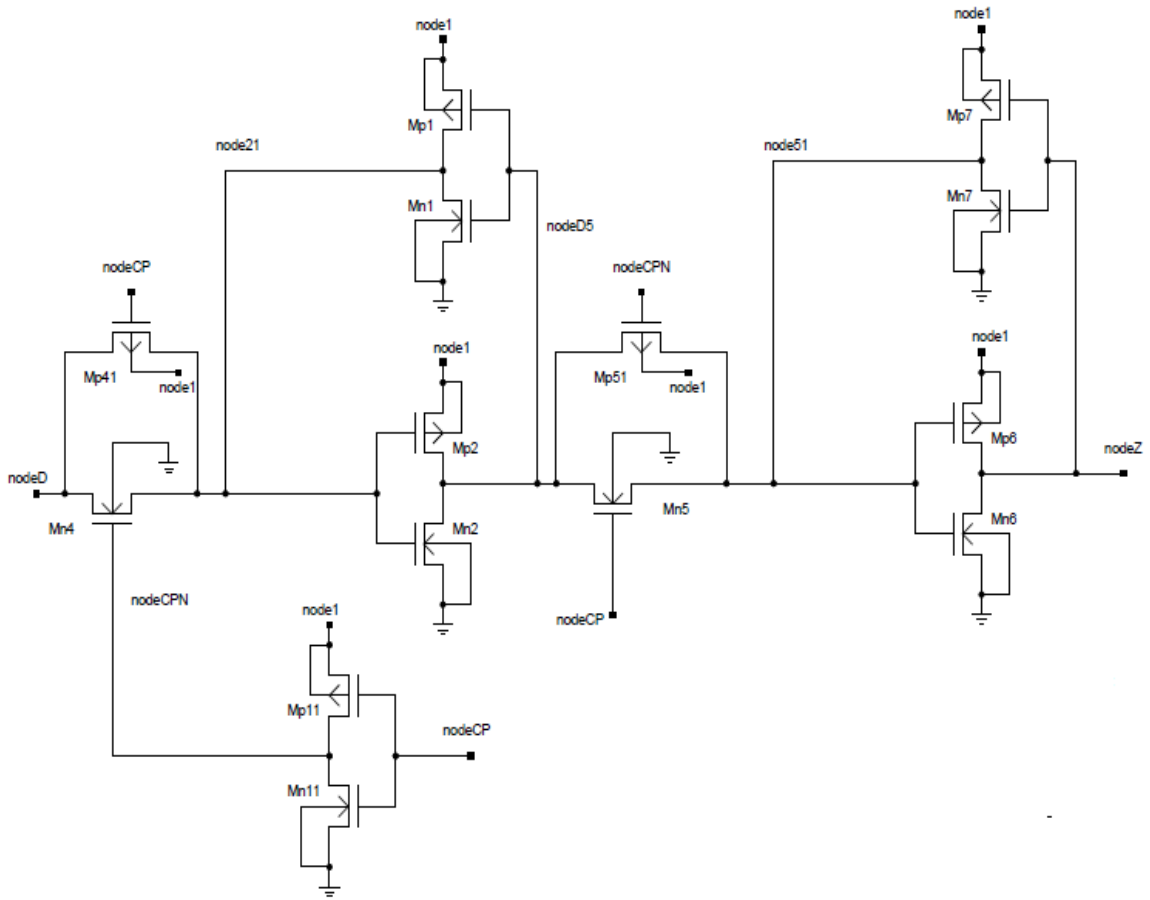
XOR2


node1
nodeA
nodeB
Mp1
Mp2
Mp3
Mp4
Mp5
nodeC
Mn5
Mn3
Mn4
Mn1
Mn2
node4
nodeCoN
Mp6
Mp7
Mp8
Mp9
node7
Mn9
Mn6
Mn7
Mn8
Mp10
Mp11
Mp12
nodeS0N
Mn12
Mn11
Mn10
Mp13
nodeCo
Mn13
Mp14
nodeS0
Mn14

Full Adder


node1
Mp1
Mn1
node21
nodeGN
Mp41
node1
nodeD
Mn4
nodeG
node1
Mp2
Mn2
node1
Mp3
Mn3
nodeZ
node1
Mp5
nodeGN
nodeG
Mn5

LDHQ


node1
Mp1
Mn1
node21
nodeD5
nodeCP
Mp41
node1
nodeD
Mn4
nodeCPN
node1
Mp2
Mn2
nodeCPN
Mp51
node1
Mn5
nodeCP
node51
node1
Mp7
Mn7
node1
Mp6
Mn6
nodeZ
node1
Mp11
nodeCP
Mn11

DFPQ