EE301 - ANALOG CIRCUIT

WORKING PROJECT :

Design of cascode amplifier and cascode current mirror in schematic and layout using LTspice and Magic tools in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (supply 0.8 V)technology node to see the effect of lowering the technology node.

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1.Introduction: The block diagram for the single-stage cascode amplifier with required biasing network . The cascode amplifier requires a biasing circuit which includes the beta multiplier and cascode current mirror circuits. The beta multiplier circuit provides the input to the cascode current mirror and cascode amplifier. One capacitor as a load added at the output of the cascode amplifier. The Characteristics due to the cascading of amplifiers are: the impedances at input and output are high.The signals amplification undergoes under high bandwidths possessed by the system. The isolation amid input and the output is high. A brief description of every block is given below:

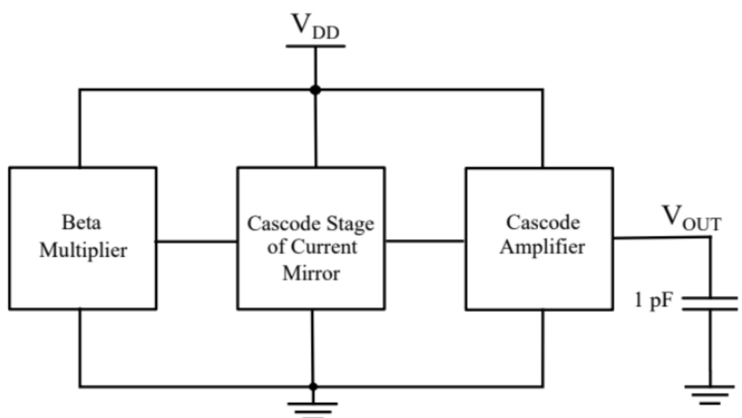


Figure 1: Block diagram of cascode amplifier with other blocks

1.1-Design of beta multiplier circuit: The beta multiplier circuit is an example of positive feedback. The beta multiplier circuit is an example of positive feedback. The resistor is added to stabilize the closed loop gain of the circuit by requiring higher VGS. The beta multiplier current reference circuit is an alternative method for (potentially) getting a PTAT-like current without utilizing bipolar transistors.

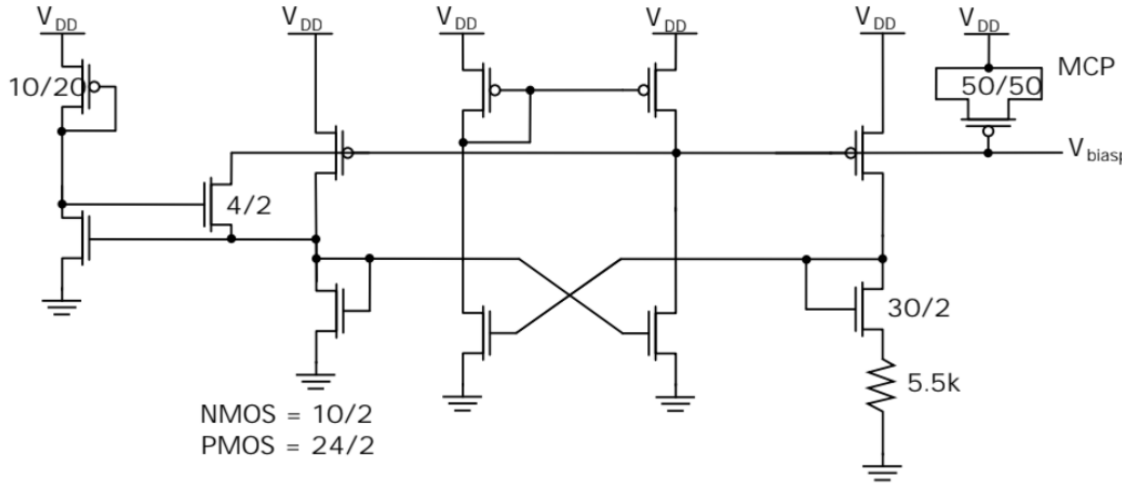


Figure 2: Circuit for beta multiplier circuit

1.2 <u>Design of cascode stage of current mirror</u>: The cascode current mirror with reference biasing circuit is shown in . The output (Vbiasp) of the beta multiplier circuit is fed to the input of the current mirror. The outputs of the circuit are Vbias1, Vbias2, and Vbias3, which are used in the cascode amplifier stage for biasing of the circuit.

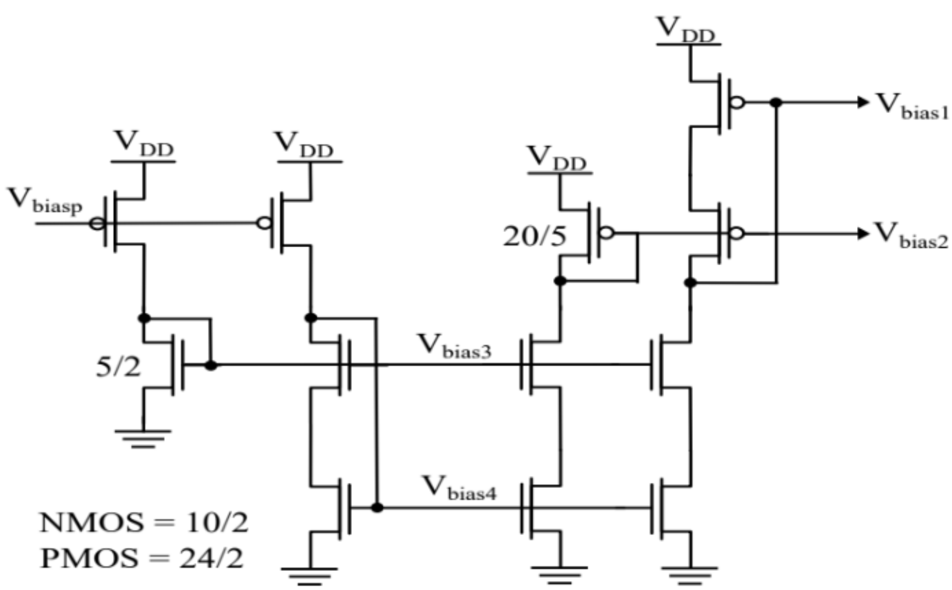


Figure 3: Circuit for cascode current mirror

1.3 <u>Cascode amplifier</u>: A cascode amplifier is also named the "telescopic" cascode. It consists of a common source stage (CS) with a common gate stage (CG). Compared to a single amplifier stage,this combination may have one or more characteristics: higher input-output isolation, higher input impedance, high output impedance, and higher bandwidth. The stability of the cascode amplifier is another essential aspect that has to be covered. The cascode design is a stable configuration itself. The bottom transistor's source and drain terminals have virtually constant voltage levels, and there's nothing to provide gate feedback. Whereas the higher transistor likewise keeps the source and gate terminal voltages constant. There are only output and input nodes with the appropriate voltage values.

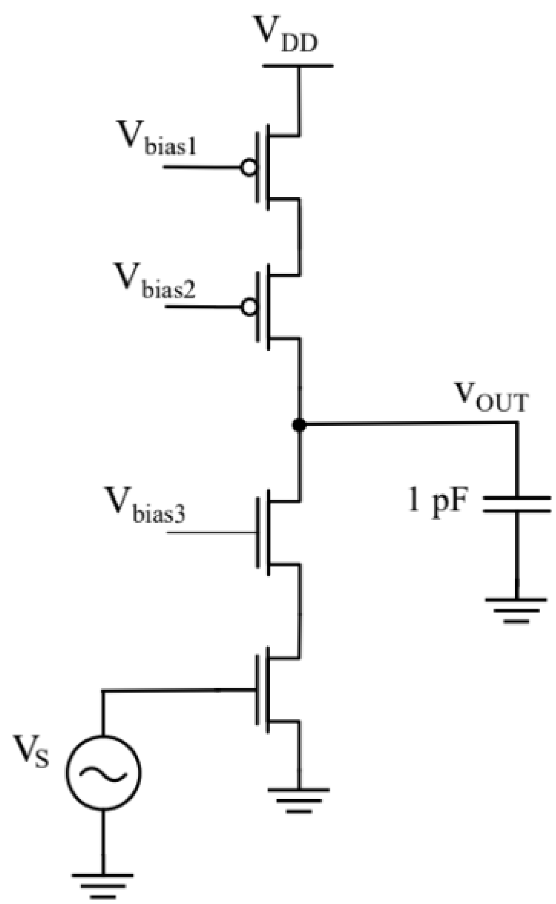
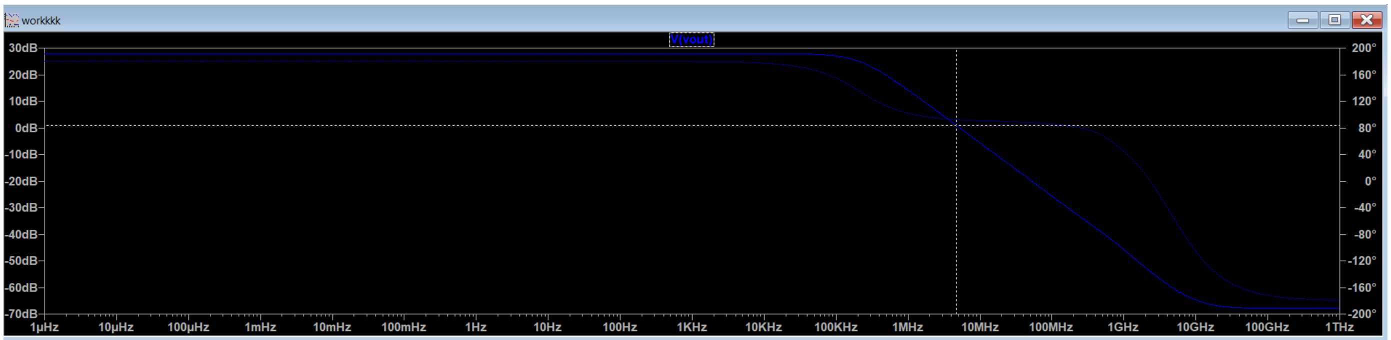
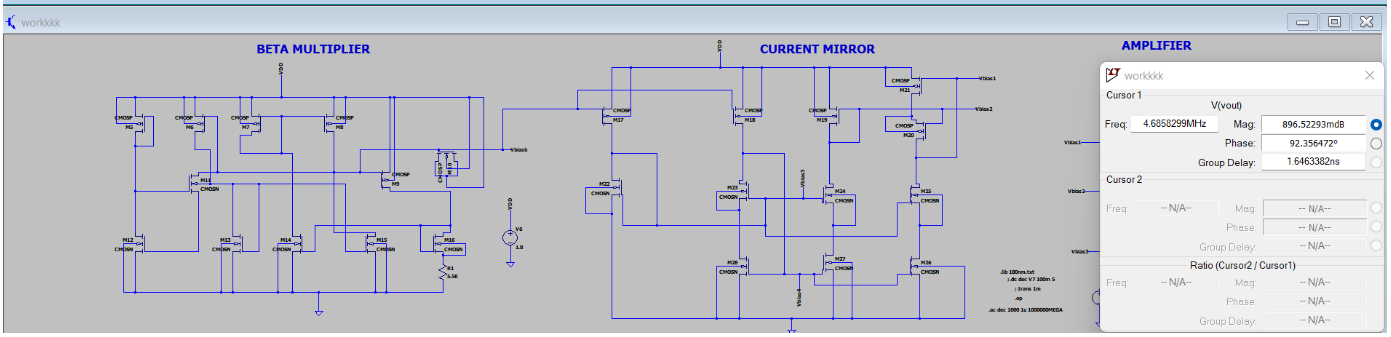


Figure 4: Circuit for cascode amplifier

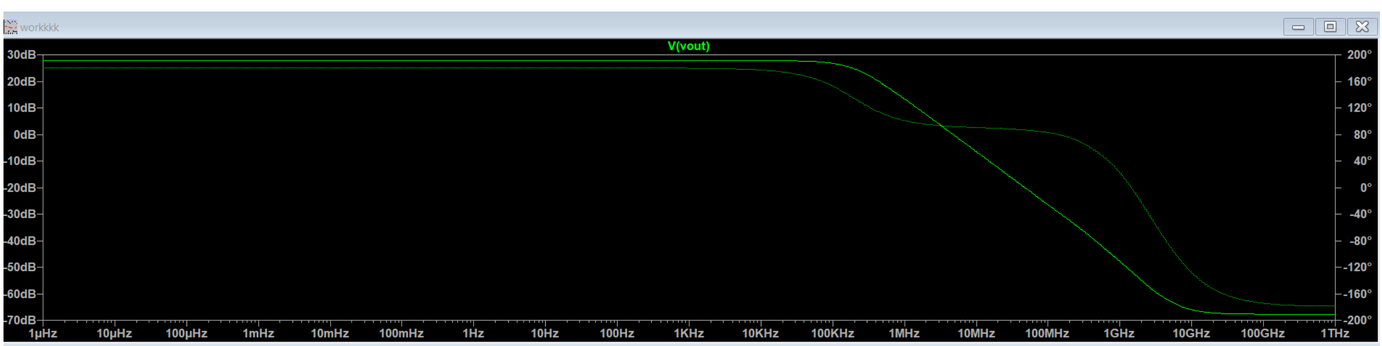
2.Using the LT spice we are getting graphs :-

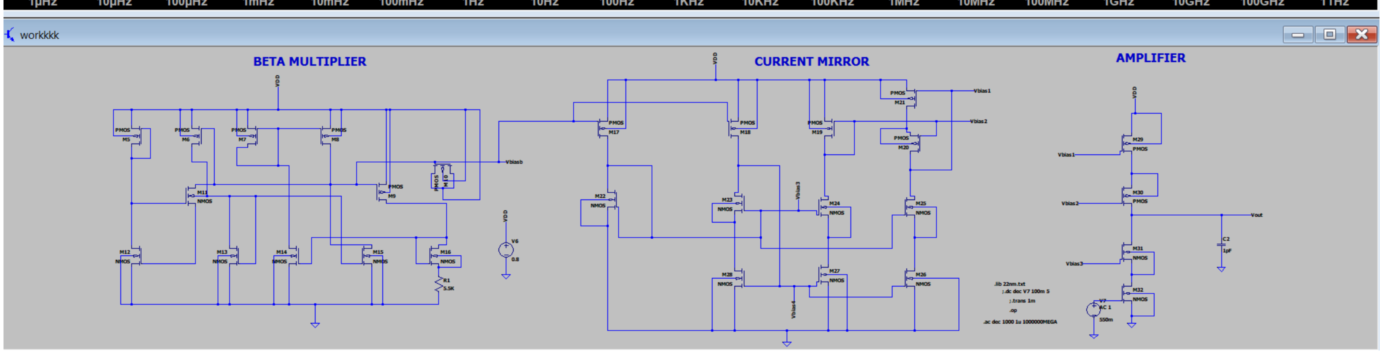
<u>Frequency response of 180nm :-</u>





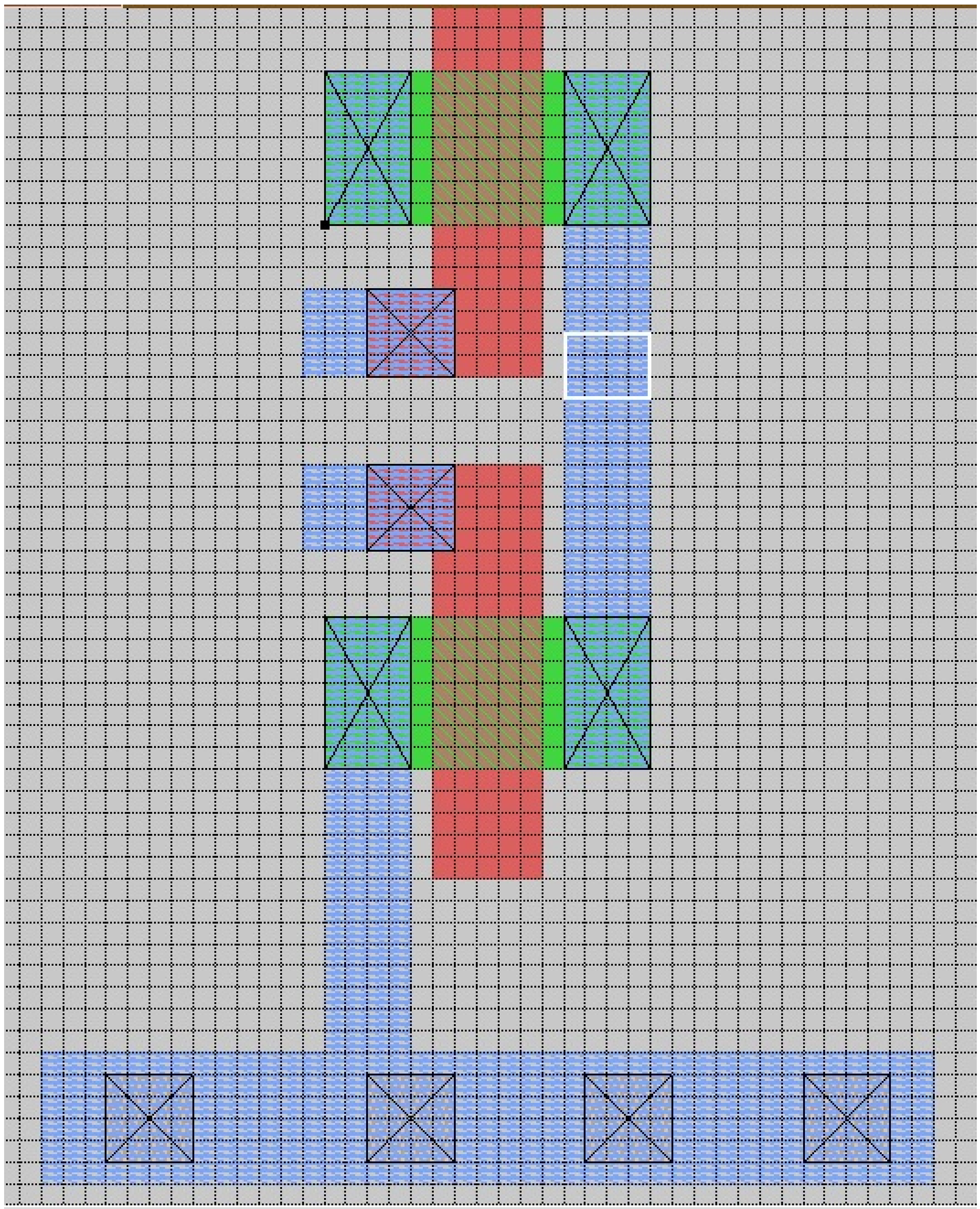
<u>Frequency response of 22nm :-</u>



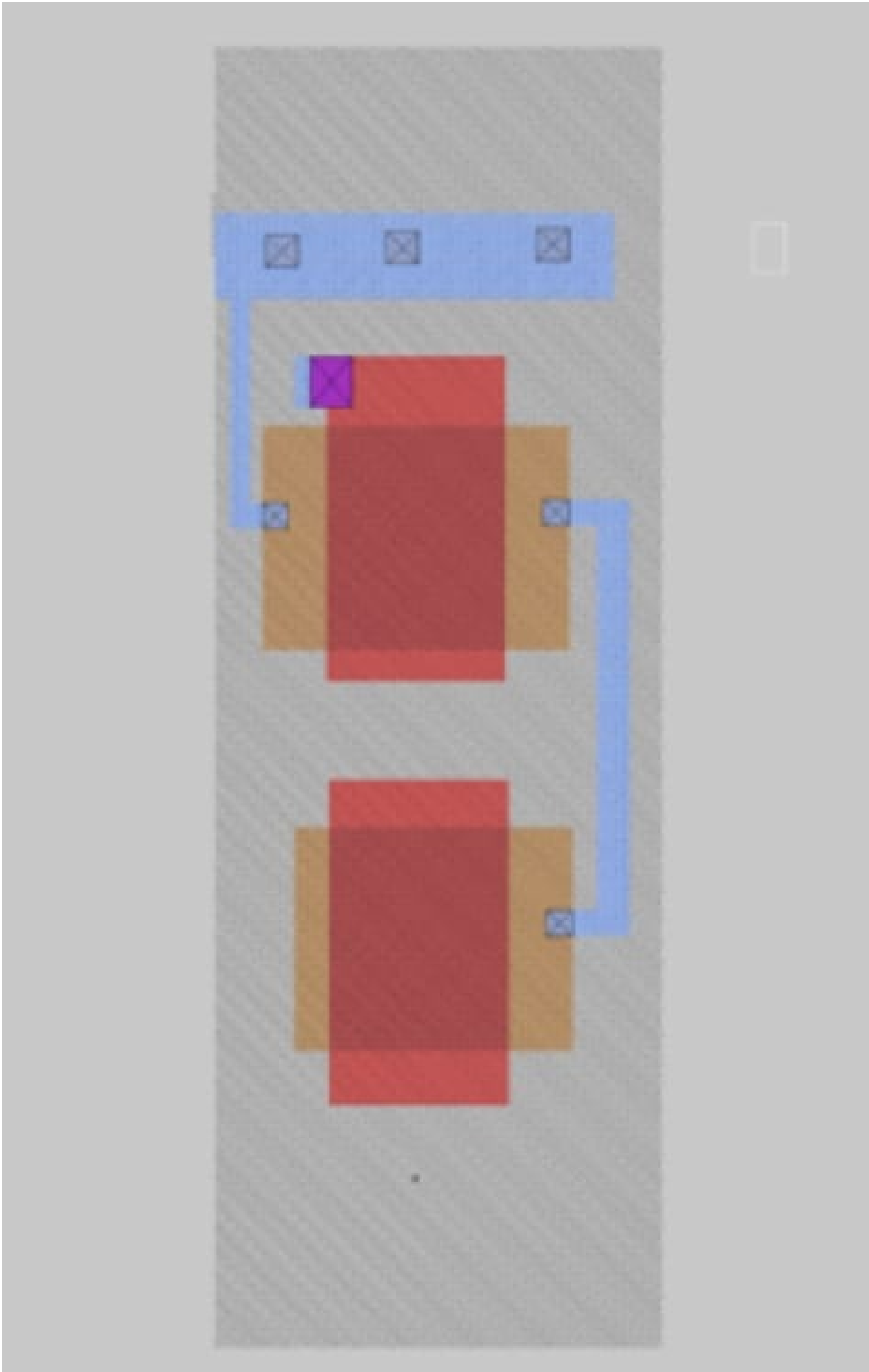


We got the magic of p mos and n mos here :-

Nmos here for 630 width and 450 is :-



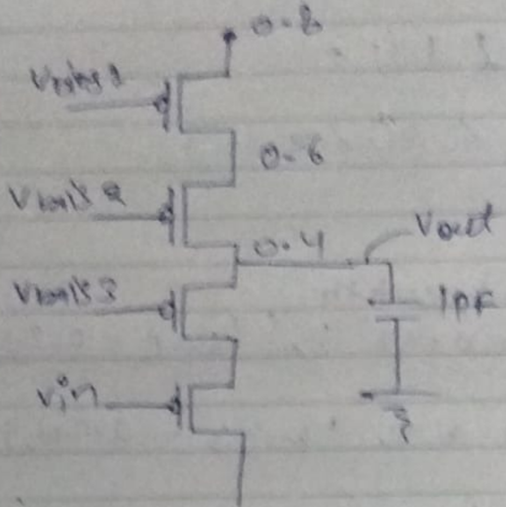
For 450 lengths and 810 pmos magic here :



Calculation

For 22 nm is :-

circuit for Cascade Amlifier calculation :-



for (22nm)

Accordingly to qustion all mosfet are saturation resion so —

$V_{th} = 0.503$ (NMOS)
$V_{th} = -0.4606$ (PMOS)

we know saturation condition is ($V_{DS} \geq V_{GS} - V_{th}$)

for Mosfet to operate ($V_{GS} > V_{th}$)
for biasing voltage

NMOS :- (for)

$V_{DS} \geq V_{GS} - V_{th}$
$0.2 - 0 \geq V_{in} - 0.503$

$V_{in} \leq 0.703$ —(i)

$V_{GS} > V_{th}$
$V_{in} > 0.503$ — (ii)

from (i) & (ii) —

$0.503 < V_{in} < 0.703$
similarly

$V_{DS} \geq V_{GS} - V_{th}$
$(0.4 - 0.2) \geq (V_{bais3} - 0.2) - 0.503$

$0.2 \geq V_{bais3} - 0.703$

$V_{bais} \leq 0.903$ — (iii)

here $V_{GS} > V_{th}$
$V_{baiS} - 0.2 > 0.503$

$V_{bais3} > 0.703$ — (iv)

(iii) & (iv)
$0.703 < V_{bais3} \leq 0.903$
all for nMOS,

Calcution of V_{bais3} & V_{bais4} :-

$V_{SD} \geq V_{SG} - V_{th}$
$0.6 - 0.4 \geq 0.6 - V_{baisa} - 0.4606$

$V_{bais2} \geq -0.0606$ — (v)

$V_{SG} \geq V_{th}$

$0.6 - V_{bias} \geq 0.4606$

$0.6 - 0.4606 \geq V_{bias2}$

$0.1394 \geq V_{bias2}$

$V_{bias2} \leq 0.1394$ — (VI)

(V) & (VI)

$-0.0606 \leq V_{bias2} \leq 0.1394$

$V_{SD} \geq V_{SG} - V_{th}$

$(0.8 - 0.6) \geq (0.8 - V_{bias1}) - 0.4606$

$V_{bias2} \geq 0.1394$ — (VII)

$V_{SG} \geq V_{th}$

$(0.8 - V_{bias1}) > 0.4606$

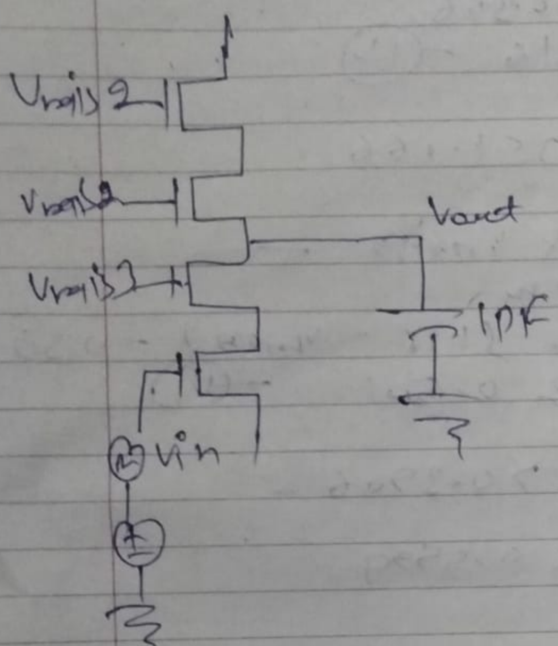
$0.3394 < V_{bias1}$ — (VIII)

(VII) & (VIII)

$0.1394 < V_{bias} < 0.3394$

For 180 nm

Circuit for cascode amplifier



for the 180nm V_n is given equal 1.8 V

Saturation cond is —

$V_{DS} \geq V_{GS} - V_{tn}$

$V_{GS} > V_{tn}$ (MOSFET)

finding Vbias & Vin —

$V_{DS2} \geq 0.9 - 0.3906$

$0.45 \geq V_{in} - 0.366$

$V_{in} \leq 0.816$ — (I)

$V_{GS} > V_{tn}$ $\quad V_{in} > 0.366$ — (II)

(I) & (II) using we get

$0.366 < V_{in} < 0.816$

sat condition — $V_{DS} \geq V_{GS} - V_{tn}$

$0.9 - 0.45 \geq (V_{bias3} - 0.45) - 0.366$

$V_{bias} \leq 1.266$ — (IV)

$V_{vg} > V_{tn}$

$(V_{rais3} - 0.45) > 0.366$

$V_{bais3} > 0.816$ — (IV)

(III) & (IV)

$0.816 \le V_{bais3} \le 1.266$

Calcution V_{bais2} & V_{rais2} —

$V_{SD} \geq V_{SG} - V_{tn}$

$(1.35 - 0.77) \geq (1.35 - V_{bais2}) - 0.39$

$V_{bais2} \geq 0.591$ — (VI)

$V_{SG} > V_{tn}$

$1.35 - V_{bais2} > 0.3906$

$V_{bais2} < 0.9594$

For bais 2

$V_{SD} \geq V_{SG} - V_{tn}$

$(1.8 - 1.35) \geq (1.8 - V_{bais2}) - 0.3906$

$V_{rais2} \geq 0.9594$ — (VII)

$V_{SG} > V_{tn}$

$1.8 - V_{bais3} > 0.3906$

$V_{rais2} < 1.8 - 0.3906$

$V_{bais} < 1.4094$ — (VIII)

(VII) & (VIII) we get

$0.9594 \le V_{bais2} < 1.4094$

4.Conclusion :-

1. Analysis of the cascode amplifier in schematic and layout using LT spice and magic tools in 180 nm(Vth =0.5v and supply 1.8) technology .
2. Analysis of the current mirror in schematic and layout using LT spice and magic tools in 180 nm (Uncox = 250-350 micro & 150-200 micro)technology .
3. We are making the circuit so that our gain Av should be greater than or equal to 26db.
4. We are getting the gain according to my LT spice circuit was Av=27.8 and frequency response act as band pass filter (fc = 5.14MHZ)