B.Tech III Year 5th Semester

Year(2022)

Branch ECE

Subject : Microelectronics **Class test : II**

Time : 1Hour **M.M : 20**

Note : Attempt All question

1: (a) Explain avalanche and Zener breakdown mechanism with the help of suitable energy band diagrams? (b) What is the root cause of the delay in switching from the on-state to off-state of a P-N junction diode? Further, define storage delay time and recovery time.

2: (a) Explain the working I-V characteristics of Tunnel diode with the help of energy band diagram? (b) Given a pnp BJT where Iep=1mA, IEn=0.01mA, Icp=0.98A and Icn=0.1μA. Calculate (i) αT (ii) IE, IB, IC (iii) γ (iv) ICBO and ICEO

3: (a) Why is it necessary for base region in a BJT to be narrow? What is the precise definition of narrow? (b) The given figure is a dimensioned energy band diagram for an ideal MOS capacitor operated at T=300K with VG≠0 . Note that EF =Ei at the Si-SiO2 interface. Calculate (i) $_{\phi}$F (ii) $_{\phi}$S (iii) VG (iv) Depletion width(x0) (v) Do the equilibrium condition prevail inside the semiconductor ?