



Experiment : 5

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Branch: CSE

Semester: 4th

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UID: 19BCS1696

Section/Group: 5/C

Subject Name: MPI lab

Subject Code: CSP-277

1. Aim/Overview of the practical: 1's complement of 8 bit number, 2's complement of 8 bit number

2. Task to be done: Finding 1's and 2's compliment of 8 bit numbers

3. Apparatus/Simulator used (For applied/experimental sciences/materials)

Jubin 8085 simulator used.



4. Algorithm/Flowchart (For programming based labs):

There is a simple algorithm to convert a binary number into 1's complement. To get 1's complement of a binary number, simply invert the given number. You can simply implement logic circuit using only NOT gate for each bit of Binary number input. Implementation of logic circuit of 4-bit 1's complement is given as following below.

5. Description/ Code:

1's complement of 8 bit number

```
LDA 7500H  
CMA  
STA 7000H  
HLT  
#ORIGIN 7500H  
#DB 85H
```

2's complement of 8 bit number

```
LDA 7500H  
CMA  
INR A  
STA 7000H  
HLT  
#ORIGIN 7500H  
#DB 85H
```

6. Result/Output/Writing

Summary: 1's complement of 8
bit number

8085 Simulator

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor Assembler Registers Memory Devices

Assembler

* Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
✓ 0000		LDA 7500	3A	3	4	13
0001			00			
0002			75			
✓ 0003		CMA	2F	1	1	4
✓ 0004		STA 7000	32	3	4	13
0005			00			
0006			70			
✓ 0007		HLT	76	1	2	5

Simulate

Start From → 0000

Backward Stop Forward

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	7A	0	1	1	1	1	0	1	0
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(H)	3A	0	0	1	1	1	0	1	0

Register	Value	S	Z	*	AC	*	P	*	CY
Flag Register	00	0	0	0	0	0	0	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	7A00
Program Counter(PC)	0007
Clock Cycle Counter	35
Instruction Counter	4

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0	0	0

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2's complement of 8 bit number

8085 Simulator

File Edit Tools Settings Simulation Subroutine View Load Sample Program Help

Editor Assembler Registers Memory Devices

Assembler

* Address	Label	Mnemonics	Hexcode	Bytes	M-Cycles	T-States
✓ 0000		LDA 7500	3A	3	4	13
0001			00			
0002			75			
✓ 0003		CMA	2F	1	1	4
✓ 0004		INR A	3C	1	1	4
✓ 0005		STA 7000	32	3	4	13
0006			00			
0007			70			
✓ 0008		HLT	76	1	2	5

Simulate

Start From → 0000

Backward Stop Forward

Registers :

Register	Value	7	6	5	4	3	2	1	0
Accumulator	7B	0	1	1	1	1	0	1	1
Register B	00	0	0	0	0	0	0	0	0
Register C	00	0	0	0	0	0	0	0	0
Register D	00	0	0	0	0	0	0	0	0
Register E	00	0	0	0	0	0	0	0	0
Register H	00	0	0	0	0	0	0	0	0
Register L	00	0	0	0	0	0	0	0	0
Memory(M)	3A	0	0	1	1	1	0	1	0

Register	Value	S	Z	*	AC	*	P	*	CY
Flag Register	04	0	0	0	0	0	1	0	0

Type	Value
Stack Pointer(SP)	0000
Memory Pointer (HL)	0000
Program Status Word(PSW)	7B04
Program Counter(PC)	0008
Clock Cycle Counter	127
Instruction Counter	17

SOD	SID	INTR	TRAP	R7.5	R6.5	R5.5
0	0	0	0	0	0	0

For SIM instruction

SOD	SDE	*	R7.5	MSE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

For RIM instruction

SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
0	0	0	0	0	0	0	0

No. Converter Tool :

Hexadecimal	Decimal	Binary
0		0

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Learning outcomes (What I have learnt):

1. Learned about 1's compliment
2. Learned about 2's compliment
3. Learned about how to work on Jubin.

Evaluation Grid (To be created as per the SOP and Assessment guidelines by the faculty):

Sr. No.	Parameters	Marks Obtained	Maximum Marks
1.			
2.			
3.			