Simulation Results:

To analyse various performance parameters, simulation has been conducted on GPDK 180nm technology using Cadence simulation tools. The post-layout simulation was carried out using the Analog Design Environment-L for the av-extracted view. Consequently, the worst case delay, average power dissipation and Power-Delay product were calculated at 1.2V (normal operating voltage), as tabulated below:

Full Adder Design	Transistor Count	Average Power Dissipation	Worst Case Delay	PDP
TGA	20	10.692 uW	15.345 ns	164.069 fJ
GDI D1	18	6.612 uW	17.851 ns	118.031 fJ
TFA	16	6.370 uW	15.393 ns	98.053 fJ
12-T	12	11.492 uW	19.985 ns	229.668 fJ

From the simulation results, we conclude that the average power dissipation is lowest for TFA with a transistor count of 16 with an appreciable delay of 15.393 ns. The best PDP so far is that of the TFA (16-T) with a value of 98.053 fJ.