I2C integration to MCU

Steps to communicate Driver with MCU:

1. Initialize I2C Bus with slave address - 0x7C
2. Initialize Driver
   * Send Start Bit
   * Send Dummy data- 8 byte high data
   * Send Stop Bit
   * Repeat step 1-2-3 again.
   * Send start Bit
   * Send Slave Address
   * Send control byte sequence -0x00 to send commands. Control Byte is always send just after slave address send to tell next byte is data or command to read or write
   * Send extension mode bits – 0xFD, enter to extension mode to mode control and software reset
   * Send software reset bits – 0x91 so BU91R64CH-M will be reset to initial condition
   * Send Stop bit
   * Send start bit
   * Send control byte – 0x00
   * Set MODSET1 to display off – so that Regardless of DDRAM data, all Segment and Common output will be stopped (VSS level).
   * Enter to extension mode
   * Set MODSET2- disable Glass breaking detection, Checksum detection, Logic error detection, SEG / COM toggle detection
   * Set MODSET3 bits- set Line Inversion, Frame frequency in Normal Frequency Mode
   * Set Contrast set by selecting VLCD voltage level = here max contrast is selected = 0xB0
   * Disable read setting using RDCTL register = 0xC0
   * Select COM for Toggle Order of COM0 to COM3
   * Enter to normal mode to set frame frequency, blink command, give write access and set address and sub address
   * Send frame frequency = 155.3Hz
   * Send blink off byte = 0xF0 for all Segments Blink Mode with blink frequency off
   * Send data write access for normal display area to write in DDRAM = 0xF8
   * Send Sub Address Set - Set sub address to define one of BU91R6xCH sub address to 0xE0 for Master/slave1
   * Send Address Set - DDRAM Address Setting to 0x00 – in reset initialization condition
   * Send stop bit
   * Send start bit
   * Send slave address
   * Send control byte = 0x40 to send data seuqence
   * Send Data sequence in group of 8 bits from 00h to 4Fh
   * Send stop signal
   * Send start bit
   * Send slave address
   * Send display ON bits - Segment and Common output will be active and will start to read the Display Data from DDRAM.
   * Send stop condition
3. Modify Data

* Send start bit
* Send control byte – 0x00
* Display Off
* Enter to extension mode
* Set MODSET2, MODSET3 bits
* Set VLCD voltage level
* Disable read setting
* Select COM
* Enter to normal mode
* Send frame frequency = 155.3Hz
* Send blink off byte
* Send data write access
* Send Sub Address Set
* Send Address Set
* Send stop bit
* Send start bit
* Send slave address
* Send control byte = 0x40 to send data sequence
* Send Data sequence in group of 8 bits from 00h to 4Fh
* Send stop signal
* Send start bit
* Send slave address
* Send display ON bits
* Send stop condition

1. Display OFF

* Send start condition
* Send slave address
* Send control byte
* Send display off
* Send Stop condition

1. Disable I2C bus

Details:

* SEG0 to SEG79 used with COM0 to COM3 (80\*4 = 320 segments) So from 00h to 4Fh Addresses respectively. Please check figure below.

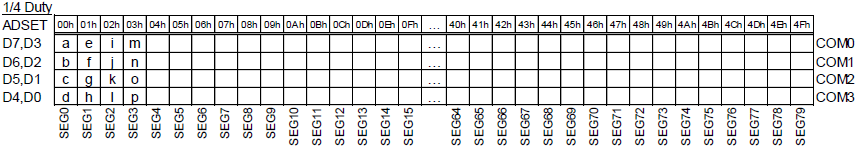


Figure 1 SEG to RAM location Mapping

* We have used SEG0 to SEG77 with COM0 to COM3(78\*4 = 312 segments)
* SEG0 is mapped on 00h, SEG1 is mapped on 01h and so on till SEG79 mapped on 4Fh.
* Whereas RAM0 is consist of 00h and 01h, RAM1 is consist of 02h and 03h, so on till RAM40 is consist of 4Eh and 4Fh.

Slave Initialization Sequence:

|  |  |  |
| --- | --- | --- |
| No. | Input | Data in hex |
| 1 | Power ON | - |
| 2 | Wait 100usec | - |
| 3 | START condition | - |
| 4 | Dummy Byte | 0xFF |
| 5 | STOP condition | - |
| 6 | START condition | - |
| 7 | Dummy Byte | 0XFF |
| 8 | STOP condition | - |
| 9 | START condition | - |
| 10 | Slave Address | 0X7C |
| 11 | Control Byte | 0X00 |
| 12 | CMDXTN | 0XFD |
| 13 | SWRST | 0X81 |
| 14 | STOP condition | - |
| 15 | START condition | - |
| 16 | Slave address | 0X7C |
| 17 | Control Byte | 0X00 |
| 18 | MODSET1 | 0XC0 |
| 19 | CMDXTN | 0XFD |
| 20 | MODSET2 | 0X90 |
| 21 | MODSET3 | 0XA0 |
| 22 | CNTSET | 0XB0 |
| 23 | RDCTL | 0XC0 |
| 24 | COMSET | 0XE0 |
| 25 | CMDXTN | 0XFC |
| 26 | FRSET | 0XEE |
| 27 | CLKCTL1 | 0XF0 |
| 28 | CLKCTL2 | 0XF8 |
| 29 | SADSET | 0XE0 |
| 30 | ADSET | 0X00 |
| 31 | STOP condition | - |
| 32 | START condition | - |
| 33 | Slave Address | 0X7C |
| 34 | Control Byte | 0X40 |
| 35 | Display Data | Send Data from 00h to 4Fh  .  .  .  .  . |
| Display Data |
| .  .  . |
| Display data |
| 36 | STOP Condition | - |
| 37 | START Condition | - |
| 38 | Slave address | 0x7C |
| 39 | Control Byte | 0X00 |
| 40 | MODSET1 | 0XC8 |
| 41 | STOP Condition | - |

Data Update Sequence:

|  |  |  |
| --- | --- | --- |
| No. | Input | Data in hex |
|  | START condition | - |
|  | Slave address | 0X7C |
|  | Control Byte | 0X00 |
|  | MODSET1 | 0XC8 |
|  | CMDXTN | 0XFD |
|  | MODSET2 | 0X90 |
|  | MODSET3 | 0XA0 |
|  | CNTSET | 0XB0 |
|  | RDCTL | 0XC0 |
|  | COMSET | 0XE0 |
|  | CMDXTN | 0XFC |
|  | FRSET | 0XEE |
|  | CLKCTL1 | 0XF0 |
|  | CLKCTL2 | 0XF8 |
|  | SADSET | 0XE0 |
|  | ADSET | 0X00 |
|  | STOP condition | - |
|  | START condition | - |
|  | Slave Address | 0X7C |
|  | Control Byte | 0X40 |
|  | Display Data | Send Data from 00h to 4Fh  .  .  .  .  . |
| Display Data |
| .  .  . |
| Display data |
|  | STOP Condition | - |

Display Digits:

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| No. | Segment Displaying  Number | Display Data (values in hex) | | | | | | | | | | |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |
|  | 1 | 5F | 06 | 6B | 2F | 36 | 3D | 7D | 07 | 7F | 3F | |
|  | 2 | 5F | 06 | 6B | 2F | 36 | 3D | 7D | 07 | 7F | 3F | |
|  | 3 | 5F | 06 | 6B | 2F | 36 | 3D | 7D | 07 | 7F | 3F | |
|  | 4 | 5F | 06 | 6B | 2F | 36 | 3D | 7D | 07 | 7F | 3F | |
|  | 5 | 5F | 06 | 6B | 2F | 36 | 3D | 7D | 07 | 7F | 3F | |
|  | 6 | 5F | 06 | 6B | 2F | 36 | 3D | 7D | 07 | 7F | 3F | |
|  | 7 | 5F | 50 | 3D | 79 | 72 | 6B | 6F | 51 | 7F | 7B | |
|  | 8 | F5 | 05 | D3 | 97 | 27 | B6 | F6 | 15 | F7 | B7 | |
|  | 9 | F5 | 05 | D3 | 97 | 27 | B6 | F6 | 15 | F7 | B7 | |
|  | 10 | 5F | 50 | 3D | 79 | 72 | 6B | 6F | 51 | 7F | 7B | |
|  | 11 | 5F | 50 | 3D | 79 | 72 | 6B | 6F | 51 | 7F | 7B | |
|  | 12 | 5F | 50 | 3D | 79 | 72 | 6B | 6F | 51 | 7F | 7B | |
|  | 13 | 5F | 50 | 3D | 79 | 72 | 6B | 6F | 51 | 7F | 7B | |
|  | 14 | 5F | 50 | 3D | 79 | 72 | 6B | 6F | 51 | 7F | 7B | |
|  | 15 | 5F | 50 | 3D | 79 | 72 | 6B | 6F | 51 | 7F | 7B | |
|  | 16 | 5F | 50 | 3D | 79 | 72 | 6B | 6F | 51 | 7F | 7B | |
|  | 17 | 5F | 50 | 3D | 79 | 72 | 6B | 6F | 51 | 7F | 7B | |
|  | 18 | 5F | 50 | 3D | 79 | 72 | 6B | 6F | 51 | 7F | 7B | |
|  | 19 | 5F | 50 | 3D | 79 | 72 | 6B | 6F | 51 | 7F | 7B | |
|  | 20 | 5F | 50 | 3D | 79 | 72 | 6B | 6F | 51 | 7F | 7B | |
|  | 21 | 5F | 50 | 3D | 79 | 72 | 6B | 6F | 51 | 7F | 7B | |
|  | 22 | 5F | 50 | 3D | 79 | 72 | 6B | 6F | 51 | 7F | 7B | |
|  | 23 | 5F | 06 | 6B | 2F | 36 | 3D | 7D | 07 | 7F | 3F | |
|  | 24 | Enable = 1, Disable =0 | | | | | | | | | | |
|  | 25 | 5F | 06 | 6B | 2F | 36 | 3D | 7D | 07 | 7F | | 3F |
|  | 26 | 5F | 06 | 6B | 2F | 36 | 3D | 7D | 07 | 7F | | 3F |

SEG to RAM Register Relation:

|  |  |  |  |
| --- | --- | --- | --- |
| No. | RAM Register No. | SEG No. | Address |
| 1 | RAM0 | SEG0,SEG1 | 00h, 01h |
| 2 | RAM1 | SEG2, SEG3 | 02h,03h |
| 3 | .  .  . | .  .  . | .  .  . |
| 4 | RAM39 | SEG76, SEG77 | 4Eh, 4Fh |

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