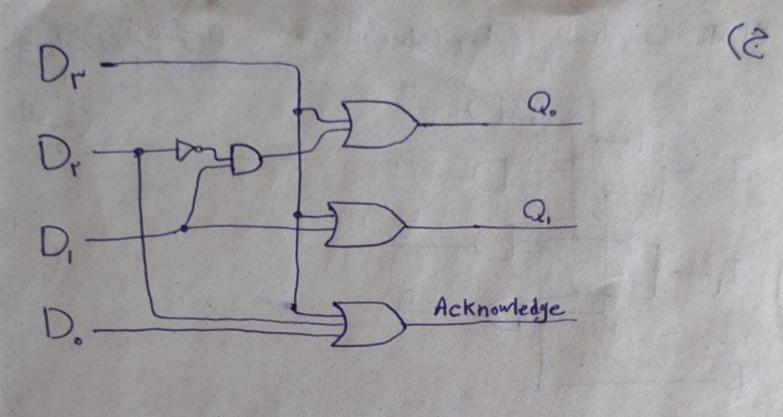
9971-16 آزماسیاه موارهای منطقی اشکان سیسا يس كرارى آزماس ك Dr



```
الف)
module Decoder2X4(I1, I0, En, D);
input Il, IO, En;
wire Il not, IO not;
output [0:3] D;
not n1(I0 not, I0);
not n2(Il not, Il);
and al(D[0], Il not, IO not, En);
and a2(D[1], I1 not, I0, En);
and a3(D[2], I1, I0 not, En);
and a4(D[3], I1, I0, En);
endmodule
                                                                                ب)
module Mux4X1(w,s,y);
input[0:3] w;
input[0:1] s;
wire[0:1] s not;
wire[0:3] ands;
output y;
not nl(s not[0],s[0]);
not n2(s not[1],s[1]);
and al(ands[0],s not[0],s not[1],w[
and a2(ands[1],s not[0],s[1],w[1]);
and a3(ands[2],s[0],s not[1],w[2]);
and a4(ands[3],s[0],s[1],w[3]);
or ol(y, ands[0], ands[1], ands[2], and:
endmodule
                                                                                ج)
module PriorityEncoder4X2(D,Q,A);
input [0:3] D;
output [0:1] Q;
output A;
wire D2 not;
wire D1 and D2 not;
not n1(D2 not, D[2]);
and al(D1 and D2 not, D2 not, D1);
or ol(Q[0],D[3],D1 and D2 not);
or o2(Q[1],D[3],D[2]);
or o3(A,D[3],D[2],D[1],D[0]);
endmodule
```