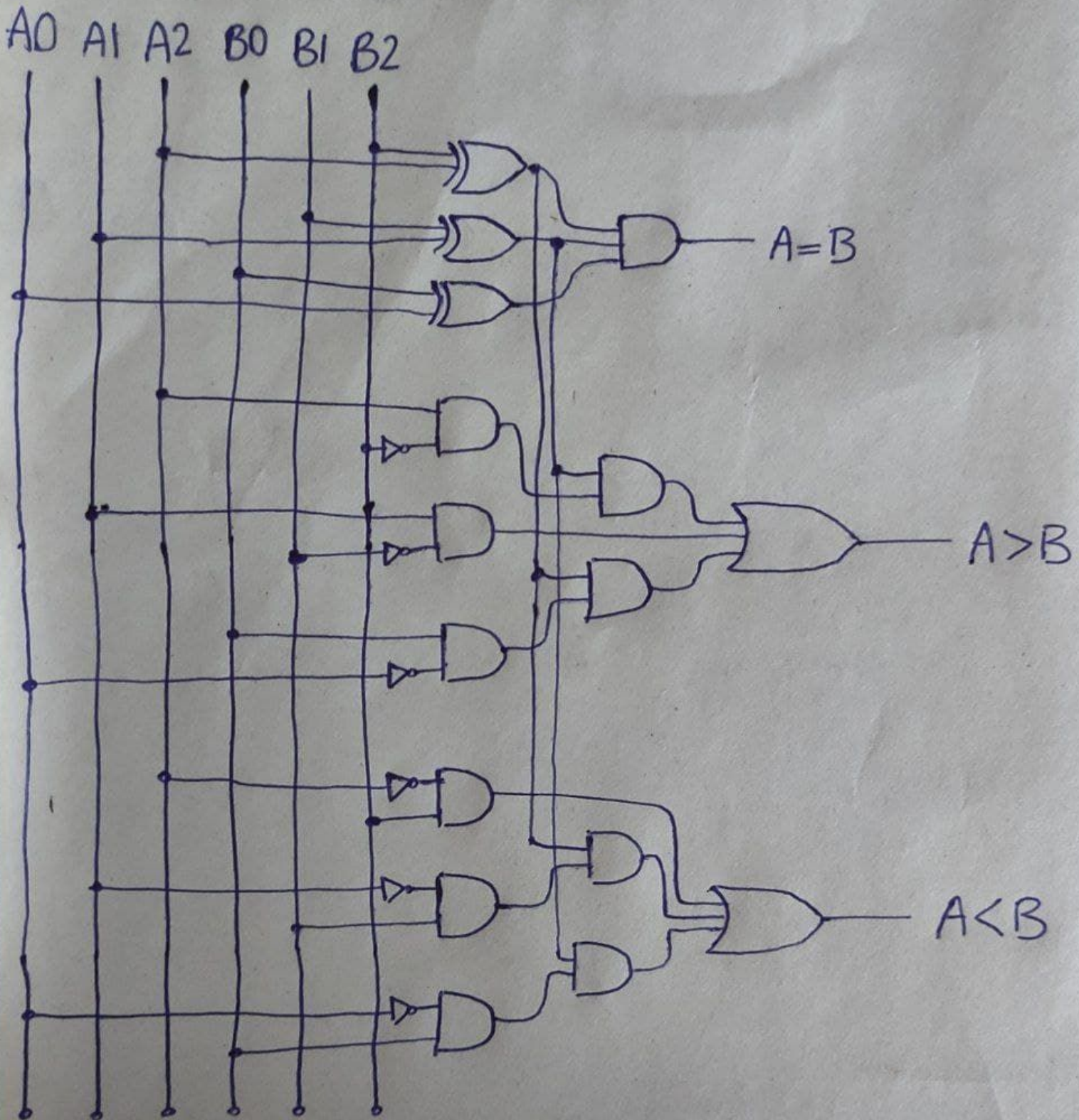
پیش گزارش آزمایش ۶ اشکان شکیبا ۹۹۳۱۰۳۰

3-bit comparator



Verilog Code

```
module three_bit_comparator(a,b,eq,lt,gt);


        input a[0:2],b[0:2];

        output eq,lt,gt;


        assign eq = (~(a[0]^b[0]))&(~(a[1]^b[1]))&(~(a[2]^b[2]));

        assign lt =
(b[2]&(~a[2]))||((~(a[2]^b[2])&(b[1]&(~a[1])))||((~(a[2]^b[2]))&(~(a[1]^b[1]))&(b[
0]&(~a[0])));

        assign gt =
(a[2]&(~b[2]))||((~(a[2]^b[2]))&(a[1]&(~b[1])))||((~(a[2]^b[2]))&(~(a[1]^b[1]))&(a
[0]&(~b[0])));

endmodule;
```