اشکان شکیبا (9931030)

پیش گزارش آزمایش نهم آزمایشگاه مدار های منطقی

```
module SR_LATCH_NAND(S_BAR, R_BAR, Q, Q_BAR);
input S_BAR, R_BAR;
output Q, Q_BAR;

nand w1(Q, S_BAR, Q_BAR);
     w2(Q_BAR, R_BAR, Q);

endmodule;
```

```
module D_LATCH(D, CLOCK, Q, Q_BAR);
input D, CLOCK;
output Q, Q_BAR;

wire D_BAR, S_BAR, R_BAR;

not w1 (D_BAR, D);
nand w2(R_BAR, D_BAR, CLOCK);
     w3(S_BAR, D, CLOCK);
SR_LATCH_NAND_VERSION w3(S_BAR, R_BAR, Q, Q_BAR);

endmodule
```

```
module FALLING_DFF(D, CLOCK, Q, Q_BAR);
input D, CLOCK;
output Q, Q_BAR;
wire Q_TEMP, Q_BAR_TEMP, CLOCK_BAR;

not w1(CLOCK_BAR, CLOCK);
D_LATCH w2(D, CLOCK, Q_TEMP, Q_TEMP_BAR);
D_LATCH w3(Q_TEMP, CLOCK_BAR, Q, Q_BAR);

endmodule
```

```
module CIRCUIT(A, B, CLOCK, Y, Z);
input A, B, CLOCK;
output Y, Z;
wire R, S, Q_BAR_1, Q_BAR_2, Y, Q2, D1, D2;

and w1(S, B, Q_BAR_2);
or  w2(D1, S, A);
nor w3(D2, D1, Q_BAR1);

FALLING_DFF w3(D1, CLOCK, Y, Q_BAR_1);
FALLING_DFF w4(D2, CLOCK, Q2, Q_BAR_2);

and w5(R, Q_BAR_2, B);
or  w6(Z, R, Q_BAR_1);

endmodule
```