Group 5 lab 1 report

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1   LUT list

```
Report Cell Usage:
+------+------+------+
|      |Cell  |Count |
+------+------+------+
|1     |LUT6  |     8|
|2     |MUXF7 |     4|
|3     |IBUF  |    35|
|4     |OBUF  |     4|
+------+------+------+
```

Figure 1: This is the LUT list of step 1

```
Report Cell Usage:
+------+------+------+
|      |Cell  |Count |
+------+------+------+
|1     |LUT6  |     8|
|2     |MUXF7 |     4|
|3     |IBUF  |    35|
|4     |OBUF  |     4|
+------+------+------+
```
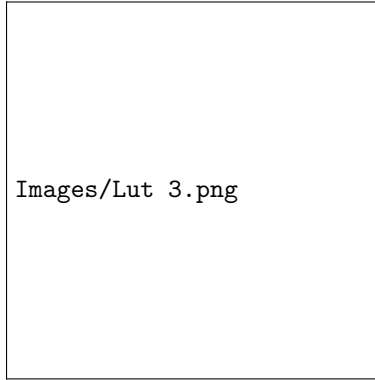
Figure 2: This is the LUT list of step 2

Figure 3: This is the LUT list of step 3

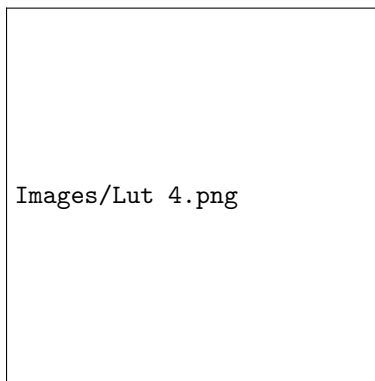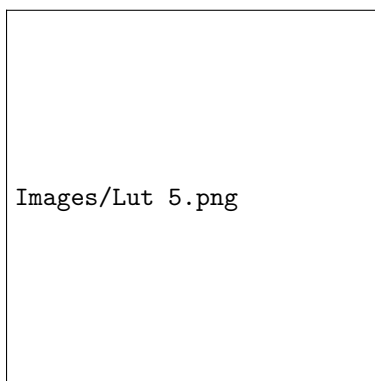
Figure 4: This is the LUT list of step 4

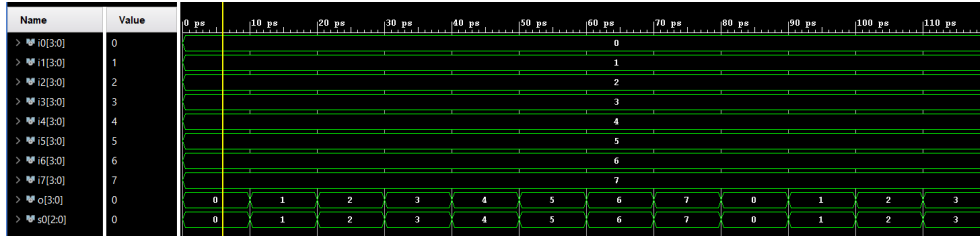Figure 5: This is the LUT list of step 5

2 Simulations
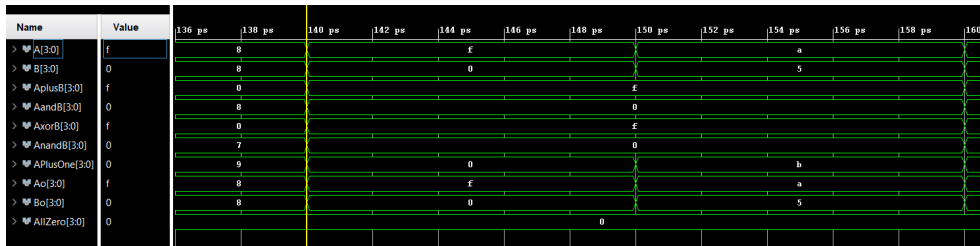

Figure 6: This is the simulation of step 1

Figure 7: This is the simulation of step 2

The following components are 3 diffrent ways to implement an 4 to one bit mutex. The IO are the following:

- i0-i3 are inputs.

- s0,s1 are select for the following input values.

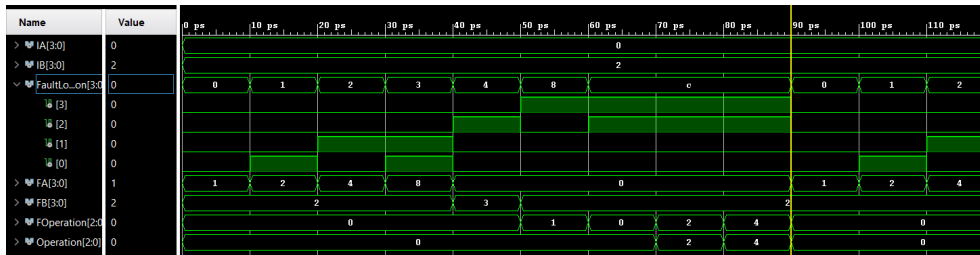- out0 are the output from the 4 to 1 mutex.

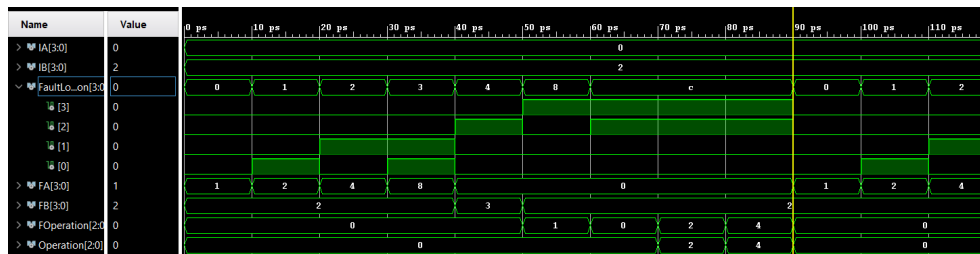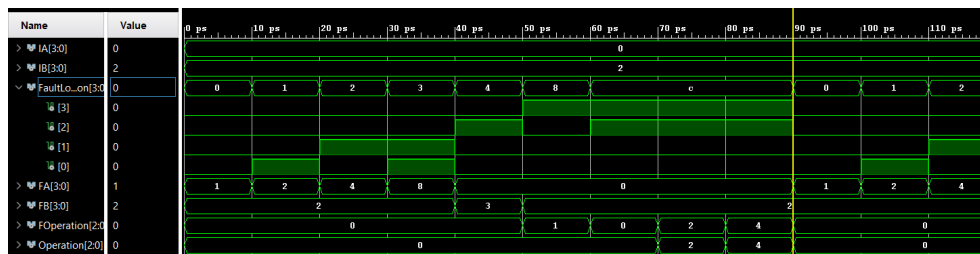Figure 8: This is the simulation of step 3

3

Figure 9: This is the simulation of step 4

Figure 10: This is the simulation of step 5

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