Group 5 lab 1 report

Ashley Björs,Elliot Bodin,Daniel Rytenberg,Jonas Gerne

January 2024

1 LUT list

```
Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT2 |     1|
|2     |IBUF |     2|
|3     |OBUF |     1|
+------+-----+------+
```

Figure 1: This is the LUT list of step 1

```
Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     1|
|2     |IBUF |     3|
|3     |OBUF |     1|
+------+-----+------+
```

Figure 2: This is the LUT list of step 2

Report Cell Usage:

	Cell	Count
1	LUT6	1
2	IBUF	6
3	OBUF	1

Figure 3: This is the LUT list of step 3

Report Cell Usage:

	Cell	Count
1	LUT6	1
2	IBUF	6
3	OBUF	1

Figure 4: This is the LUT list of step 4

Report Cell Usage:

	Cell	Count
1	IBUF	1
2	OBUF	2

Figure 5: This is the LUT list of step 5

2 Simulations

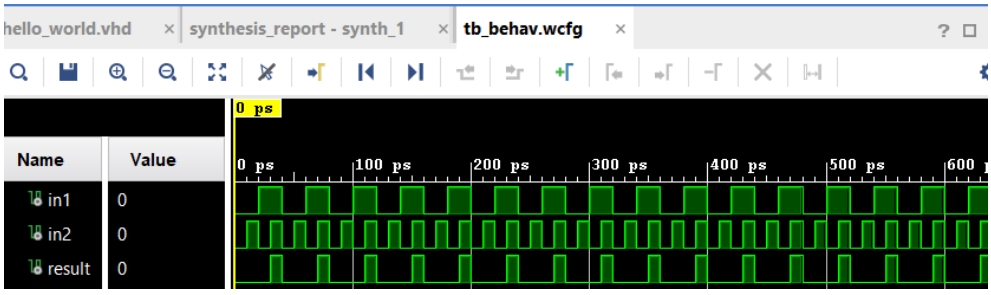

Figure 6: This is the simulation of step 1

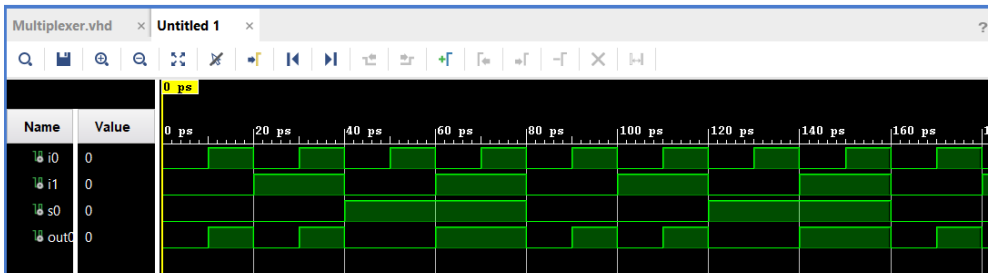

Figure 7: This is the simulation of step 2

The following components are 3 diffrent ways to implement an 4 to one bit mutex. The IO are the following:

- i0-i3 are inputs.
- s0,s1 are select for the following input values.
- out0 are the output from the 4 to 1 mutex.

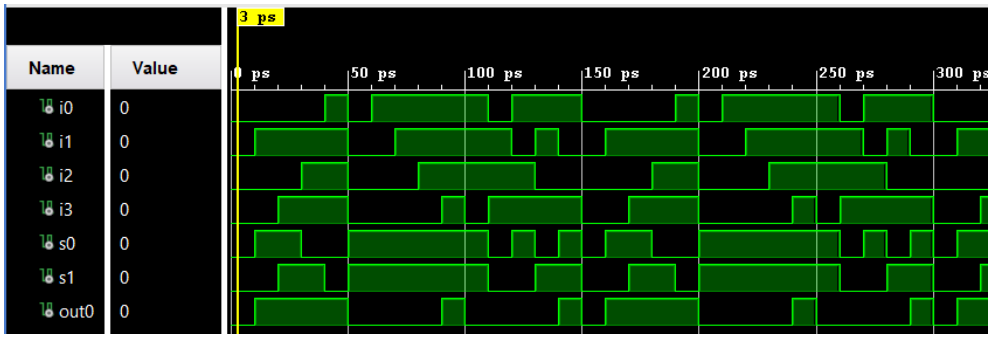

Figure 8: This is the simulation of step 3

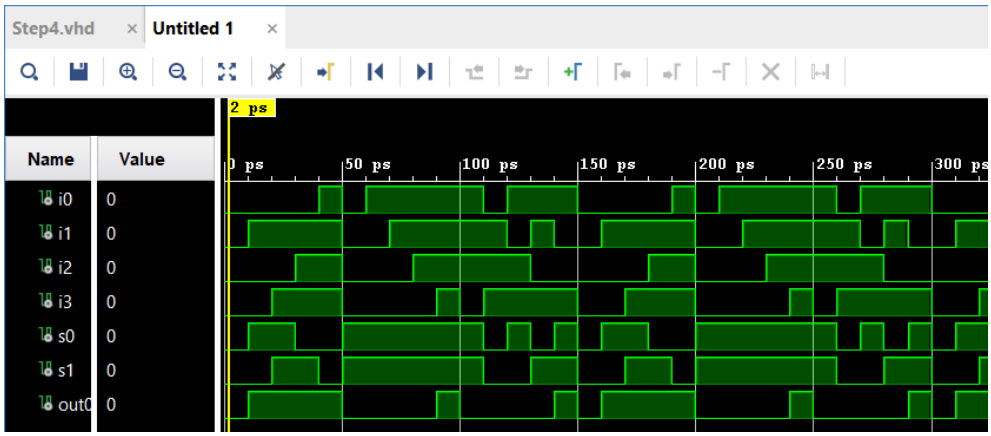

Figure 9: This is the simulation of step 4

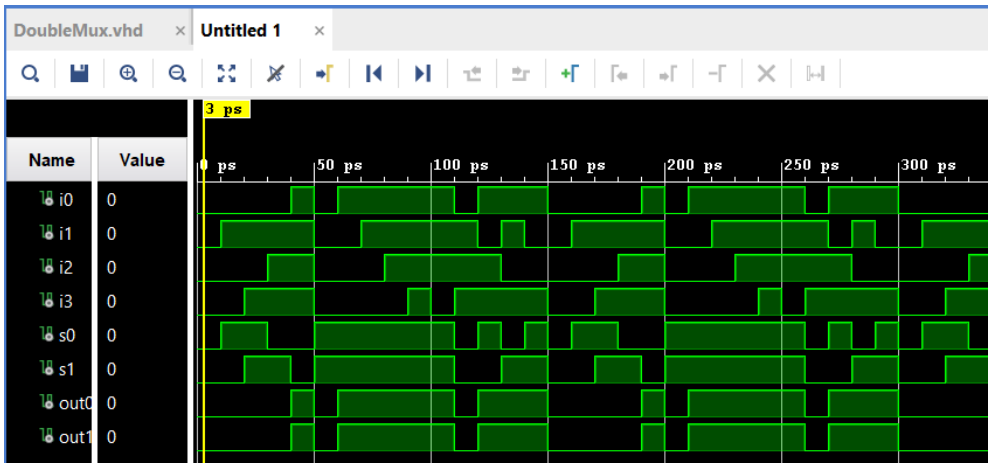

Figure 10: This is the simulation of step 5