钱雨馨

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教育经历

宾夕法尼亚大学 (Upenn) 2023年08月 - 2025年07月
电气电子工程 硕士 工程与应用科学学院 美国

- GPA：4.0 / 4.0
- 相关课程：数字集成电路和VLSI基础，模拟集成电路设计，计算机架构和设计，物联网边缘计算，物联网传感器和系统

西交利物浦大学（XJTLU） 2019年09月 - 2023年06月
电子科学与技术 本科 智能工程学院 苏州

- GPA：3.9 / 4.0
- 荣誉/奖项：最佳学术表现（Top 1%），最佳毕业设计（Top 1%），学术杰出奖（Top 5%），学术成就奖 （Top 10%）
- 相关课程：CMOS数字集成电路，集成电路的概念和设计，数字系统设计HDL，射频工程，嵌入式系统，微纳米制造技术，信号处理与数字滤波，高级电路与电磁学，能量转换和电力系统，C/C++编程和软件工程

项目经历

物联网边缘计算项目：振动路径腕带（Vibra-Path wristband）设计 2024年01月 - 至今
设计并开发了一款基于SAMW25的盲人辅助智能腕带的嵌入式产品

- 集成了超声波传感器进行测距，并通过触觉电机和马达实现不同振动模式，以及搭配三轴传感器实现跌倒检测和自动报警
- 设计并实现了电路原理图和PCB布局，使用Altium Designer软件完成设计并进行3D渲染验证
- 开发了基于C语言的嵌入式软件，使用FreeRTOS操作系统并辅以Percepio进行编程，并集成了I2C、SPI、UART协议

全流水线数据通路设计 2024年03月 - 至今
使用SystemVerilog成功设计了一个具有分支预测和旁路传递的五级流水线处理器

- 实现了基于RV32IM指令集的全流水线数据通路设计
- 提高了处理器性能，具备处理复杂数据依赖和特殊指令执行的能力

FPGA中可配置单元（CLB）设计与优化 2023年11月 - 2023年12月
设计并验证了CLB，包括设计中的非重叠时钟系统，16:1 MUX，6T SRAM单元，SRAM阵列及基于DFF的SIPO寄存器等组件

- 应用多种设计指标来评估CLB性能，包括最大频率、平均能量、加载能量、有效能量和面积等
- 在Cadence .6u工艺下完成设计与布局，顺利通过DRC、LVS验证
- 建立了模拟提取验证流程，并综合分析评估了面积、能量、频率等指标

宽带跨阻抗放大器（TIA）设计 2023年10月 - 2023年12月
设计优化了TIA拓扑结构和测试电路，利用Cadence软件完成直流、交流及瞬态仿真，评估性能

- 成功实现了150kΩ跨阻增益及150MHz以上带宽
- 通过稳态性能评估和噪声分析仿真，确保放大器目标频率下稳定运行，显著提升信噪比
- 运用晶体管尺寸匹配及偏置技术，优化放大器性能，实现噪声性能和功耗效率最优化

研究经历

基于摩擦电触觉传感器的机器学习辅助实时识别系统 2022年07月 - 2023年06月
西交利物浦大学 苏州
将摩擦纳米发电机TENG与机器学习算法相结合，开发了实时识别的多种应用系统

- 制备了单电极TENG，并设计信号处理电路与ADC模块，确保了数据采集的准确性与实时性
- 通过MATLAB软件运用人工神经网络（ANN）模型实现数据处理和训练，并应用t-SNE数据降维技术进行数据分析和优化
- 成功实现了两种实时识别应用开发，实时力度识别和材料识别

实习经历

科大讯飞股份有限公司 2021年07月 - 2021年09月
硬件中心 合肥
参与科大讯飞研发的智能编程机器人(U-Car)的测试和优化：

- 协助工程师测试U-Car的导航模块和自动避障功能，并分析测试结果
- 熟练使用Linux命令行进行系统配置和调试

其他

编程语言： C/C++ | Verilog | SystemVerilog | MATLAB | Python | Java | AHDL | ARM | Arduino ID
软件： Cadence | Altium Designer | Vscode | Altera Quartus II | VisUAL | LTspice XVII | Solidwork | Origin | Microsoft office
英语能力：雅思6.5

Yuxin Qian

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EDUCATION BACKGROUND

University of Pennsylvania (Upenn), USA 08/2023 - 07/2025

Master of Science in Electrical Engineering | Cum GPA: 4.0/4.0

Core Courses: Digital Integrated Circuits And VLSI-Fundamentals | Analog Integrated Circuits | Iot Edge Computing | Computer Organization & Design | Internet of Things Sensors and Systems

Xi'an Jiaotong-Liverpool University (XJTLU), China 09/2019 - 07/2023

B.E. in Electronic Science and Technology | Cum GPA: 3.9/4.0 | Ranking: 1

Core Courses: CMOS Digital ICs | Digital System Design with HDL | Integrated Electronics and Design | Electromagnetism | RF Engineering | Signal Processing and Digital Filtering | Embedded Systems | Energy Conversion and Power Systems | C/C++ Programming and Software Engineering

RESEARCH EXPERIENCES

Machine-learning Assisted Real-time Recognition System Based on the Triboelectric Nanogenerators (TENG)

Final Year Project, XJTLU 09/2022 – 05/2023

- Combined TENG with machine learning algorithms to develop real-time identification applications:
  - Fabricated single-electrode TENGs; designed signal processing circuits and ADC modules for data collection
  - Implemented artificial neural network (ANN) models for data processing and training; applied t-Distributed Stochastic Neighbor Embedding (t-SNE) for data analysis and optimization
  - Successfully investigated real-time force and material identification

PROJECTS

***IoT Edge Computing Project: Vibra-Path Wristband* Course Project, Upenn** 01/2024 – 05/2024

- Designed and developed an embedded product: a smart wristband for the visually impaired based on the SAMW25:
  - Integrated ultrasonic sensors for distance measurement, a 3-axis accelerometer for fall detection and automatic alerting, and a haptic driver with a vibrating motor for obstacle warning vibrations
  - Designed and implemented circuit schematics and PCB layouts, completing the design with Altium Designer software and validating through 3D rendering
  - Developed embedded software in C, utilizing the FreeRTOS operating system with Percepio for programming, and integrated multiple communication protocols such as I2C, SPI, and UART

***Configurable Logic Blocks (CLBs) in FPGAs Design* Course Project, Upenn** 11/2023 – 12/2023

- Designed and validated CLBs, including a non-overlapping clock system, a 16:1 multiplexer, 6T SRAM cells, SRAM arrays, and SIPO registers based on DFFs:
  - Applied various design metrics to measure CLB performance, including maximum frequency, average energy, loading energy, effective energy, and area
  - Executed the design in Cadence .6u process, finalized layout, cleared DRC and LVS checks, established simulation validation, and analyzed the area-energy-frequency FOM

***Wideband Trans-impedance Amplifier (TIA) Design* Course Project, Upenn** 10/2023 – 12/2023

- Designed and optimized the topology and test circuit of a TIA and conducted DC, AC, and transient simulations using Cadence software for performance evaluation:
  - Achieved a transimpedance gain of 150kΩ and a bandwidth exceeding 150MHz
  - Performed steady-state performance evaluations and noise analysis simulations to ensure amplifier stability at the target operating frequency and significantly improve the signal-to-noise ratio
  - Applied transistor size matching and biasing techniques to optimize overall amplifier performance, including optimal noise performance and power efficiency

***Traffic Light Control System Design Based on Verilog* Course Project, XJTLU** 11/2022 – 12/2022

- Designed a traffic light control system using Verilog, simulated and debugged with Quartus II software, and conducted hardware testing on a DE1 board:
  - Implemented complex state machine logic to control transitions between green, yellow, and red lights
  - Features real-time countdown display on a seven-segment screen, with support for emergency braking, resetting, and critical timing adjustments

INTERNSHIP EXPERIENCES

***Hardware Engineer Intern* | iFlytek Co., Ltd., Hefei, China** 07/2021 – 09/2021

- Participated in the testing and optimization of iFlytek's intelligent programming robot (U-Car):
  - Assisted engineers in testing U-Car's navigation and obstacle avoidance and analyzing results
  - Learned to use the Linux command line for system configuration and debugging

SKILLS AND HONORS

Programming Languages: C/C++ | Verilog | SystemVerilog | MATLAB | Python | Java | AHDL | ARM | Arduino ID

Software: Cadence | Altium Designer | Vscode | Altera Quartus II | VisUAL | LTspice XVII | Solidwork | Origin

Scholarship: Best Overall Academic Performance (2023); Best Performance in Final Year Project (2023); University Academic Excellence Award (2022); University Academic Achievement Award (2021)