VANDERBILT UNIVERSITY
SCHOOL OF ENGINEERING

ECE 4380 ELECTRONICS II

SEMESTER DESIGN REPORT

A Wireless Personal Area Network Receiver Amplifier

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Executive Summary

The goal of this project was to design a wireless Personal Area Network (PAN) receiver amplifier, as a multi-stage feedback amplifier capable of delivering a gain of 65 dB with a tolerance of 1.5 dB and a bandwidth of at least 100 kHz to 5.8 MHz. Additionally, the amplifier was specified to have a matched input impedance of 75 Ω to maximize power transfer, and an output impedance of less than 75 Ω to minimize signal loss. The power budget for this amplifier was a maximum of 12 mA DC current drawn from a 6 V power supply. Lastly, the design outlined that the amplifier must be tolerant to Beta variations of 50% and still remain within all previously stated specifications.

To accomplish this, the design process of the amplifier was split into five phases. In Phase I, a top-level conceptual design was conceived for the amplifier based on gain, bandwidth, input impedance, and output impedance requirements. The choice was made to divide the amplifier into four stages, an input stage with the explicit purpose of input impedance matching, two gain stages to deliver the high voltage gain needed, and an output stage to carefully select the output impedance. For this purpose, a common base BJT amplifier was chosen for the input, two matched cascode amplifiers for the two gain stages, and an emitter follower stage for the output due to its low output impedance. In Phase II, each stage was carefully designed to individually help meet the desired specifications, in which all components and DC biasing values were chosen. In Phase III, each individual stage was simulated to verify expected performance, and alterations were made at this step using insight obtained from the simulations to improve upon the design. In Phase IV, the completed stages were connected, comprising the entire amplifier, and simulations were conducted to again measure performance and make any necessary adjustments. Using the analysis from Phase III, feedback was introduced to the amplifier to increase the bandwidth and decrease the gain to fall within the specified tolerance range. After all modifications were completed, final simulations were conducted to determine the voltage gain, bandwidth, input impedance, output impedance, and power consumption of the amplifier. Each of these experiments was conducted three times, for nominal, low (50% decrease from nominal), and high (50% increase from nominal) values of the transistor's Beta parameter. In Phase V, the final portion of our design process, a cost analysis was performed to determine the tradeoffs and overall feasibility of the design.

The experiments and analysis conducted verified that the final amplifier design met or exceeded all performance specifications including midband voltage gain, bandwidth, input impedance, output impedance, power constraints, and tolerance to Beta variations, proving that this design will effectively and reliability fulfill its intended purpose as a Personal Area Network (PAN) receiver amplifier.

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1. Introduction

This project aimed to design and construct a high-gain, wideband, multi-stage feedback amplifier to serve as the front-end receiving amplifier in a magnetic near-field personal area network (PAN) communication system. Unlike conventional PAN systems such as Bluetooth which rely on propagating electromagnetic radiation, or radio waves, this architecture leverages magnetically-coupled near-field communication as originally proposed by Richley (Xerox)[1]. This method employs a loop antenna to generate a magnetic near field at 5.4 MHz and achieves data transmission via modulation at up to 250 kbps, resulting in a required operational bandwidth of at least 5.8 MHz to capture the entire signal spectrum. The Richeley approach represents advantages for portable and wearable electronics, especially the ability to conserve power by coupling only when a receiver is nearby.

In this project, the amplifier's role is to receive a weak, modulated carrier signal from the antenna, amplify it with minimal distortion, and drive a downstream demodulation circuit. To ensure maximum power transfer and signal integrity, the input impedance needs to be matched to the antenna's 75Ω impedance within 10%, and the output impedance kept below 75Ω. Design constraints required a voltage gain of 65 dB ± 1.5 dB over a minimum bandwidth of 100 kHz to 5.8 MHz while drawing no more than 12 mA from a +6V supply, simulating the energy-limited nature of magnetically-coupled power delivery systems. To further support power and performance goals, all resistors need to be selected with 1% tolerance to ensure precision and predictability. Moreover, the overall gain Vin/Vout is required to tolerate a $\beta F = \beta o$ range of ± 50% the nominal β value, thus the inclusion of feedback topologies would be necessary.

These stringent specifications led to careful consideration of transistor selection, biasing, power efficiency, and bandwidth optimization. The final amplifier design was verified using LTspice simulations under β variations, to ensure robustness and consistent performance.

[1] Patent #5,437,057

2. Conceptual Design

To meet the stringent performance requirements of the PAN[2] system receiver, the team developed a four-stage feedback amplifier that ensures a high gain of 65 dB ± 1.5 dB, a wide bandwidth of 100 kHz to 5.8 MHz, input impedance matching, low output impedance, and power efficiency. The amplifier architecture consists of a dedicated input stage, two cascaded gain stages, and an output stage as outlined in Figure 1 . To achieve the required input impedance matching with the 75Ω loop antenna within ± 10% across the operating bandwidth, a common-base amplifier configuration was selected for the input stage due to its inherently low input impedance and high-frequency performance. The gain stages consist of cascode amplifiers which provide high gain with improved bandwidth. Additionally, series-shunt feedback topology was applied around the gain stages to stabilize the gain and reduce sensitivity to current gain (β) variations. The final output stage was implemented using an emitter-follower configuration to ensure a low output impedance well below the 75Ω threshold for efficient signal transfer to the demodulation circuit which is not included in this design. Finally, all stages are AC-coupled to prevent DC biasing interaction, and components are selected with 1% tolerance to ensure reliability.

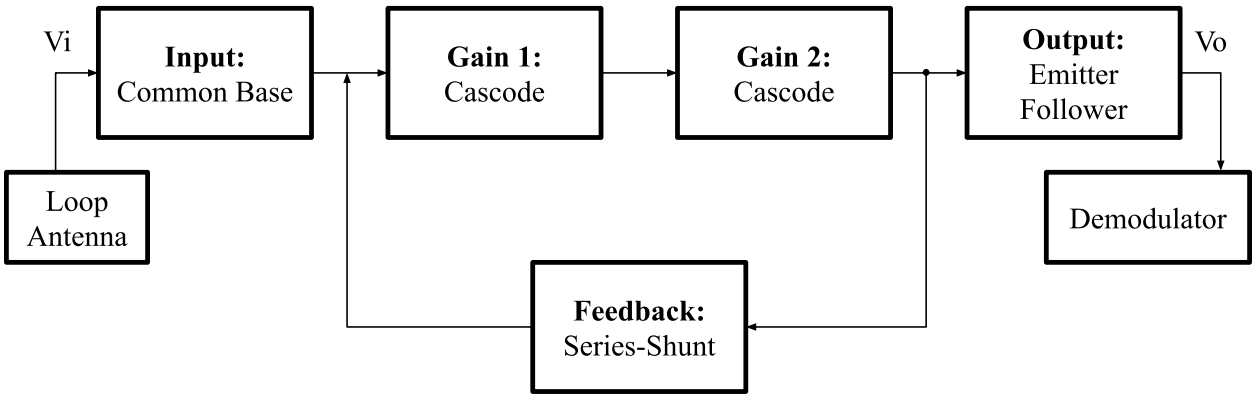


Figure 1. Conceptual Design Block Diagram

[2] Personal Area Network

3. Design Implementation

3.1 Input Stage

The common-base amplifier was chosen for the input stage due to its low input impedance and good high frequency response. Since the input impedance of the common base is modeled by 1/gm, careful biasing of the DC collector current Ic is critical. Using the relation gm = Ic / Vt , where Vt is the thermal voltage (approximately 26 mV at room temperature), it was determined that achieving an input impedance of 75Ω requires a transconductance of 0.013 A/V, corresponding to a collector current Ic of 0.35 mA.

To ensure the transistor operates in the active region, the “Rule of Thirds” design guideline was applied when selecting component values. Specifically, the collector and emitter resistors RC1 and RE2 were chosen to be 5.62 kΩ which provided a desired collector current of 0.35 mA and emitter voltage of 2V, while the biasing resistors RB11 and RB12 were selected as 280 kΩ and 221 kΩ respectively to establish a stable base-emitter voltage,VBE, of approximately 0.7 V. The loop antenna is modeled using its Thevenin equivalent – a 75Ω resistor in series with a 1V AC signal source, as shown in Figure 2. Coupling capacitors are inserted at the input and base to preserve the DC biasing conditions. Finally, an NPN transistor ZTX107 was selected to enhance the frequency response.

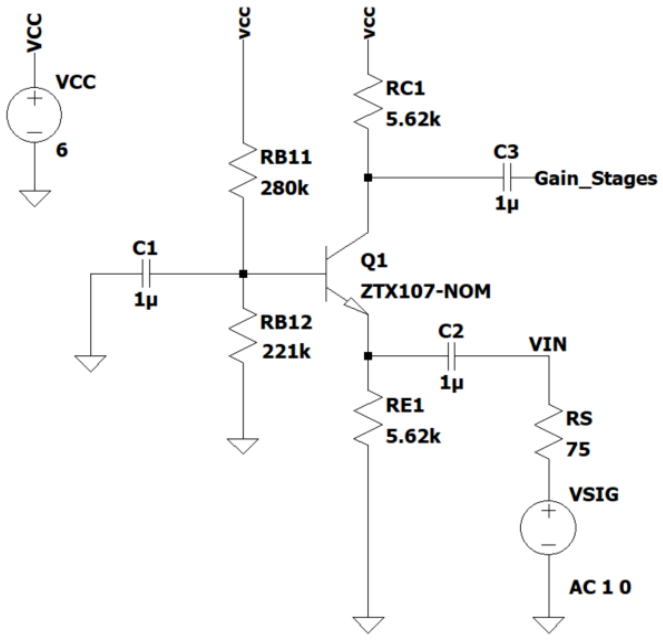


Figure 2. Input Stage Common Base Circuit

3.2 Output Stage

The emitter follower was selected as the output stage amplifier due to its low output impedance. It further acts as a buffer between the amplified signal and the output of the circuit to the demodulator. In this design, featured in Figure 3, a DC collector current Ic of 5 mA was chosen to simplify the initial design stages that involved heavy hand calculations. To minimize the output resistance, an emitter resistor RE of 200 Ω was selected, which, according to Ohm's Law, results in an emitter voltage of 1V, assuming that the DC emitter current is approximately equivalent to the collector current. To maintain the 0.7V difference between the base and emitter, the base voltage was set to 1.7V by setting bias resistors RB41 and RB42 to 150 kΩ and 61.9 kΩ respectively. The ZTX107 NPN transistor was used to optimize the frequency response, and coupling capacitors at the input and output stages were employed to isolate the DC operating point, while the load resistance RL = 75 Ω was used to simulate the impedance of a demodulation circuit. Resistor values were selected carefully to limit power dissipation while maintaining proper transistor operation in the active region.

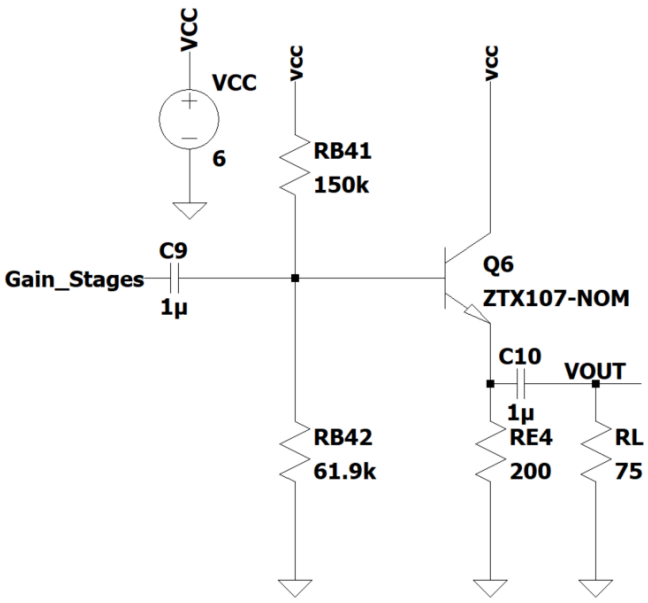


Figure 3. Output Stage Emitter Follower Circuit

3.3 Gain Stages

The cascode broadband amplifier, consisting of a traditional common emitter amplifier with an AC-grounded emitter feeding into a common base amplifier, was chosen for each of the two gain stages in our conceptual design. This amplifier configuration was selected for its high voltage gain and its superior frequency performance offering substantial bandwidth. To reduce complexity, a matched biasing scheme was chosen for each cascode. For the biasing scheme and design of each cascode, shown in Figure 4, the ZTX107 NPN BJT was chosen for its combination of optimal frequency response and high Beta value to assist in meeting the frequency bandwidth and voltage gain requirements. A DC collector current of 2 mA was chosen for this design to match the design 2 mA collector current used to obtain a Beta value of 300 for the ZTX transistor. Due to the large Beta value of 300 for the transistor, it was assumed in all DC biasing calculations that the collector and emitter currents for the two transistors comprising the cascode were roughly equal.

The first step in the DC biasing design was to set the value of the DC emitter voltage for transistor Q1 in Figure 4. A value of 1 V was chosen in order to provide a moderately wide for the emitter voltage to avoid the voltage reaching that of the signal ground. According to Ohm's Law, this would require a resistor value of roughly 500 Ω. Consequently, this design decision dictated the value of the DC base voltage of transistor Q1 to be 1.7 V due to the roughly constant 0.7 V base to emitter voltage. The next design choice was to choose the voltage of the shared node between the two transistors, which corresponds to the emitter voltage of Q2 and the collector voltage of Q1. This value was chosen to be 3 V, to allow each transistor to have an equal collector to emitter voltage range of half the power supply voltage. Using the same 0.7 V base to emitter junction principle, the value of the base voltage of transistor Q2 would be desired to be roughly equal to 3.7 V. This knowledge was important in selecting the value of the collector resistor, as the value of the collector voltage on transistor Q2 needed to be higher than this voltage to prevent the transistor from operating in the saturation region as opposed to the active region. As a result, a value of 1 kΩ was chosen for the collector resistor, which according to Ohm's Law, would bias the collector voltage at roughly 4 V with a collector current of 2 mA. Finally, using the values of 1.7 V and 3.7 V for the base voltages of Q1 and Q2, respectively, and choosing a moderate value of 20 kΩ for bias resistor RB3 in order to minimize signal loss and power dissipation, while also maximizing the high frequency cutoff, resistance values for RB1 and RB2 were calculated using Ohm's Law. Nominal 1% resistor values were chosen based on these calculations of 24.3 kΩ for RB1 and 22.1 kΩ for RB2. The full schematic of both gain stages is shown below in Figure 5.

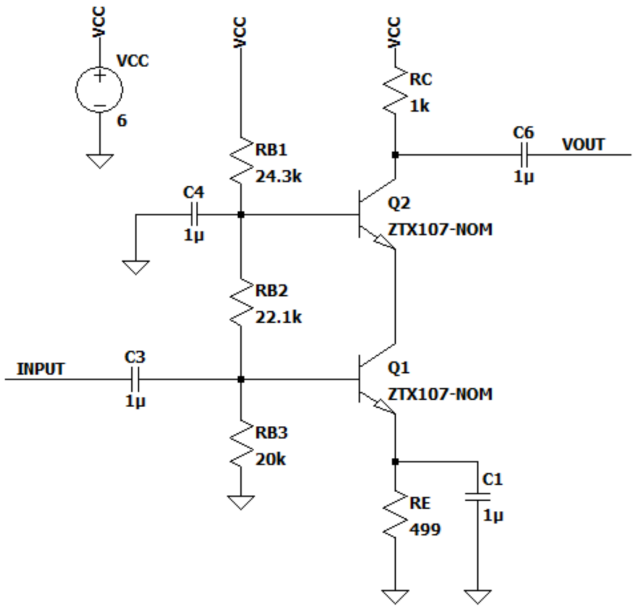


Figure 4. Single Gain Stage Cascode Circuit

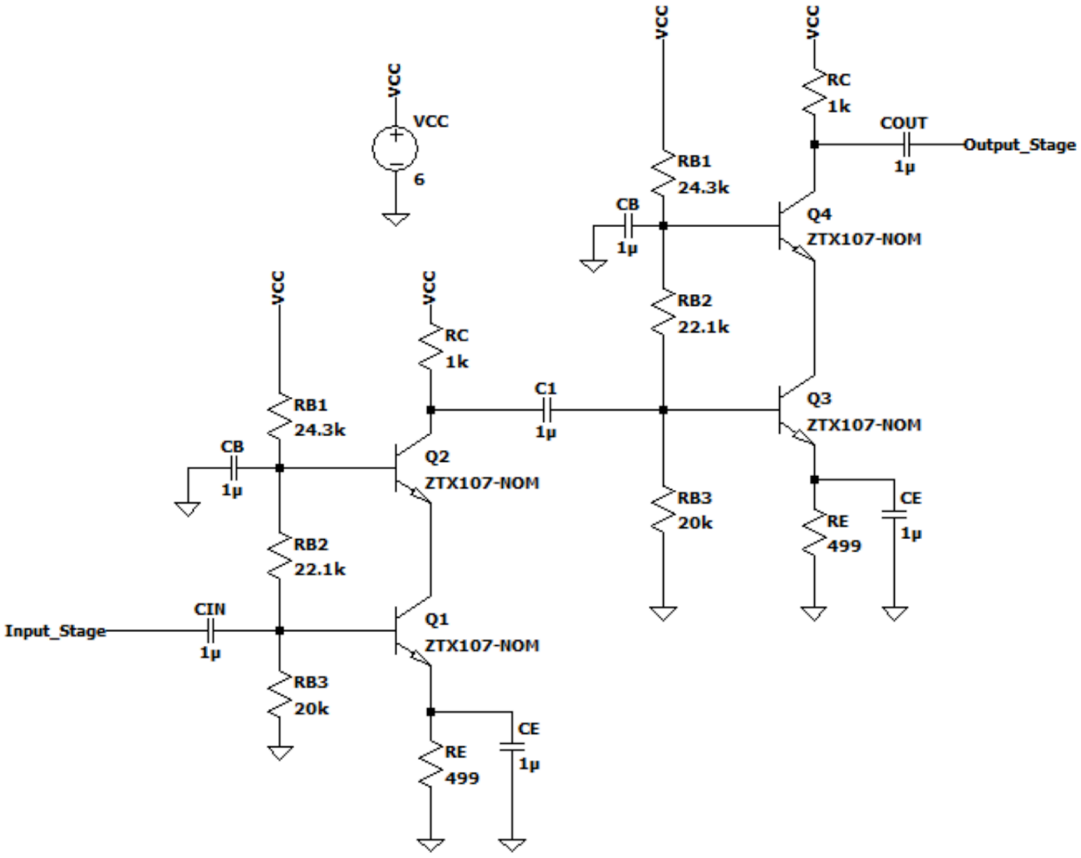


Figure 5. Combined Gain Stages Circuit

3.4 Feedback Design

In order to stabilize the gain and frequency response of the amplifier, as well as reduce sensitivity to Beta variations, feedback was applied around the two gain stages. Feedback was placed around both gain stages, as opposed to feedback around each of them, to maintain simplicity. Since a single cascode amplifier has an inverting gain, our two gain stages, each consisting of one cascode, together produced a non-inverting gain. Due to this fact, a series-shunt feedback topology was chosen to avoid causing instability in our circuit. This series shunt topology would include an emitter resistor on the first cascode connected to a feedback resistor which samples the output of the second cascode. However, because an emitter resistor would be added to the first cascode, the slight voltage gain loss in the first gain stage had to be considered, as well as the need to maintain the original DC biasing scheme.

Using the calculations for the voltage gain and high frequency poles for each stage, which is shown in Appendix E, the initial voltage gain and high frequency cutoff frequency were determined to be 63 dB and 1.44 MHz, respectively. The derivations of the effects of feedback on the gain stage of the circuit are shown in Appendix E. The feedback network was initially designed to bring the cutoff frequency from 1.44 MHz to the 5.8 MHz. Feedback theory was used to accomplish this by setting the value of the amount of feedback, or $1+A_{OL}B$, to the ratio of the two frequencies. After performing this calculation, it was determined that in order to meet the minimum frequency requirements, and choosing the resistor on the emitter to be a moderately small value of 100 Ω to avoid modifying the DC biasing scheme and avoid excess voltage gain loss, the necessary value of RF2 was found to be 12.1 kΩ. This feedback scheme was then assessed to determine the fulfillment of the necessary gain requirements. It was then found that the gain of the two cascode gain stages would result in a voltage gain of 6 dB higher than the 65 dB specification in calculations shown in Appendix F. To remedy this, the resistor values were resolved using a similar set of equations and by decreasing the voltage gain of the two cascades with feedback by a factor of 2, as shown in Appendix G. From this final calculation, the necessary value of RF2 to meet both gain and frequency bandwidth requirements was found to be 5.36 kΩ. To preserve the DC biasing of the first cascode, a bypass capacitor was placed between RF1 and the initial emitter resistor, which we reduced to 400 Ω, so the 500 Ω resistance on the emitter for DC voltages would be maintained. This completed feedback network, shown around the combined gain stages, is depicted in Figure 6.

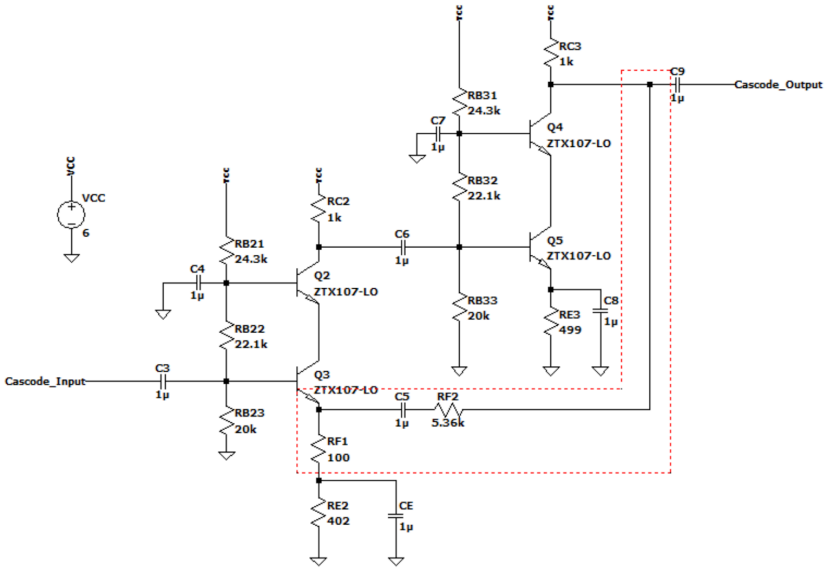


Figure 6. Schematic of Combined Gain Stages with Feedback Network

4. Simulation Experiment

In order to verify and validate the required specifications for this amplifier design, LTSpice simulations were conducted in place of experiments performed on a physical prototype. The entire amplifier design was fabricated within LTSpice, and various experiments were conducted for each design requirement. The methodology and measurements taken for these tests are outlined for each specification below. For each test, to simulate the AC behavior of the circuit, an AC Analysis simulation was performed in LTSpice. To simulate the DC behavior of the circuit, a DC Operating Point simulation was conducted as well. The AC analysis was performed as a decade sweep with 1000 points per decade, over a frequency range of 10 Hz to 100 MHz. Each experiment was first conducted with nominal Beta value ZTX107 BJTs.

4.1 Voltage Gain

The voltage gain of the amplifier was tested using the AC Analysis Simulation in LTSpice. The amplifier was driven with a 0 V DC, 1 V AC amplitude source, named VSIG, placed on the input of the common base input stage. The signal resistance, RSIG, was placed in series with the voltage source VSIG, and the node coupling the signal voltage and resistance to the input of the amplifier was labelled VIN, as shown in Figure 7 below. After running the simulation, the value of the output voltage of the emitter follower output stage was plotted divided by the input voltage of the common base stage. This value of VOUT/VIN represented the intrinsic voltage gain for the amplifier. The midband gain was measured using the cursor function in LTSpice. To verify the requirement of 65 dB +/- 1.5 dB over the entire bandwidth, cursors were placed at the lower and upper bounds of the required bandwidth, 100 kHz and 5.8 MHz, respectively, and the gain was verified to fall within the required range at all points within the bandwidth.

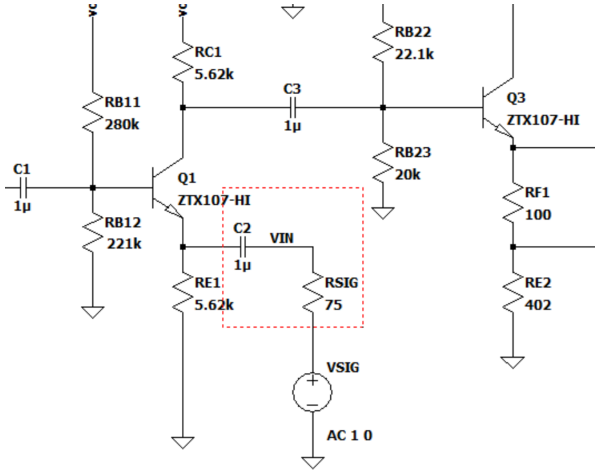


Figure 7. Voltage Gain Simulation Input Source

4.2 Bandwidth

The required bandwidth of 100 kHz to 5.8 MHz was verified using the same testing strategy and simulation settings as outlined in Section 4.1. The ratio of the output voltage of the emitter follower stage and the input voltage of the common base stage, or VOUT/VIN, was plotted over the frequency range given by the AC analysis settings, and cursors were placed on the plot to determine the midband gain. Once the midband gain was found, the cursors were adjusted to be placed at the lower and upper -3 dB voltage gain frequencies, or the frequencies at which the voltage gain dropped to 3 dB less than the midband gain voltage. Once these frequencies were found, the lower frequency was verified to be at no greater than 100 kHz, and the upper frequency was verified to be at least 5.8 MHz.

4.3 Input Impedance

The input impedance of the amplifier was specified to match the input impedance of 75 Ω within a tolerance of +/- 10 % over all frequencies. In order to verify this requirement, again the same simulation settings were applied to the schematic. The input voltage divided by the current through the coupling capacitor on the input of the amplifier was plotted. The red box in Figure 8 below shows the node on the schematic containing this voltage and current. This value, the input source voltage divided by the current moving through the input source, was equal to the input impedance. Once plotted, cursors were placed at the upper and lower bounds of the bandwidth, and the impedance was verified to be within 10 % of 75 Ω over the entire range.

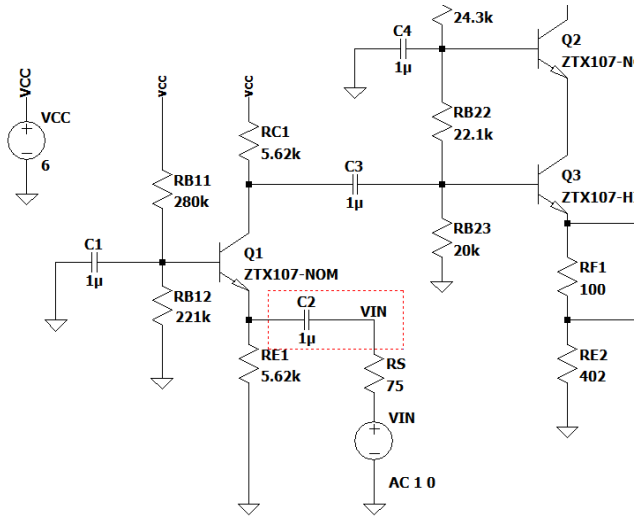


Figure 8. Location of voltage and current used to plot input impedance

4.4 Output Impedance

The output impedance was required to be less than 75 Ω to avoid impedance transformation and signal loss at the output of the amplifier. To guarantee the fulfillment of this requirement, an LTSpice simulation was run using the same settings as outlined above. However, in this experiment, the VIN input source described in earlier experiments was set to an AC and DC value of 0, effectively grounding the input of the amplifier. Next, using the principle of source driving, the load resistor was replaced with an AC source Vx of amplitude = 1V, as shown in Figure 9. Thus, the output impedance would be equivalent to Vx divided by the current going into source Vx, or I(Vx). After running the simulation, we plotted the value of Vx/I(Vx) to check the output impedance over the entire bandwidth. Once plotted, cursors were placed at the upper and lower bounds of the bandwidth, and the impedance was verified to be less than 75 Ω over the entire bandwidth.

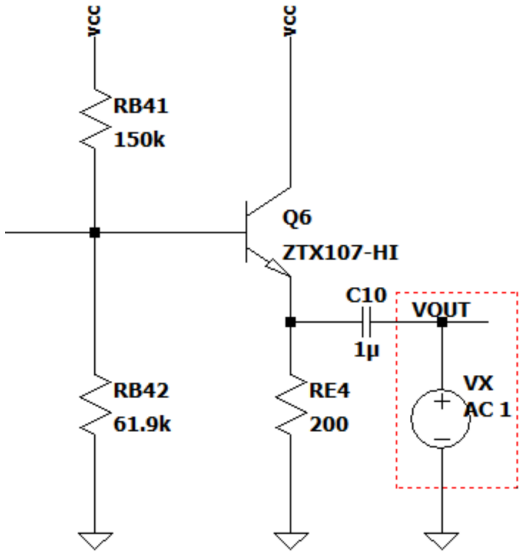


Figure 9. Calculating Output Impedance Using Source Driving Technique

4.5 Power Budget

This design includes a power constraint limiting current draw from the 6 V source to 12 mA, in order to reduce the amount of power diverted by the amplifier from the receiver antenna. To determine the DC power drawn from the 6 V source, shown in Figure 10, the same schematic from the first experiment was used, with the 1 V AC source at the input and the expected load at the output. Then, a DC operating point simulation was conducted in LTSpice. From the output log obtained from this simulation, the current being drawn from the power supply was obtained. This current value multiplied by the DC value of the voltage source produced the total amount of power drawn from the source by the amplifier.

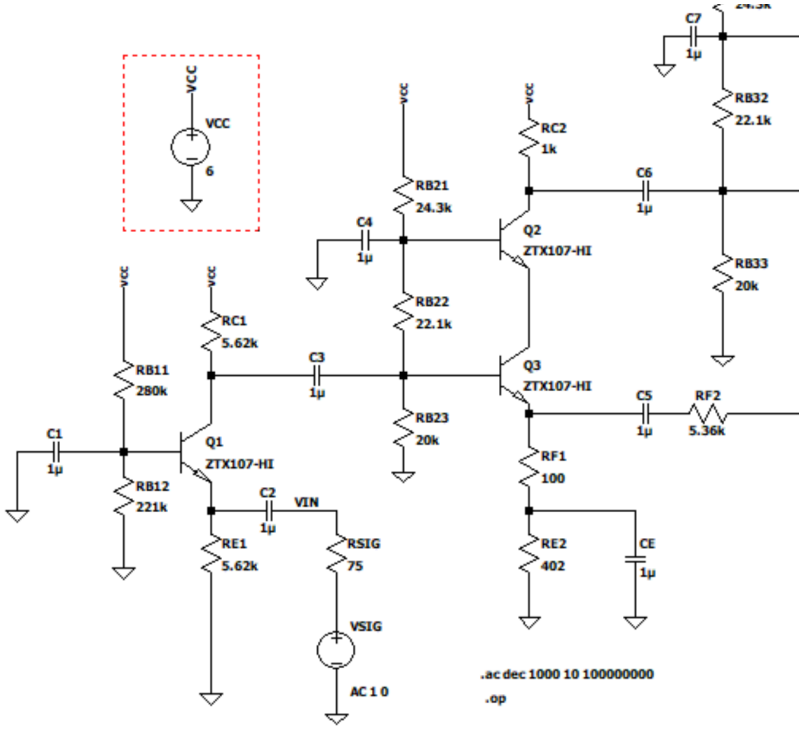


Figure 10. Voltage Source and Current Used to Determine Power Draw

4.6 Beta Variation Tolerance

The last design specification for this amplifier was that it be insensitive to Beta variations of +/- 50 % from the nominal Beta value, meaning that it should maintain compliance with all previous specifications in a Beta range of 150 to 750. To verify this requirement, each of the previous simulations were conducted twice more, with ZTX107-LO transistors, which have a Beta value of 150, and ZTX107-HI transistors, with a Beta value of 750, as shown in Figure 11. Reverifying each specification by performing each simulation with the high or low Beta variation of the ZTX107 BJT was sufficient to check that each design requirement was met, and that the design requirements were all met regardless of major Beta variations.

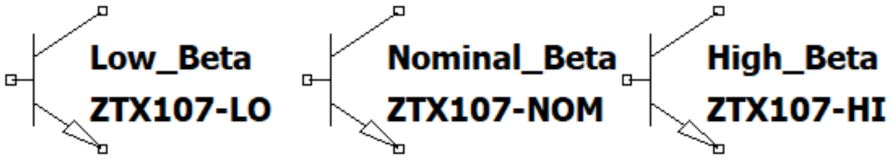


Figure 11. Low, Nominal, and High Beta Variations of ZTX107 BJT

5. Results & Analysis

The midband gain of the circuit varies from 64.6 dB to 65.9 dB, with a nominal gain of 65.4 dB. Table 1 summarizes the result of changes in gain and bandwidth with respect to changes in beta, and the changes in frequency response due to beta variation. All gain values meet the design constraint of 65 dB ± 1.5 dB voltage gain over the full bandwidth of at least 100 kHz to 5.8 MHz. The low frequency cutoff frequency varies from 4.3 kHz to 4.38 kHz, with a nominal 3 dB low cutoff frequency of 4.3 kHz. The high frequency cutoff varies from 9.83 MHz to 10.6 MHz, with a nominal 3 dB high cutoff of 10.3 MHz. Thus, the overall bandwidth (4.3 kHz -10.3 MHz) extends generously beyond the requirement of 100 kHz to 5.8 MHz.

Table 1. Midband Gain and Frequency Response Summary with Beta Variation

Beta	**$\lvert Vout/Vin \rvert_{dB}$**	**Vout/Vin**	**Relative Error of Gain**	**Bandwidth**
Nom = 400	65.4 dB	1862.09 V/V	0.615%	4.3 kHz - 10.3 MHz
Hi = 700	65.9 dB	1972.42 V/V	1.38%	4.38 kHz - 10.6 MHz
Lo = 250	64.6 dB	1698.24 V/V	0.615%	4.3 kHz - 9.83 MHz

Table 2 and Table 3 summaries input and output impedances under beta variation. Columns 2 and 3 of both tables show the result corresponding to the desired bandwidth (100kHz - 5.8MHz) and it can be concluded that all input resistances are well contained within the required constraint of 75Ω ± 10%, or 67.5 to 82.5 Ω. Moreover, all output resistances are well below 75Ω. Therefore, the amplifier design effectively meets all design requirements. The following sections (5.1 - 5.3) will entail a detailed description of the simulation results for each beta value. Section 5.4 will be power analysis and the cost analysis will be covered in section 5.5.

Table 2. Rin Summary with Beta Variation

Beta	**Rin @ 100KHz**	**Rin @ 5.8MHz**	**Rin @ Low -3dB**	**Rin @ High -3dB**
Nom = 400	78.5Ω	77.9Ω	86.6Ω	76.5Ω
Hi = 700	76.9Ω	76.3Ω	85.2Ω	74.8Ω
Lo = 250	80.8Ω	80.1Ω	88.8Ω	78.8Ω

Table 3. Rout Summary with Beta Variation

Beta	**Rout @ 100KHz**	**Rout @ 5.8MHz**	**Rout @ Low -3dB**	**Rout @ High -3dB**
Nom = 400	9.03Ω	7.54Ω	39.1Ω	40.7Ω
Hi = 700	7.87Ω	6.71Ω	37.5Ω	43.3Ω
Lo = 250	10.6Ω	9.16Ω	39.2Ω	37.3Ω

5.1 Nominal Beta

The bode gain plot of the amplifier simulated using AC analysis and nominal beta value is shown in Figure 12 (refer to Appendix A.1 for the complete schematic). The amplifier has a wide bandwidth of 4.3kHz to 10.3MHz and a nominal midband gain of 65.4 dB. The DC operating point of the circuit can be found in Appendix A.2. The important factors to note from Appendix A.2 are the values of VBE, VBC, and VCE. For BJT in the active region – best for amplification usage – the following rule VC > VB > VE needs to be satisfied. For the nominal beta analysis, all VBE are positive and approximately 0.7 V. All VCE values are positive and greater than 0.2V – indicating active operation – and all VBC values are negative as expected.

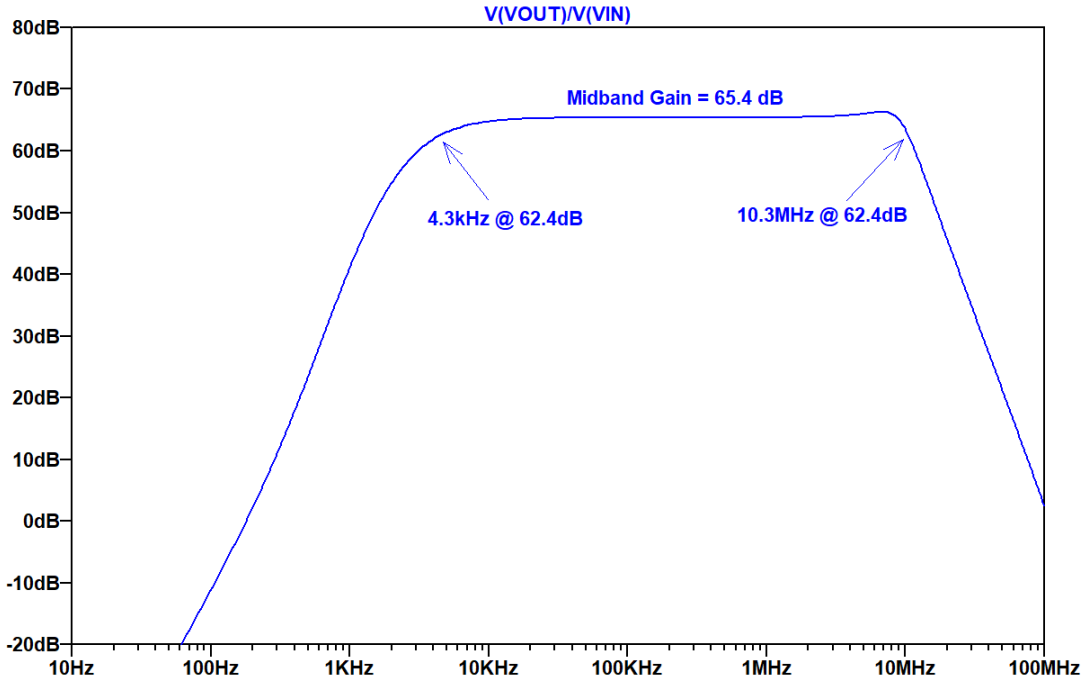


Figure 12. Nominal Beta Bode Gain Plot

The input impedance is shown in Figure 13, and it varies from 78.5Ω to 77.9Ω in the minimum operating frequency of 100KHz to 5.8 MHz, indicated by the green labels in Figure 13. These values are well contained within the required constraint of 75Ω ± 10%, or 67.5 to 82.5 Ω. The blue labels in the same figure mark the input impedances at -3dB frequencies of the circuit. While the resistance value at the high-3 dB frequency (76.5Ω at 10.3 MHz) remains within the specified range, the value at the low -3 dB point (86.6Ω at 4.3 kHz) exceeds it. This discrepancy arises because 4.3 kHz falls well below the defined minimum operating frequency of 100 kHz, where the circuit's impedance behavior is no longer within specification.

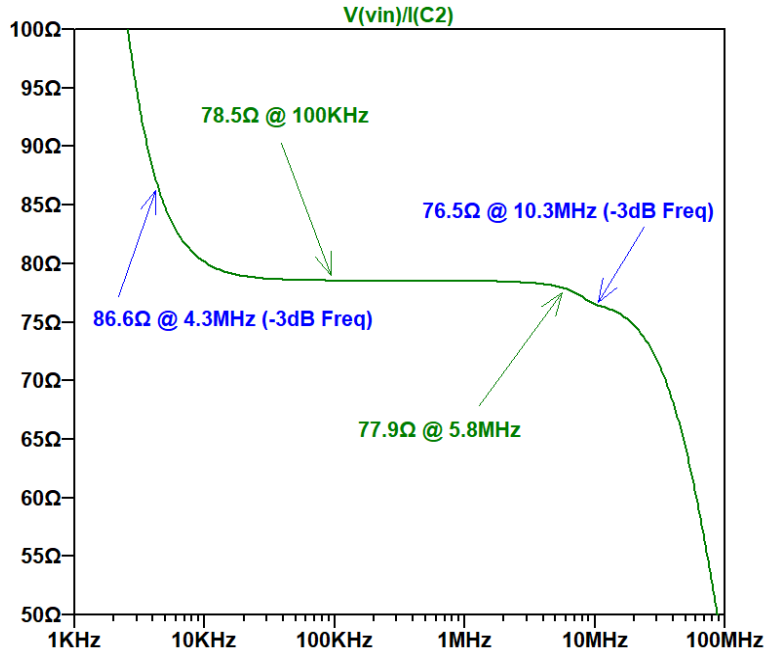


Figure 13. Input Impedance of Nominal Beta Amplifier

The output impedance of the circuit ranges from 9.03 Ω to 7.54 Ω in the minimum operating frequency of 100 kHz to 5.8 MHz (indicated by green marking in Figure 14), and from 39.1 Ω to 40.7 Ω (indicated by blue marking in Figure 14) in the circuit's high and low cut off frequencies range. These values satisfy the design constraint that the output impedance needs to be less than 75Ω.

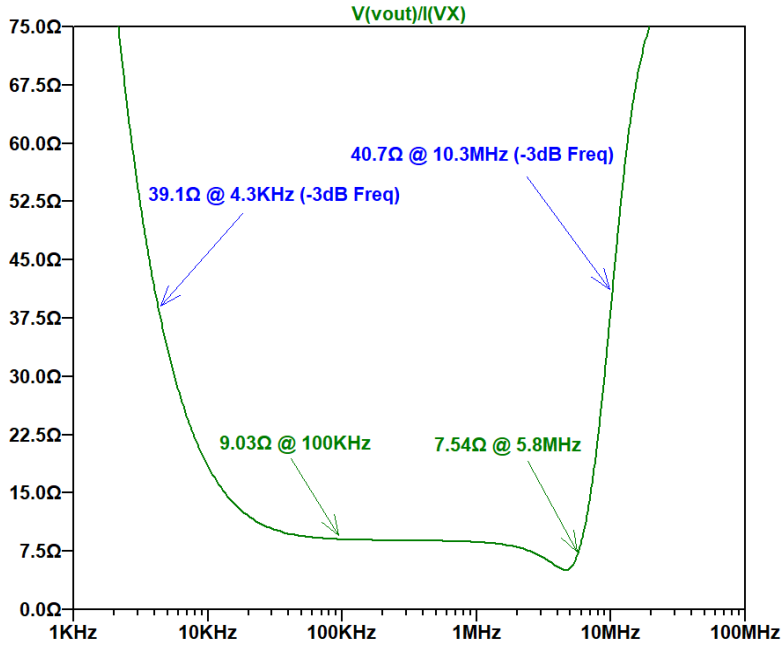


Figure 14. Output Impedance of Nominal Beta Amplifier

5.2 High Beta

Similar to the nominal beta result (Section 5.1), the high beta simulation results satisfy the design constraints with a bandwidth of 4.38 kHz to 10.6 MHz and a midband gain of 65.9 dB, as shown in **Figure 15**. The circuit schematic is in Appendix B.1, and the DC operating point is found in Appendix B.2. The transistors uphold the active operating region as VC > VB > VE. Furthermore, all transistors have VCE value greater than 0.2V indicating that they are not saturated.

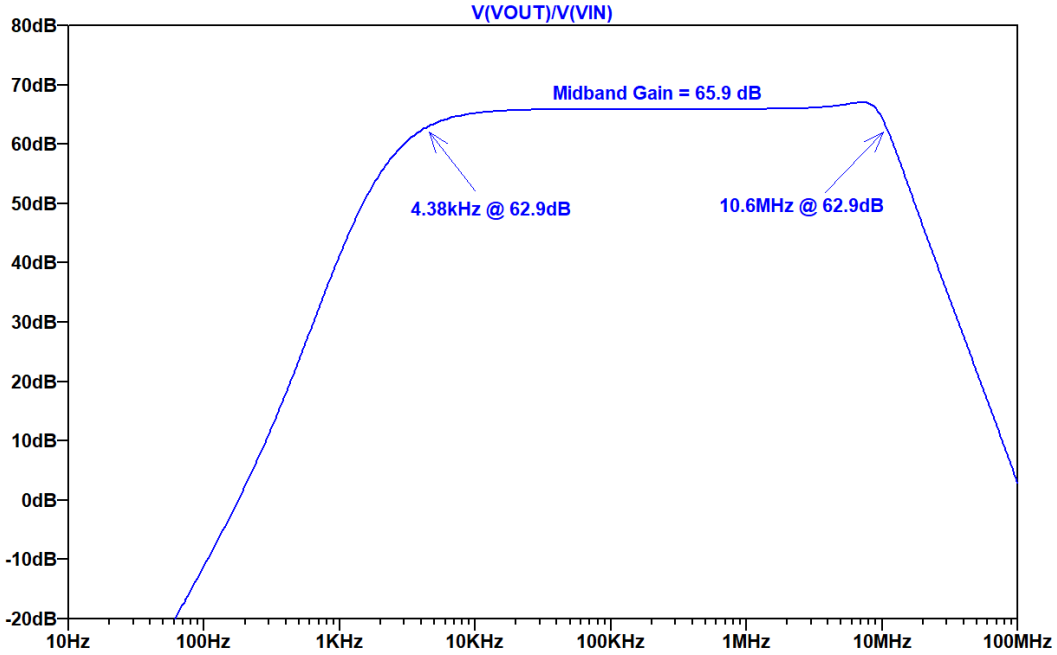


Figure 15. High Beta Bode Gain Plot

Table 2 and Table 3 summarizes the input and output impedances of the circuit under high beta variation. The amplifier satisfies the design constraint that the minimum bandwidth (100 kHz - 5.8 MHz) has an input impedance (Figure 16) within 67.5 to 82.5 Ω and an output impedance (Figure 17) less than 75 Ω, and any variations outside the required bandwidth are beyond consideration.

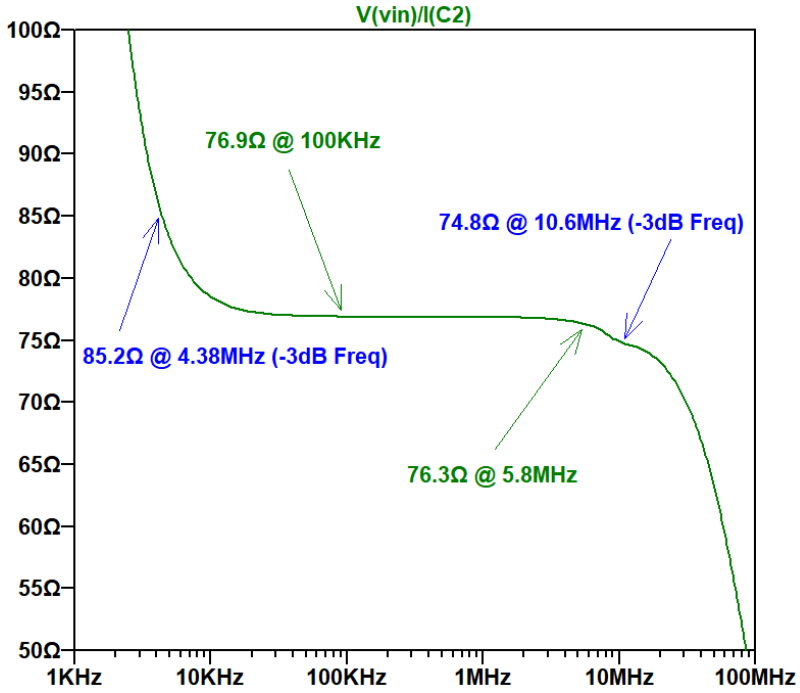


Figure 16. Input Impedance of High Beta Amplifier

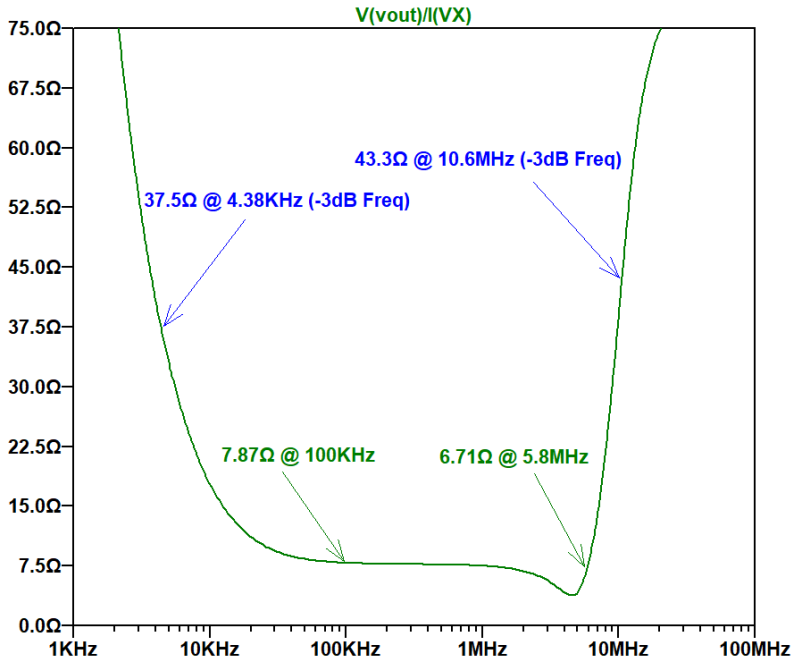


Figure 17. Output Impedance of High Beta Amplifier

5.3 Low Beta

The low beta simulation results satisfy the design constraints with a bandwidth of 4.3 kHz to 9.83 MHz and a midband gain of 64.6 dB, as shown in Figure 18. Appendix C.1 shows the schematic and Appendix C.2 shows the DC operating point of the circuit. The transistors uphold the active operating region as VCE value is greater than 0.2 V and VC > VB > VE.

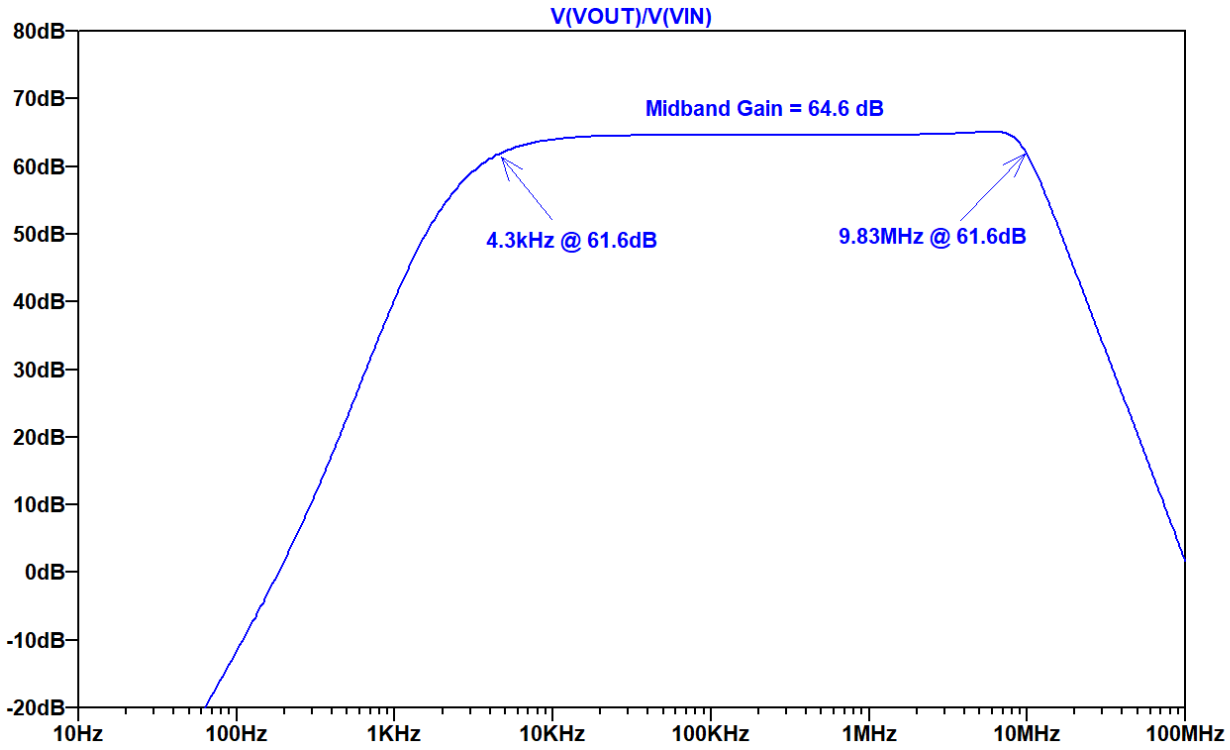


Figure 18. Low Beta Bode Gain Plot

The amplifier also meets the design specifications regarding input and output resistances in the low beta variation, summarized in Table 2 and 3. Figure 19 and Figure 20 demonstrate the plots of the input and output impedances, visualizing that for the required bandwidth (100 kHz - 5.8 MHz) the amplifier has an input resistance between 67.5 to 82.5 Ω and an output impedance less than 75 Ω.

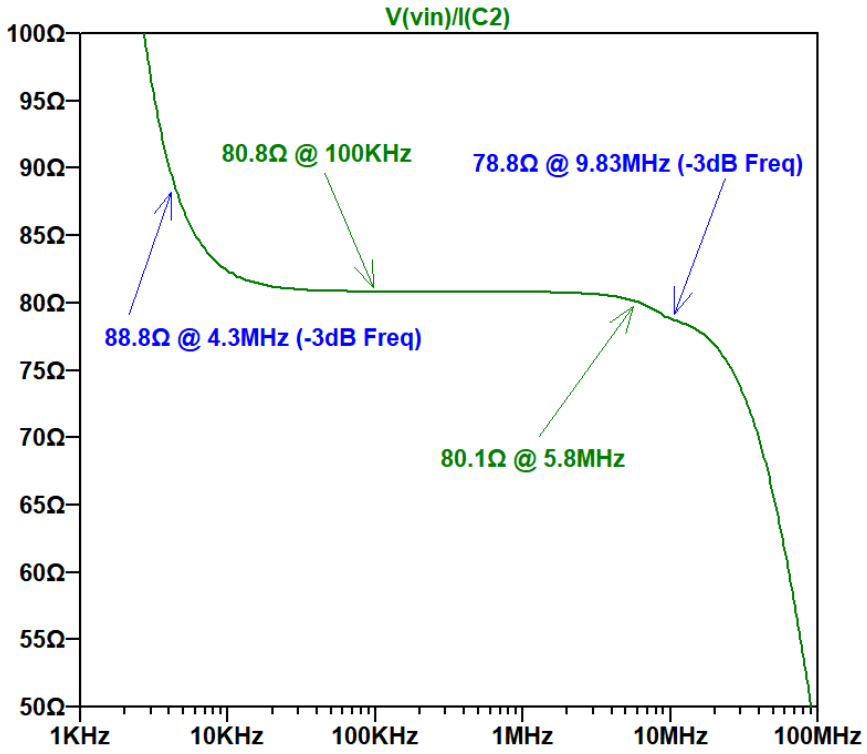


Figure 19. Input Impedance of Low Beta Amplifier

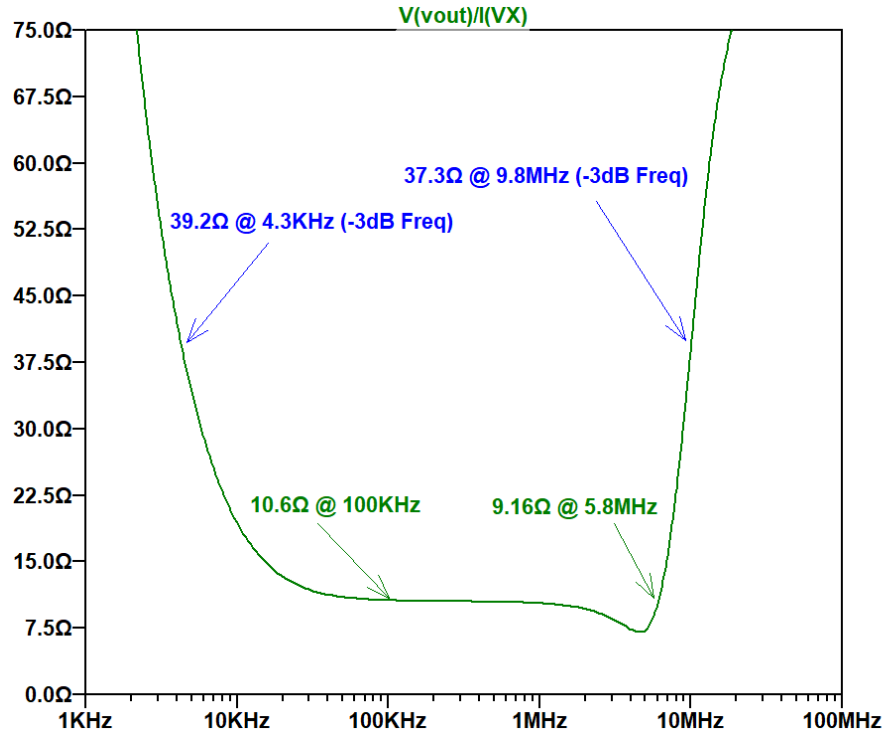


Figure 20. Output Impedance of Low Beta Amplifier

5.4 Power Analysis

After conducting the power analysis procedure as outlined in the simulation experiment section, the current drawn from the 6 V power supply was determined for high, low, and nominal Beta values for the transistors, the results of which are presented in Table 4 below.

Table 4. Power Consumption Over Range of Beta Variations

Beta Value	**Power Supply Current**	**Total Power Consumption**
High Beta	8.37 mA	50.22 mW
Nominal Beta	7.68 mA	46.08 mW
Low Beta	6.95 mA	41.7 mW

The current drawn was found to be greatest for the high range of Beta values, as shown in Figure 21 below in the portion of the DC Operating Point output log. From this current value of 8.37 mA, the maximum power consumption of the amplifier was calculated by multiplying this current by the voltage of the power supply, and the maximum power drawn was determined to be 50.22 mW.

```
I(Rsig):        1.86875e-18    device_current
I(Vsig):        1.86875e-18    device_current
I(Vcc):         -0.00768337    device_current
```

Figure 21. High Beta DC Operating Point Results

Because the value of maximum power consumption was below the maximum allowed 72 mW power draw per the design requirements, over the entire range of Beta variations, this requirement was confirmed to be met.

5.5 Cost Analysis

A cost analysis was performed as part of the verification of design requirements. The table in Appendix D presents a reference for all components used in the design along with associated costs. Summing the costs per unit multiplied with the quantities for each part, a materials cost of $11.64 was obtained. In addition to physical materials, there was a power penalty of $.15 per mW over 40mW power drawn. Additionally, accounting for the 50.22 mW of power drawn for this amplifier, which was 10.22 mW over the 40 mW limit, an additional $1.54 power profit penalty was incurred for this amplifier. Consequently, the total estimated cost of this amplifier was found to be $11.64. Table 5 below outlines the breakdown of costs for this amplifier.

Table 5. Amplifier Associated Costs Itemization

Item	**Amount**	**Cost Per Unit**	**Total Cost**
1% Tolerance Resistor	19	$0.10	$1.90
1 μF Capacitor	11	$0.20	$2.20
ZTX107 BJT	6	$1.00	$6.00
Power Profit Penalty	10.22 mW	$0.15 per mW	$1.54
Total Amplifier Cost			**$11.64**

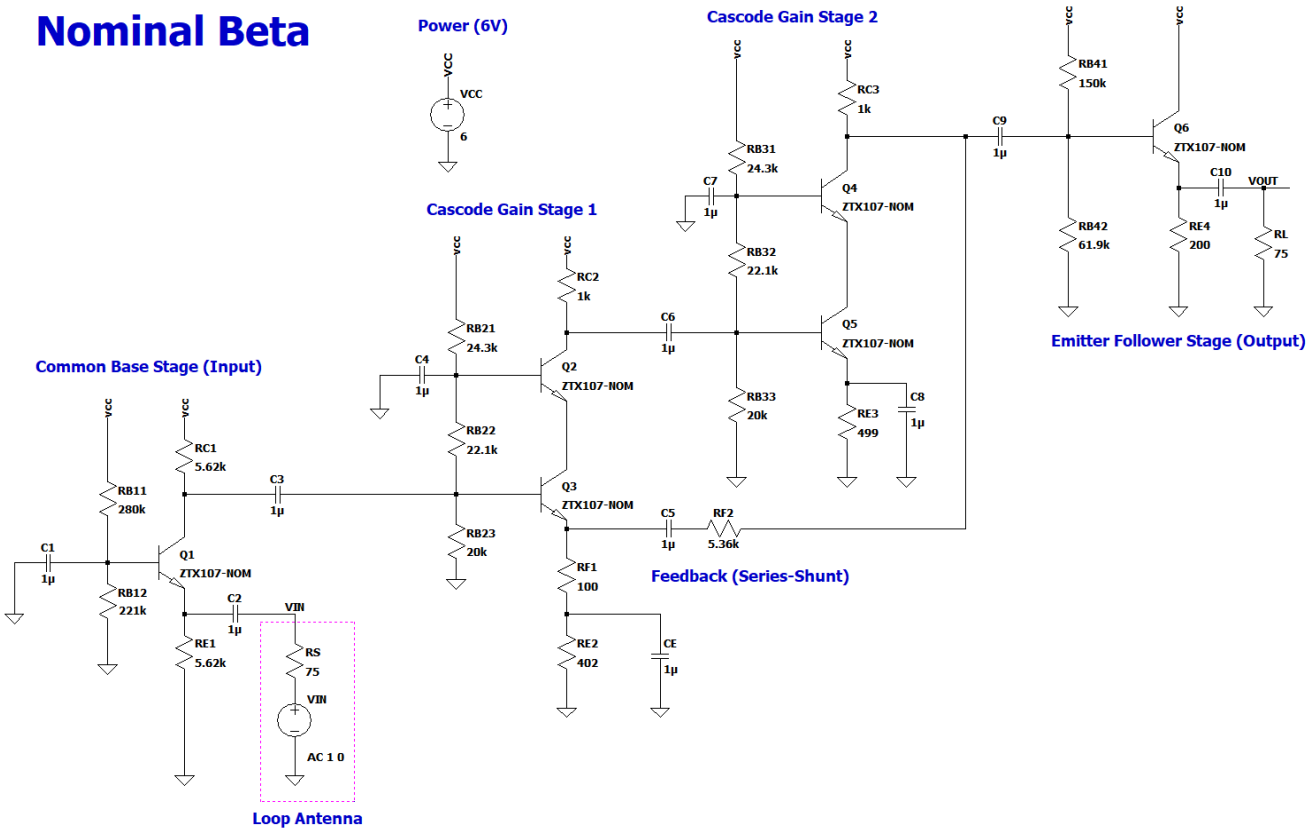
6. Conclusions

The objective of this project was to design a wireless Personal Area Network (PAN) receiver amplifier, as a multi-stage feedback amplifier capable of delivering a gain of 65 dB with a tolerance of 1.5 dB and a bandwidth of at least 100 kHz to 5.8 MHz. Additionally, the amplifier was required to have an impedance matching of 75 Ω input impedance and less than 75 Ω. The design was limited to a 12 mA maximum DC current from a 6 V power supply. Lastly, the design specifications stated that the amplifier must be insensitive to Beta variations, meaning that for Beta variations of up to 50%, the amplifier must remain within all previously stated specifications. After completing all phases of the design process and simulating our final results using LTSpice, the fulfillment of all performance requirements of the amplifier was verified. This amplifier design has a nominal midband voltage gain of 65.4 dB, a bandwidth of 4.3 kHz to 10.3 MHz, an input impedance of 77.9 Ω to 78.5 Ω, and an output impedance of 39.1 Ω to 40.7 Ω. Additionally, despite Beta variations, this amplifier configuration remained within all specifications. This amplifier design proved to be a potentially effective and reliable implementation for a wireless Personal Area Network (PAN) receiver amplifier.

Throughout the design process, several obstacles were encountered that had to be overcome before further progress could be made. For instance, in the initial cascode biasing schemes, a bias current of 0.35 mA was chosen to limit DC power dissipation, and the voltage gain was set before other design parameters. However, because this was far below the nominal 2 mA specified for the ZTX107 transistor, this resulted in the transistors in the cascode stages falling outside of the active region, causing them to fall short in delivering the necessary voltage gain. The takeaway from this was that when designing a DC biasing scheme for a circuit, it is most important to take into account transistor operating regions first, and then secondarily choose parameters such as gain and bandwidth, as gain and bandwidth can be modified through feedback, but it is more difficult to use feedback to change the operating region of the transistor. The second takeaway from this project was that in designs like these it is sometimes desirable to first ensure that gain is maximized, allowing for more leniency in feedback implementation in later stages of the design process, as excess bandwidth is often advantageous, but excess gain is not necessarily a desirable outcome. The third takeaway was that the most effective design tool is hand calculations coupled with engineering insight, which allows for efficient use of time and resources when undertaking large multi-stage design projects. Using engineering insight provides a method for delivering impactful results with the least amount of wasted time and computations. Lastly, this project provided reminders that initial assumptions and strategies need to be re-evaluated in any design process. The separation of this project in phases supplies a useful outline for further project strategies, in that room must always be left for modifications or improvements to enable engineers to deliver reliable and functional designs.

7. Appendix

Appendix A.1 Nominal Beta Circuit Schematic

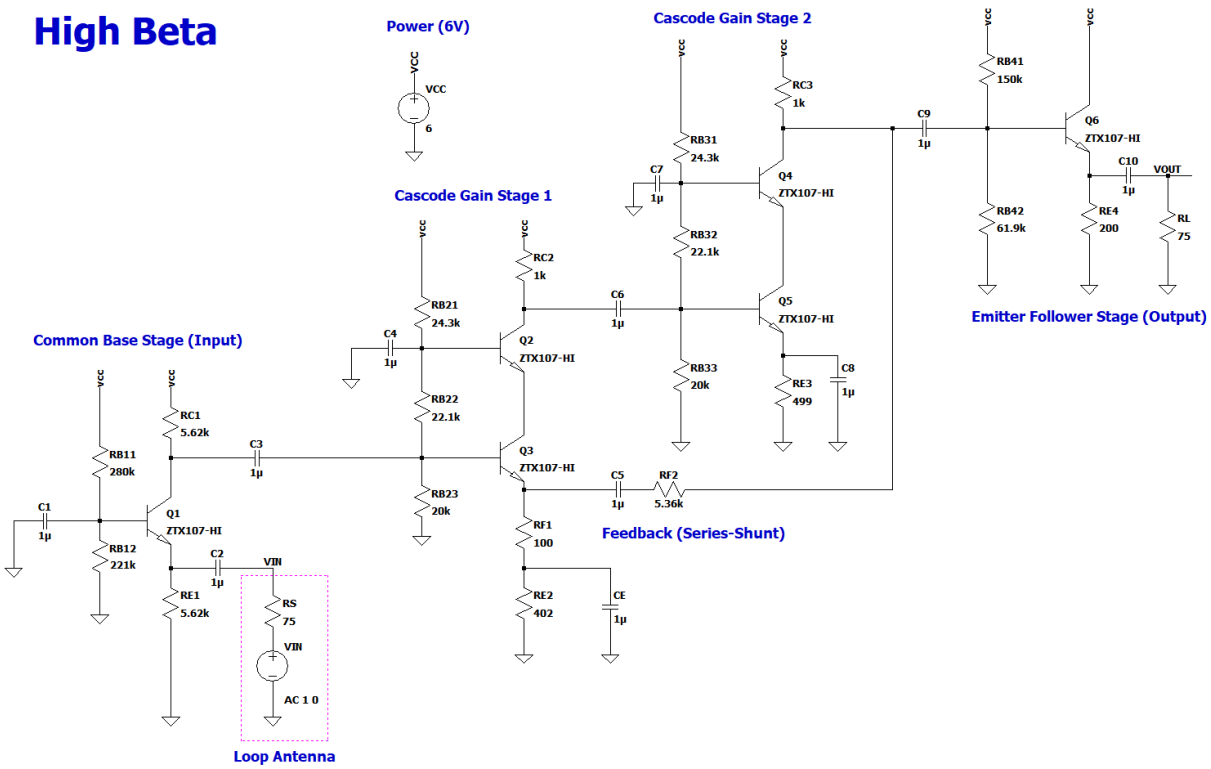


Appendix A.2 DC Operating Point Log for Nominal Beta

```
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                         --- Bipolar Transistors ---
Name:        q1           q2           q3           q4           q5
Model:   ztx107-nom   ztx107-nom   ztx107-nom   ztx107-nom   ztx107-nom
Ib:        1.36e-06     7.04e-06     6.98e-06     7.07e-06     7.01e-06
Ic:        3.31e-04     1.98e-03     1.99e-03     1.99e-03     2.00e-03
Vbe:       6.10e-01     6.57e-01     6.57e-01     6.58e-01     6.57e-01
Vbc:      -1.66e+00    -3.75e-01    -1.33e+00    -3.66e-01    -1.33e+00
Vce:       2.27e+00     1.03e+00     1.99e+00     1.02e+00     1.99e+00
BetaDC:    2.43e+02     2.81e+02     2.85e+02     2.81e+02     2.85e+02
Gm:        1.28e-02     7.56e-02     7.59e-02     7.60e-02     7.63e-02
Rpi:       2.14e+04     3.97e+03     4.01e+03     3.95e+03     3.99e+03
Rx:        5.60e-01     5.60e-01     5.60e-01     5.60e-01     5.60e-01
Ro:        2.35e+05     3.85e+04     3.88e+04     3.83e+04     3.86e+04
Cbe:       2.79e-11     6.88e-11     6.90e-11     6.90e-11     6.92e-11
Cbc:       2.52e-12     3.36e-12     2.66e-12     3.37e-12     2.66e-12
Cjs:       0.00e+00     0.00e+00     0.00e+00     0.00e+00     0.00e+00
BetaAC:    2.74e+02     3.00e+02     3.04e+02     3.00e+02     3.04e+02
Cbx:       0.00e+00     0.00e+00     0.00e+00     0.00e+00     0.00e+00
Ft:        6.70e+07     1.67e+08     1.69e+08     1.67e+08     1.69e+08

Name:        q6
Model:   ztx107-nom
Ib:        1.03e-05
Ic:        3.14e-03
Vbe:       6.69e-01
Vbc:      -4.70e+00
Vce:       5.37e+00
BetaDC:    3.04e+02
Gm:        1.19e-01
Rpi:       2.68e+03
Rx:        5.60e-01
Ro:        2.56e+04
Cbe:       9.69e-11
Cbc:       1.89e-12
Cjs:       0.00e+00
BetaAC:    3.20e+02
Cbx:       0.00e+00
Ft:        1.92e+08
```

Appendix B.1 High Beta Circuit Schematic



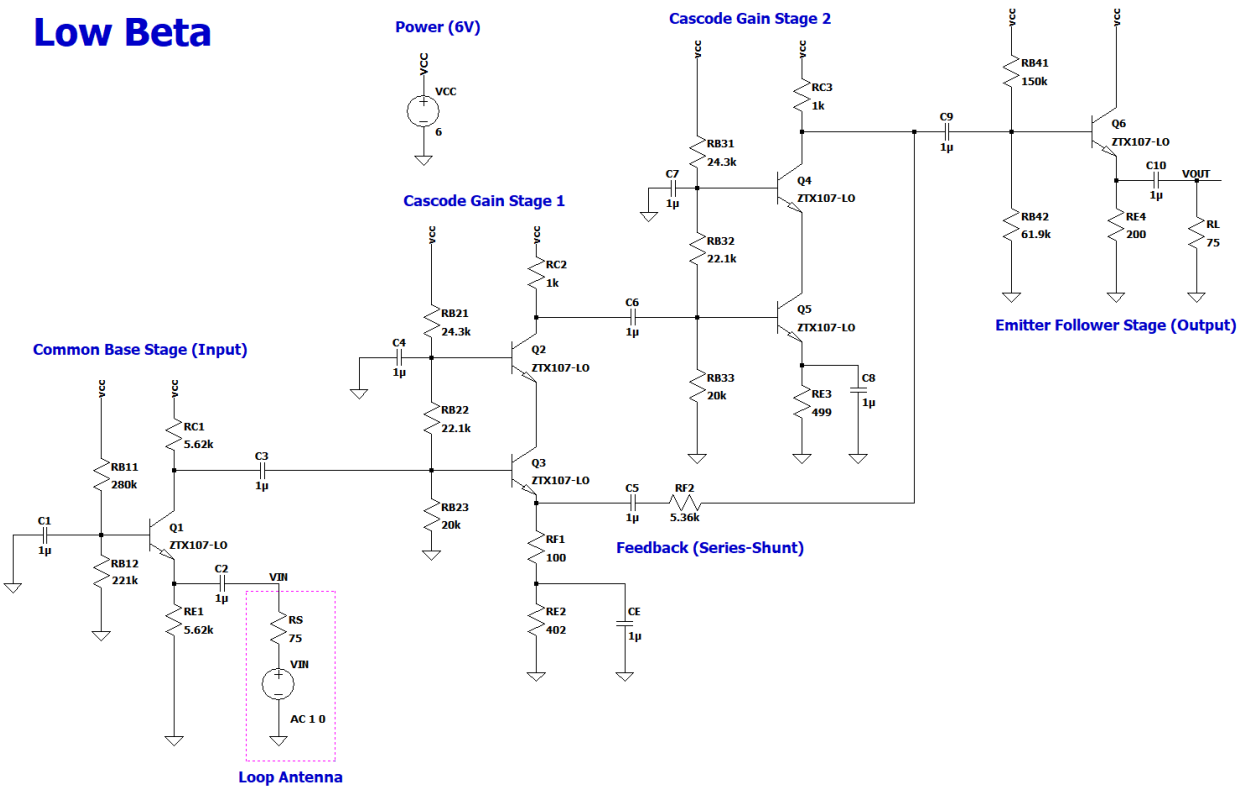
Appendix B.2 DC Operating Point Log for High Beta

--- Bipolar Transistors ---

Name:	q1	q2	q3	q4	q5
Model:	ztx107-hi	ztx107-hi	ztx107-hi	ztx107-hi	ztx107-hi
Ib:	1.02e-06	4.98e-06	4.93e-06	5.00e-06	4.95e-06
Ic:	3.39e-04	2.07e-03	2.07e-03	2.08e-03	2.08e-03
Vbe:	6.10e-01	6.59e-01	6.58e-01	6.59e-01	6.59e-01
Vbc:	-1.57e+00	-2.40e-01	-1.33e+00	-2.29e-01	-1.33e+00
Vce:	2.18e+00	8.98e-01	1.99e+00	8.88e-01	1.99e+00
BetaDC:	3.33e+02	4.16e+02	4.21e+02	4.16e+02	4.21e+02
Gm:	1.31e-02	7.89e-02	7.91e-02	7.94e-02	7.96e-02
Rpi:	3.02e+04	5.85e+03	5.92e+03	5.82e+03	5.89e+03
Rx:	5.60e-01	5.60e-01	5.60e-01	5.60e-01	5.60e-01
Ro:	2.29e+05	3.68e+04	3.72e+04	3.65e+04	3.70e+04
Cbe:	2.81e-11	7.09e-11	7.11e-11	7.12e-11	7.13e-11
Cbc:	2.55e-12	3.54e-12	2.65e-12	3.56e-12	2.65e-12
Cjs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
BetaAC:	3.95e+02	4.62e+02	4.68e+02	4.62e+02	4.68e+02
Cbx:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Ft:	6.80e+07	1.69e+08	1.71e+08	1.69e+08	1.71e+08

Name:	q6
Model:	ztx107-hi
Ib:	7.93e-06
Ic:	3.65e-03
Vbe:	6.73e-01
Vbc:	-4.59e+00
Vce:	5.27e+00
BetaDC:	4.60e+02
Gm:	1.38e-01
Rpi:	3.62e+03
Rx:	5.60e-01
Ro:	2.20e+04
Cbe:	1.09e-10
Cbc:	1.90e-12
Cjs:	0.00e+00
BetaAC:	5.00e+02
Cbx:	0.00e+00
Ft:	1.98e+08

Appendix C.1 Low Beta Circuit Schematic



Appendix C.2 DC Operating Point Log for Low Beta

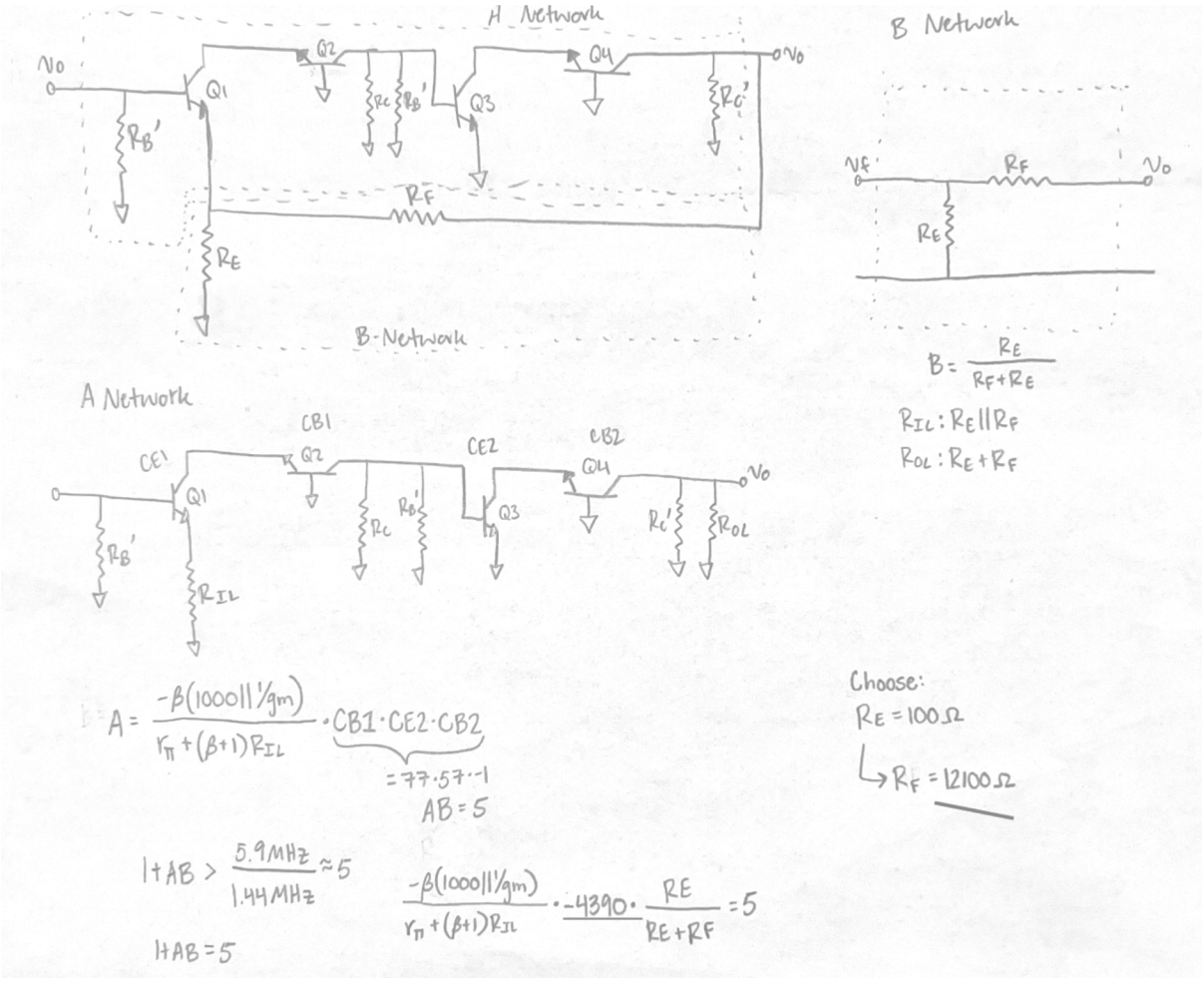
```
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- Bipolar Transistors ---
Name:       q1          q2          q3          q4          q5
Model:   ztx107-lo   ztx107-lo   ztx107-lo   ztx107-lo   ztx107-lo
Ib:       1.82e-06    9.63e-06    9.58e-06    9.67e-06    9.63e-06
Ic:       3.21e-04    1.87e-03    1.88e-03    1.88e-03    1.89e-03
Vbe:      6.09e-01    6.56e-01    6.56e-01    6.56e-01    6.56e-01
Vbc:     -1.77e+00   -5.47e-01   -1.33e+00   -5.39e-01   -1.33e+00
Vce:      2.38e+00    1.20e+00    1.98e+00    1.19e+00    1.98e+00
BetaDC:   1.76e+02    1.94e+02    1.96e+02    1.94e+02    1.96e+02
Gm:       1.24e-02    7.14e-02    7.17e-02    7.17e-02    7.21e-02
Rpi:      1.55e+04    2.83e+03    2.85e+03    2.82e+03    2.83e+03
Rx:       5.60e-01    5.60e-01    5.60e-01    5.60e-01    5.60e-01
Ro:       2.43e+05    4.09e+04    4.11e+04    4.07e+04    4.09e+04
Cbe:      2.76e-11    6.61e-11    6.63e-11    6.63e-11    6.65e-11
Cbc:      2.47e-12    3.18e-12    2.66e-12    3.18e-12    2.66e-12
Cjs:      0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
BetaAC:   1.92e+02    2.02e+02    2.04e+02    2.02e+02    2.04e+02
Cbx:      0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Ft:       6.55e+07    1.64e+08    1.66e+08    1.64e+08    1.66e+08

Name:       q6
Model:   ztx107-lo
Ib:       1.27e-05
Ic:       2.64e-03
Vbe:      6.64e-01
Vbc:     -4.81e+00
Vce:      5.47e+00
BetaDC:   2.07e+02
Gm:       1.00e-01
Rpi:      2.13e+03
Rx:       5.60e-01
Ro:       3.05e+04
Cbe:      8.47e-11
Cbc:      1.88e-12
Cjs:      0.00e+00
BetaAC:   2.14e+02
Cbx:      0.00e+00
Ft:       1.84e+08
```

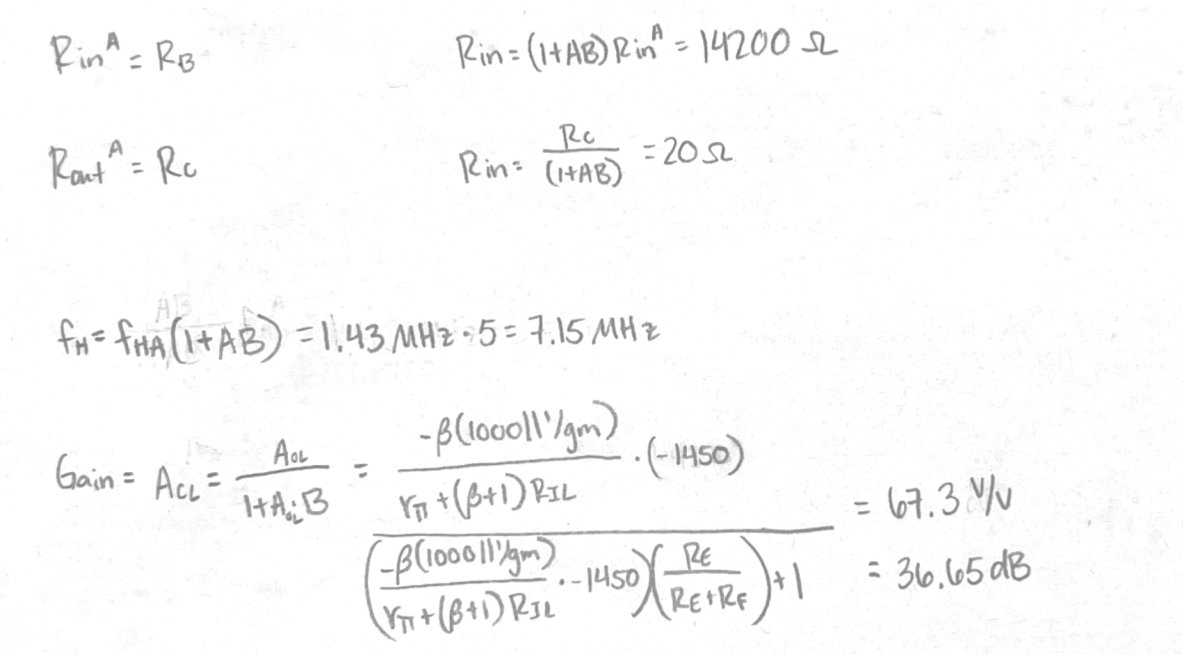
Appendix D Parts List with Costing Information

Part Name	Cost Per Unit
Resistor	$0.10
Capacitor	$0.20
Q2N2222 NPN BJT	$0.50
TIS98 NPN BJT	$0.75
ZTX107 NPN BJT	$1.00
Q2N2222 PNP BJT	$0.50
TIS98 PNP BJT	$0.75
ZTX107 PNP BJT	$1.00

Appendix E.1 Feedback Network Calculations



Appendix E.2 Calculation of Initial Feedback Effects



Appendix E.2 Final Modification of Feedback

```
Solve[{AORIGINAL == (-300 * (1/(1/1000 + 2/26)))/(300.0 * 26/2 + 301 * (1/(1/100 + 1/12100))) * -77 * 57, BORIGINAL == 100/(100 + 12100), RE == 100, A/(1 + A * B) == AORIGINAL/(1 + AORIGINAL * BORIGINAL) * .5,
 A == (-300 * (1/(1/1000 + 2/26)))/(300.0 * 26/2 + 301 * (1/(1/RE + 1/RF))) * -77 * 57, B == RE/(RE + RF)}, {AORIGINAL, BORIGINAL, RE, A, RF, B}]
```

Solve: Solve was unable to solve the system with inexact coefficients. The answer was obtained by solving a corresponding exact system and numericizing the result.

```
{{AORIGINAL → 500.616, BORIGINAL → 0.00819672, RE → 100., A → 505.217, RF → 5332.07, B → 0.0184092}}
```