Imperas models for SW developers

Update for OpenHW SW tools group

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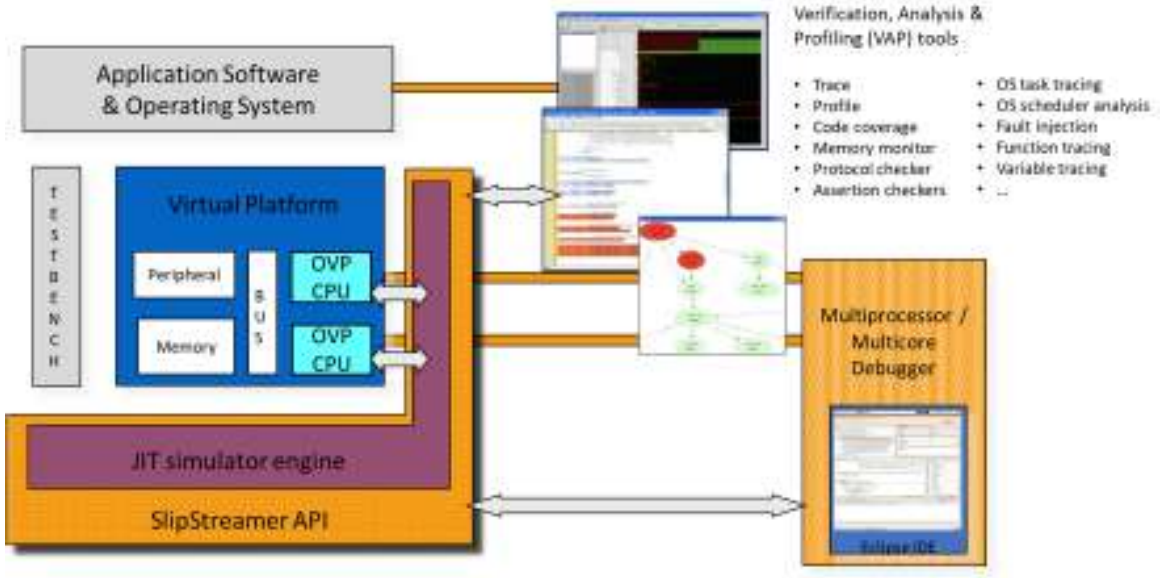
Imperas – providing solutions to SW developers for over 10 years



ISAs: Arm, MIPS, Power, RISCV, Microblaze, Nios, Renesas, DSP…

CPUs: 250+ processor models
Peripherals: 300+ models
Reference platforms: 30+

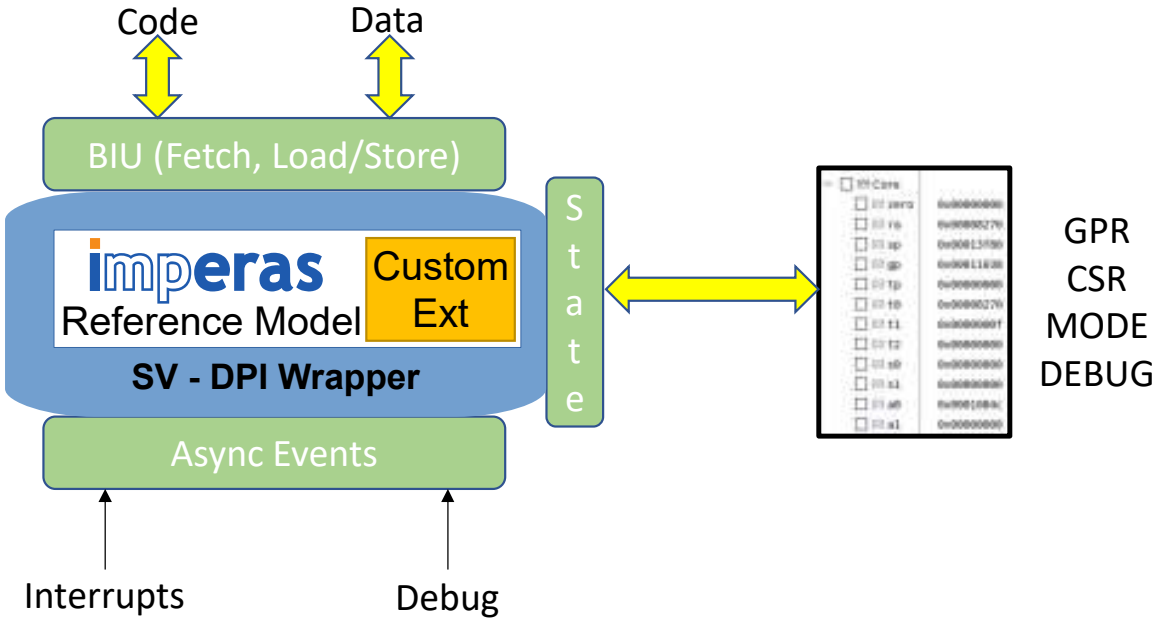
Tools: trace, coverage, profiling, assertions, checkers, fault injection, OS aware analysis

- Used by embedded SW developers and SW tools developers
  - Usage: compilers, RTOS, OS, bare metal, full reference platforms, full App stacks
- Imperas' focus is world leading processor models and platform emulation
  - Helping SW teams is Imperas' core business

Imperas Reference Model (at the core of Imperas solutions)

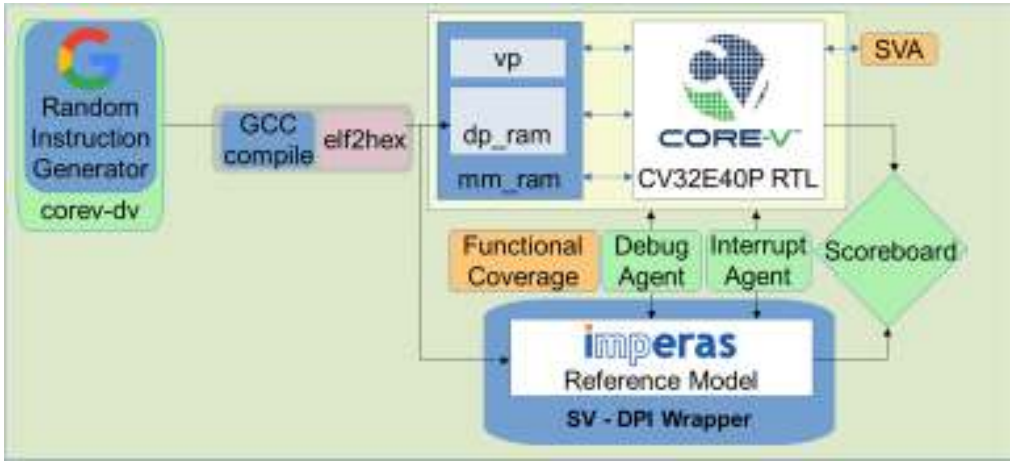
- Imperas reference model covers the envelope of the full RISC-V specification
  - RV32/64 IMAFDCEN (2.2/2.3, 1.10/1.11 specs), M,S,U,D
  - Privileged, Unprivileged (user), Debug, and CLIC Specification
  - Soon to be ratified specs:
    - B – bitmanip
    - K – crypto (scalar)
    - V – vector
    - P – DSP / SIMD
    - H – hypervisor
  - Model is available under Apache 2.0 Open Source
- For each spec of the ISA Imperas model can have version of spec specified
  - Fundamental feature – to ensure that the model is what you are designing/using
- For each spec of the ISA Imperas model can have legal options selected (133 currently)
- Designed for quality, speed, efficiency, accuracy, flexibility, maintenance
  - Technology is World leading - supports 13+ public ISAs, faster than all others
- Useable in many simulation environments; C, C++, SystemC, SystemVerilog
  - Designed to work in users environments
- Used as golden reference by many leading Arm, MIPS, RISCV, custom users

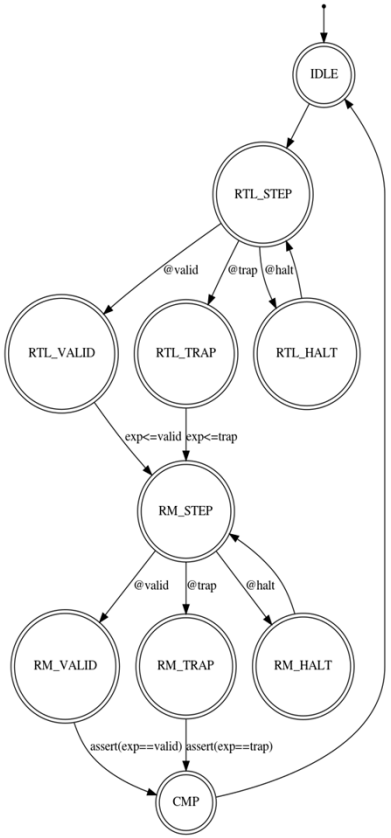
Imperas Reference Model Usage: HW DV



- Encapsulate ref model with assets for use in C, C++, SystemVerilog simulators
- Can extend with custom extension without modifying core code
- Central component of quality DV methodology

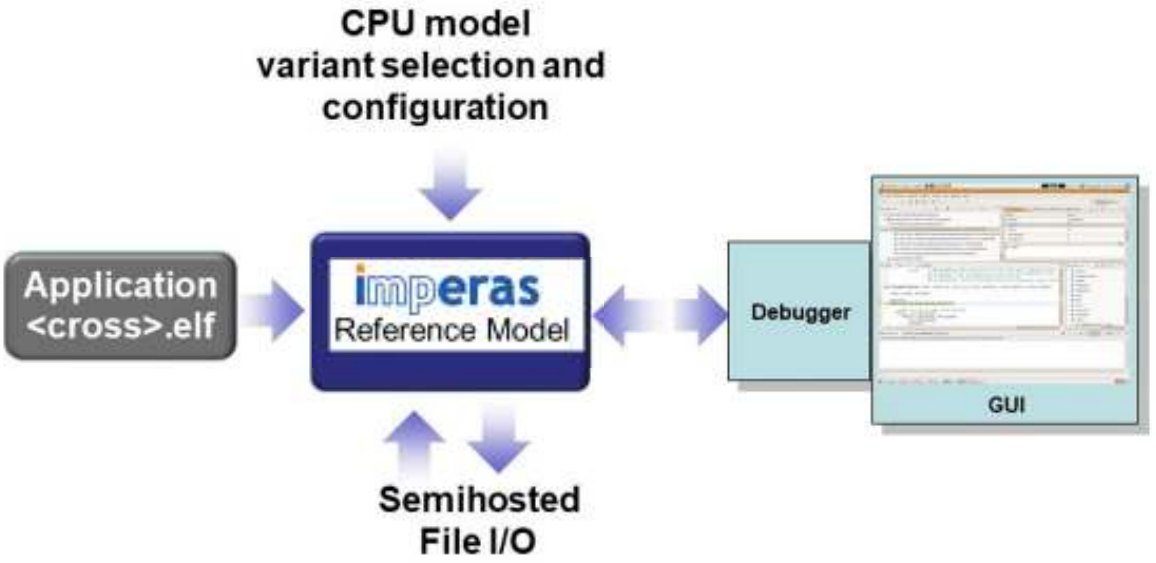
Imperas model key part of advanced UVM verification





- OpenHW Core-V-Verif UVM solution

Imperas model at the centre of free Instruction Set Simulators

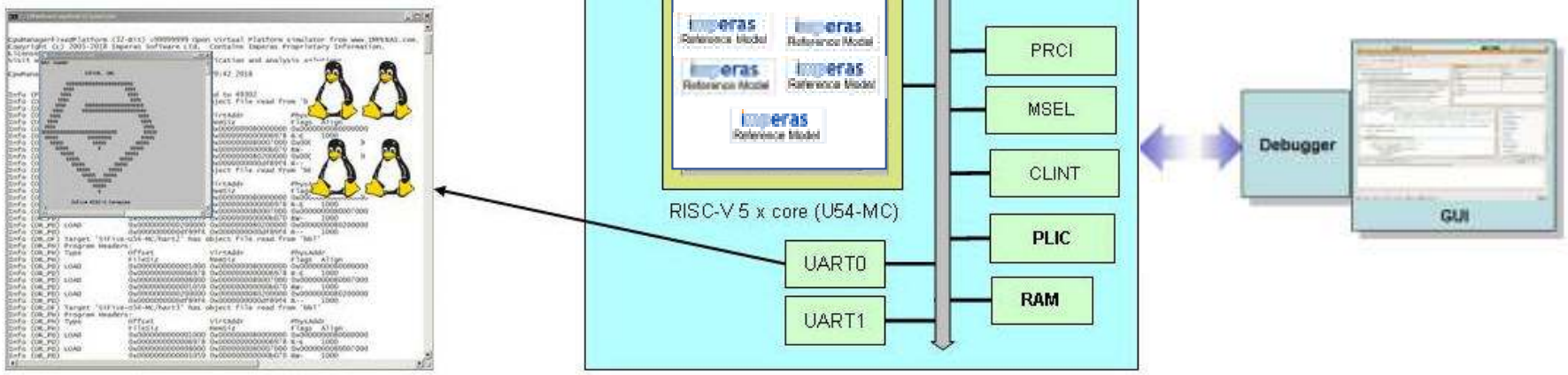


- Complete, fully functional, configurable model / simulator
  - Select from many built in variants
- Includes built-in instruction functional coverage
- Includes full open source Apache 2.0 model
- Allows configurable memory regions
- Works 'out of the box' with full tracing, debug, and many other options
- Includes GDB connection and Eclipse integration
- Closed source binary proprietary freeware simulator (like Google Chrome etc)
- FREE, un-restricted usage – no FlexLM licensing etc

Example: riscvOVPsimPlus.exe
https://www.ovpworld.org/riscvOVPsimPlus/

Imperas model at the centre of the free platform emulators

Imperas FU540 Fixed Virtual Platform



- Example SiFive FU540 Fixed Virtual Platform - includes all needed models – just like reference board
- Delivered as .exe
- Works 'out of the box' with full tracing, debug, and many other options
- Includes GDB connection and Eclipse integration
- Closed source binary proprietary freeware simulator (like Google Chrome etc)
- Can be FREE, un-restricted usage – no FlexLM licensing etc

Imperas and OpenHW SW tools

- Imperas can develop and provide for SW developers:
  - OpenHWriscvOVPsim.exe – free, reference of OpenHW cores for SW developers
    - includes accurate models of all OpenHW cores and appropriate options
    - full program loading, tracing, gdb, eclipse debug
    - closed source proprietary freeware = free, no FlexLM
    - (similar to riscvOVPsimPlus used for compliance and 'low end' DV solutions)
  - OpenHWriscvMCU.exe – free, fixed MCU virtual platform for SW development
    - includes accurate model of OpenHW core
    - includes required peripherals
    - full program loading, tracing, gdb, eclipse debug
    - closed source proprietary freeware = free, no FlexLM
- Lets discuss…
  - These solutions address the needs of the OpenHW SW tools group – with no effort