School of

Electronics and Communication Engineering

Minor Project-2 Report on

NB-IoT UPLINK TRANSMISSION CHAIN

By:

1. **L Ashok Kumar Reddy** USN: 01FE21BEC223
2. **Soundarya Prabhu** USN: 01FE21BEC227
3. **Shreya Prabhu** USN: 01FE21BEC228
4. **Lavanya R Muttagi** USN: 01FE22BEC415

Semester: VI, 2023-2024

Under the Guidance of

Dr. Saroja V. Siddamal

K.L.E SOCIETY'S
KLE Technological University,
HUBBALLI-580031
2023-24

SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that the project entitled "**NB-IoT UPLINK TRANSMITTER CHAIN**" is a bonafide work carried out by the student team of "**L Ashok Kumar Reddy (01FE21BEC223), Soundarya Prabhu (01FE21BEC227), Shreya Prabhu (01FE21BEC228), Lavanya R Muttagi (01FE22BEC415)**". The project report has been approved as it satisfies the requirements concerning the minor-project-2 work prescribed by the university curriculum for BE (VI semester) in the School of Electronics and Communication Engineering of KLE Technological University for the academic year 2023-24.

Dr. Saroja V. Siddamal	**Dr. Suneeta V. Budihal**	**Dr.B. S. Anami**
Guide	**Head of School**	**Registrar**

External Viva:

Name of Examiners	**Signature with date**
1. Saroja V. S	20/6
2. Gireesha H. M.	20/6/24

ACKNOWLEDGMENT

We would like to extend our gratitude to the educators who helped in the completion of this project. Their support, guidance, and the information about the project they provided have been invaluable throughout this journey.

We would like to convey our gratitude to Dr. Saroja V. Siddamal, our project's guide, for her unwavering support, inspiration, and leadership in keeping us motivated throughout the project. She established high expectations for us and gave us the latitude we needed to carry out the job, for which we are grateful.

Our sincere gratitude goes out to Dr. P. G. Tewari, Principal of KLE Technological University, Hubballi, Dr. Ashok Shettar, Vice Chancellor of KLE Technological University, Hubballi, and Dr. Suneeta V. Budihal, Head of School of Electronics and Communication, for giving us the chance to enroll in this special course and pursue our research interests.

-Ashok R, Soundarya P, Shreya P, Lavanya M

ABSTRACT

The project is to design a robust system that combines essential components for reliable communication. The Turbo code, operating at a 1/3 coding rate, employs parallel concatenated recursive systematic convolutional (RSC) codes. The Channel Interleaver spreads errors discretely, minimizing data loss. Additionally, a Repetition block ensures error-free data delivery in challenging reception areas. The DMRS (Demodulation Reference Signal) block aids accurate channel estimation, enhancing overall coverage and performance. By integrating these elements, our system achieves extended coverage and efficient data transmission.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

NB-IoT is based on a Long-Term Evolution (LTE) and thus operates in the licensed spectrum. It is designed to take into account most of the IoT service requirements. Internet of Things [IoT] is an ecosystem that includes Narrowband Internet of Things (NB-IoT) which is a communication technology that is designed to enable efficient communication between devices. It includes very good indoor coverage, support for massive numbers of connected devices, very low cost of connectivity, low power consumption, and optimized network architecture. It is LPWAN-based wireless communication developed by 3GPP for devices that require low bandwidth and a small amount of data transfer. Most of NB-IoT's functionality, along with its key channels and signals, are carried over from LTE. NB-IoT user equipment modules have low power and low cost, thus to accommodate these limits, the complexity of these channels and signals was decreased. Fewer channels and signals were used to accommodate the new NB-IoT frame structure. The system was intended to operate in the 180 kHz frequency range. To preserve LTE system performance and guarantee coexistence with LTE operators, the NB-IoT defined three operation modes: - In-band mode: One PRB of the LTE bandwidth is taken up by the NB-IoT transmission. -Guard-band mode: The NB-IoT signal uses one PRB of the LTE bandwidth's unused guard band PRBs. -Stand-alone mode: The Global System for Mobile Communications (GSM) system's freed spectrum is meant to be occupied by the NB-IoT signal. In this instance, the 200 kHz GSM carrier and the 180 kHz NB-IoT signal are still in use, with a 10 kHz band guard on either side of the spectrum. In this project, we have done some NB-IoT Uplink transmission chain blocks like Turbo encoder, Channel Interleaver, Repetitive block, and DMRS.

1.1 Motivation

NB-IoT is a significant research area in the field of communication systems. It has many features like reliability in communication, data integrity, and security which is important in environments where error is high. The transmission block helps in enhancing the transmission of messages properly over the channel. Turbo Encoder is a type of encoding technique that uses shift registers and feedback connection allowing them to encode the information in a continuous way rather than in fixed blocks. It has features like bandwidth efficiency and low complexity decoding which make it a better technique for encoding. This project not only navigates the complexity of Turbo Encoding but also contributes to the harmony of NB-IoT technology. The other blocks that are designed with this project in the transmission chain are shown in Figure 1.

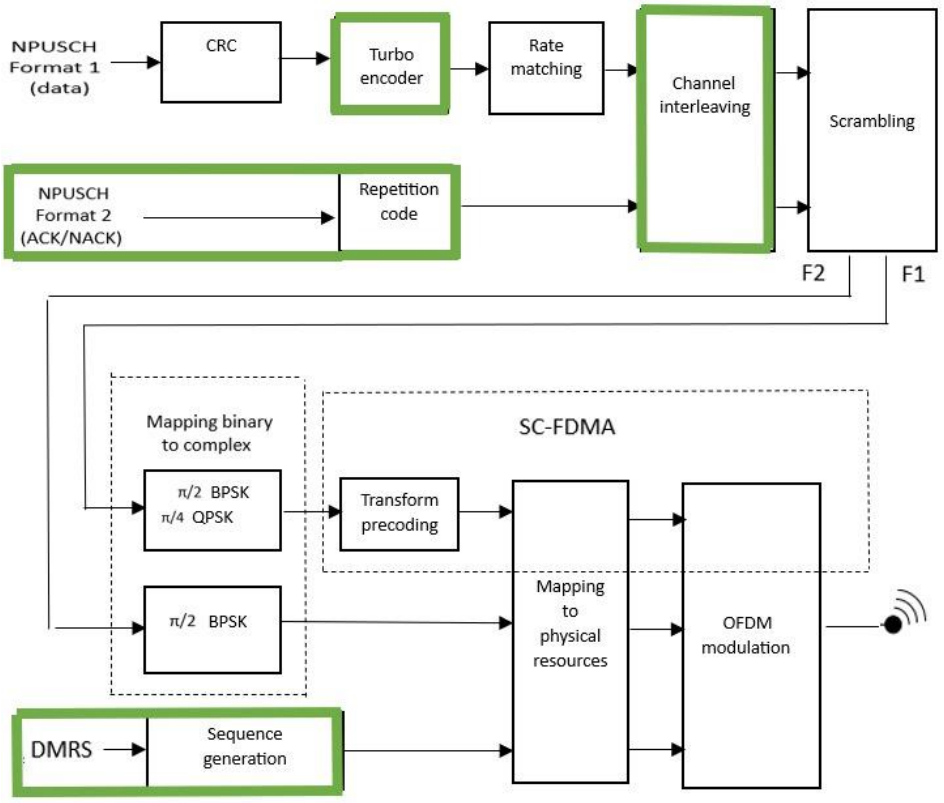


Fig .1. NB-IoT UPLINK Transmission chain

1.2 Objectives

1. To design and implement a Turbo encoder using 1/3 coding rate.
2. To design Channel Interleaver based on the number of input bits.
3. To set a proper generator polynomial sequence as per the design specification.
4. To design and implement Repetition blocks using format specifiers.
5. To design a DMRS using specifications.

1.3 Literature Survey

1. “Software-Defined NB-IoT Uplink Framework—The Design, Implementation and Use Cases by Alicja OlejniczakORCID, Olga Błaszkiewicz, Krzysztof K. Cwalina ORCID, Piotr RajchowskiORCID and Jarosław Sadowski ORCID”: This paper presents a software-defined NB-IoT uplink framework in the design domain, along with its implementation and its applications. The framework can be developed, examined, and optimized for digital transmitter pathways as an academic tool. The main components of the NB-IoT interface's physical layer—which is utilized by sensor devices—are the focus of the suggested realization. In addition, the article emphasizes the necessity of optimizing data processing to reduce power consumption and resource usage of the NB-IoT node while sending collected telemetric data [1].

2. “3rd Generation Partnership Project; Technical Specification Group Radio Access

Network; Evolved Universal Terrestrial Radio Access (E-UTRA); Multiplexing and channel coding (Release 10)". The document provides thorough technical requirements and protocols for effective data transmission in wireless communication networks, and it acts as a comprehensive guide for implementing coding, multiplexing, and channel mapping in the E-UTRA system [2].

3. "Design and FPGA-Based Hardware Implementation of NB-IoT Physical Uplink Shared Channel Transmitter and Physical Downlink Shared Channel Receiver": The study highlights the useful features of developing and implementing such systems for Internet of Things applications, offering insightful information on the hardware implementation of NB-IoT communication systems. To satisfy the various needs of IoT services, the study advances low-power wide-area (LPWA) technologies, with an emphasis on NB-IoT [3].

4. "Evolved Universal Terrestrial Radio Access (E-UTRA); Physical layer procedures (3GPP TS 36.213 version 15.2.0 Release 15)": The paper presents about physical layer and specifies and establishes the characteristics of the physical layer procedures in the FDD and TDD modes of E-UTRA [4].

5. "3GPP TS 36.213 version 14.2.0 Release 14: Evolved Universal Terrestrial Radio Access (E-UTRA); Physical layer procedures": The paper explains Physical uplink shared channel-related procedures and resource allocation for PDCCH/EPDCCH with uplink DCI format [5].

6. "3GPP TS 36.212 version 13.4.0 Release 13: Evolved Universal Terrestrial Radio Access (E-UTRA); Multiplexing and channel coding": The paper details different channel quality information feedback forms and setups for PDSCH transmissions are provided. There are many transmission modes with specific antenna ports and PMI/RI reporting [6].

7. "3GPP TS 36.212 version 15.2.1 Release 15: Evolved Universal Terrestrial Radio Access (E-UTRA); Multiplexing and channel coding": The literature explains all transmission blocks including uplink transmission chain blocks and their specific parameters including related polynomials [7].

8. "Matthieu Kanj, Vincent Savaux, Mathieu Le Guen. A Tutorial on NB-IoT Physical Layer Design Communications Surveys and Tutorials"2020": Based on the 3GPP Version 13 standard, the article offers an in-depth guide on the physical layer design of Narrowband Internet of Things (NB-IoT) technology. NB-IoT is one of the prominent low-power wide-area (LPWA) technologies that have emerged as a result of the Internet of Things (IoT) exponential expansion. This tutorial covers both the transmitter and receiver parts of the NB-IoT base station (eNB) and user equipment (UE), with an emphasis on the physical layer features of NB-IoT. A detailed examination of the characteristics, scheduling, and transmission methods of physical channels and signals in the downlink and uplink directions is one of the tutorial's main strengths. By providing useful insights without going into great detail about 3GPP requirements, the paper seeks to make the NB-IoT system easier to understand. Examples and use cases are provided for each idea to help improve understanding. Moreover, the paper expands its scope to include the improvements and new characteristics that have been included in NB-IoT. The detailed

summary is an invaluable tool for researchers, engineers, and students who want to learn the basics of the NB-IoT standard Additionally, the study acknowledges the open-source program OpenAI Interface has implemented the PHY layer functionalities of the 3GPP standard, as demonstrated in the tutorial, and stresses its usefulness as a starting point for academics interested in the NB-IoT system. This creates opportunities for real-world testing and possible innovation in demodulation procedures, receiving, and other NB-IoT technology areas. The paper's hands-on approach makes it unique and an important addition to the literature survey for anyone interested in NB-IoT technology [8].

1.4 Problem statement

Design and implement a communication system with a 1/3 rate Turbo encoder for a K=2560, utilizing a 24-bit CRC, a Channel Interleaver with specified parameters, format 2 with a Repetition code of 24 bits, and an implementation of DMRS using single-tone and multitone transmission.

1.5 Organization of the report

Until now, Chapter 1 has the introduction, motivation, and objectives of the problem statement described so far in this work.

- The block diagram and the information on system design are discussed in Chapter 2.
- Chapter 3 includes the flow chart of the Turbo encoder, Channel Interleaver, repetition code, DMRS the device and its specification, and the algorithm.
- Chapter 4 gives information about the result obtained and analysis of it through the calculation of the total time the Turbo encoder, Channel Interleaver, repetition block, and DMRS design took to produce the desired output bits.
- Chapter 5 includes the conclusion and the future scope of our project.

Chapter 2

System Design

This chapter elaborates on all the transmitter blocks and the methodology used to design them.

2.1 CRC Block

This block is used for error-detecting of data and information present in the communication channel. For the uplink channel, 24 bits of CRC attachment is done with the payload and sent to the next block of the transmitter. The input bits of CRC are denoted by i0, i1, i2, i3....i(n-1) and the parity bits by p0, p1, p2...p(l-1). Here 'n' is the size of the input sequence, and 'l' is several parity bits. The generator polynomial used for the uplink channel is

$$g24 = [C^{24}+C^{23}+C^{18}+C^{17}+C^{14}+C^{11}+C^{10}+C^{7}+C^{6}+C^{5}+C^{4}+C^{3}+C+1] \quad (2.1)$$

2.2 Channel coding

2.2.1 Turbo Encoder

The turbo encoder uses parallel Concatenation Convolution Code (PCC). This consists of two RSC encoders and a Turbo Interleaver. The code rate is 1/3. The polynomial equation used is:

$$g\,[1] = 1 + g^2 + g^3 \quad (2.2.1)$$

$$g\,[2] = 1 + g + g^3 \quad (2.2.2)$$

The input bits to this block are 2560 bits.

The RSC encoder is similar to the convolution encoder. It has constraint length L=4 and memory register m=3.

Turbo Interleaver: The method used is Quadratic permutation polynomial. The parameters considered are w1=39, w2=80, and block size B=2560. The input sequence is denoted as n0, n1, n2...n(B-1), where B is the number of input bits. The output bits from Turbo code Interleaver are denoted by n'0, n'1, n'2.... n'(B-1). The input and output equations are related as;

$$n'i = n\pi(i), i = 0, 1 \ldots (B - 1) \quad (2.2.3)$$

. The relation of output index 'i' and input index pi(i) is;

$$\pi(i) = (w1 * i + w2 * i2) mod B \quad (2.2.4)$$

Trellis termination: It is adding tail bits to the output sequence by performing shifting operations. The shift sequence is given below;

$A_k^{(0)} = P_k$	$A_{k+1}^{(0)} = Q_{k+1}$	$A_{k+2}^{(0)} = P'_k$	$A_{k+3}^{(0)} = Q_{k+1}'$
$A_k^{(1)} = Q_k$	$A_{k+1}^{(1)} = P_{k+2}$	$A_{k+2}^{(1)} = Q'_k$	$A_{k+3}^{(1)} = P_{k+1}'$
$A_k^{(2)} = P_{k+1}$	$A_{k+1}^{(2)} = Q_{k+2}$	$A_{k+2}^{(2)} = P'_{k+1}$	$A_{k+3}^{(2)} = Q_{k+2}'$

2.3 Rate matching

It consists of three parts:

- Sub-block Interleaver
- Bit collection
- Bit selection and pruning.
- Ak(0), Ak(1), Ak(2) are input to rate matching.
- It is used to match the bits in the transport block to the bits that can be transmitted in a given allocation.

2.4 Repetition Block

It consists of ACK/NACK bits that are repeated 16 times and sent to Channel Interleaver blocks. For ACK (1 bit) and NACK (0 bit). This also adds randomness to a sequence which helps in improving the error.

2.5 Channel Interleaver

The Channel Interleaver is used to improve the error of data transmitted in the channel. The method used is Block Interleaver in which inputs are stored column-wise and output is read row-wise. The parameters considered are n_row = 216, n_col = 12, and the total bits is T = n_row * n_col i.e. 2592.

$$n\_row = N\_sc * N\_ru * Qm \quad (2.5.1)$$

$$n\_col = \left(N_{sym} - 1\right) * \ n\_slots \quad (2.5.2)$$

Where N_sc=18, N_ru=6, n_slots=2, Nsym=7, Qm=2.

The row and column are taken based on the input entering the block. As input bits are 2564 the minimum combination of row and column that can make up to 2564 is 2592.

2.6 Scrambler

The input for this block comes from Channel Interleaver. The first input from format 1 has a bit size of 2592. The second input from format 2 has a bit size of 16.

2.7 Modulation

In modulation, data bits are converted into symbols. For format 1 QPSK modulation is used in which two bits are converted into one symbol. For format 2 π/2 BPSK modulation is used in which one bit is converted into one symbol.

2.8 DMRS (sequence generator)

DMRS is called the pilot of the uplink. It is used for channel estimation in the frequency domain. For single-tone transmission i.e. Nsc=1,

$$Tu(n) = 1/\sqrt{2} * (1 + j)(1 - 2c(n))w(n \ mod \ 16) \quad (2.8.1)$$

Where n is 0 to Nseq-1. Nseq=Mrep*Nslot*Nru=128*16*10. c(n) is pseudo random sequence, w(n) is Hadamard sequence. w(n) is depended on 'u'= ncelllid mod 16, ncellid=11.

For format 1 r(n)=Tu(n),

Format 2; r * (3*n + m) =Tu(n)*w' (m)

For Nsc >1 multitone transmission,

Tu(n)=ejαneπ/4Ø(n)

For n is 0 to Nsc-1, i.e. 0 to 11.

If Nsc = 12, α=0.

Here Ø(n) depends on the 'u' parameter. For formats 1 and 2, the equation is the same.

$$c(n)=(x_1(n+N_c) +x_2(n+N_c)) \text{ mod}2$$

$$x_1(n+31) =(x_1(n+3) +x_1(n)) \text{ mod}2$$

$$x_2(n+31) =(x_2(n+3) +x_2(n+2) +x_2(n+1) +x_2(n)) \text{ mod}2$$

The sequence number for c(n) is 20480. Nc=1600, x1(0) =1, x1(1 to 30) =0.

The Sequence for x2 is Cinit=35, x2(0) =1, x2(2) =1, x2(5) =1, remaining up to x2(30) is 0.

Chapter 3

Implementation details

(Methodology and Working of Model)

This part shows the methodology used for implementing the project and its specifications. The algorithm is also depicted in this part which is done according to the blocks and equation mentioned in Chapter 2.

3.1 Turbo Encoder:

Turbo Encoder is composed of two recursive systematic convolutional (RSC) encoders and a Channel Interleaver. The two recursive systematic convolutional (RSC) encoders are parallelly concatenated with the input of the first RSC encoder is passed through Turbo code internal Interleaver logic and the output of Turbo code internal Interleaver is given as input to the second RSC encoder.

The RSC encoder structure is composed of a 4-bit serial in-serial out shift register. RSC encoder is fed with one-bit input for every posedge of the clock from the input data stored in a register and the data in flipflops is shifted to the right and will get 2 output bits, one is a systematic output bit and another one is parity output bit for every one-bit input. This is shown in Figure 2.

For example, let input data be c=1011, x be the systematic output, z be the parity output

m [0:3] is a shift register

systematic output, x=c is the same as input data.

Parity output, z =m [0] ^m [1] ^m [3]

m [0] =m [3] ^m [2] ^c

initially m=0000

clk=1, m=1000, x=1, z=1

clk=1, m=0100, x=0, z=1

clk=1, m=1010, x=1, z=1

clk=1, m=0101, x=1, z=0

therefore, after completion, the systematic and parity outputs are x=1011 and z=1110 respectively.

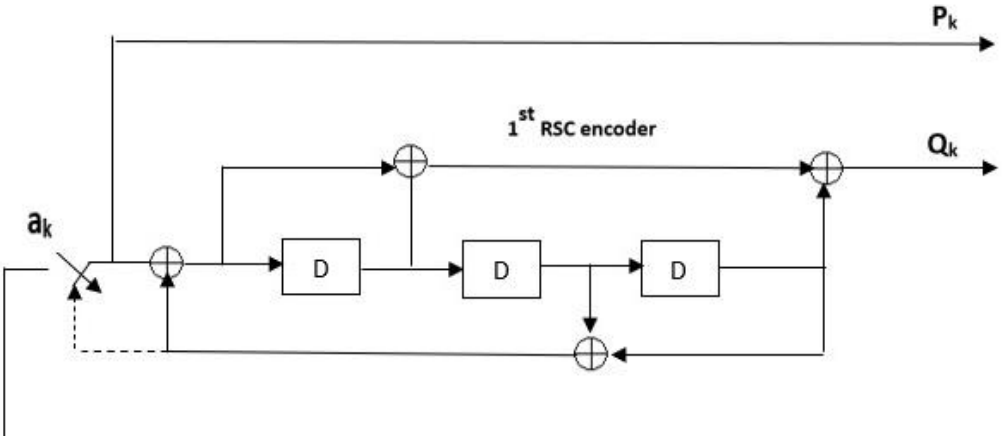


Fig. 2. RSC Encoder 1

Trellis's termination of the RSC encoder is done to bring the state of the shift register to 000.

For example, for trellis termination, after the last bit is fed to the RSC encoder the state of the shift register is shifted to the right once, and the state is used for tail bits calculation.

m=0010

m [1:3] =010

for trellis termination, the following operation is done at every posedge of clk until the state of the shift register is 0000.

m [3] =m [2]

m [2] =m [1]

m [1] = 0

systematic tail bits = m [3] ^ m [2]

parity tail bits= m [1] ^m [3]

clk=1, m [1:3] = 010, systematic tail bits=1, parity tail bits=0

clk=1, m [1:3] = 001, systematic tail bits =1, parity tail bits=1

clk=1, m [1:3] = 000, systematic tail bits=0, parity tail bits =0

After completion, the values of systematic and parity tail bits are 110 and 010 respectively. This is shown in Figure 3.

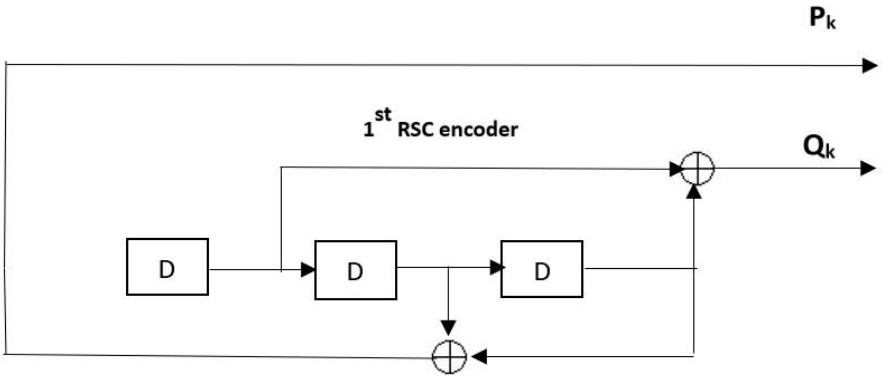


Fig. 3. Trellis Termination

K is the input data length.

relation between i and out_index is given by

out_index=((f1*i) + (f2*i*i)) %K;

f1 and f2 are the parameters used to permute the indices which are the standard ones depending on the value of K and based on the K value we can take f1 and f2 values from table 5.1.3-3 of 36.212 v15 3GPP paper.

For example, if K=40 then f1=3 and f2=10

If k=2560 the f1=39 and f2=80.

The output of this Turbo code internal Interleaver is given as input to the RSC encoder second and this encoder operation is the same as that of RSC encoder first. But from this encoder, we will only consider parity bit output z, and systematic output is ignored as it is permuted sequence of the systematic output of the RSC encoder first. Both systematic and parity tail bits are considered for trellis termination. This is shown in Figure 4.

Overall if we input a sequence of length K to a turbo encoder, we will get three

output sequences systematic output and parity output of RSC encoder first, Parity output of RSC encoder second with tail bits appended to these outputs in the shown in the figure. These three output bits are of Length K+4.

We have taken the length of input sequence K=2560 which will be from the output of the CRC block.

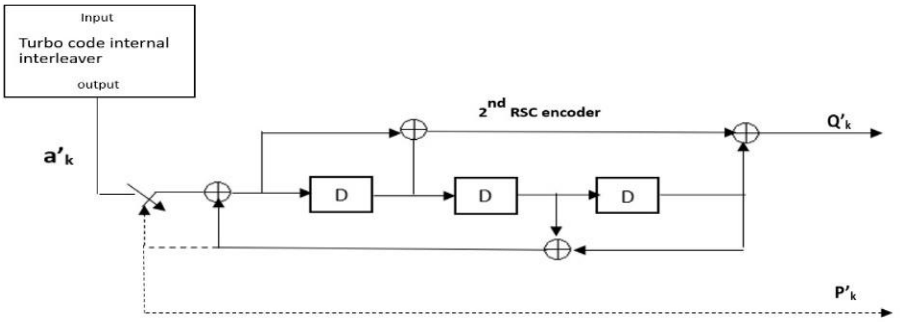


Fig.4. RSC Encoder 2

3.2 Channel Interleaver:

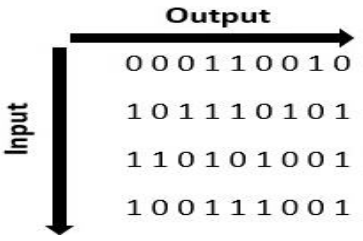
The type of Interleaver used is Block Interleaver, the function of that Interleaver is that it takes the inputs in a column fashion and reads out the output in a row fashion. The number of rows and columns is decided according to the equations mentioned in the system design part.

For example;

Input a = 0 1 1 1 0 0 1 0 0 1 0 0 1 1 1 1 1 1 0 1 0 0 1 1 0 1 0 0 1 0 0 0 0 1 1 1

In matrix format this input is taken as;

Output is: 0 0 0 1 1 0 0 1 0 1 0 1 1 1 0 1 0 1 1 1 0 1 0 1 0 0 1 1 0 0 1 1 1 0 0 1



3.3 Repetition Block:

This input belongs to format 1 as seen in the figure. As per the figure the other input comes from format 2 through the repetition block. The repetition block gives the 1 for ACK,0 for NACK for 16 times and the working is similar to the Block Interleaver as mentioned above.

3.4 Demodulation Reference signal:

In the NBIOT framework, the Demodulation reference signal (DMRS) is the signal that is generated by following the set of steps discussed further and is used to facilitate efficient and accurate transmission of data in the NBIOT network. Either format 1 or format 2 of DMRS is always linked to NPUSCH slots.

- DMRS for multi-tone transmission:

Multitone transmission implies that a number of subcarriers are more than one i.e., Nsc>1 standard ones are {3,.6,12}.

The reference signal sequence Tu(n) is given by

Tu(n) $= e^{j\alpha n}.e^{j\varphi(n)\left(\frac{\pi}{4}\right)}$,0<=n<Nsc → eq (1)

where n=0,1,2, …., Nsc-1

Where α is the cyclic shift, this value for Nsc=3,6 is derived from the higher layer parameters cyclic shift three-tone and cyclic shift six-tone respectively as defined in table 10.1.4.1.2-3 of 3GPP 36.212 rel15.

For Nsc=12, cyclic shift $\alpha = 0$.

For Nsc=3, $\varphi(n)$ is given by the table 10.1.4.1.2-1.

For Nsc=6, $\varphi(n)$ is given by the table 10.1.4.1.2-2.

For Nsc=12, $\varphi(n)$ is given by the table 5.5.1.2-1.

DMRS Example, for Nsc =12

Since $\alpha = 0$, eq (1) becomes ru(n)= $e^{j\varphi(n)\left(\frac{\pi}{4}\right)}$, this can be written in terms of sin and cos.

ru(n)= cos ($\varphi(n)\pi/4$) + j sin ($\varphi(n)\pi/4$)

To get $\varphi(n)$ values from the table we need to get U value which is given by

U=N_{cell}^{ID} % 16

NcellID=11

U=11.

For U =11, $\varphi(n)$ is given by

$\{\varphi(0), \varphi(1), \varphi(2), \ldots\ldots \varphi(11)\}$ {3,1, -1, -1,3,3, -3,1,3,1,3,3}

Since the 1, -1,3, and -3 are the only values and are repeated, we will get four combinations of sin and cos of each which is shown in Table 1.

Table 1. Sine and Cosine Values for Nsc=12

Equation	Real value	Binary value
cos ($\pi/4$)	0.707	00111111001101001111110111110100
cos ($-\pi/4$)	0.707	00111111001101001111110111110100
cos ($3\pi/4$)	-0.707	10111111001101001111110111110100
cos ($-3\pi/4$)	-0.707	10111111001101001111110111110100
sin ($\pi/4$)	0.707	00111111001101001111110111110100
sin (-$\pi/4$)	-0.707	10111111001101001111110111110100
sin ($3\pi/4$)	0.707	00111111001101001111110111110100
sin ($-3\pi/4$)	-0.707	10111111001101001111110111110100

$$r_u(0) = \cos(\varphi(0)\pi/4) + j \sin(\varphi(0)\pi/4)$$
$$r_u(0) = \cos(3\pi/4) + j \sin(3\pi/4)$$
$$r_u(0) = \cos(3\pi/4) + j \sin(3\pi/4)$$

Similarly, find the values of ru(1) to ru(11) we get;

ru(1)=00111111001101001111110111110100+j00111111001101001111110111110100

ru(2)=10111111001101001111110111110100+j00111111001101001111110111110100

ru(3)=00111111001101001111110111110100+j10111111001101001111110111110100

ru(4)=10111111001101001111110111110100+j00111111001101001111110111110100

ru(5)=10111111001101001111110111110100+j00111111001101001111110111110100

ru(6)=10111111001101001111110111110100+j10111111001101001111110111110100

ru(7)=00111111001101001111110111110100+j00111111001101001111110111110100

ru(8)=10111111001101001111110111110100+j00111111001101001111110111110100

ru(9)=00111111001101001111110111110100+j00111111001101001111110111110100

ru(10)=10111111001101001111110111110100+j00111111001101001111110111110100

ru(11)=10111111001101001111110111110100+j00111111001101001111110111110100

In the above example, the complex numbers ru (0) to ru (11) are the DMRS sequence for Nsc=12 for multitone transmissions.

- DMRS for single-tone transmission Nsc=1:

The mathematical equation for generation for DMRS for Nsc=1 is given by

ru(n)= 1/√2 (1 + j) * (1 − 2c(n)) * w (n mod 16)

Where n=0,1,2,.....,Nseq-1

For Nsc=1 , Nseq=nslots=16

The values of c(n) are either 0 or 1 and are generated with a pseudo-random gold

the sequence is given by;

c(n)= (x1(n+Nc) + x2(n+Nc)) % 2

x1(n+31) = (x1(n+3) + x1(n)) %2

x2(n+31) = (x2(n+3) +x2(n+2) +x2(n+1) +x2(n)) %2

Nc=1600.

n=0,1, 2, 3, ……., Mpn-1

Where Mpn is the length of the final sequence c(n) given by

Mpn=Mrep * N_{slots}^{UL} * NRU

Where Number of resource units, NRU=10.

Number of uplink slots, $N_{slots}^{UL} = 16$

Number of Repetitions, Mrep=128.

Mpn=20480.

The first 31 bits of x1 and x2 are initialized with x1_init and x2_init respectively.

Where x1_init=10000000000000000000000000000000

X2_init=11000100000000000000000000000000

First, x1 and x2 sequences are generated, and then by using these two sequences we will get the c(n) sequence of length Mpn=20480.

w(n) is a Hadamard sequence of length 16 found in Table 10.1.4.1.1.-1. The w(n) values are chosen as a function of the values of the u parameter where,

U=N_{cell}^{ID} % 16

N_{cell}^{ID} = 3*cell_id +cell_id_sector

Where cell_id=168 and cell_id_sector = 3

N_{cell}^{ID} = 504

U=504%16

U=11.

For U=11, {w(0),w(1),……,w(15)}={1,-1,-1,1,1,-1,-1,1,-1,1,1,-1,-1,1,1,-1}

By substituting c(n) and w(n) values for ru(n) equation for n=0,1, 2, ….., Mpn-1.

We will get the base DMRS sequence for Nsc=1.

Chapter 4

Results and discussion

In Chapter 4 results and discussion are done based on the input and output obtained from each transmitter block written according to behavioral modeling described in the algorithm part.

4.1 Results

1. The result of input and output obtained from the Turbo encoder block for the input of 2560 bits is shown in Figure 5, and the RTL view is shown in Figure 6.

Fig. 5. Turbo Encoder Output in Binary format.

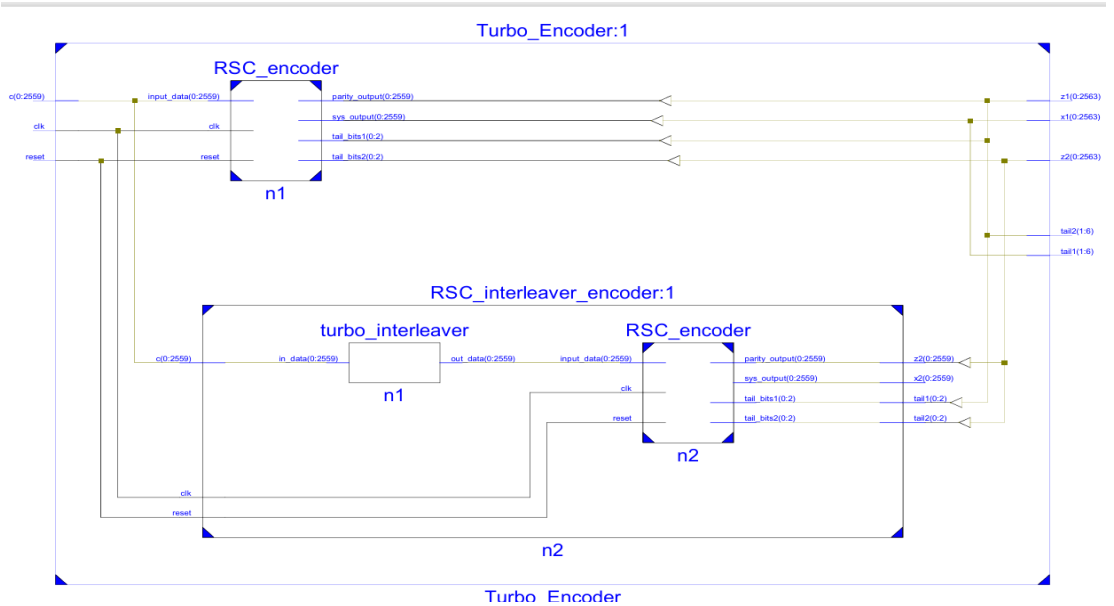


Fig. 6. RTL view of Turbo Encoder

2. The result of input and output obtained from the Channel Interleaver block for the input of 2592 bits is shown in Figure 7 and Figure 8.

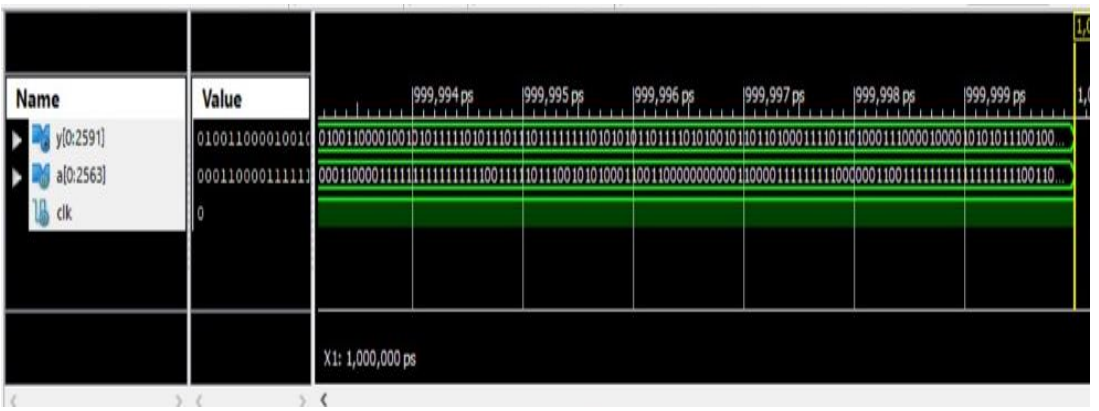


Fig.7. Channel Interleaver Output

Fig.8. Channel Interleaver Output Display (2592 bits)

3. The result of input and output obtained from the repetition block for input of 16 bits is shown in Figure 9.

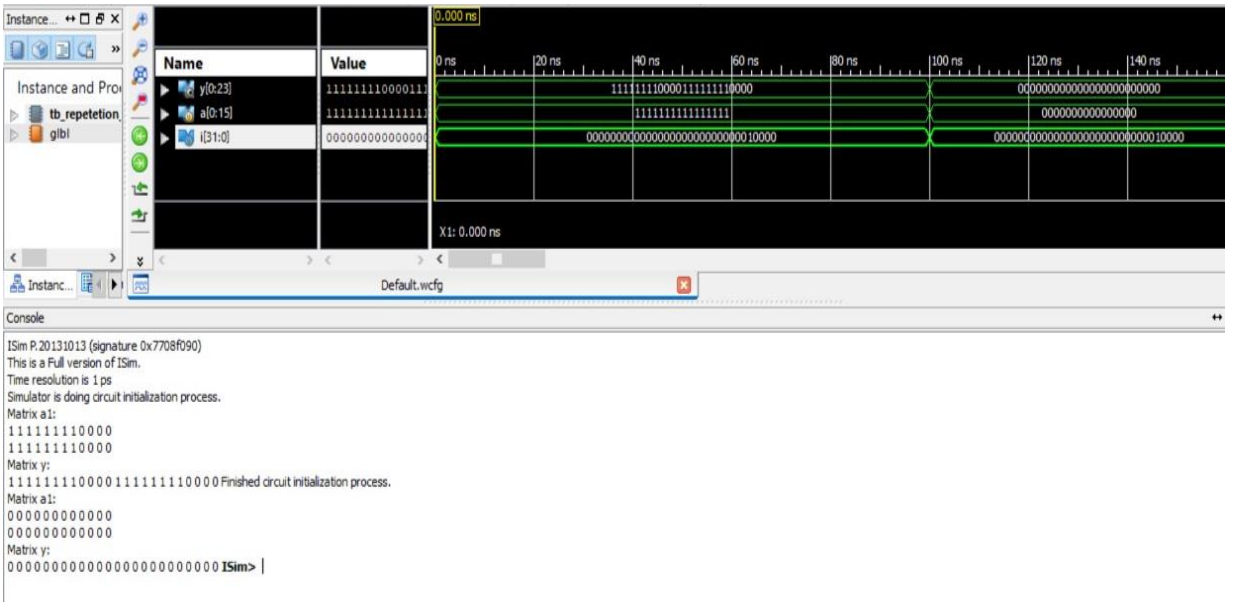


Fig.9. Repetition Block Output

4. The result of input and output obtained from the DMRS sequence generator block for multitone transmission with the input of 12 indexes of 32 bits is shown in Figure 10 and Figure 11.

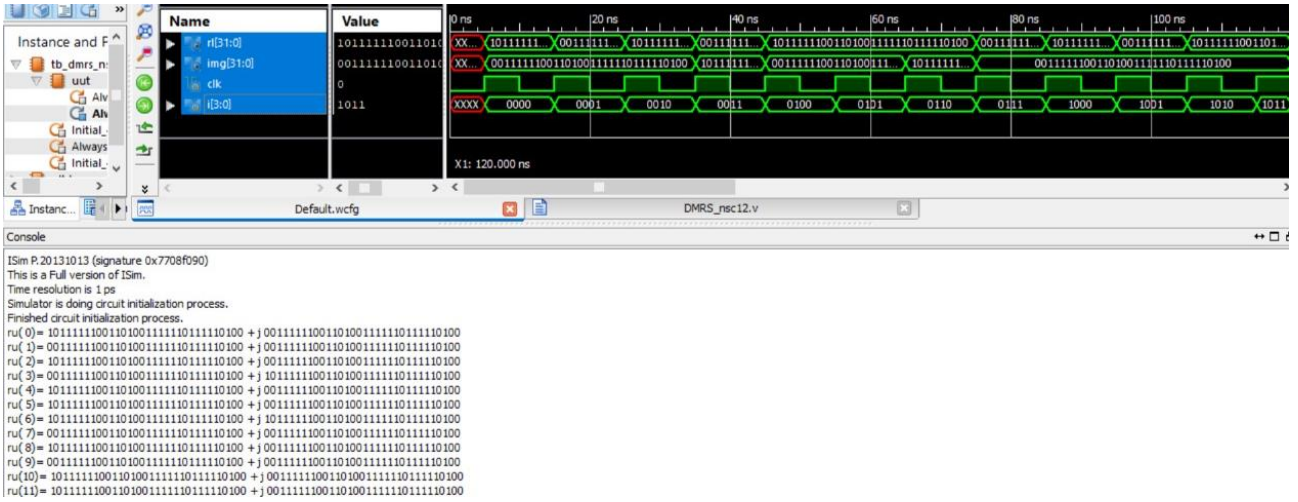


Fig.10. DMRS output for Nsc>1

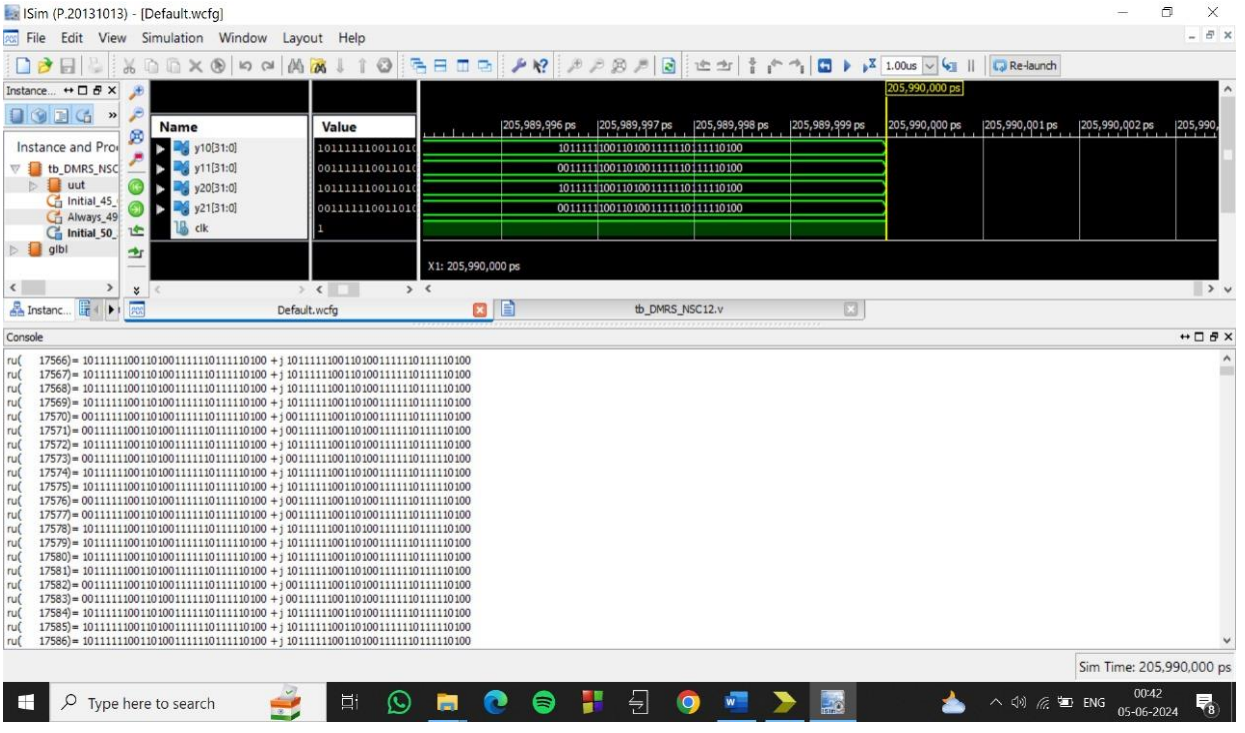


Fig.11. DMRS output for Nsc = 1

Chapter 5

Conclusions and Future Scope

This chapter includes the Conclusion and Future scope of the project.

5.1 Conclusion

In this work, our project focused on the simulation and hardware implementation of a turbo encoder using a 1/3 coding rate, a crucial error correction coding scheme, usually in wireless communication. We also focused on the Channel Interleaver block, which plays an important role, particularly in deep fading channels where errors frequently happen in bursts and consecutive bits. In repetition code, is a data repeat or retransmission mechanism that NB-IoT uses to send error-free data packets to regions with bad reception. Finally, we design a DMRS signal that is used at the receiver, allowing the receiver to perform channel estimation and helpful for data reception and decoding. Utilizing the Xilinx ISE 14.7 EDA tool and board for implementation, our results demonstrate the successful verification of simulation and implementation outcomes.

5.2 Future scope

Future work on the NB-IoT uplink transmission chain project will focus on completing the remaining blocks such as Sub-carrier mapping, IFFT, DFT and SC-FDMA, as well as optimizing performance through algorithm refinement and hardware acceleration. Emphasis on advanced error correction, adaptive coding and modulation, and security enhancements like encryption and authentication is critical. Real-world testing, including field trials and end-to-end system integration, will validate practical performance.

Bibliography

1.Software-Defined NB-IoT Uplink Framework—The Design, Implementation and Use Cases by Alicja Olejniczak ORCID, Olga Błaszkiewicz, Krzysztof K. Cwalina *ORCID, Piotr Rackowski ORCID and Jarosław Sadowski ORCID.

2. 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Evolved Universal Terrestrial Radio Access (E-UTRA); Multiplexing and channel coding (Release 10).

3. Design and FPGA-Based Hardware Implementation of NB-IoT Physical Uplink Shared Channel Transmitter and Physical Downlink Shared Channel Receiver.

4. Evolved Universal Terrestrial Radio Access (E-UTRA); Physical layer procedures (3GPP TS 36.213 version 15.2.0 Release 15).

5. 3GPP TS 36.213 version 14.2.0 Release 14: Evolved Universal Terrestrial Radio Access (E-UTRA); Physical layer procedures.

6. 3GPP TS 36.212 version 13.4.0 Release 13: Evolved Universal Terrestrial Radio Access (E-UTRA); Multiplexing and channel coding.

7. 3GPP TS 36.212 version 15.2.1 Release 15: Evolved Universal Terrestrial Radio Access (E-UTRA); Multiplexing and channel coding.

8.Matthieu Kanj," Vincent Savaux, Mathieu Le Guen. A Tutorial on NB-IoT Physical Layer Design Communications Surveys and Tutorials"2020.

Minor-2

ORIGINALITY REPORT

8%	7%	7%	%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	hal.archives-ouvertes.fr Internet Source	2%
2	www.mdpi.com Internet Source	1%
3	www.etsi.org Internet Source	1%
4	patents.justia.com Internet Source	1%
5	Sakshi Popli, Rakesh Kumar Jha, Sanjeev Jain. "Adaptive Small Cell position algorithm (ASPA) for green farming using NB-IoT", Journal of Network and Computer Applications, 2021 Publication	<1%
6	iss.rs Internet Source	<1%
7	www.sist.si Internet Source	<1%
8	Matthieu Kanj, Vincent Savaux, Mathieu Le Guen. "A Tutorial on NB-IoT Physical Layer	<1%

Design", IEEE Communications Surveys & Tutorials, 2020
Publication

9	David Segura, Emil J. Khatib, Jorge Munilla, Raquel Barco. "NB-IoT latency evaluation with real measurements", 2022 IEEE Workshop on Complexity in Engineering (COMPENG), 2022 Publication	<1 %
10	pdffox.com Internet Source	<1 %
11	www.jocm.us Internet Source	<1 %
12	zaguan.unizar.es Internet Source	<1 %
13	Abdallah Abostait, Rania M. Tawfik, M. Saeed Darweesh, Hassan Mostafa. "Design and FPGA-Based Hardware Implementation of NB-IoT Physical Uplink Shared Channel Transmitter and Physical Downlink Shared Channel Receiver", Electronics, 2023 Publication	<1 %
14	Alicja Olejniczak, Olga Błaszkiewicz, Krzysztof K. Cwalina, Piotr Rajchowski, Jarosław Sadowski. "Software-Defined NB-IoT Uplink Framework—The Design, Implementation and Use Cases", Sensors, 2021 Publication	<1 %

15 Myung. "SC-FDMA in 3GPP Long Term Evolution", Single Carrier FDMA A New Air Interface for Long Term Evolution, 10/31/2008 <1%

Publication

Exclude quotes	On	Exclude matches	< 5 words
Exclude bibliography	On		