User Manual

for S32K3 RM Driver

Document Number: UM34RMASRR21-11 Rev0000R3.0.0 Rev. 1.0

Chapter 1

Revision History

Revision	Date	Author	Description
1.0	31.03.2023	NXP RTD Team	S32K3 Real-Time Drivers AUTOSAR 4.4 & R21-11 Version 3.0.0

Chapter 2

Introduction

This User Manual describes Resource Manager for S32K3. Resource Manager driver configuration parameters and deviations from the specification are described in Driver chapter of this document.

2.1 Supported Derivatives

The software described in this document is intended to be used with the following microcontroller devices of NXP Semiconductors:

- s32k310_mqfp100
- s32k310_lqfp48
- s32k311_mqfp100 / MWCT2015S_mqfp100
- s32k311_lqfp48
- s32k312_mqfp100 / MWCT2016S_mqfp100
- s32k312_mqfp172 / MWCT2016S_mqfp172
- s32k314_mqfp172
- s32k314_mapbga257
- s32k322_mqfp100 / MWCT2D16S_mqfp100
- s32k322_mqfp172 / MWCT2D16S_mqfp172
- s32k324_mqfp172 / MWCT2D17S_mqfp172

- s32k324_mapbga257
- s32k341_mqfp100
- s32k341_mqfp172
- s32k342_mqfp100
- s32k342_mqfp172
- s32k344_mqfp172
- s32k344_mapbga257
- s32k394_mapbga289
- s32k396_mapbga289
- s32k358_mqfp172
- s32k358_mapbga289
- s32k328_mqfp172
- s32k328_mapbga289
- s32k338_mqfp172
- s32k338_mapbga289
- s32k348_mqfp172
- s32k348_mapbga289
- s32m274_lqfp64
- s32m276_lqfp64

All of the above microcontroller devices are collectively named as S32K3.

Note: MWCT part numbers contain NXP confidential IP for Qi Wireless Power.

2.2 Overview

AUTOSAR (AUTomotive Open System ARchitecture) is an industry partnership working to establish standards for software interfaces and software modules for automobile electronic control systems.

AUTOSAR:

- paves the way for innovative electronic systems that further improve performance, safety and environmental friendliness.
- is a strong global partnership that creates one common standard: "Cooperate on standards, compete on implementation".
- is a key enabling technology to manage the growing electrics/electronics complexity. It aims to be prepared for the upcoming technologies and to improve cost-efficiency without making any compromise with respect to quality.
- facilitates the exchange and update of software and hardware over the service life of the vehicle.

2.3 About This Manual

This Technical Reference employs the following typographical conventions:

- **Boldface** style: Used for important terms, notes and warnings.
- *Italic* style: Used for code snippets in the text. Note that C language modifiers such "const" or "volatile" are sometimes omitted to improve readability of the presented code.

Notes and warnings are shown as below:

Note

This is a note.

Warning

This is a warning

2.4 Acronyms and Definitions

Term	Definition
API	Application Programming Interface
ASM	Assembler
AXBS	Crossbar Switch
BSMI	Basic Software Make file Interface
C/CPP	C and C++ Source Code
DEM	Diagnostic Event Manager
DET	Development Error Tracer
DMAMUX	Direct Memory Access Multiplexer
ECU	Electronic Control Unit
LSB	Least Signifigant Bit
MCU	Micro Controller Unit
MIDE	Multi Integrated Development Environment
MRC	Memory Region Controller
MSB	Most Significant Bit
MSCM	Miscellaneous System Control Module
N/A	Not Applicable
PFLASH	Flash Memory Controller
RAM	Random Access Memory
RM	Resource Manager
SEMA42	Semaphores 2
SIU	Systems Integration Unit
SWS	Software Specification
XBIC	Crossbar Integrity Checker
XML	Extensible Markup Language
XRDC	Extended Resource Domain Controller
VIRT_WRAPPER	Virtualization Wrapper

2.5 Reference List

#	Title	Version
1	S32K3xx Reference Manual	S32K3xx Reference Manual, Rev.6, Draft B, 01/2023
2	S32K39 and S32K37 Reference Manual	S32K39 and S32K37 Reference Manual, Rev. 2 Draft A, 11/2022
3	S32M27x Reference Manual	S32M27x Reference Manual, Rev.2, Draft A, — 02/2023
4	S32K3xx DataSheet	S32K3xx Data Sheet, Rev. 6, 11/2022
5	S32K396 DataSheet	S32K396 Data Sheet, Rev. 1.1 — 08/2022
6	S32M2xx DataSheet	S32M2xx Data Sheet, Rev. 2 RC — 12/2022
7	S32K358 Errata	S32K358_0P14E Mask Set Errata – Rev. 28, 9/2022
8	S32K396 Errata	S32K396_0P40E Mask Set Errata, Rev. DEC2022, 12/2022
9	S32K311 Errata	S32K311_0P98C Mask Set Errata, Rev. 6/March/2023, 3/2023

#	Title	Version
10	S32K312 Errata	S32K312 Mask Set Errata for Mask 0P09C, Rev. 25/April/2022
11	S32K342 Errata	S32K342 Mask Set Errata for Mask 0P97C, Rev. 10,11/2022
12	S32K3x4 Errata	Mask Set Errata for Mask 0P55A/1P55A, Rev. 14/Oct/2022

Chapter 3

Driver

3.1 Requirements

Resource Manager is a Complex Device Driver (CDD), so there are no AUTOSAR requirements regarding this module.

It has vendor-specific requirements and implementation.

3.2 Driver Design Summary

The RM module provides a way to initialize and control the resource domains allocation and memory protection on the chip with the supported peripherals.

3.3 Hardware Resources

#	Hardware IP	S32K310	S32K311	S32K3x2	S32K3x4	S32K3x8	S32K39x	S32M27x	Description
1	AXBS	No	No	Yes	Yes	Yes	Yes	No	Crossbar Switch
2	Pflash	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Flash Memory Controller
3	Sema42	No	No	Yes	Yes	Yes	Yes	No	Semaphores 2
4	Virt_Wrapper	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Virtualization Wrapper
5	XBIC	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Crossbar Integrity Checker
6	XRDC	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Extended Resource Domain Controller
7	MSCM	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Miscellaneous System Control Module
8	DMA MUX	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Direct Memory Access Multiplexer

3.4 Deviations from Requirements

Since this is a CDD Module, there are no AUTOSAR requirements for the functionality.

3.5 Driver Limitations

None.

3.6 Driver usage and configuration tips

3.6.1 HLD usage

Prior usage of the RM CDD in an application, the configuration files must be generated with the configurator.

3.6.1.1 API controls

Initialization of all hardware resources is done using Rm_Init. Considering that the function is configuring domains and access to resources it is recommended that it is called before other bus masters are active, or that they are not accesing those resources.

The rest of the API controls directly the allocated hardware resources. Check the references below for more information:

- Rm_XrdcSetProcessID
- Rm_XrdcGetDomainID
- Rm_XrdcGetDomainIDErrorStatus
- Rm_XrdcInstanceInit
- Rm_SemaphoreGetStatus
- Rm_SemaphoreLockGate
- Rm_SemaphoreUnlockGate
- Rm_SemaphoreResetGate
- Rm_SemaphoreResetAllGates
- Rm_SemaphoreGetResetGateDomainId
- Rm_SemaphoreIsResetGateStateIdle
- Rm_SemaphoreGetResetedGate
- Rm_XbicEnableMasterFeedbackCheck
- Rm_XbicEnableSlaveEDCCheck
- Rm_XbicFeedbackCheckAndEDCCheckDisable
- Rm_XbicGetErrorStatus
- Rm_XbicErrorInjection
- Rm_XbicErrorInjectionDisable
- Rm_AxbsDeInit

  Here is list of Xbic instance which will be used for Xbic's APIs above:

#	Instance name	Instance number
1	Xbic Axbs Main	0
2	Xbic Axbs Peripheral	1
3	Xbic Axbs eDMA	2
4	Xbic Axbs Tcm	3
5	Xbic Axbs Tcm PRAM	4
6	Xbic Axbs ACE Hse_B	5
7	Xbic Axbs ACE	6

Information about XBIC master/slave port please check Reference Manual document.

3.6.2 LLD usage

RM CDD does not support LLD.

3.6.3 Interface configuration

User can choose enable / disable checkbox to use the corresponding modules.

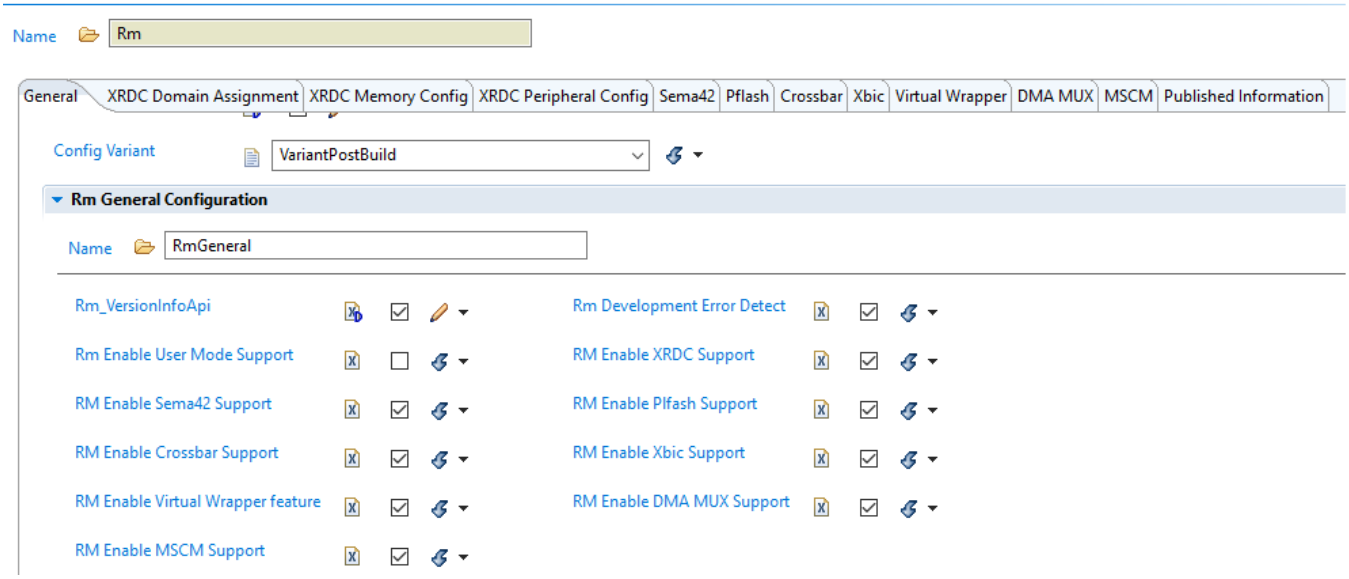

Figure 3.1 RM general config

3.6.4 Multicore initialization

None.

3.6.5 XRDC configuration

3.6.5.1 XRDC registers lock

When **Xrdc Registers Lock** is enabled, MRGD and PDAC registers can be locked by enabling **Xrdc MRGD Lock Bit** and **Xrdc PDAC Lock Bit** of each element in **XRDC Memory Config** and **XRDC Peripheral Config**.

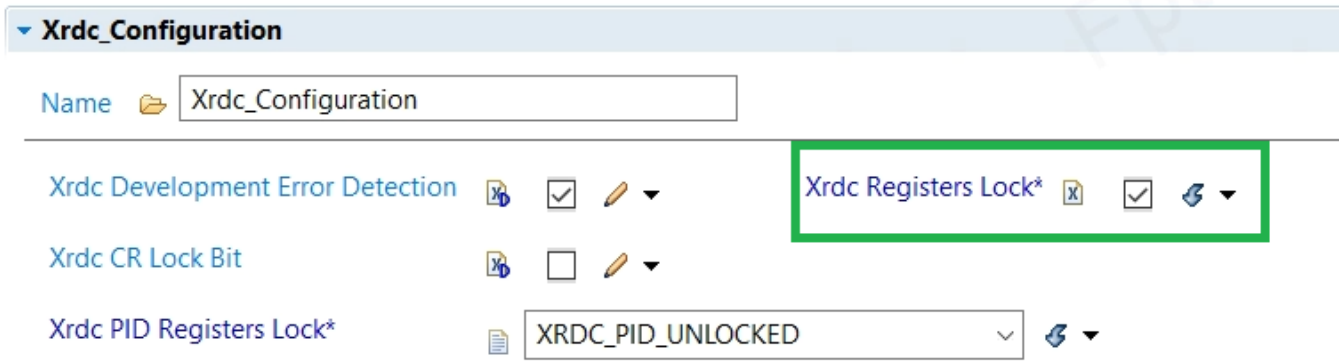

Figure 3.2 Xrdc Registers lock

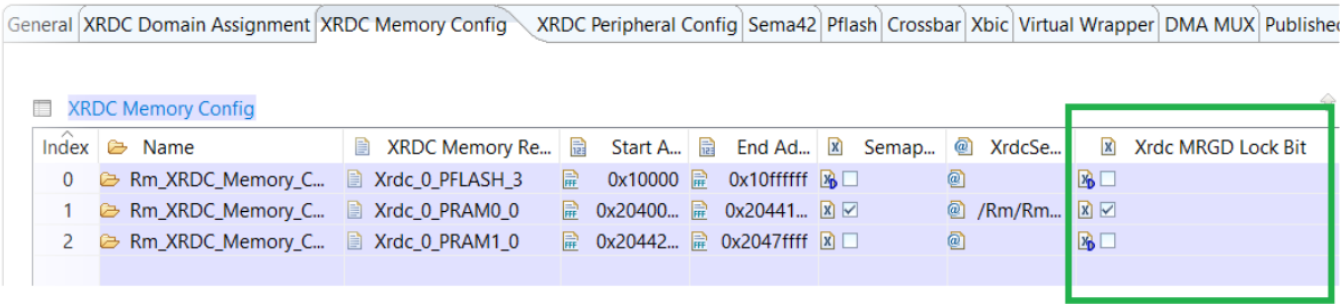

Figure 3.3 Xrdc MRGD Lock Bit

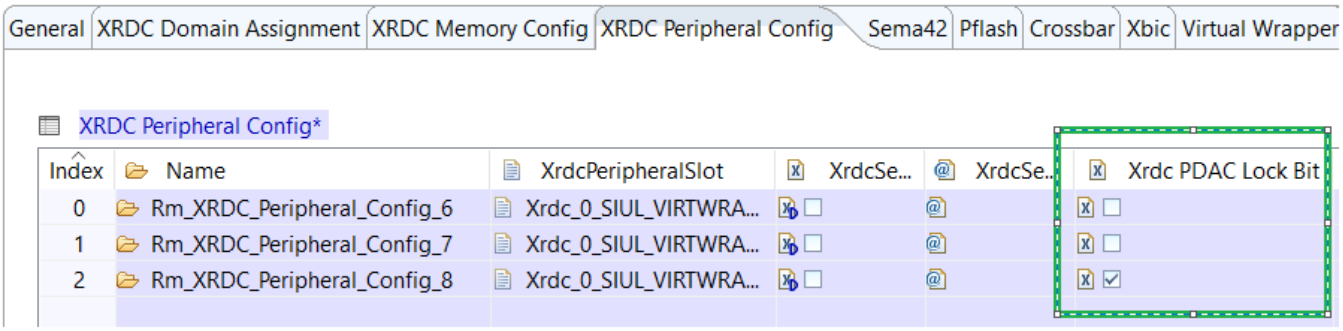

Figure 3.4 Xrdc PDAC Lock Bit

If **Xrdc CR lock bit** is enabled, Control register(CR) will be locked. That mean Xrdc can not be enabled/disabled again after Rm init.
For **Xrdc PID Registers Lock**, Tresos configuration provides users with 3 available options which are listed in figure and table below

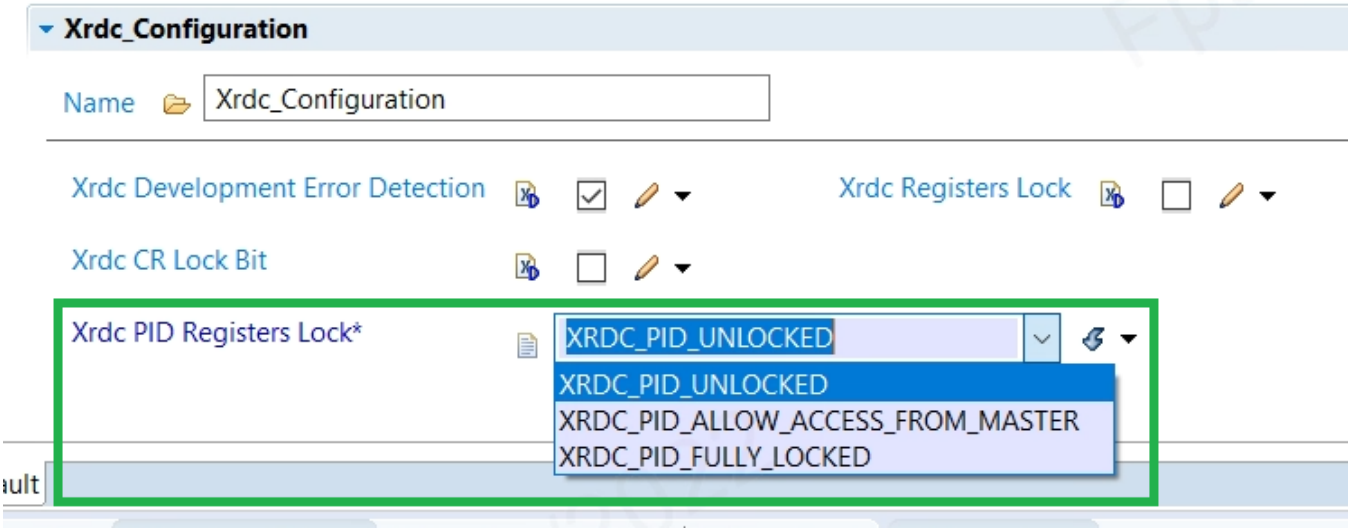

Figure 3.5 XRDC PID Registers lock options

Option	XRDC_PIDm registers status
XRDC_PID_UNLOCKED	Register can be written to by any secure privileged write
XRDC_PID_ALLOW_ACCESS_FROM_MASTER	Register can only be written by a secure privileged write from bus master m
XRDC_PID_FULLY_LOCKED	Register locked (read-only) until the next reset

The selected PID lock option will be applied for PID register of configured core masters in "Domain master assigment"
Note:

3.6.5.2 XRDC Domain Assignment

Users can create a new domain assignment by click on Add button in configuration field.

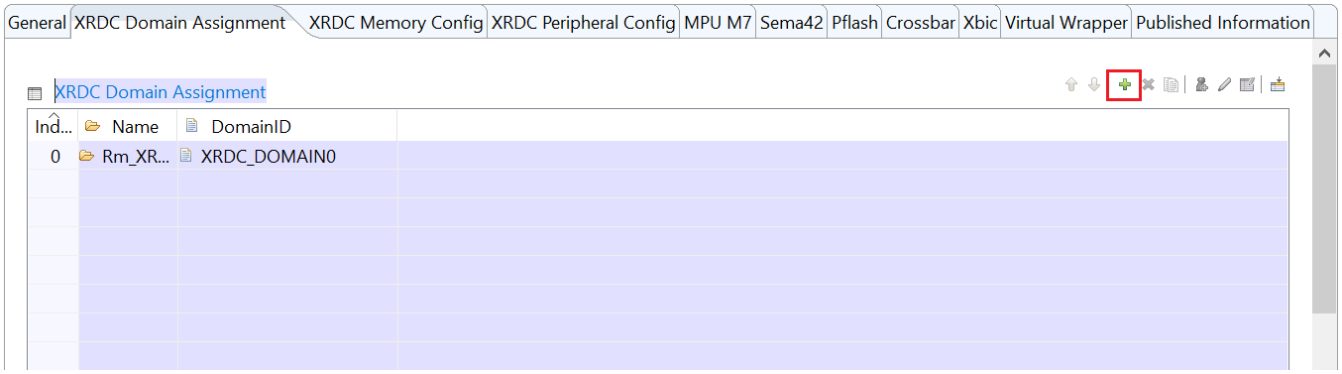

Figure 3.6 Xrdc Domain Assignment Configuration

3.6.5.2.1 XRDC Master Domain Assignment

Users can add new elements to choose which masters will be assigned to the corresponding domain ID and configure their assignment attributes.

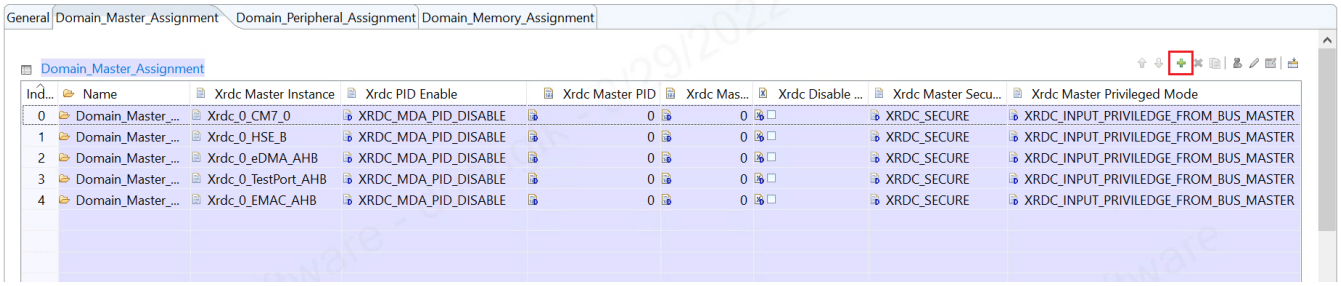

Figure 3.7 XRDC Domain Master Assignment Configuration

For ProcessID evaluation, Tresos configuration provides users with 3 available options which are listed in figure and table below

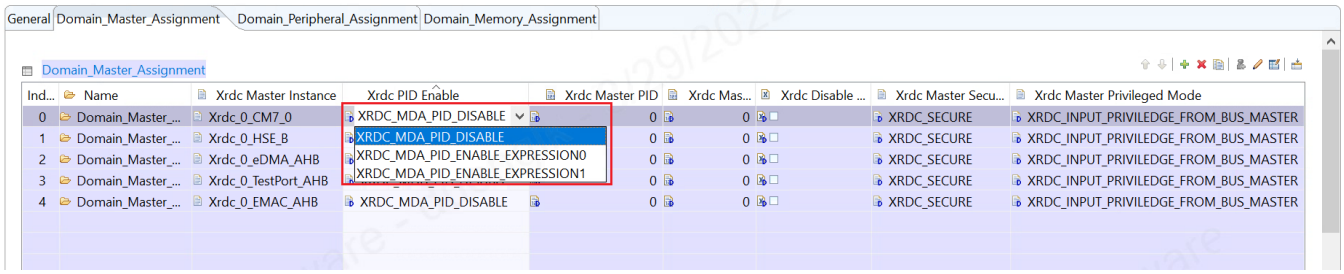

Figure 3.8 ProcessID options

Option	PID evaluation
XRDC_MDA_PID_DISABLE	No process identifier is included in the domain hit evaluation
XRDC_MDA_PID_ENABLE_EXPRESSION0	Domain assignment hit when ((PID & ~PIDM) == (PIDn[PID] &~PIDM))
XRDC_MDA_PID_ENABLE_EXPRESSION1	Domain assignment hit when ~((PID & ~PIDM) == (PIDn[PID] &~PIDM))

3.6.5.2.2 XRDC Peripheral Domain Assignment

Users can add new elements to configure domain access policy for a specific peripheral slot.

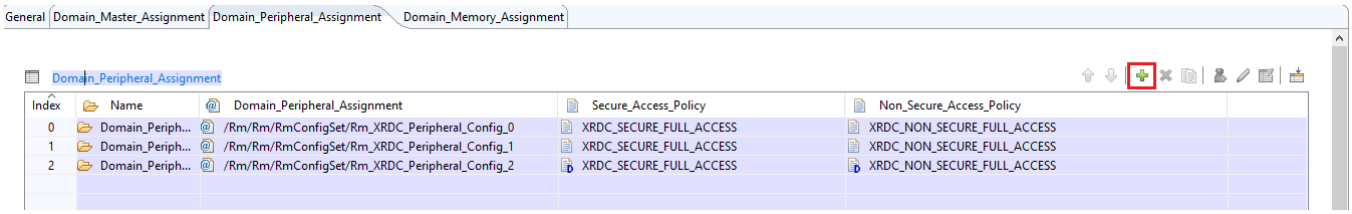

Figure 3.9 XRDC Domain Peripheral Assignment

Selections of **DomainPeripheralAssignment** field refer to XRDC Peripheral Configuration

Combination of **SecurityAccessPolicy** and **NonSecurityAccessPolicy** field defines final access policy for the peripheral slot (found in ***Access policy look up table*** shown below)

3.6.5.2.3 XRDC Memory Domain Assignment

Users can add new elements to configure domain access policy for a specific memory region.

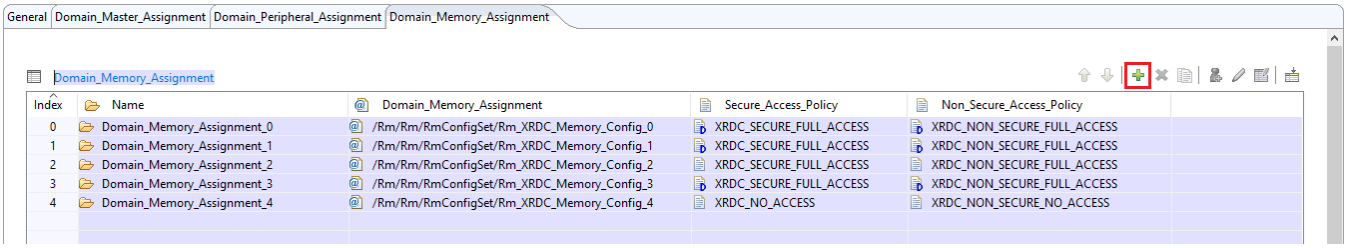

Figure 3.10 XRDC Domain Memory Assignment

Selections of **DomainMemoryAssignment** field refer to XRDC Memory Configuration

Combination of **SecurityAccessPolicy** and **NonSecurityAccessPolicy** field defines final access policy for the memory region (found in ***Access policy look up table*** shown below)

Configuration Fields		Allowable accesses			
Secure_Access_Policy	**Non_Secure_Access_Policy**	**Secure Privileged**	**Secure User**	**NonSecure Privileged**	**NonSecure User**
XRDC_FULL_ACCESS	XRDC_FULL_ACCESS	R,W	R,W	R,W	R,W
XRDC_FULL_ACCESS	XRDC_SUPERVISOR_ACCESS_ONLY	R,W	R,W	R,W	None
XRDC_FULL_ACCESS	XRDC_READ_ONLY	R,W	R,W	R	R
XRDC_FULL_ACCESS	XRDC_SUPERVISOR_READ_ONLY	R,W	R,W	R	None
XRDC_FULL_ACCESS	XRDC_NO_ACCESS	R,W	R,W	None	None
XRDC_SUPERVISOR_ACCESS_ONLY	NA	R,W	None	None	None
XRDC_READ_ONLY	NA	R	R	None	None
XRDC_NO_ACCESS	NA	None	None	None	None

Figure 3.11 Access policy look up table

3.6.5.3 XRDC Peripheral Configuration

Users can add new elements to configure attributes of peripheral slots

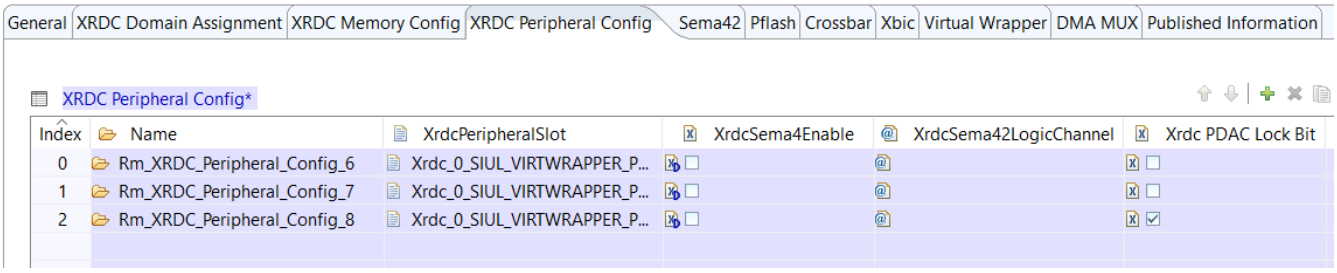

Figure 3.12 XRDC Domain Peripheral Configuration

Note:
-**XrdcSema42LogicChannel** will be aborted unless **XrdcSema4Enable** is checked.
-**XrdcSema42LogicChannel** can be mapped to logical channels mentioned in Sema42 logic channel configuration

3.6.5.4 XRDC Memory Configuration

Users can add new elements to configure attributes of memory regions.

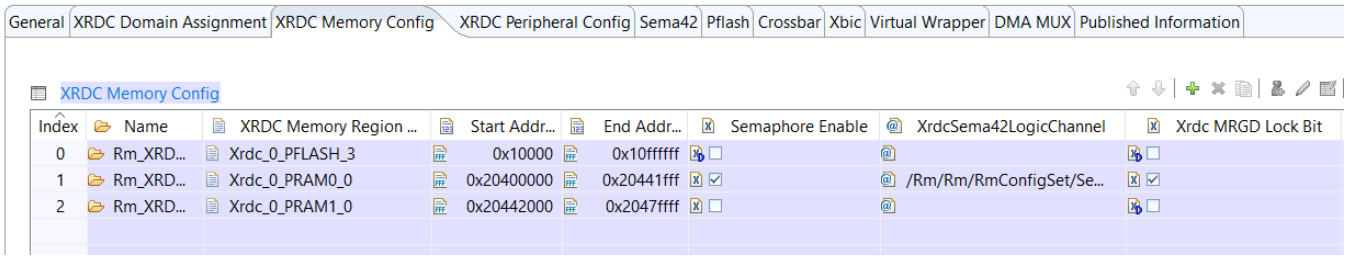

Figure 3.13 XRDC Domain Memory Configuration

Note:
-**XrdcSema42LogicChannel** will be aborted unless **XrdcSema4Enable** is checked.
-**XrdcSema42LogicChannel** can be mapped to logical channels mentioned in Sema42 logic channel configuration
-Each memory region need to be protected by an appropriate MRC instance, details are mentioned in the Reference manual

3.6.6 Sema42 logic channel configuration

Users can use logic channel instead of hardware instance and hardware channel. The logic channel is stand for both hardware instance and hardware channel which is configured in configration application.

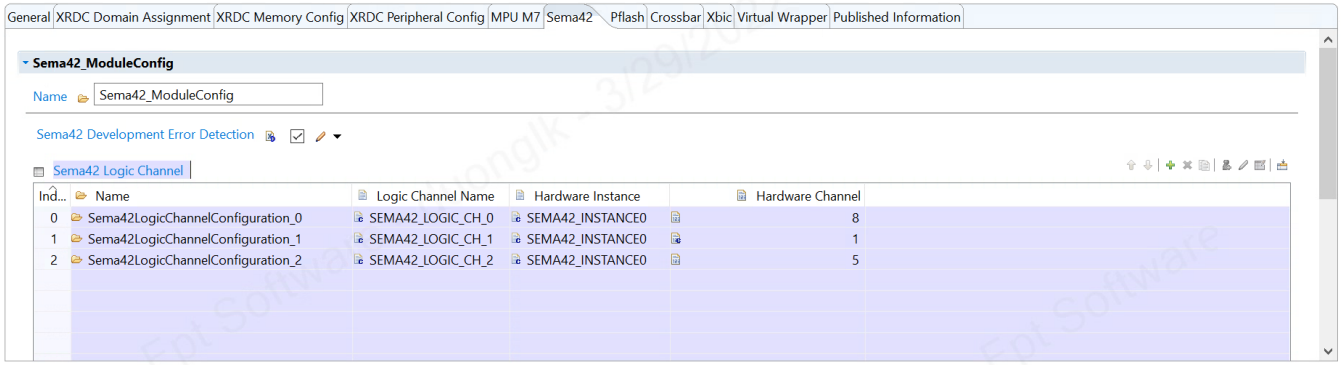

Figure 3.14 Sema42 LogicChannel Configuration

Example: In the picture, there are 3 logic channel:

- Logic channel 1 is equal to Sema42 instance 0 gate 8.
- Logic channel 2 is equal to Sema42 instance 0 gate 1.
- Logic channel 3 is equal to Sema42 instance 0 gate 5.

Note: In Rm_Semaphore API, we should use the name which is defined in column **Logic Channel Name** in configuration application with the prefix "RM_" (Because it is a macro so all characters are uppercase). We can find out them in file "CDD_Rm_Ipw_Cfg.h" with identify "RM_<Logic Channel Name>". As in picture, if users want to invoke Sema42 instance 0 gate 5, the argument they must pass into Rm_Semaphore API is RM_SEMA42_L↩ OGIC_CH_2.

3.6.7 AXBS configuration

Users can configure AXBS by instance. **RmCrossbarInstance** table contains the instance that will be configured. Double click in Axbs instance want to configure, then the user can configure for each Axbs slave port and Axbs master port.

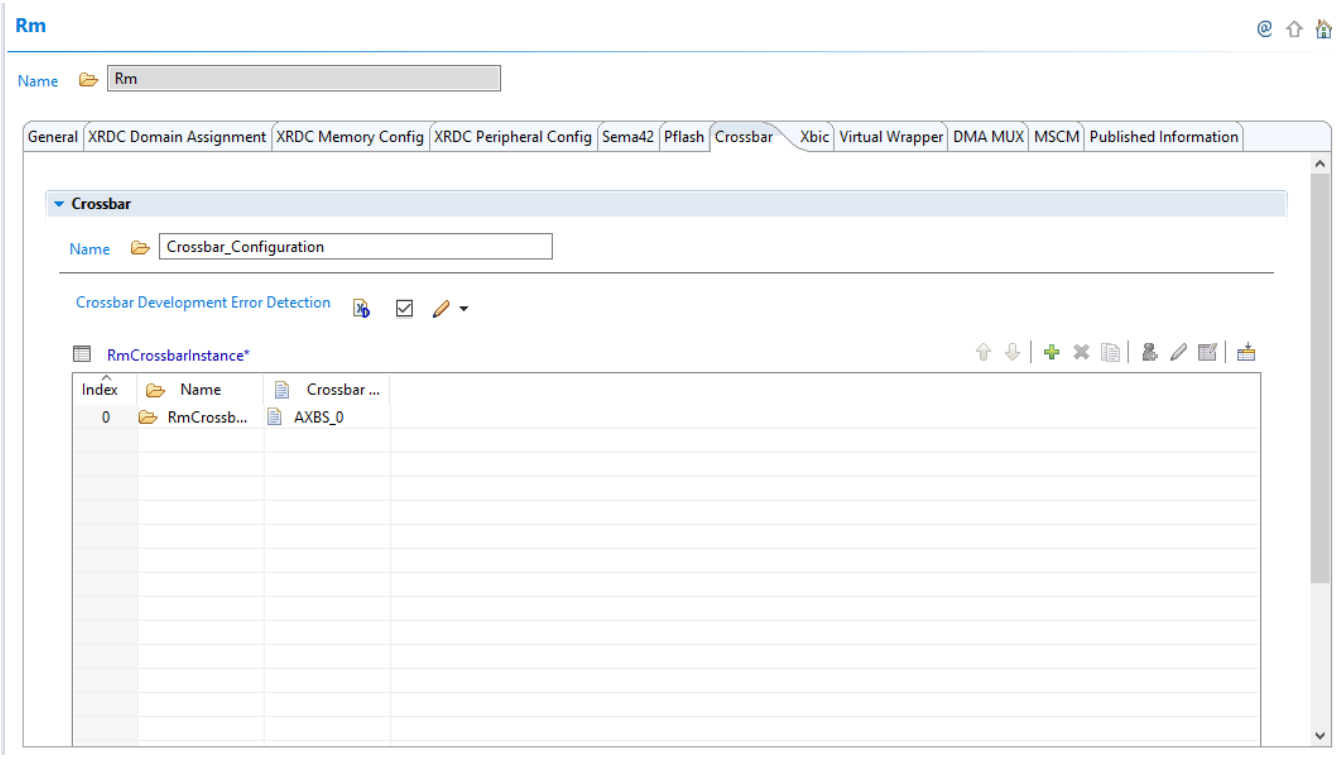

Figure 3.15 AXBS Instance Configuration

3.6.7.1 Axbs slave port configuration

RmCrossbarHwSlavePort tab will support the user to configure the master's access priority, lock configuration register, parking control, ... per slave port.

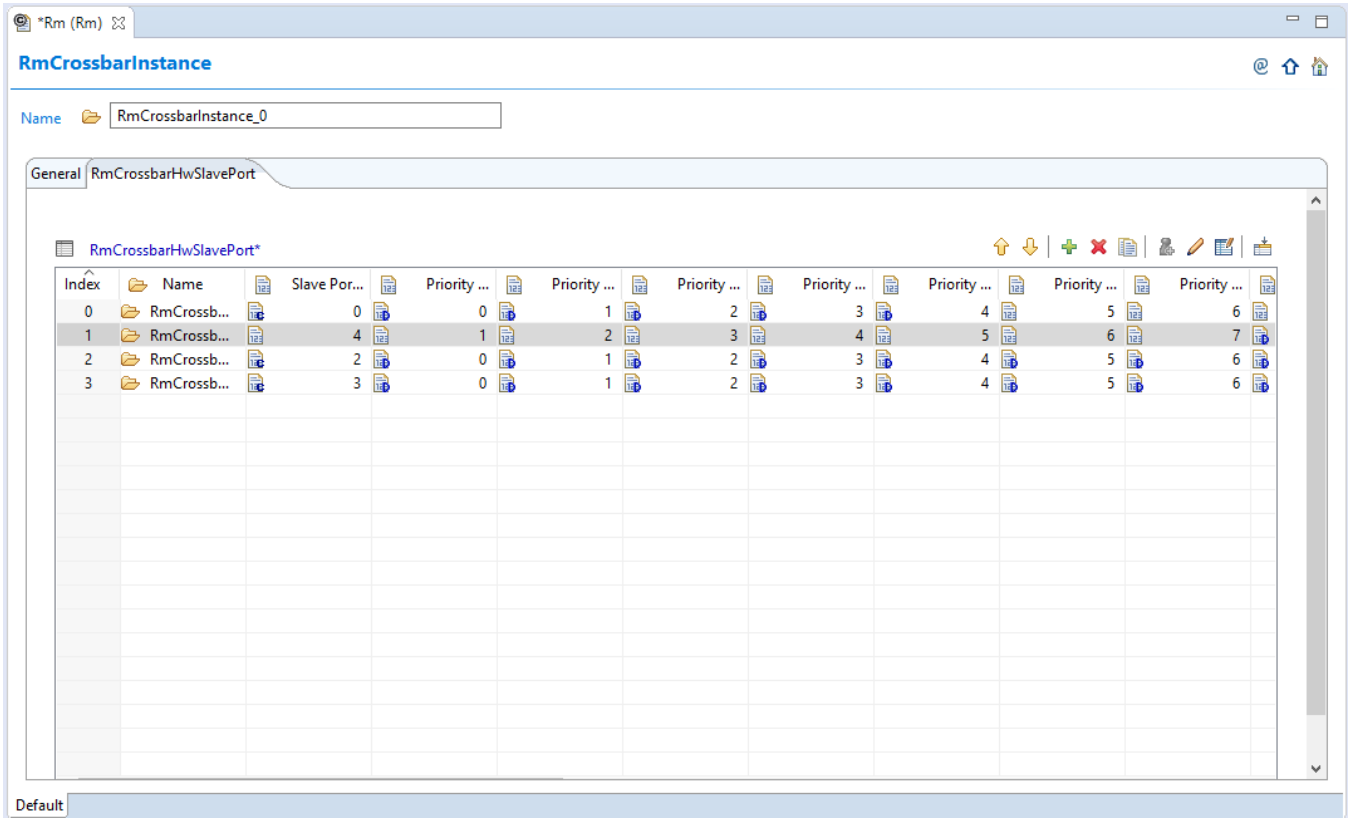

Figure 3.16 AXBS Slave Port Configuration

3.6.8 XBIC configuration

Xbic configuration support users configure Xbic by instance. **XbicCheckingControl** table contains the instance that will be configured.

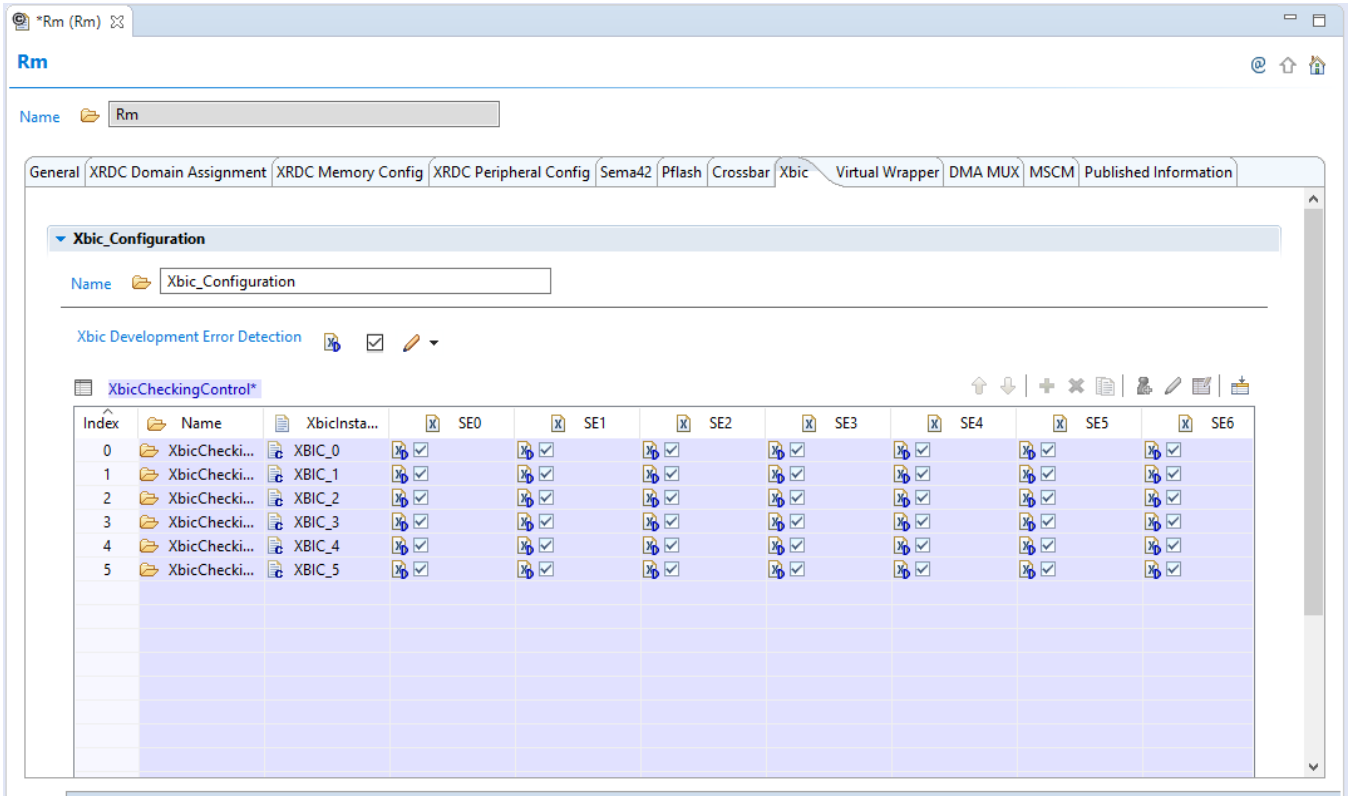

Figure 3.17 XBIC Instance Configuration

This application can enable slave port EDC error detection and master port feedback integrity check by a tick in corresponding node SEn, MEn.

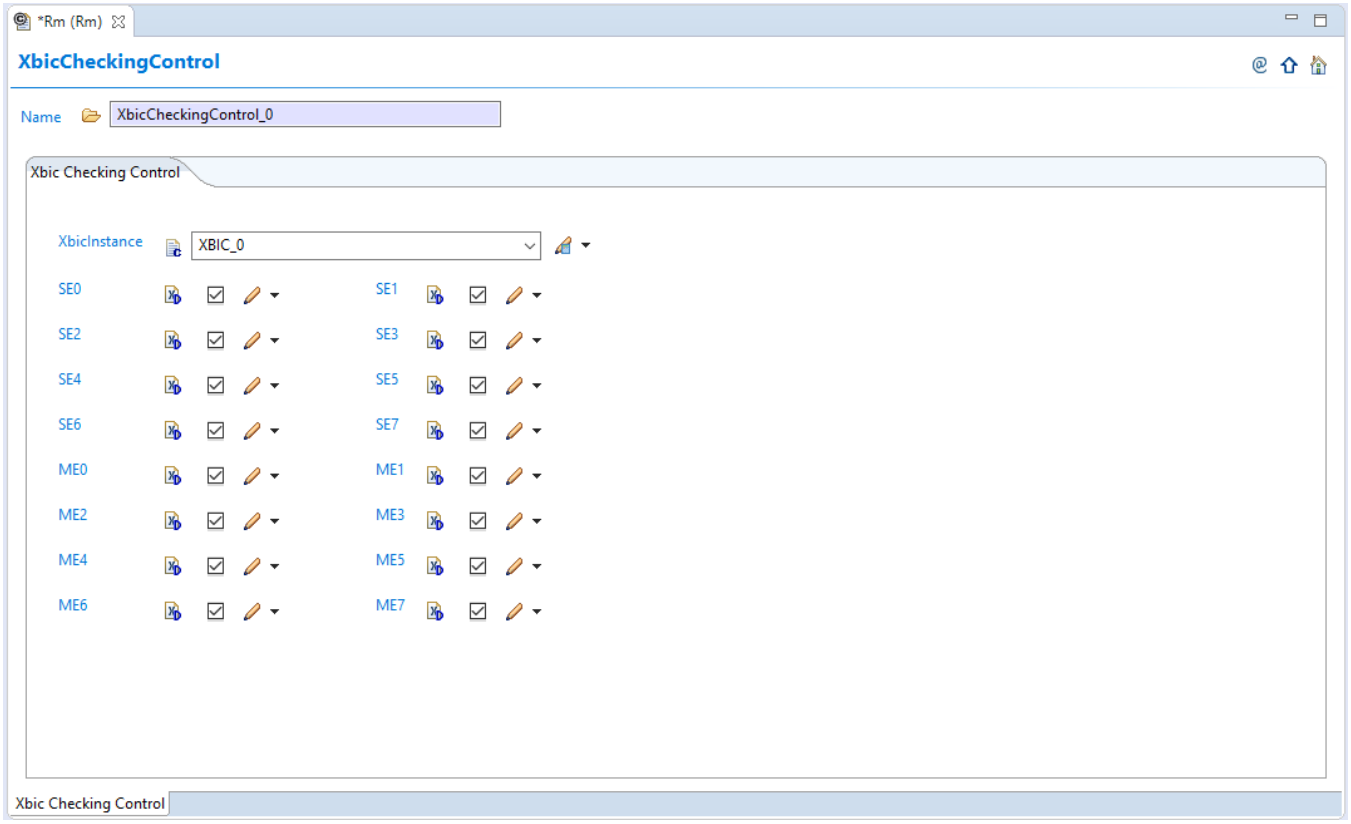

Figure 3.18 XBIC Port Configuration

Note: Only available slave ports and master ports can be configured.

3.6.9 MSCM configuration

Mscm configuration support users configure Mscm by instance. **MSCM Configuration** table contains the instance that will be configured.

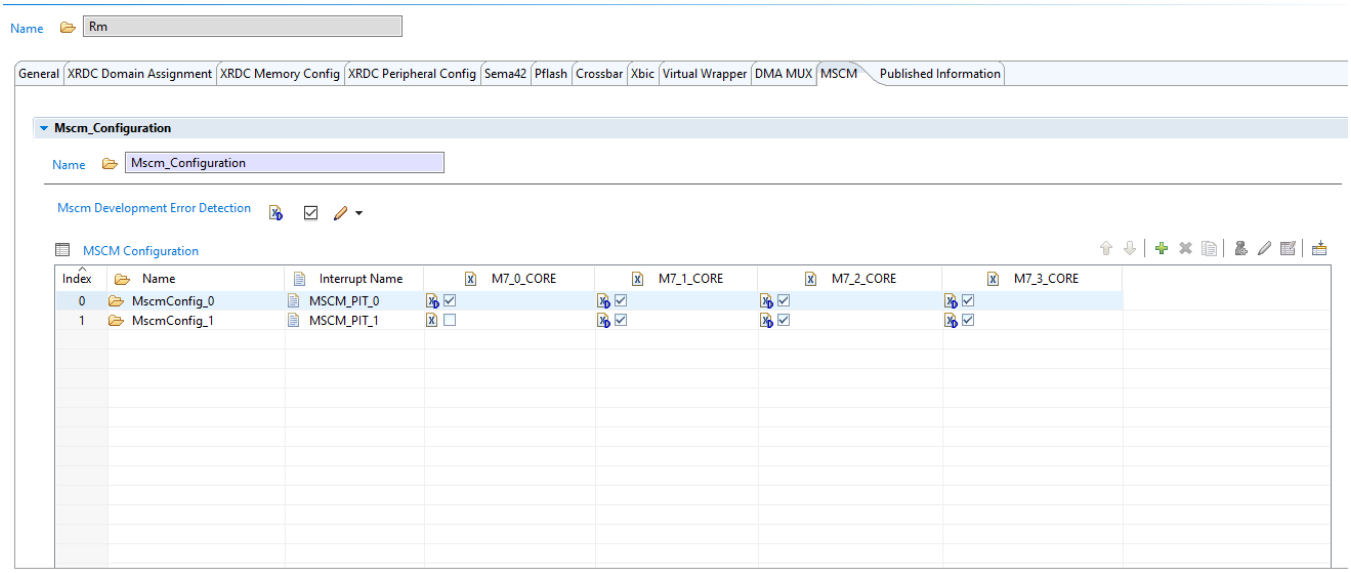

Figure 3.19 MSCM Instance Configuration

This application can enable and disable individual interrupts for each core in a multi-core system.

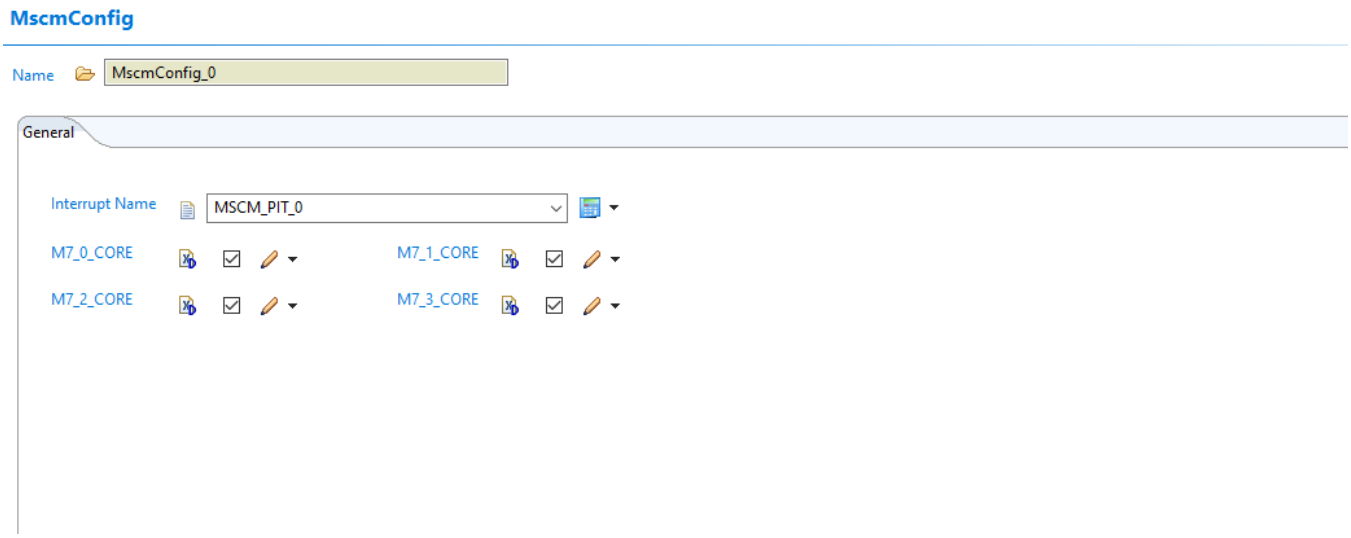

Figure 3.20 MSCM Configuration

3.7 Runtime errors

The driver generates the following DET errors at runtime.

Function	Error Code	Condition triggering the error
Rm_Init()	RM_E_UNINIT_U8	API service called without module initialization.
Rm_Init()	RM_E_ALREADY_INITIALIZED_U8	Module is already initialized
Rm_Init()	RM_E_INIT_FAILED_U8	In precompile mode, specifies that a non-null parameter was used for init. In other cases, a null pointer was used for initialization
Rm_GetVersionInfo()	RM_E_PARAM_POINTER	Input pointer parameter is invalid
Rm_SemaphoreGetStatus(), Rm_SemaphoreLockGate(), Rm_SemaphoreUnlockGate(), Rm_SemaphoreResetGate()	RM_E_INVALID_SEMA4_CHANNEL_U8	Semaphore channel is invalid
Rm_SemaphoreLockGate()	RM_E_ALREADY_LOCKED_U8	Semaphore is already locked
Rm_SemaphoreLockGate(), Rm_SemaphoreUnlockGate()	RM_E_LOCKED_BY_OTHER_CORE_U8	Semaphore is locked by another core
Rm_SemaphoreLockGate()	RM_E_ALREADY_UNLOCKED_U8	Semaphore is already unlocked

3.8 Symbolic Names Disclaimer

All containers having symbolicNameValue set to TRUE in the AUTOSAR schema will generate defines like:

#define <Mip>Conf_<Container_ShortName>_<Container_ID>

For this reason it is forbidden to duplicate the names of such containers across the RTD configurations or to use names that may trigger other compile issues (e.g. match existing `#ifdefs` arguments).

Chapter 4

Tresos Configuration Plug-in

This chapter describes the Tresos configuration plug-in for the driver. All the parameters are described below.

- Module Rm
  - Container RmGeneral
    - Parameter Rm_VersionInfoApi
    - Parameter RmDevErrorDetect
    - Parameter RmEnableUserModeSupport
    - Parameter RmEnableXRDCSupport
    - Parameter RmEnableSema42Support
    - Parameter RmPflashConfigurable
    - Parameter RmCrossbarConfigurable
    - Parameter RmXbicConfigurable
    - Parameter RmVirtWrapperConfigurable
    - Parameter RmEnableDmaMuxSupport
    - Parameter RmEnableMscmSupport
  - Container RmConfigSet
    - Container Xrdc_Configuration
      - Parameter XrdcDevErrorDetect
      - Parameter XrdcRegistersLock
      - Parameter XrdcCRLockBit
      - Parameter XrdcPIDRegisterLock
    - Container Rm_XRDC_Domain_Assignment
      - Parameter DomainID
      - Container Domain_Master_Assignment
      - Parameter XrdcMasterInstance
      - Parameter XrdcPIDEnable
      - Parameter XrdcMasterPID
      - Parameter XrdcMasterPIDMask
      - Parameter XrdcDIDBDisable
      - Parameter XrdcMDADFMTLockBit
      - Parameter XrdcMasterMode
      - Parameter XrdcMasterPriviledgeMode

- Container Domain_Peripheral_Assignment
- Parameter Secure_Access_Policy
- Parameter Non_Secure_Access_Policy
- Reference Domain_Peripheral_Assignment
- Container Domain_Memory_Assignment
- Parameter Secure_Access_Policy
- Parameter Non_Secure_Access_Policy
- Reference Domain_Memory_Assignment

* Container Rm_XRDC_Memory_Config
  - Parameter XrdcMrcInstance
  - Parameter XrdcStartAddress
  - Parameter XrdcEndAddress
  - Parameter XrdcSema4Enable
  - Parameter XrdcMRGDLockBit
  - Reference XrdcSema42LogicChannel
* Container Rm_XRDC_Peripheral_Config
  - Parameter XrdcPeripheralSlot
  - Parameter XrdcSema4Enable
  - Parameter XrdcPDACLockBit
  - Reference XrdcSema42LogicChannel
* Container Sema42_ModuleConfig
  - Parameter Sema42DevErrorDetect
  - Container Sema42LogicChannelConfiguration
  - Parameter Sema42LogicChannel_LogicName
  - Parameter Sema42HardwareInstance
  - Parameter Sema42HardwareChannel
* Container Pflash_Configuration
  - Parameter PflashDevErrorDetect
  - Container PflashMasterProtection
  - Parameter PflashMaster
  - Parameter PflashMasterAccess
* Container Crossbar_Configuration
  - Parameter CrossbarDevErrorDetect
  - Container RmCrossbarInstance
  - Parameter RmCrossbarHwInstance
  - Container RmCrossbarHwSlavePort
  - Parameter RmSlavePortNumber
  - Parameter RmCrossbarPrioMaster0
  - Parameter RmCrossbarPrioMaster1

- Parameter RmCrossbarPrioMaster2
- Parameter RmCrossbarPrioMaster3
- Parameter RmCrossbarPrioMaster4
- Parameter RmCrossbarPrioMaster5
- Parameter RmCrossbarPrioMaster6
- Parameter RmCrossbarPrioMaster7
- Parameter RmCrossbarEnableLock
- Parameter RmCrossbarHaltLowPrio
- Parameter RmCrossbarEnablePrioElevM0
- Parameter RmCrossbarEnablePrioElevM1
- Parameter RmCrossbarEnablePrioElevM2
- Parameter RmCrossbarEnablePrioElevM3
- Parameter RmCrossbarEnablePrioElevM4
- Parameter RmCrossbarEnablePrioElevM5
- Parameter RmCrossbarEnablePrioElevM6
- Parameter RmCrossbarEnablePrioElevM7
- Parameter RmCrossbarEnableFixedPrio
- Parameter RmCrossbarParkingControl
- Parameter RmCrossbarParkField

* Container Xbic_Configuration
  - Parameter XbicDevErrorDetect
  - Container XbicCheckingControl
  - Parameter XbicInstance
  - Parameter SE0
  - Parameter SE1
  - Parameter SE2
  - Parameter SE3
  - Parameter SE4
  - Parameter SE5
  - Parameter SE6
  - Parameter SE7
  - Parameter ME0
  - Parameter ME1
  - Parameter ME2
  - Parameter ME3
  - Parameter ME4
  - Parameter ME5
  - Parameter ME6
  - Parameter ME7
* Container Virt_Wrapper_Configuration
  - Parameter VirtWrapperDevErrorDetect
  - Container Mscr_Config_List
  - Parameter MscrName
  - Parameter MscrNumber
  - Parameter MscrSiul2Instance
  - Parameter MscrPinMux
  - Parameter MscrMirror

- Container Imcr_Config_List
- Parameter ImcrName
- Parameter ImcrNumber
- Parameter ImcrSiul2Instance
- Parameter ImcrInput
- Parameter ImcrPad
- Parameter ImcrMirror
- Container Other_Config_List
- Parameter OtherName
- Parameter OtherNumber
- Parameter OthersSiul2Instance
- Parameter OtherInput
- Parameter OtherMirror

* Container Dma_Mux_Configuration
  - Parameter Dma_Mux_DevErrorDetect
  - Container Dma_Mux_Module_Config
  - Parameter Dma_Mux_HwInstance
  - Parameter Dma_Mux_HwChannel
  - Parameter Dma_Mux_Enable_Trigger
  - Parameter Dma_Mux_Source0
  - Parameter Dma_Mux_Source1
  - Parameter Dma_Mux_Source2
  - Parameter Dma_Mux_Source3
* Container Mscm_Configuration
  - Parameter MscmDevErrorDetect
  - Container MscmConfig
  - Parameter IsrName
  - Parameter IsrTargetCore0
  - Parameter IsrTargetCore1
  - Parameter IsrTargetCore2
  - Parameter IsrTargetCore3

– Container CommonPublishedInformation

* Parameter ArReleaseMajorVersion
* Parameter ArReleaseMinorVersion
* Parameter ArReleaseRevisionVersion
* Parameter ModuleId
* Parameter SwMajorVersion
* Parameter SwMinorVersion
* Parameter SwPatchVersion
* Parameter VendorApiInfix
* Parameter VendorId

4.1 Module Rm

Vendor specific: Configuration of the Rm (Resource Manager) module.

Included containers:

- RmGeneral
- RmConfigSet
- CommonPublishedInformation

Property	Value
type	ECUC-MODULE-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantSupport	true
supportedConfigVariants	VARIANT-POST-BUILD, VARIANT-PRE-COMPILE

4.2 Container RmGeneral

Vendor specific: Configuration of general Rm parameters.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.3 Parameter Rm_VersionInfoApi

Vendor specific: Enables/Disables the get version info API function

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

4.4 Parameter RmDevErrorDetect

Vendor specific:

Switches the Development Error Detection and Notification on or off.

true: Enabled.

false: Disabled.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.5 Parameter RmEnableUserModeSupport

When this parameter is enabled, the RM module will adapt to run from User Mode, with the following measures:
b) using 'call trusted function' stubs for all internal function calls that access registers requiring supervisor mode.
for more information, please see chapter 5.7 User Mode Support in IM
Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.6 Parameter RmEnableXRDCSupport

When this parameter is enabled, the Xrdc APIs are enabled to the user

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.7 Parameter RmEnableSema42Support

When this parameter is enabled, the Sema42 APIs are enabled to the user

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.8 Parameter RmPflashConfigurable

RmPflashConfigurable

Check this in order to be able to use the Master protection.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.9 Parameter RmCrossbarConfigurable

RmCrossbarConfigurable

Check this in order to be able to use the crossbar configuration feature.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.10 Parameter RmXbicConfigurable

RmXbicConfigurable

Check this in order to be able to use XBIC api sets to verify the integrity of crossbar transfers.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.11 Parameter RmVirtWrapperConfigurable

RmVirtWrapperConfigurable

Check this in order to be able Virtual wrapper feature. This feature need to enable along side with port virtual wrapper feature to ensure collaboration set of pads protection. When virtual wrapper is enable RM driver will automatically ajust configuration for hw protection.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.12 Parameter RmEnableDmaMuxSupport

When this parameter is enabled, the Dma Mux APIs are enabled to the user

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.13 Parameter RmEnableMscmSupport

When this parameter is enabled, the MSCM APIs are enabled to the user

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.14 Container RmConfigSet

Vendor specific: This container is the base for a multiple configuration set

Included subcontainers:

- Xrdc_Configuration
- Rm_XRDC_Domain_Assignment
- Rm_XRDC_Memory_Config
- Rm_XRDC_Peripheral_Config
- Sema42_ModuleConfig
- Pflash_Configuration
- Crossbar_Configuration
- Xbic_Configuration
- Virt_Wrapper_Configuration
- Dma_Mux_Configuration
- Mscm_Configuration

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.15 Container Xrdc_Configuration

Configuration for the Xrdc.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.16 Parameter XrdcDevErrorDetect

XrdcDevErrorDetect

Switches the Development Error Detection and Notification ON or OFF.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.17 Parameter XrdcRegistersLock

Lock XRDC registers (except PIDm registers) in order to prevent them from being unintentionally modified during Runtime.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.18 Parameter XrdcCRLockBit

Variable for setting the CR bit lock! XrdcRegisterLock should be true

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.19 Parameter XrdcPIDRegisterLock

Select lock mode for PIDm registers

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	XRDC_PID_UNLOCKED
literals	['XRDC_PID_UNLOCKED', 'XRDC_PID_ALLOW_ACCESS_FROM_M↩ ASTER', 'XRDC_PID_FULLY_LOCKED']

4.20 Container Rm_XRDC_Domain_Assignment

All data need to configure one Domain.

Included subcontainers:

- Domain_Master_Assignment
- Domain_Peripheral_Assignment
- Domain_Memory_Assignment

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.21 Parameter DomainID

Vendor specific:

Id for the current Domain.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	XRDC_DOMAIN0
literals	['XRDC_DOMAIN0', 'XRDC_DOMAIN1', 'XRDC_DOMAIN2']

4.22 Container Domain_Master_Assignment

Vendor specific:

All data need to configure one Master.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.23 Parameter XrdcMasterInstance

Select the master of XRDC

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true

Property	Value
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	Xrdc_0_CM7_0
literals	['Xrdc_0_CM7_0', 'Xrdc_0_eDMA_AHB', 'Xrdc_0_HSE_B', 'Xrdc_0_C↩ M7_1', 'Xrdc_0_GMAC_0', 'Xrdc_0_CM7_2', 'Xrdc_0_uSDHC_AHB']

4.24 Parameter XrdcPIDEnable

PID mode enable - only valid if the master instance is core type

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	XRDC_MDA_PID_DISABLE
literals	['XRDC_MDA_PID_DISABLE', 'XRDC_MDA_PID_ENABLE_EXPRES↩ SION0', 'XRDC_MDA_PID_ENABLE_EXPRESSION1']

4.25 Parameter XrdcMasterPID

Process Identifier. This field only has meaning if the core is core master type and PID mode enable

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE

Property	Value
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	63
min	0

4.26 Parameter XrdcMasterPIDMask

Process Identifier Mask. This field only has meaning if the core is core master type and PID mode enable

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	63
min	0

4.27 Parameter XrdcDIDBDisable

Disabled DID bypass. This field only has meaning if the core is non-core master type

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.28 Parameter XrdcMDADFMTLockBit

Variable for setting the MDA_DFMT bit lock! XrdcRegisterLock should be true.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.29 Parameter XrdcMasterMode

Specifies the secure attribute. This field only has meaning if the core is non-core master type

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	XRDC_SECURE
literals	['XRDC_SECURE', 'XRDC_NON_SECURE', 'XRDC_INPUT_FROM_BU↩ S_MASTER']

4.30 Parameter XrdcMasterPriviledgeMode

Specifies the privileged (supervisor/user) attribute. This field only has meaning if the core is non-core master type

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	XRDC_INPUT_PRIVILEDGE_FROM_BUS_MASTER
literals	['XRDC_USER_MODE', 'XRDC_PRIVILEDGE_MODE', 'XRDC_INPUT↩ _PRIVILEDGE_FROM_BUS_MASTER']

4.31 Container Domain_Peripheral_Assignment

Vendor specific:

All data need to configure Peripheral for one Domain.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.32 Parameter Secure_Access_Policy

Vendor specific:

Mode access to policy of mode Secure.

Access policy look up table:

Configuration Fields

Allowable accesses

Secure_Access_Policy

Non_Secure_Access_Policy

Secure Privileged

Secure User

NonSecure Privileged

NonSecure User

XRDC_FULL_ACCESS

XRDC_FULL_ACCESS

R,W

R,W

R,W

R,W

XRDC_FULL_ACCESS

XRDC_SUPERVISOR_ACCESS_ONLY

R,W

R,W

R,W

None

XRDC_FULL_ACCESS

XRDC_READ_ONLY

R,W

R,W

R

R

XRDC_FULL_ACCESS

XRDC_SUPERVISOR_READ_ONLY

R,W

R,W

R

None

XRDC_FULL_ACCESS

XRDC_NO_ACCESS

R,W

R,W

None

None

XRDC_SUPERVISOR_ACCESS_ONLY

NA

R,W

None

None

None

XRDC_READ_ONLY

NA

R

R

None

None

XRDC_NO_ACCESS

NA

None

None

None

None

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	XRDC_FULL_ACCESS
literals	['XRDC_FULL_ACCESS', 'XRDC_READ_ONLY', 'XRDC_SUPERVISOR↩ _ACCESS_ONLY', 'XRDC_NO_ACCESS']

4.33 Parameter Non_Secure_Access_Policy

Vendor specific:

Mode access to policy of mode Non_Secure.

Access policy look up table:

Configuration Fields

Allowable accesses

Secure_Access_Policy

Non_Secure_Access_Policy

Secure Privileged

Secure User

NonSecure Privileged

NonSecure User

XRDC_FULL_ACCESS

XRDC_FULL_ACCESS

R,W

R,W

R,W

R,W

XRDC_FULL_ACCESS

XRDC_SUPERVISOR_ACCESS_ONLY

R,W

R,W

R,W

None

XRDC_FULL_ACCESS

XRDC_READ_ONLY

R,W

R,W

R

R

XRDC_FULL_ACCESS

XRDC_SUPERVISOR_READ_ONLY

R,W

R,W

R

None

XRDC_FULL_ACCESS

XRDC_NO_ACCESS

R,W

R,W

None

None

XRDC_SUPERVISOR_ACCESS_ONLY

NA

R,W

None

None

None

XRDC_READ_ONLY

NA

R

R

None

None

XRDC_NO_ACCESS

NA

None

None

None

None

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	XRDC_FULL_ACCESS
literals	['XRDC_FULL_ACCESS', 'XRDC_SUPERVISOR_ACCESS_ONLY', 'XR↩DC_READ_ONLY', 'XRDC_SUPERVISOR_READ_ONLY', 'XRDC_NO_↩ACCESS']

4.34 Reference Domain_Peripheral_Assignment

Vendor specific:

Reference to Peripheral config.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
requiresSymbolicNameValue	False
destination	/TS_T40D34M30I0R0/Rm/RmConfigSet/Rm_XRDC_Peripheral_Config

4.35 Container Domain_Memory_Assignment

Vendor specific:

All data need to configure Memory for one Domain.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.36 Parameter Secure_Access_Policy

Vendor specific:

Mode access to policy of mode Secure.

Access policy look up table:

Configuration Fields

Allowable accesses

Secure_Access_Policy

Non_Secure_Access_Policy

Secure Privileged

Secure User

NonSecure Privileged

NonSecure User

XRDC_FULL_ACCESS

XRDC_FULL_ACCESS

R,W

R,W

R,W

R,W

XRDC_FULL_ACCESS

XRDC_SUPERVISOR_ACCESS_ONLY

R,W

R,W

R,W

None

XRDC_FULL_ACCESS

XRDC_READ_ONLY

R,W

R,W

R

R

XRDC_FULL_ACCESS

XRDC_SUPERVISOR_READ_ONLY

R,W

R,W

R

None

XRDC_FULL_ACCESS

XRDC_NO_ACCESS

R,W

R,W

None

None

XRDC_SUPERVISOR_ACCESS_ONLY

NA

R,W

None

None

None

XRDC_READ_ONLY

NA

R

R

None

None

XRDC_NO_ACCESS

NA

None

None

None

None

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	XRDC_FULL_ACCESS
literals	['XRDC_FULL_ACCESS', 'XRDC_READ_ONLY', 'XRDC_SUPERVISOR↩ _ACCESS_ONLY', 'XRDC_NO_ACCESS']

4.37 Parameter Non_Secure_Access_Policy

Vendor specific:

Mode access to policy of mode Non_Secure.

Access policy look up table:

Configuration Fields

Allowable accesses

Secure_Access_Policy

Non_Secure_Access_Policy

Secure Privileged

Secure User

NonSecure Privileged

NonSecure User

XRDC_FULL_ACCESS

XRDC_FULL_ACCESS

R,W

R,W

R,W

R,W

XRDC_FULL_ACCESS

XRDC_SUPERVISOR_ACCESS_ONLY

R,W

R,W

R,W

None

XRDC_FULL_ACCESS

XRDC_READ_ONLY

R,W

R,W

R

R

XRDC_FULL_ACCESS

XRDC_SUPERVISOR_READ_ONLY

R,W

R,W

R

None

XRDC_FULL_ACCESS

XRDC_NO_ACCESS

R,W

R,W

None

None

XRDC_SUPERVISOR_ACCESS_ONLY

NA

R,W

None

None

None

XRDC_READ_ONLY

NA

R

R

None

None

XRDC_NO_ACCESS

NA

None

None

None

None

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	XRDC_FULL_ACCESS
literals	['XRDC_FULL_ACCESS', 'XRDC_SUPERVISOR_ACCESS_ONLY', 'XR↩ DC_READ_ONLY', 'XRDC_SUPERVISOR_READ_ONLY', 'XRDC_NO_↩ ACCESS']

4.38 Reference Domain_Memory_Assignment

Choose Memory configuration

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
requiresSymbolicNameValue	False
destination	/TS_T40D34M30I0R0/Rm/RmConfigSet/Rm_XRDC_Memory_Config

4.39 Container Rm_XRDC_Memory_Config

Vendor specific:

All data need to configure Memory use for Domain.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	9
upperMultiplicity	Infinite
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.40 Parameter XrdcMrcInstance

Select Memory region controller will be used to control the address range below

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	Xrdc_0_PFLASH_0
literals	['Xrdc_0_PFLASH_0', 'Xrdc_0_PFLASH_1', 'Xrdc_0_PFLASH_3', 'Xrdc↩ _0_PFLASH_WR', 'Xrdc_0_PRAM0_0', 'Xrdc_0_PRAM1_0', 'Xrdc_0_↩ TCM', 'Xrdc_0_QuadSPI', 'Xrdc_0_PRAM2_0']

4.41 Parameter XrdcStartAddress

Start address of Memory region

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	412316860416
min	0

4.42 Parameter XrdcEndAddress

End address of Memory region

Property	Value
type	ECUC-INTEGER-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4294967295
max	412316860416
min	0

4.43 Parameter XrdcSema4Enable

Enable Semaphore would require the domain must own the gate to have access right for this memory range

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.44 Parameter XrdcMRGDLockBit

Variable for setting the MRGD bit lock! XrdcRegisterLock should be true

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.45 Reference XrdcSema42LogicChannel

Select XrdcSema42LogicChannel to select specified Sema42 Logic Channel

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
requiresSymbolicNameValue	False
destination	/TS_T40D34M30I0R0/Rm/RmConfigSet/Sema42_ModuleConfig/Sema42↩ LogicChannelConfiguration

4.46 Container Rm_XRDC_Peripheral_Config

Vendor specific:

All data need to configure Peripheral for Domain.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0

Property	Value
upperMultiplicity	Infinite
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.47 Parameter XrdcPeripheralSlot

Peripheral slot number of a block of peripherals. Checking Reference manual for chip specific

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	Xrdc_0_ERM_1

Property	Value
literals	['Xrdc_0_ERM_1', 'Xrdc_0_TRGMUX', 'Xrdc_0_BCTU', 'Xrdc_0_EMIOS_0', 'Xrdc_0_EMIOS_1', 'Xrdc_0_EMIOS_2', 'Xrdc_0_LCU_0', 'Xrdc_0_LCU_1', 'Xrdc_0_ADC_0', 'Xrdc_0_ADC_1', 'Xrdc_0_ADC_2', 'Xrdc_0_PIT_0', 'Xrdc_0_PIT_1', 'Xrdc_0_MU_2_MUA', 'Xrdc_0_MU_2_MUB', 'Xrdc_0_AXBS', 'Xrdc_0_System_XBIC', 'Xrdc_0_Periph_XBIC', 'Xrdc_0_EDMA', 'Xrdc_0_EDMA_TCD_0', 'Xrdc_0_EDMA_TCD_1', 'Xrdc_0_EDMA_TCD_2', 'Xrdc_0_EDMA_TCD_3', 'Xrdc_0_EDMA_TCD_4', 'Xrdc_0_EDMA_TCD_5', 'Xrdc_0_EDMA_TCD_6', 'Xrdc_0_EDMA_TCD_7', 'Xrdc_0_EDMA_TCD_8', 'Xrdc_0_EDMA_TCD_9', 'Xrdc_0_EDMA_TCD_10', 'Xrdc_0_EDMA_TCD_11', 'Xrdc_0_Debug_APB_Page0', 'Xrdc_0_Debug_APB_Page1', 'Xrdc_0_Debug_APB_Page2', 'Xrdc_0_Debug_APB_Page3', 'Xrdc_0_Debug_APB_Paged_Area', 'Xrdc_0_SDA_AP', 'Xrdc_0_ERM_0', 'Xrdc_0_MSCM', 'Xrdc_0_PRAM_0', 'Xrdc_0_PFC', 'Xrdc_0_PFC_alt', 'Xrdc_0_SWT_0', 'Xrdc_0_STM_0', 'Xrdc_0_XRDC', 'Xrdc_0_INTM', 'Xrdc_0_DMAMUX_0', 'Xrdc_0_DMAMUX_1', 'Xrdc_0_RTC', 'Xrdc_0_MC_RGM', 'Xrdc_0_SIUL2_VIRTWRAPPER_PDAC0_HSE_B_0', 'Xrdc_0_SIUL2_VIRTWRAPPER_PDAC0_HSE_B_1', 'Xrdc_0_SIUL2_VIRTWRAPPER_PDAC1_M7_0_0', 'Xrdc_0_SIUL2_VIRTWRAPPER_PDAC1_M7_0_1', 'Xrdc_0_SIUL2_VIRTWRAPPER_PDAC2_M7_1_0', 'Xrdc_0_SIUL2_VIRTWRAPPER_PDAC2_M7_1_1', 'Xrdc_0_SIUL2_VIRTWRAPPER_PDAC3', 'Xrdc_0_DCM', 'Xrdc_0_WKPU', 'Xrdc_0_CMU_0_6', 'Xrdc_0_TSPC', 'Xrdc_0_SIRC', 'Xrdc_0_SXOSC', 'Xrdc_0_FIRC', 'Xrdc_0_FXOSC', 'Xrdc_0_MC_CGM', 'Xrdc_0_MC_ME', 'Xrdc_0_PLL', 'Xrdc_0_PLL_2', 'Xrdc_0_PMC', 'Xrdc_0_FMU', 'Xrdc_0_FMU_alt', 'Xrdc_0_PIT_2', 'Xrdc_0_FlexCAN_0', 'Xrdc_0_FlexCAN_1', 'Xrdc_0_FlexCAN_2', 'Xrdc_0_FlexCAN_3', 'Xrdc_0_FlexCAN_4', 'Xrdc_0_FlexCAN_5', 'Xrdc_0_FlexCAN_6', 'Xrdc_0_FlexCAN_7', 'Xrdc_0_FlexIO', 'Xrdc_0_LPUART_0', 'Xrdc_0_LPUART_1', 'Xrdc_0_LPUART_2', 'Xrdc_0_LPUART_3', 'Xrdc_0_LPUART_4', 'Xrdc_0_LPUART_5', 'Xrdc_0_LPUART_6', 'Xrdc_0_LPUART_7', 'Xrdc_0_LPI2C_0', 'Xrdc_0_LPI2C_1', 'Xrdc_0_LPSPI_0', 'Xrdc_0_LPSPI_1', 'Xrdc_0_LPSPI_2', 'Xrdc_0_LPSPI_3', 'Xrdc_0_SAI_0', 'Xrdc_0_LPCMP_0', 'Xrdc_0_LPCMP_1', 'Xrdc_0_TMU', 'Xrdc_0_CRC', 'Xrdc_0_FCCU', 'Xrdc_0_MU_0', 'Xrdc_0_JDC', 'Xrdc_0_CONFIGURATION_GPR', 'Xrdc_0_STCU', 'Xrdc_0_SELFTEST_GPR', 'Xrdc_0_EDMA_XBIC', 'Xrdc_0_PRAM2_TCM_XBIC', 'Xrdc_0_EDMA_TCD_12', 'Xrdc_0_EDMA_TCD_13', 'Xrdc_0_EDMA_TCD_14', 'Xrdc_0_EDMA_TCD_15', 'Xrdc_0_EDMA_TCD_16', 'Xrdc_0_EDMA_TCD_17', 'Xrdc_0_EDMA_TCD_18', 'Xrdc_0_EDMA_TCD_19', 'Xrdc_0_EDMA_TCD_20', 'Xrdc_0_EDMA_TCD_21', 'Xrdc_0_EDMA_TCD_22', 'Xrdc_0_EDMA_TCD_23', 'Xrdc_0_EDMA_TCD_24', 'Xrdc_0_EDMA_TCD_25', 'Xrdc_0_EDMA_TCD_26', 'Xrdc_0_EDMA_TCD_27', 'Xrdc_0_EDMA_TCD_28', 'Xrdc_0_EDMA_TCD_29', 'Xrdc_0_EDMA_TCD_30', 'Xrdc_0_EDMA_TCD_31', 'Xrdc_0_SEMA_42', 'Xrdc_0_PRAM_1', 'Xrdc_0_PRAM_2', 'Xrdc_0_SWT_1', 'Xrdc_0_STM_1', 'Xrdc_0_STM_2', 'Xrdc_0_GMAC_0', 'Xrdc_0_LPUART_8', 'Xrdc_0_LPUART_9', 'Xrdc_0_LPUART_10', 'Xrdc_0_LPUART_11', 'Xrdc_0_LPUART_12', 'Xrdc_0_LPUART_13', 'Xrdc_0_LPUART_14', 'Xrdc_0_LPUART_15', 'Xrdc_0_LPSPI_4', 'Xrdc_0_LPSPI_5', 'Xrdc_0_QuadSPI', 'Xrdc_0_SAI_1', 'Xrdc_0_USDHC', 'Xrdc_0_LPCMP_2', 'Xrdc_0_MU_1', 'Xrdc_0_EIM_0', 'Xrdc_0_EIM_1', 'Xrdc_0_EIM_2']

4.48 Parameter XrdcSema4Enable

Enable Semaphore would require the domain must own the gate to have access right for this peripheral

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.49 Parameter XrdcPDACLockBit

Variable for setting the PDAC bit lock! XrdcRegisterLock should be true.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.50 Reference XrdcSema42LogicChannel

Select XrdcSema42LogicChannel to select specified Sema42 Logic Channel

Property	Value
type	ECUC-REFERENCE-DEF

Property	Value
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
requiresSymbolicNameValue	False
destination	/TS_T40D34M30I0R0/Rm/RmConfigSet/Sema42_ModuleConfig/Sema42↩ LogicChannelConfiguration

4.51 Container Sema42_ModuleConfig

Configuration for the Semaphores2.

Included subcontainers:

- Sema42LogicChannelConfiguration

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.52 Parameter Sema42DevErrorDetect

Sema42DevErrorDetect

Switches the Development Error Detection and Notification ON or OFF.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.53 Container Sema42LogicChannelConfiguration

Configuration for Sema42 Instance

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

4.54 Parameter Sema42LogicChannel_LogicName

Vendor specific:

Logic Channel Name.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A

Property	Value
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	SEMA42_LOGIC_CH_0

4.55 Parameter Sema42HardwareInstance

Vendor specific: Select the physical Sema42 Instance.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	true
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SEMA42_INSTANCE0
literals	['SEMA42_INSTANCE0']

4.56 Parameter Sema42HardwareChannel

Vendor specific: Select the physical Sema42 Channel.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD

Property	Value
defaultValue	0
max	15
min	0

4.57 Container Pflash_Configuration

Configuration for the "Pflash.

Included subcontainers:

- PflashMasterProtection

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.58 Parameter PflashDevErrorDetect

PflashDevErrorDetect

Switches the Development Error Detection and Notification ON or OFF.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.59 Container PflashMasterProtection

Pflash Master Protection

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.60 Parameter PflashMaster

Select master for mode protection

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	Pflash_0_CM7_0
literals	['Pflash_0_CM7_0', 'Pflash_0_CM7_1', 'Pflash_0_eDMA', 'Pflash_0_GM↩ AC_0', 'Pflash_0_uSDHC', 'Pflash_0_CM7_2']

4.61 Parameter PflashMasterAccess

Select access right for each master

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	PFLASH_READ_NOT_ALLOWED
literals	['PFLASH_READ_NOT_ALLOWED', 'PFLASH_READ_ALLOWED']

4.62 Container Crossbar_Configuration

Configuration for the Crossbar.

Included subcontainers:

- RmCrossbarInstance

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.63 Parameter CrossbarDevErrorDetect

CrossbarDevErrorDetect

Switches the Development Error Detection and Notification ON or OFF.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.64 Container RmCrossbarInstance

Vendor specific: Configuration of a crossbar instance.

Included subcontainers:

- RmCrossbarHwSlavePort

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	2
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.65 Parameter RmCrossbarHwInstance

Vendor specific:

Select the crossbar switch instance.

Note: For S32K3XX, only XRDC_1 (XRDC Lite Peripheral) is programmable. Also for S32K312, AXBS is not programmable.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	AXBS_0
literals	['AXBS_0', 'AXBS_1', 'AXBS_2', 'AXBS_4', 'AXBS_5']

4.66 Container RmCrossbarHwSlavePort

Hardware slave port configuration.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	8
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.67 Parameter RmSlavePortNumber

Vendor specific:

Slave port number in hardware.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	7
min	0

4.68 Parameter RmCrossbarPrioMaster0

Vendor specific:

Priority of the master 0 on the cross bar.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	7
min	0

4.69 Parameter RmCrossbarPrioMaster1

Vendor specific:

Priority of the master1 on the cross bar.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	7
min	0

4.70 Parameter RmCrossbarPrioMaster2

Vendor specific:

Priority of the master2 on the cross bar.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	2
max	7
min	0

4.71 Parameter RmCrossbarPrioMaster3

Vendor specific:

Priority of the master3 on the cross bar.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	3
max	7
min	0

4.72 Parameter RmCrossbarPrioMaster4

Vendor specific:

Priority of the master4 on the cross bar.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4
max	7
min	0

4.73 Parameter RmCrossbarPrioMaster5

Vendor specific:

Priority of the master5 on the cross bar.

Property	Value
type	ECUC-INTEGER-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	5
max	7
min	0

4.74 Parameter RmCrossbarPrioMaster6

Vendor specific:

Priority of the master6 on the cross bar.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	6
max	7
min	0

4.75 Parameter RmCrossbarPrioMaster7

Vendor specific:

Priority of the master7 on the cross bar.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	7
max	7
min	0

4.76 Parameter RmCrossbarEnableLock

Vendor specific: Locks the configuration registers for the respective slave port.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.77 Parameter RmCrossbarHaltLowPrio

Vendor specific: Sets the initial arbitration priority for low power mode requests. Setting this bit will not affect the request

for low power mode from attaining highest priority once it has control of the slave ports. Disabled = The low power mode request has the highest priority for arbitration on this slave port;

Enabled = The low power mode request has the lowest initial priority for arbitration on this slave port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.78 Parameter RmCrossbarEnablePrioElevM0

Vendor specific: On this slave port, enable priority elevation for master 0. If enabled, the master is able to elevate its priority

to the highest.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.79 Parameter RmCrossbarEnablePrioElevM1

Vendor specific: On this slave port, enable priority elevation for master 1. If enabled, the master is able to elevate its priority

to the highest.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.80 Parameter RmCrossbarEnablePrioElevM2

Vendor specific: On this slave port, enable priority elevation for master 2. If enabled, the master is able to elevate its priority

to the highest.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.81 Parameter RmCrossbarEnablePrioElevM3

Vendor specific: On this slave port, enable priority elevation for master 3. If enabled, the master is able to elevate its priority

to the highest.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.82 Parameter RmCrossbarEnablePrioElevM4

Vendor specific: On this slave port, enable priority elevation for master 4. If enabled, the master is able to elevate its priority

to the highest.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.83 Parameter RmCrossbarEnablePrioElevM5

Vendor specific: On this slave port, enable priority elevation for master 5. If enabled, the master is able to elevate its priority

to the highest.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.84 Parameter RmCrossbarEnablePrioElevM6

Vendor specific: On this slave port, enable priority elevation for master 6. If enabled, the master is able to elevate its priority

to the highest.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.85 Parameter RmCrossbarEnablePrioElevM7

Vendor specific: On this slave port, enable priority elevation for master 7. If enabled, the master is able to elevate its priority

to the highest.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.86 Parameter RmCrossbarEnableFixedPrio

Vendor specific: On this slave port, select the arbitraion mode: if enabled the arbitration mode will be FIXED PRIORITY, if disabled it will be ROUND ROBIN.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.87 Parameter RmCrossbarParkingControl

Determines the slave port?s parking control. The low-power park feature results in an overall power savings if the slave port is not saturated; however, this forces an extra latency clock when any master tries to access the slave port while not in use because it is not parked on any master.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	ParkField
literals	['ParkField', 'LastMaster', 'LowPowerPark']

4.88 Parameter RmCrossbarParkField

Vendor specific:

Determines which master port the current slave port parks on when no masters are actively making requests and the RmCrossbarParkingControl=ParkField.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	7
min	0

4.89 Container Xbic_Configuration

Configuration for the Xbic.

Included subcontainers:

- XbicCheckingControl

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.90 Parameter XbicDevErrorDetect

XbicDevErrorDetect

Switches the Development Error Detection and Notification ON or OFF.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.91 Container XbicCheckingControl

Xbic Checking Control

Configuration enable/disable slave port EDC Error Detection (SE) and master port for Feedback Integrity Check (ME) of all of Xbic Instances.

Note: Any SE and ME that are not configured will be enabled by default

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	4
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.92 Parameter XbicInstance

Select Xbic instance

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	XBIC_0
literals	['XBIC_0', 'XBIC_1', 'XBIC_2', 'XBIC_4']

4.93 Parameter SE0

Enable/Disable Attribute integrity checking for slave port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE

Property	Value
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.94 Parameter SE1

Enable/Disable Attribute integrity checking for slave port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.95 Parameter SE2

Enable/Disable Attribute integrity checking for slave port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.96 Parameter SE3

Enable/Disable Attribute integrity checking for slave port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.97 Parameter SE4

Enable/Disable Attribute integrity checking for slave port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.98 Parameter SE5

Enable/Disable Attribute integrity checking for slave port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.99 Parameter SE6

Enable/Disable Attribute integrity checking for slave port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.100 Parameter SE7

Enable/Disable Attribute integrity checking for slave port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A

Property	Value
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.101 Parameter ME0

Enable/Disable Feedback integrity checking for master port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.102 Parameter ME1

Enable/Disable Feedback integrity checking for master port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.103 Parameter ME2

Enable/Disable Feedback integrity checking for master port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.104 Parameter ME3

Enable/Disable Feedback integrity checking for master port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.105 Parameter ME4

Enable/Disable Feedback integrity checking for master port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.106 Parameter ME5

Enable/Disable Feedback integrity checking for master port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.107 Parameter ME6

Enable/Disable Feedback integrity checking for master port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A

Property	Value
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.108 Parameter ME7

Enable/Disable Feedback integrity checking for master port

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.109 Container Virt_Wrapper_Configuration

Configuration for the "Virtual Wrapper.

Included subcontainers:

- Mscr_Config_List
- Imcr_Config_List
- Other_Config_List

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.110 Parameter VirtWrapperDevErrorDetect

VirtWrapperDevErrorDetect

Switches the Development Error Detection and Notification ON or OFF.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.111 Container Mscr_Config_List

Vendor specific:

Virtual wrraper for MSCR.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	233
upperMultiplicity	233
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.112 Parameter MscrName

Select output pad

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	PTA0
literals	['PTA0', 'PTA1', 'PTA2', 'PTA3', 'PTA4', 'PTA5', 'PTA6', 'PTA7', 'PTA8', 'PTA9', 'PTA10', 'PTA11', 'PTA12', 'PTA13', 'PTA14', 'PTA15', 'PTA16', 'PTA17', 'PTA18', 'PTA19', 'PTA20', 'PTA21', 'PTA22', 'PTA23', 'PTA24', 'PTA25', 'PTA26', 'PTA27', 'PTA28', 'PTA29', 'PTA30', 'PTA31', 'PTB0', 'PTB1', 'PTB2', 'PTB3', 'PTB4', 'PTB5', 'PTB8', 'PTB9', 'PTB10', 'PTB11', 'PTB12', 'PTB13', 'PTB14', 'PTB15', 'PTB16', 'PTB17', 'PTB18', 'PTB19', 'PTB20', 'PTB21', 'PTB22', 'PTB23', 'PTB24', 'PTB25', 'PTB26', 'PTB27', 'PTB28', 'PTB29', 'PTB30', 'PTB31', 'PTC0', 'PTC1', 'PTC2', 'PTC3', 'PTC4', 'PTC5', 'PTC6', 'PTC7', 'PTC8', 'PTC9', 'PTC10', 'PTC11', 'PTC12', 'PTC13', 'PTC14', 'PTC15', 'PTC16', 'PTC17', 'PTC18', 'PTC19', 'PTC20', 'PTC21', 'PTC22', 'PTC23', 'PTC24', 'PTC25', 'PTC26', 'PTC27', 'PTC28', 'PTC29', 'PTC30', 'PTC31', 'PTD0', 'PTD1', 'PTD2', 'PTD3', 'PTD4', 'PTD5', 'PTD6', 'PTD7', 'PTD8', 'PTD9', 'PTD10', 'PTD11', 'PTD12', 'PTD13', 'PTD14', 'PTD15', 'PTD16', 'PTD17', 'PTD18', 'PTD19', 'PTD20', 'PTD21', 'PTD22', 'PTD23', 'PTD24', 'PTD25', 'PTD26', 'PTD27', 'PTD28', 'PTD29', 'PTD30', 'PTD31', 'PTE0', 'PTE1', 'PTE2', 'PTE3', 'PTE4', 'PTE5', 'PTE6', 'PTE7', 'PTE8', 'PTE9', 'PTE10', 'PTE11', 'PTE12', 'PTE13', 'PTE14', 'PTE15', 'PTE16', 'PTE17', 'PTE18', 'PTE19', 'PTE20', 'PTE21', 'PTE22', 'PTE23', 'PTE24', 'PTE25', 'PTE26', 'PTE27', 'PTE29', 'PTE31', 'PTF0', 'PTF1', 'PTF2', 'PTF3', 'PTF4', 'PTF5', 'PTF6', 'PTF7', 'PTF8', 'PTF9', 'PTF10', 'PTF11', 'PTF12', 'PTF13', 'PTF14', 'PTF15', 'PTF16', 'PTF17', 'PTF18', 'PTF19', 'PTF20', 'PTF21', 'PTF22', 'PTF23', 'PTF24', 'PTF25', 'PTF26', 'PTF27', 'PTF28', 'PTF29', 'PTF30', 'PTF31', 'PTG0', 'PTG1', 'PTG2', 'PTG3', 'PTG4', 'PTG5', 'PTG6', 'PTG7', 'PTG8', 'PTG9', 'PTG10', 'PTG11', 'PTG12', 'PTG13', 'PTG14', 'PTG15', 'PTG16', 'PTG17', 'PTG18', 'PTG19', 'PTG20', 'PTG21', 'PTG22', 'PTG23', 'PTG24', 'PTG25', 'PTG26', 'PTG27', 'PTG28', 'PTG29', 'PTG30', 'PTG31', 'PTH0', 'PTH1', 'PTH2', 'PTH3', 'PTH4', 'PTH5', 'PTH6', 'PTH7', 'PTH8', 'PTH9', 'PTH10', 'PTH11', 'PTH12']

4.113 Parameter MscrNumber

Seclect pad number

Property	Value
type	ECUC-INTEGER-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	65535
min	0

4.114 Parameter MscrSiul2Instance

Select SIUL2 Instance

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SIUL2_0
literals	['SIUL2_0']

4.115 Parameter MscrPinMux

Select Pin Mux

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	False

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	GPIO_0

4.116 Parameter MscrMirror

Select SIUL2 Mirror

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	Xrdc_0_SIUL2_VIRTWRAPPER_PDAC0_HSE_B_0
literals	['Xrdc_0_SIUL2_VIRTWRAPPER_PDAC0_HSE_B_0', 'Xrdc_0_SIUL2_↩ VIRTWRAPPER_PDAC0_HSE_B_1', 'Xrdc_0_SIUL2_VIRTWRAPPER↩ _PDAC1_M7_0_0', 'Xrdc_0_SIUL2_VIRTWRAPPER_PDAC1_M7_0_1', 'Xrdc_0_SIUL2_VIRTWRAPPER_PDAC2_M7_1_0', 'Xrdc_0_SIUL2_VI↩ RTWRAPPER_PDAC2_M7_1_1', 'Xrdc_0_SIUL2_VIRTWRAPPER_PD↩ AC3']

4.117 Container Imcr_Config_List

Vendor specific:

IMCR configuration list.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	314
upperMultiplicity	314
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.118 Parameter ImcrName

Select input register

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SIUL2_0_IMCR512

Property	Value
literals	['SIUL2_0_IMCR512', 'SIUL2_0_IMCR513', 'SIUL2_0_IMCR514', 'SIUL2_0_IMCR515', 'SIUL2_0_IMCR516', 'SIUL2_0_IMCR517', 'SIUL2_0_IMCR929', 'SIUL2_0_IMCR930', 'SIUL2_0_IMCR801', 'SIUL2_0_IMCR802', 'SIUL2_0_IMCR803', 'SIUL2_0_IMCR806', 'SIUL2_0_IMCR807', 'SIUL2_0_IMCR804', 'SIUL2_0_IMCR805', 'SIUL2_0_IMCR808', 'SIUL2_0_IMCR813', 'SIUL2_0_IMCR814', 'SIUL2_0_IMCR812', 'SIUL2_0_IMCR656', 'SIUL2_0_IMCR657', 'SIUL2_0_IMCR658', 'SIUL2_0_IMCR659', 'SIUL2_0_IMCR560', 'SIUL2_0_IMCR570', 'SIUL2_0_IMCR571', 'SIUL2_0_IMCR572', 'SIUL2_0_IMCR573', 'SIUL2_0_IMCR574', 'SIUL2_0_IMCR575', 'SIUL2_0_IMCR576', 'SIUL2_0_IMCR577', 'SIUL2_0_IMCR578', 'SIUL2_0_IMCR579', 'SIUL2_0_IMCR561', 'SIUL2_0_IMCR580', 'SIUL2_0_IMCR581', 'SIUL2_0_IMCR582', 'SIUL2_0_IMCR583', 'SIUL2_0_IMCR562', 'SIUL2_0_IMCR563', 'SIUL2_0_IMCR564', 'SIUL2_0_IMCR565', 'SIUL2_0_IMCR566', 'SIUL2_0_IMCR567', 'SIUL2_0_IMCR568', 'SIUL2_0_IMCR569', 'SIUL2_0_IMCR592', 'SIUL2_0_IMCR602', 'SIUL2_0_IMCR603', 'SIUL2_0_IMCR604', 'SIUL2_0_IMCR605', 'SIUL2_0_IMCR606', 'SIUL2_0_IMCR607', 'SIUL2_0_IMCR608', 'SIUL2_0_IMCR609', 'SIUL2_0_IMCR610', 'SIUL2_0_IMCR611', 'SIUL2_0_IMCR593', 'SIUL2_0_IMCR612', 'SIUL2_0_IMCR613', 'SIUL2_0_IMCR614', 'SIUL2_0_IMCR615', 'SIUL2_0_IMCR594', 'SIUL2_0_IMCR595', 'SIUL2_0_IMCR596', 'SIUL2_0_IMCR597', 'SIUL2_0_IMCR598', 'SIUL2_0_IMCR599', 'SIUL2_0_IMCR600', 'SIUL2_0_IMCR601', 'SIUL2_0_IMCR624', 'SIUL2_0_IMCR634', 'SIUL2_0_IMCR635', 'SIUL2_0_IMCR636', 'SIUL2_0_IMCR637', 'SIUL2_0_IMCR638', 'SIUL2_0_IMCR639', 'SIUL2_0_IMCR640', 'SIUL2_0_IMCR641', 'SIUL2_0_IMCR642', 'SIUL2_0_IMCR643', 'SIUL2_0_IMCR625', 'SIUL2_0_IMCR644', 'SIUL2_0_IMCR645', 'SIUL2_0_IMCR646', 'SIUL2_0_IMCR647', 'SIUL2_0_IMCR626', 'SIUL2_0_IMCR627', 'SIUL2_0_IMCR628', 'SIUL2_0_IMCR629', 'SIUL2_0_IMCR630', 'SIUL2_0_IMCR631', 'SIUL2_0_IMCR632', 'SIUL2_0_IMCR633', 'SIUL2_0_IMCR660', 'SIUL2_0_IMCR661', 'SIUL2_0_IMCR664', 'SIUL2_0_IMCR665', 'SIUL2_0_IMCR674', 'SIUL2_0_IMCR675', 'SIUL2_0_IMCR676', 'SIUL2_0_IMCR677', 'SIUL2_0_IMCR678', 'SIUL2_0_IMCR679', 'SIUL2_0_IMCR680', 'SIUL2_0_IMCR681', 'SIUL2_0_IMCR682', 'SIUL2_0_IMCR683', 'SIUL2_0_IMCR666', 'SIUL2_0_IMCR684', 'SIUL2_0_IMCR685', 'SIUL2_0_IMCR686', 'SIUL2_0_IMCR687', 'SIUL2_0_IMCR688', 'SIUL2_0_IMCR689', 'SIUL2_0_IMCR690', 'SIUL2_0_IMCR691', 'SIUL2_0_IMCR692', 'SIUL2_0_IMCR693', 'SIUL2_0_IMCR667', 'SIUL2_0_IMCR694', 'SIUL2_0_IMCR695', 'SIUL2_0_IMCR668', 'SIUL2_0_IMCR669', 'SIUL2_0_IMCR670', 'SIUL2_0_IMCR671', 'SIUL2_0_IMCR672', 'SIUL2_0_IMCR673', 'SIUL2_0_IMCR855', 'SIUL2_0_IMCR696', 'SIUL2_0_IMCR697', 'SIUL2_0_IMCR698', 'SIUL2_0_IMCR723', 'SIUL2_0_IMCR724', 'SIUL2_0_IMCR725', 'SIUL2_0_IMCR726', 'SIUL2_0_IMCR727', 'SIUL2_0_IMCR728', 'SIUL2_0_IMCR729', 'SIUL2_0_IMCR730', 'SIUL2_0_IMCR731', 'SIUL2_0_IMCR732', 'SIUL2_0_IMCR733', 'SIUL2_0_IMCR734', 'SIUL2_0_IMCR735', 'SIUL2_0_IMCR736', 'SIUL2_0_IMCR737', 'SIUL2_0_IMCR738', 'SIUL2_0_IMCR739', 'SIUL2_0_IMCR740', 'SIUL2_0_IMCR741', 'SIUL2_0_IMCR742', 'SIUL2_0_IMCR743', 'SIUL2_0_IMCR744', 'SIUL2_0_IMCR745', 'SIUL2_0_IMCR746', 'SIUL2_0_IMCR747', 'SIUL2_0_IMCR748', 'SIUL2_0_IMCR749', 'SIUL2_0_IMCR750', 'SIUL2_0_IMCR751', 'SIUL2_0_IMCR752', 'SIUL2_0_IMCR753', 'SIUL2_0_IMCR754', 'SIUL2_0_IMCR755', 'SIUL2_0_IMCR756', 'SIUL2_0_IMCR757', 'SIUL2_0_IMCR758', 'SIUL2_0_IMCR759', 'SIUL2_0_IMCR760', 'SIUL2_0_IMCR761', 'SIUL2_0_IMCR762', 'SIUL2_0_IMCR763', 'SIUL2_0_IMCR764', 'SIUL2_0_IMCR765', 'SIUL2_0_IMCR766', 'SIUL2_0_IMCR767', 'SIUL2_0_IMCR768', 'SIUL2_0_IMCR769', 'SIUL2_0_IMCR770', 'SIUL2_0_IMCR771', 'SIUL2_0_IMCR772', 'SIUL2_0_IMCR773', 'SIUL2_0_IMCR774', 'SIUL2_0_IMCR775', 'SIUL2_0_IMCR776', 'SIUL2_0_IMCR777', 'SIUL2_0_IMCR778', 'SIUL2_0_IMCR779', 'S…

Property	Value

4.119 Parameter ImcrNumber

Seclect pad number

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	65535
min	0

4.120 Parameter ImcrSiul2Instance

Select SIUL2 Instance

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SIUL2_0
literals	['SIUL2_0']

4.121 Parameter ImcrInput

Input signal controlled by IMCR

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	CAN0_RX

4.122 Parameter ImcrPad

Input pad controlled by IMCR

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	PTC2

4.123 Parameter ImcrMirror

Select SIUL2 Mirror

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	Xrdc_0_SIUL2_VIRTWRAPPER_PDAC0_HSE_B_0
literals	['Xrdc_0_SIUL2_VIRTWRAPPER_PDAC0_HSE_B_0', 'Xrdc_0_SIUL2_↩ VIRTWRAPPER_PDAC0_HSE_B_1', 'Xrdc_0_SIUL2_VIRTWRAPPER↩ _PDAC1_M7_0_0', 'Xrdc_0_SIUL2_VIRTWRAPPER_PDAC1_M7_0_1', 'Xrdc_0_SIUL2_VIRTWRAPPER_PDAC2_M7_1_0', 'Xrdc_0_SIUL2_VI↩ RTWRAPPER_PDAC2_M7_1_1', 'Xrdc_0_SIUL2_VIRTWRAPPER_PD↩ AC3']

4.124 Container Other_Config_List

Vendor specific:

All data need to configure Peripheral for one Domain.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.125 Parameter OtherName

Select input register

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	Siul2_0_IntCtrl
literals	['Siul2_0_IntCtrl']

4.126 Parameter OtherNumber

Seclect pad number

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	65535
min	0

4.127 Parameter OthersSiul2Instance

Select SIUL2 Instance

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SIUL2_0
literals	['SIUL2_0']

4.128 Parameter OtherInput

Registers controlled

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	InterruptRegisters

4.129 Parameter OtherMirror

Select SIUL2 Mirror

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A

Property	Value
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	Xrdc_0_SIUL2_VIRTWRAPPER_PDAC0_HSE_B_0
literals	['Xrdc_0_SIUL2_VIRTWRAPPER_PDAC0_HSE_B_0', 'Xrdc_0_SIUL2_↩ VIRTWRAPPER_PDAC0_HSE_B_1', 'Xrdc_0_SIUL2_VIRTWRAPPER↩ _PDAC1_M7_0_0', 'Xrdc_0_SIUL2_VIRTWRAPPER_PDAC1_M7_0_1', 'Xrdc_0_SIUL2_VIRTWRAPPER_PDAC2_M7_1_0', 'Xrdc_0_SIUL2_VI↩ RTWRAPPER_PDAC2_M7_1_1', 'Xrdc_0_SIUL2_VIRTWRAPPER_PD↩ AC3']

4.130 Container Dma_Mux_Configuration

The Direct Memory Access Multiplexer (DMAMUX) routes DMA sources configuration.

Included subcontainers:

- Dma_Mux_Module_Config

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.131 Parameter Dma_Mux_DevErrorDetect

Dma_Mux_DevErrorDetect

Switches the Development Error Detection and Notification ON or OFF.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.132 Container Dma_Mux_Module_Config

DMA MUX configuration.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD

4.133 Parameter Dma_Mux_HwInstance

Vendor specific:

Select the Hardware DMA Instance.

NOTE: This is an Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A

Property	Value
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DMA_INSTANCE_0
literals	['DMA_INSTANCE_0']

4.134 Parameter Dma_Mux_HwChannel

Vendor specific:

Select the physical eDMA Channel.

NOTE: This is an Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DMA_CHANNEL_0
literals	['DMA_CHANNEL_0', 'DMA_CHANNEL_1', 'DMA_CHANNEL_2', 'DM↩ A_CHANNEL_3', 'DMA_CHANNEL_4', 'DMA_CHANNEL_5', 'DMA_C↩ HANNEL_6', 'DMA_CHANNEL_7', 'DMA_CHANNEL_8', 'DMA_CHAN↩ NEL_9', 'DMA_CHANNEL_10', 'DMA_CHANNEL_11', 'DMA_CHANNE↩ L_12', 'DMA_CHANNEL_13', 'DMA_CHANNEL_14', 'DMA_CHANNEL↩ _15', 'DMA_CHANNEL_16', 'DMA_CHANNEL_17', 'DMA_CHANNEL_↩ 18', 'DMA_CHANNEL_19', 'DMA_CHANNEL_20', 'DMA_CHANNEL_21', 'DMA_CHANNEL_22', 'DMA_CHANNEL_23', 'DMA_CHANNEL_24', 'D↩ MA_CHANNEL_25', 'DMA_CHANNEL_26', 'DMA_CHANNEL_27', 'DM↩ A_CHANNEL_28', 'DMA_CHANNEL_29', 'DMA_CHANNEL_30', 'DMA↩ _CHANNEL_31']

4.135 Parameter Dma_Mux_Enable_Trigger

Enables the periodic trigger capability for the triggered DMA channel.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.136 Parameter Dma_Mux_Source0

Dma Mux Source

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DMA_MUX_0_REQ_DISABLED

Property	Value
literals	['DMA_MUX_0_REQ_DISABLED', 'DMA_MUX_0_SIUL2_0', 'DMA_MUX_0_SIUL2_1', 'DMA_MUX_0_SIUL2_2', 'DMA_MUX_0_SIUL2_3', 'DMA_MUX_0_SIUL2_4', 'DMA_MUX_0_SIUL2_5', 'DMA_MUX_0_SIUL2_6', 'DMA_MUX_0_SIUL2_7', 'DMA_MUX_0_BCTU_FIFO1_REQUEST', 'DMA_MUX_0_BCTU_0', 'DMA_MUX_0_BCTU_1', 'DMA_MUX_0_EMIOS_0_0', 'DMA_MUX_0_EMIOS_0_1', 'DMA_MUX_0_EMIOS_0_9', 'DMA_MUX_0_EMIOS_0_10', 'DMA_MUX_0_EMIOS_1_0', 'DMA_MUX_0_EMIOS_1_1', 'DMA_MUX_0_EMIOS_1_9', 'DMA_MUX_0_EMIOS_1_10', 'DMA_MUX_0_EMIOS_2_0', 'DMA_MUX_0_EMIOS_2_1', 'DMA_MUX_0_EMIOS_2_9', 'DMA_MUX_0_EMIOS_2_10', 'DMA_MUX_0_LCU_0_0', 'DMA_MUX_0_LCU_1_0', 'DMA_MUX_0_FLEXCAN_0_REQUEST', 'DMA_MUX_0_FLEXCAN_1_REQUEST', 'DMA_MUX_0_FLEXCAN_2_REQUEST', 'DMA_MUX_0_FLEXCAN_3_REQUEST', 'DMA_MUX_0_FLEXIO_SHIFTER0', 'DMA_MUX_0_FLEXIO_TIMER0', 'DMA_MUX_0_FLEXIO_SHIFTER1', 'DMA_MUX_0_FLEXIO_TIMER1', 'DMA_MUX_0_FLEXIO_SHIFTER2', 'DMA_MUX_0_FLEXIO_TIMER2', 'DMA_MUX_0_FLEXIO_SHIFTER3', 'DMA_MUX_0_FLEXIO_TIMER3', 'DMA_MUX_0_LPUART_0_TRANSMIT', 'DMA_MUX_0_LPUART_8_TRANSMIT', 'DMA_MUX_0_LPUART_0_RECEIVE', 'DMA_MUX_0_LPUART_8_RECEIVE', 'DMA_MUX_0_LPUART_1_TRANSMIT', 'DMA_MUX_0_LPUART_9_TRANSMIT', 'DMA_MUX_0_LPUART_1_RECEIVE', 'DMA_MUX_0_LPUART_9_RECEIVE', 'DMA_MUX_0_LPI2C0_RX_REQUEST', 'DMA_MUX_0_LPI2C0_RX_SLAVE_REQUEST', 'DMA_MUX_0_LPI2C0_TX_REQUEST', 'DMA_MUX_0_LPI2C0_TX_SLAVE_REQUEST', 'DMA_MUX_0_LPSPI_0_TX_REQUEST', 'DMA_MUX_0_LPSPI_0_RX_REQUEST', 'DMA_MUX_0_LPSPI_1_TX_REQUEST', 'DMA_MUX_0_LPSPI_1_RX_REQUEST', 'DMA_MUX_0_LPSPI_2_TX_REQUEST', 'DMA_MUX_0_LPSPI_2_RX_REQUEST', 'DMA_MUX_0_LPSPI_3_TX_REQUEST', 'DMA_MUX_0_LPSPI_3_RX_REQUEST', 'DMA_MUX_0_QSPI_RX_BUFFER_DRAIN', 'DMA_MUX_0_QSPI_TX_BUFFER_FILL', 'DMA_MUX_0_SAI_0_RECEIVE_REQUEST', 'DMA_MUX_0_SAI_0_TRANSMIT_REQUEST', 'DMA_MUX_0_USDHC_DMA_REQUEST', 'DMA_MUX_0_ADC_0_REQUEST', 'DMA_MUX_0_ADC_1_REQUEST', 'DMA_MUX_0_ADC_2_REQUEST', 'DMA_MUX_0_LPCMP_0_COUT_REQUEST', 'DMA_MUX_0_REQ_ALWAYS_ON_0', 'DMA_MUX_0_REQ_ALWAYS_ON_1']

4.137 Parameter Dma_Mux_Source1

Physical Core ID

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DMA_MUX_1_REQ_DISABLED
literals	['DMA_MUX_1_REQ_DISABLED', 'DMA_MUX_1_SIUL2_8', 'DMA_MUX_1_SIUL2_9', 'DMA_MUX_1_SIUL2_10', 'DMA_MUX_1_SIUL2_11', 'DMA_MUX_1_SIUL2_12', 'DMA_MUX_1_SIUL2_13', 'DMA_MUX_1_SIUL2_14', 'DMA_MUX_1_SIUL2_15', 'DMA_MUX_1_BCTU_FIFO2_REQUEST', 'DMA_MUX_1_BCTU_2', 'DMA_MUX_1_EMIOS_0_16', 'DMA_MUX_1_EMIOS_0_17', 'DMA_MUX_1_EMIOS_0_18', 'DMA_MUX_1_EMIOS_0_19', 'DMA_MUX_1_EMIOS_1_16', 'DMA_MUX_1_EMIOS_1_17', 'DMA_MUX_1_EMIOS_1_18', 'DMA_MUX_1_EMIOS_1_19', 'DMA_MUX_1_EMIOS_2_16', 'DMA_MUX_1_EMIOS_2_17', 'DMA_MUX_1_EMIOS_2_18', 'DMA_MUX_1_EMIOS_2_19', 'DMA_MUX_1_LCU_0_1', 'DMA_MUX_1_LCU_0_2', 'DMA_MUX_1_LCU_1_1', 'DMA_MUX_1_LCU_1_2', 'DMA_MUX_1_GMAC_0_PTP_TIMER_CH0', 'DMA_MUX_1_GMAC_0_PTP_TIMER_CH1', 'DMA_MUX_1_FLEXCAN_4_REQUEST', 'DMA_MUX_1_FLEXCAN_5_REQUEST', 'DMA_MUX_1_FLEXCAN_6_REQUEST', 'DMA_MUX_1_FLEXCAN_7_REQUEST', 'DMA_MUX_1_FLEXIO_SHIFTER4', 'DMA_MUX_1_FLEXIO_TIMER4', 'DMA_MUX_1_FLEXIO_SHIFTER5', 'DMA_MUX_1_FLEXIO_TIMER5', 'DMA_MUX_1_FLEXIO_SHIFTER6', 'DMA_MUX_1_FLEXIO_TIMER6', 'DMA_MUX_1_FLEXIO_SHIFTER7', 'DMA_MUX_1_FLEXIO_TIMER7', 'DMA_MUX_1_LPUART_2_TRANSMIT', 'DMA_MUX_1_LPUART_10_TRANSMIT', 'DMA_MUX_1_LPUART_2_RECEIVE', 'DMA_MUX_1_LPUART_10_RECEIVE', 'DMA_MUX_1_LPUART_3_TRANSMIT', 'DMA_MUX_1_LPUART_11_TRANSMIT', 'DMA_MUX_1_LPUART_3_RECEIVE', 'DMA_MUX_1_LPUART_11_RECEIVE', 'DMA_MUX_1_LPUART_4_TRANSMIT', 'DMA_MUX_1_LPUART_12_TRANSMIT', 'DMA_MUX_1_LPUART_4_RECEIVE', 'DMA_MUX_1_LPUART_12_RECEIVE', 'DMA_MUX_1_LPUART_5_TRANSMIT', 'DMA_MUX_1_LPUART_13_TRANSMIT', 'DMA_MUX_1_LPUART_5_RECEIVE', 'DMA_MUX_1_LPUART_13_RECEIVE', 'DMA_MUX_1_LPUART_6_TRANSMIT', 'DMA_MUX_1_LPUART_14_TRANSMIT', 'DMA_MUX_1_LPUART_6_RECEIVE', 'DMA_MUX_1_LPUART_14_RECEIVE', 'DMA_MUX_1_LPUART_7_TRANSMIT', 'DMA_MUX_1_LPUART_15_TRANSMIT', 'DMA_MUX_1_LPUART_7_RECEIVE', 'DMA_MUX_1_LPUART_15_RECEIVE', 'DMA_MUX_1_LPI2C1_RX_REQUEST', 'DMA_MUX_1_LPI2C1_RX_SLAVE_REQUEST', 'DMA_MUX_1_LPI2C1_TX_REQUEST', 'DMA_MUX_1_LPI2C1_TX_SLAVE_REQUEST', 'DMA_MUX_1_LPSPI_4_TX_REQUEST', 'DMA_MUX_1_LPSPI_4_RX_REQUEST', 'DMA_MUX_1_LPSPI_5_TX_REQUEST', 'DMA_MUX_1_LPSPI_5_RX_REQUEST', 'DMA_MUX_1_SAI_1_RECEIVE_REQUEST', 'DMA_MUX_1_SAI_1_TRANSMIT_REQUEST', 'DMA_MUX_1_GMAC_0_PTP_TIMER_CH2', 'DMA_MUX_1_GMAC_0_PTP_TIMER_CH3', 'DMA_MUX_1_LPCMP_1_COUT_REQUEST', 'DMA_MUX_1_LPCMP_2_COUT_REQUEST', 'DMA_MUX_1_REQ_ALWAYS_ON_0', 'DMA_MUX_1_REQ_ALWAYS_ON_1']

4.138 Parameter Dma_Mux_Source2

Physical Core ID

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NOT_USED
literals	['NOT_USED']

4.139 Parameter Dma_Mux_Source3

Physical Core ID

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NOT_USED
literals	['NOT_USED']

4.140 Container Mscm_Configuration

Routing configuration for the interrupts.

Included subcontainers:

- MscmConfig

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.141 Parameter MscmDevErrorDetect

MscmDevErrorDetect

Switches the Development Error Detection and Notification ON or OFF.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.142 Container MscmConfig

Vendor specific:

Configuration for interrupt requests.

Warning: This is a precompile configuration.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	174
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.143 Parameter IsrName

Vendor specific:

Interrupt Name.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	MSCM_CPU_TO_CPU_INT0

Property	Value
literals	['MSCM_CPU_TO_CPU_INT0', 'MSCM_CPU_TO_CPU_INT1', 'MSCM_CPU_TO_CPU_INT2', 'MSCM_CPU_TO_CPU_INT3', 'MSCM_DMA_TCD_0', 'MSCM_DMA_TCD_1', 'MSCM_DMA_TCD_2', 'MSCM_DMA_TCD_3', 'MSCM_DMA_TCD_4', 'MSCM_DMA_TCD_5', 'MSCM_DMA_TCD_6', 'MSCM_DMA_TCD_7', 'MSCM_DMA_TCD_8', 'MSCM_DMA_TCD_9', 'MSCM_DMA_TCD_10', 'MSCM_DMA_TCD_11', 'MSCM_DMA_TCD_12', 'MSCM_DMA_TCD_13', 'MSCM_DMA_TCD_14', 'MSCM_DMA_TCD_15', 'MSCM_DMA_TCD_16', 'MSCM_DMA_TCD_17', 'MSCM_DMA_TCD_18', 'MSCM_DMA_TCD_19', 'MSCM_DMA_TCD_20', 'MSCM_DMA_TCD_21', 'MSCM_DMA_TCD_22', 'MSCM_DMA_TCD_23', 'MSCM_DMA_TCD_24', 'MSCM_DMA_TCD_25', 'MSCM_DMA_TCD_26', 'MSCM_DMA_TCD_27', 'MSCM_DMA_TCD_28', 'MSCM_DMA_TCD_29', 'MSCM_DMA_TCD_30', 'MSCM_DMA_TCD_31', 'MSCM_ERROR_REPORTING_SINGLE_BIT_ECC', 'MSCM_ERROR_REPORTING_MULTI_BIT_ECC', 'MSCM_MCM', 'MSCM_SYSTEM_TIMER_MODULE_0', 'MSCM_SYSTEM_TIMER_MODULE_1', 'MSCM_SYSTEM_TIMER_MODULE_2', 'MSCM_WATCHDOG_0', 'MSCM_WATCHDOG_1', 'MSCM_CTI_INTERRUPT_0', 'MSCM_CTI_INTERRUPT_1', 'MSCM_FLASH_PROGRAM_OR_ERASE_COMPLETED', 'MSCM_FLASH_MAIN_WATCHDOG_TIMEOUT_INTERRUPT', 'MSCM_FLASH_ALTERNATE_WATCHDOG_TIMEOUT_INTERRUPT', 'MSCM_RESET_GENERATION_MODULE', 'MSCM_PMC', 'MSCM_SIUL_IRQ0', 'MSCM_SIUL_IRQ1', 'MSCM_SIUL_IRQ2', 'MSCM_SIUL_IRQ3', 'MSCM_EMIOS_0_INTERRUPT_REQUEST_23', 'MSCM_EMIOS_0_INTERRUPT_REQUEST_19', 'MSCM_EMIOS_0_INTERRUPT_REQUEST_15', 'MSCM_EMIOS_0_INTERRUPT_REQUEST_11', 'MSCM_EMIOS_0_INTERRUPT_REQUEST_7', 'MSCM_EMIOS_0_INTERRUPT_REQUEST_3', 'MSCM_EMIOS_1_INTERRUPT_REQUEST_23', 'MSCM_EMIOS_1_INTERRUPT_REQUEST_19', 'MSCM_EMIOS_1_INTERRUPT_REQUEST_15', 'MSCM_EMIOS_1_INTERRUPT_REQUEST_11', 'MSCM_EMIOS_1_INTERRUPT_REQUEST_7', 'MSCM_EMIOS_1_INTERRUPT_REQUEST_3', 'MSCM_EMIOS_2_INTERRUPT_REQUEST_23', 'MSCM_EMIOS_2_INTERRUPT_REQUEST_19', 'MSCM_EMIOS_2_INTERRUPT_REQUEST_15', 'MSCM_EMIOS_2_INTERRUPT_REQUEST_11', 'MSCM_EMIOS_2_INTERRUPT_REQUEST_7', 'MSCM_EMIOS_2_INTERRUPT_REQUEST_3', 'MSCM_WAKEUP_UNIT', 'MSCM_CMU_0', 'MSCM_CMU_1', 'MSCM_CMU_2', 'MSCM_BODY_CROSS_TRIGGERING_UNIT', 'MSCM_LOGIC_CONTROL_UNIT_0', 'MSCM_LOGIC_CONTROL_UNIT_1', 'MSCM_PIT_0', 'MSCM_PIT_1', 'MSCM_PIT_2', 'MSCM_RTC', 'MSCM_FLEXCAN0_0', 'MSCM_FLEXCAN0_1', 'MSCM_FLEXCAN0_2', 'MSCM_FLEXCAN0_3', 'MSCM_FLEXCAN1_0', 'MSCM_FLEXCAN1_1', 'MSCM_FLEXCAN1_2', 'MSCM_FLEXCAN2_0', 'MSCM_FLEXCAN2_1', 'MSCM_FLEXCAN2_2', 'MSCM_FLEXCAN3_0', 'MSCM_FLEXCAN3_1', 'MSCM_FLEXCAN4_0', 'MSCM_FLEXCAN4_1', 'MSCM_FLEXCAN5_0', 'MSCM_FLEXCAN5_1', 'MSCM_FLEXCAN6_0', 'MSCM_FLEXCAN6_1', 'MSCM_FLEXCAN7_0', 'MSCM_FLEXCAN7_1', 'MSCM_FLEXCAN1_3', 'MSCM_FLEXCAN2_3', 'MSCM_FLEXCAN3_2', 'MSCM_FLEXCAN4_2', 'MSCM_FLEXCAN5_2', 'MSCM_FLEXCAN6_2', 'MSCM_FLEXCAN7_2', 'MSCM_FLEXIBLE_IO', 'MSCM_LPUART_0', 'MSCM_LPUART_1', 'MSCM_LPUART_2', 'MSCM_LPUART_3', 'MSCM_LPUART_4', 'MSCM_LPUART_5', 'MSCM_LPUART_6', 'MSCM_LPUART_7', 'MSCM_LPUART_8', 'MSCM_LPUART_9', 'MSCM_LPUART_10', 'MSCM_LPUART_11', 'MSCM_LPUART_12', 'MSCM_LPUART_13', 'MSCM_LPUART_14', 'MSCM_LPUART_15', 'MSCM_LPI2C_0_MASTER_INTERRUPT', 'MSCM_LPI2C_1_MASTER_INTERRUPT', 'MSCM_LPSPI_0', 'MSCM_LPSPI_1', 'MSCM_LPSPI_2', 'MSCM_LPSPI_3', 'MSCM_LPSPI_4', 'MSCM_LPSPI_5', 'MSCM_QSPI', 'MSCM_SYNCHRONOUS_AUDIO_INTERFACE_0', 'MSCM_SYNCHRONOUS_AUDIO_

Property	Value

4.144 Parameter IsrTargetCore0

Vendor specific:

Select the target core for the interrupt request. Parameter is readonly if this target core is not available.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.145 Parameter IsrTargetCore1

Vendor specific:

Select the target core for the interrupt request. Parameter is readonly if this target core is not available.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.146 Parameter IsrTargetCore2

Vendor specific:

Select the target core for the interrupt request. Parameter is readonly if this target core is not available.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.147 Parameter IsrTargetCore3

Vendor specific:

Select the target core for the interrupt request. Parameter is readonly if this target core is not available.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.148 Container CommonPublishedInformation

Vendor specific:

Common container, aggregated by all modules. It contains published information about vendor and versions.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.149 Parameter ArReleaseMajorVersion

Vendor specific:

Major version number of AUTOSAR specification on which the appropriate implementation is based on.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	4
max	4
min	4

4.150 Parameter ArReleaseMinorVersion

Vendor specific:

Minor version number of AUTOSAR specification on which the appropriate implementation is based on.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	7
max	7
min	7

4.151 Parameter ArReleaseRevisionVersion

Vendor specific:

Revision version number of AUTOSAR specification on which the appropriate implementation is based on.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	0
max	0
min	0

4.152 Parameter ModuleId

Vendor specific:

Module ID of this module from Module List.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	255
max	255
min	255

4.153 Parameter SwMajorVersion

Vendor specific:

Major version number of the vendor specific implementation of the module. The numbering is vendor specific.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	3
max	3
min	3

4.154 Parameter SwMinorVersion

Vendor specific:

Minor version number of the vendor specific implementation of the module. The numbering is vendor specific.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	0
max	0
min	0

4.155 Parameter SwPatchVersion

Vendor specific:

Patch level version number of the vendor specific implementation of the module. The numbering is vendor specific.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	0
max	0
min	0

4.156 Parameter VendorApiInfix

Vendor specific:

In driver modules which can be instantiated several times on a single ECU, BSW00347 requires

that the name of APIs is extended by the VendorId and a vendor specific name.

This parameter is used to specify the vendor specific name. In total, the

implementation specific name is generated as follows: <ModuleName>_>VendorId>_<VendorApiInfix>.

E.g. assuming that the VendorId of the implementor is 123 and the implementer chose a VendorApiInfix of "v11r456" a api name Can_Write defined in the SWS will translate to Can_123_v11r456Write.

This parameter is mandatory for all modules with upper multiplicity > 1. It shall not be used for modules with upper multiplicity =1.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	

4.157 Parameter VendorId

Vendor specific:

Vendor ID of the dedicated implementation of this module according to the AUTOSAR vendor list.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	43
max	43
min	43

Chapter 5

Module Index

5.1 Software Specification

Here is a list of all modules:

Chapter 6

Module Documentation

6.1 AXBS IPV Driver

6.1.1 Detailed Description

Data Structures

- struct Axbs_Ip_SlavePortConfigType

  Configuration structure for Slave ports. *More...*
- struct Axbs_Ip_ConfigType

  Configuration structure for Axbs Ip. *More...*

Types Reference

- typedef uint8 Axbs_Ip_PortNumberType
- typedef uint32 Axbs_Ip_InstanceNumberType
- typedef uint32 Axbs_Ip_PortPriorityType
- typedef uint32 Axbs_Ip_PortControlType
- typedef uint8 Axbs_Ip_CrossbarPortType

  Axbs port type.

6.1.2 Data Structure Documentation

6.1.2.1 struct Axbs_Ip_SlavePortConfigType

Configuration structure for Slave ports.

Definition at line 131 of file Axbs_Ip_Types.h.

Data Fields

Type	Name	Description
const Axbs_Ip_PortNumberType	Axbs_PortNumber	hardware slave port number
const Axbs_Ip_InstanceNumberType	Axbs_InstanceNumber	hardware instance
const Axbs_Ip_PortControlType	Axbs_PortControlConfig	port control config

6.1.2.2 struct Axbs_Ip_ConfigType

Configuration structure for Axbs Ip.

Definition at line 148 of file Axbs_Ip_Types.h.

Data Fields

Type	Name	Description
const Axbs_Ip_CrossbarPortType	AxbsCrossbarIpNumPorts	The number of slave port.
const Axbs_Ip_SlavePortConfigType(*const	pAxbsCrossbarSlaveHwIpConfig)[]	configuration of the crossbar IP for Slave

6.1.3 Types Reference

6.1.3.1 Axbs_Ip_PortNumberType

```
typedef uint8 Axbs_Ip_PortNumberType
```

Axbs port number type

Definition at line 107 of file Axbs_Ip_Types.h.

6.1.3.2 Axbs_Ip_InstanceNumberType

```
typedef uint32 Axbs_Ip_InstanceNumberType
```

Axbs instance number type

Definition at line 111 of file Axbs_Ip_Types.h.

6.1.3.3 Axbs_Ip_PortPriorityType

```
typedef uint32 Axbs_Ip_PortPriorityType
```

Axbs port priority config

Definition at line 115 of file Axbs_Ip_Types.h.

6.1.3.4 Axbs_Ip_PortControlType

```
typedef uint32 Axbs_Ip_PortControlType
```

Axbs port control type

Definition at line 119 of file Axbs_Ip_Types.h.

6.1.3.5 Axbs_Ip_CrossbarPortType

```
typedef uint8 Axbs_Ip_CrossbarPortType
```

Axbs port type.

Definition at line 123 of file Axbs_Ip_Types.h.

6.2 RM Driver

6.2.1 Detailed Description

Macros

- #define RM_STOP_SEC_CONFIG_DATA_UNSPECIFIED

Function Reference

- void Rm_Init (Rm_ConfigType const *ConfigPtr)
  This function initializes the RM hardware components.

6.2.2 Macro Definition Documentation

6.2.2.1 RM_STOP_SEC_CONFIG_DATA_UNSPECIFIED

```
#define RM_STOP_SEC_CONFIG_DATA_UNSPECIFIED
```

Export RM configurations.

Definition at line 116 of file CDD_Rm.h.

6.2.3 Function Reference

6.2.3.1 Rm_Init()

```
void Rm_Init (
            Rm_ConfigType const * ConfigPtr )
```

This function initializes the RM hardware components.

This service is a non reentrant function used for driver initialization. The Initialization function shall initialize all relevant registers of the configured hardware with the values of the structure referenced by the parameter Config↩ Ptr. If the hardware allows for only one usage of the register, the driver module implementing that functionality is responsible for initializing the register. The initialization function of this module shall always have a pointer as a parameter, even though for Variant PC no configuration set shall be given. Instead a NULL pointer shall be passed to the initialization function.

Parameters

in	*ConfigPtr*	Pointer to a selected configuration structure.

Returns

void

6.3 DMA_MUX IPV Driver

6.3.1 Detailed Description

Data Structures

- struct Dma_Mux_Ip_ChannelConfigType

  Configuration structure containing the channel configuration. *More...*
- struct Dma_Mux_Ip_ConfigType

  IP configuration structure. *More...*

6.3.2 Data Structure Documentation

6.3.2.1 struct Dma_Mux_Ip_ChannelConfigType

Configuration structure containing the channel configuration.

Definition at line 82 of file Dma_Mux_Ip_Types.h.

Data Fields

Type	Name	Description
uint8	Instance	Select the instance request source.
uint8	Channel	Select the channel request source.
uint8	ConfigValue	Configuration value for the channel.

6.3.2.2 struct Dma_Mux_Ip_ConfigType

IP configuration structure.

Definition at line 92 of file Dma_Mux_Ip_Types.h.

Data Fields

Type	Name	Description
uint8	ChannelConfigCnt	Channel Count
const Dma_Mux_Ip_ChannelConfigType *	pChannelConfigArr	Channel configuration array

6.4 Mscm IPV Driver

6.4.1 Detailed Description

Data Structures

- struct Mscm_Ip_IrqRouteConfigType

  Structure storing the configuration for interrupt Router. *More...*
- struct Mscm_Ip_ConfigType

  Structure storing the list of state configurations for interrupt Router. *More...*

6.4.2 Data Structure Documentation

6.4.2.1 struct Mscm_Ip_IrqRouteConfigType

Structure storing the configuration for interrupt Router.

Definition at line 72 of file Mscm_Ip_Types.h.

Data Fields

Type	Name	Description
uint16	u16IrqNumber	Interrupt number.
uint16	u16TargetCores	Target cores for the interrupt.

6.4.2.2 struct Mscm_Ip_ConfigType

Structure storing the list of state configurations for interrupt Router.

Definition at line 82 of file Mscm_Ip_Types.h.

Data Fields

Type	Name	Description
uint32	u32GlobalRouteConfigCount	Total of SPI interrupts routing.
const Mscm_Ip_IrqRouteConfigType *	aGlobalRouteConfig	List of interrupts routing configurations.

6.5 Pflash IPV Driver

6.5.1 Detailed Description

Data Structures

- struct Pflash_Ip_MasterProtectionType
  Structure containing the configuration of the Pflash Ip. More...
- struct Pflash_Ip_ConfigType
  Structure containing the configuration of the Pflash Ip. More...

Enum Reference

- enum Pflash_Ip_MasterAccessType
  Enumeration listing Pflash access type.

6.5.2 Data Structure Documentation

6.5.2.1 struct Pflash_Ip_MasterProtectionType

Structure containing the configuration of the Pflash Ip.

Definition at line 109 of file Pflash_Ip_Types.h.

Data Fields

Type	Name	Description
Pflash_Ip_MasterType	Pflash_Master	Pflash master access protection field
Pflash_Ip_MasterAccessType	Pflash_Access	Pflash access type

6.5.2.2 struct Pflash_Ip_ConfigType

Structure containing the configuration of the Pflash Ip.

Definition at line 118 of file Pflash_Ip_Types.h.

Data Fields

Type	Name	Description
const uint32	u32Pflash_MasterProtectionConfigCnt	Pflash Size of Master Protection configuration array
const Pflash_Ip_MasterProtectionType *	Pflash_MasterProtectionConfig	Pflash Master Protection configuration array

6.5.3 Enum Reference

6.5.3.1 Pflash_Ip_MasterAccessType

enum Pflash_Ip_MasterAccessType

Enumeration listing Pflash access type.

Definition at line 97 of file Pflash_Ip_Types.h.

6.6 Sema42 IPV Driver

6.6.1 Detailed Description

Enum Reference

- enum Sema42_Ip_StatusType
  Enumeration listing the possible return codes for Sema42 Ip driver.

6.6.2 Enum Reference

6.6.2.1 Sema42_Ip_StatusType

```
enum Sema42_Ip_StatusType
```

Enumeration listing the possible return codes for Sema42 Ip driver.

Enumerator

Sema42_Ip_Success	Operation successful
Sema42_Ip_Error	Operation resulted in error

Definition at line 86 of file Sema42_Ip_Types.h.

6.7 Virt Wrapper IPV Driver

6.7.1 Detailed Description

Data Structures

- struct Virt_Wrapper_Ip_RegConfigType
  Configuration structure containing the Pin configuration for virtual wrapper. More...
- struct Virt_Wrapper_Ip_ConfigType
  Configuration structure containing the Pin configuration for virtual wrapper. More...

Enum Reference

- enum Virt_Wrapper_Ip_SlotType
  Enumeration listing pad (MSCR or IMCR) slot in a single Virtual Wrapper Parameter_n Register.
- enum Virt_Wrapper_Ip_AccessType
  Enumeration listing which PDAC will be assigned to access by the pad.

6.7.2 Data Structure Documentation

6.7.2.1 struct Virt_Wrapper_Ip_RegConfigType

Configuration structure containing the Pin configuration for virtual wrapper.

Definition at line 141 of file Virt_Wrapper_Ip_Types.h.

6.7.2.2 struct Virt_Wrapper_Ip_ConfigType

Configuration structure containing the Pin configuration for virtual wrapper.

Definition at line 152 of file Virt_Wrapper_Ip_Types.h.

6.7.3 Enum Reference

6.7.3.1 Virt_Wrapper_Ip_SlotType

`enum Virt_Wrapper_Ip_SlotType`

Enumeration listing pad (MSCR or IMCR) slot in a single Virtual Wrapper Parameter_n Register.

Definition at line 106 of file Virt_Wrapper_Ip_Types.h.

6.7.3.2 Virt_Wrapper_Ip_AccessType

`enum Virt_Wrapper_Ip_AccessType`

Enumeration listing which PDAC will be assigned to access by the pad.

Definition at line 118 of file Virt_Wrapper_Ip_Types.h.

6.8 XBIC IPV Driver

6.8.1 Detailed Description

Data Structures

- struct Xbic_Ip_ErrorStatusType

  Structure for error informations of Xbic Ip. *More...*
- struct Xbic_Ip_ConfigType

  Configuration structure for Xbic Ip. *More...*

6.8.2 Data Structure Documentation

6.8.2.1 struct Xbic_Ip_ErrorStatusType

Structure for error informations of Xbic Ip.

Definition at line 100 of file Xbic_Ip_Types.h.

Data Fields

Type	Name	Description
boolean	bErrorStatusValid	No Error /Error detected—all fields of the ESR and EAR registers are valid
boolean	aDataPhaseSlavePortError[XBIC_IP_NUM_SLAVE]	Feedback integrity error detected on slave
boolean	aDataPhaseMasterPortError[XBIC_IP_NUM_MASTER]	Feedback integrity error detected on master
uint8	masterID	The logical master ID number of the bus master which requested the most recent transfer with an attribute integrity check error detected.
uint8	slavePort	Slave port targeted by the most recent transfer with an attribute integrity check error detected.
uint8	synError	Indicate which syndrome calculated for the most recent transfer with an attribute integrity check error detected
uint32	errAddressDetect	Indicate which address of the most recent transfer with an attribute integrity check error detected.

6.8.2.2 struct Xbic_Ip_ConfigType

Configuration structure for Xbic Ip.

Definition at line 114 of file Xbic_Ip_Types.h.

Data Fields

Type	Name	Description
uint32	u32XbicTurnCheckOnPerPort[XBIC_IP_INSTANCE_COUNT]	This will be write on XBIC Module Control Register(MCR):to turn attribute integrity checking and feedback integrity checking on or off on a per-port basis

6.9 XRDC IPV Driver

6.9.1 Detailed Description

Data Structures

- struct Xrdc_Ip_MemConfigType

  Configuration structure containing XRDC memory region configuration. *More...*
- struct Xrdc_Ip_PeripheralConfigType

  Configuration structure containing XRDC peripheral slot configuration. *More...*
- struct Xrdc_Ip_ErrorStatusType

  Structure used to retrieve violation details. *More...*
- struct Xrdc_Ip_DomainIDErrStatusType

  Structure used to retrieve information violation details and the domain ID where violation occured. *More...*
- struct Xrdc_Ip_DomainConfigType

  Configuration structure containing XRDC domain configuration. *More...*
- struct Xrdc_Ip_InstanceConfigType

  IP configuration structure. *More...*
- struct Xrdc_Ip_ConfigType

  IP configuration structure. *More...*

Enum Reference

- enum Xrdc_Ip_MDACInstanceType

  Enumeration listing MDAC instances.
- enum Xrdc_Ip_SecureAttributeType

  Enumeration listing secure attributes of a XRDC master.
- enum Xrdc_Ip_PriviledgedAttributeType

  Enumeration listing priviledge attributes of a XRDC master.
- enum Xrdc_Ip_PIDLockBit

  Enumeration listing of a PID lock registers.
- enum Xrdc_Ip_DomainIDType

  Enumeration listing XRDC domain IDs.
- enum Xrdc_Ip_MasterCoreType

  Enumeration listing XRDC master core.
- enum Xrdc_Ip_MasterType

  Enumeration listing XRDC masters type.
- enum Xrdc_Ip_ErrorStateType

  Enumeration listing states of access violations.
- enum Xrdc_Ip_ErrorAccessType

  Enumeration listing errors occurred on a read or write access.
- enum Xrdc_Ip_ErrorAttributeType

  Enumeration listing error attributes of access violations.

6.9.2 Data Structure Documentation

6.9.2.1 struct Xrdc_Ip_MemConfigType

Configuration structure containing XRDC memory region configuration.

Definition at line 308 of file Xrdc_Ip_Types.h.

Data Fields

Type	Name	Description
const uint32	u32XrdcMrcInstance	Corresponding MRC instance of current memory region.
const uint32	u32XrdcMrcRegionDescriptor	Selection of descriptor for current memory region.
const uint32	u32XrdcStartAddress	Start address of current memory region.
const uint32	u32XrdcEndAddress	End address of current memory region.
const uint32	u32XrdcSema4Enable	Enable or disable Semaphore support.
const uint32	u32XrdcSema4Number	Semaphore number used in access evaluation.
const uint32	u32XrdcMRGDLockBit	Enable or disable MRGD bit lock.
const uint32	u32XrdcMemPolicy	Access policy of current memory region.
const uint32	u32XrdcMemPolicy1	

6.9.2.2 struct Xrdc_Ip_PeripheralConfigType

Configuration structure containing XRDC peripheral slot configuration.

Definition at line 324 of file Xrdc_Ip_Types.h.

Data Fields

Type	Name	Description
const uint32	u32XrdcPdacInstance	Corresponding PDAC instance of current peripheral slot.
const uint32	u32XrdcSema4Enable	Enable or disable Semaphore support.
const uint32	u32XrdcSema4Number	Semaphore number used in access evaluation.
const uint32	u32XrdcPDACLockBit	Enable or disable PDAC bit lock.
const uint32	u32XrdcPerPolicy	Access policy of current peripheral slot.
const uint32	u32XrdcPerPolicy1	

6.9.2.3 struct Xrdc_Ip_ErrorStatusType

Structure used to retrieve violation details.

Definition at line 337 of file Xrdc_Ip_Types.h.

Data Fields

Type	Name	Description
uint32	u32AddError	Address of an access violation.
uint32	u32AddErrorRemain	
Xrdc_Ip_ErrorStateType	ErrState	State of access violations.
uint32	u32ErrPort	Port number of the MRC that detected the access violation.
Xrdc_Ip_ErrorAccessType	ErrAccess	Whether the captured access violation occurred on a read or write access.
Xrdc_Ip_ErrorAttributeType	ErrAttribute	Attributes of the access violation.

6.9.2.4 struct Xrdc_Ip_DomainIDErrStatusType

Structure used to retrieve information violation details and the domain ID where violation occured.

Definition at line 350 of file Xrdc_Ip_Types.h.

Data Fields

Type	Name	Description
Xrdc_Ip_DomainIDType	DomainIDAccessError	Domain ID of the access violation.
Xrdc_Ip_ErrorStatusType	ErrorStatus[XRDC_MAX_OF_ERROR_RECORDED]	Error status of the access violation.

6.9.2.5 struct Xrdc_Ip_DomainConfigType

Configuration structure containing XRDC domain configuration.

Definition at line 359 of file Xrdc_Ip_Types.h.

Data Fields

Type	Name	Description
Xrdc_Ip_DomainIDType	u32XrdcDomainID	XRDC domain ID.
Xrdc_Ip_MDACInstanceType	XrdcMdacInstance	Corresponding MDA instance of current master.
Xrdc_Ip_MasterType	XrdcCoreMdacInstance	Core or noncore attribute of current master.
const uint32	u32XrdcProcessID	PID value of curent domain ID.
const uint32	u32XrdcProcessIDMask	PIDM value of current domain ID.
const uint32	u32XrdcProcessIDEnable	Enable or disable PID support.
const uint32	u32XrdcThreeStateModel	If core master support three-state model or not.
const uint32	u32XrdcWordDescriptor	Selection of descriptor for current core master.

Data Fields

Type	Name	Description
const uint32	u32XrdcDIDBypassDisable	Enable or disable DID bypass.
const uint32	u32XrdcMDADFMTLockBit	Enable or disable MDA_DFMT bit lock.
Xrdc_Ip_SecureAttributeType	eXrdcSecureOutput	Secure attribute of current master.
Xrdc_Ip_PriviledgedAttributeType	eXrdcPriviledgeOutput	Priviledged attribute of current master.

6.9.2.6 struct Xrdc_Ip_InstanceConfigType

IP configuration structure.

Definition at line 381 of file Xrdc_Ip_Types.h.

Data Fields

Type	Name	Description
const uint32	u32XrdcInstance	XRDC instance.
const Xrdc_Ip_DomainConfigType *	pDomainConfig	Pointer to a list of configured domains.
const uint32	u32DomainConfigCnt	Number of configured domains.
const Xrdc_Ip_MemConfigType *	pMemoryDesConfig	Pointer to a list of configured memory regions.
const uint32	u32MemoryConfigCnt	Number of configured memory regions.
const Xrdc_Ip_PeripheralConfigType *	pPeripheralDescriptorConfig	Pointer to a list of configured peripheral slots.
const uint32	u32PeripheralConfigCnt	Number of configured peripheral slots.
const uint32	u32XrdcCRLockBit	Enable or disable CR bit lock.
Xrdc_Ip_PIDLockBit	XrdcPIDLockBit	Enable or disable CR bit lock.

6.9.2.7 struct Xrdc_Ip_ConfigType

IP configuration structure.

Definition at line 397 of file Xrdc_Ip_Types.h.

Data Fields

Type	Name	Description
const Xrdc_Ip_InstanceConfigType *const *const	pInstanceConfig	Pointer to a list of configured instances.
const uint32	u32InstanceConfigCnt	Number of configured instances.
const uint32 *const	pInstanceInUsed	Pointer to a list of configured XRDC instances.
const uint32	u32InstanceInUsedCnt	Number of configured XRDC instances.

6.9.3 Enum Reference

6.9.3.1 Xrdc_Ip_MDACInstanceType

enum Xrdc_Ip_MDACInstanceType

Enumeration listing MDAC instances.

Definition at line 148 of file Xrdc_Ip_Types.h.

6.9.3.2 Xrdc_Ip_SecureAttributeType

enum Xrdc_Ip_SecureAttributeType

Enumeration listing secure attributes of a XRDC master.

Definition at line 194 of file Xrdc_Ip_Types.h.

6.9.3.3 Xrdc_Ip_PriviledgedAttributeType

enum Xrdc_Ip_PriviledgedAttributeType

Enumeration listing priviledge attributes of a XRDC master.

Definition at line 204 of file Xrdc_Ip_Types.h.

6.9.3.4 Xrdc_Ip_PIDLockBit

enum Xrdc_Ip_PIDLockBit

Enumeration listing of a PID lock registers.

Definition at line 214 of file Xrdc_Ip_Types.h.

6.9.3.5 Xrdc_Ip_DomainIDType

enum Xrdc_Ip_DomainIDType

Enumeration listing XRDC domain IDs.

Definition at line 224 of file Xrdc_Ip_Types.h.

6.9.3.6 Xrdc_Ip_MasterCoreType

enum Xrdc_Ip_MasterCoreType

Enumeration listing XRDC master core.

most significant byte is XRDC instance. least significant byte is Master core number. Ex: 0x110 - XRDC instance 1, Master core number 16.

Definition at line 251 of file Xrdc_Ip_Types.h.

6.9.3.7 Xrdc_Ip_MasterType

enum Xrdc_Ip_MasterType

Enumeration listing XRDC masters type.

Definition at line 260 of file Xrdc_Ip_Types.h.

6.9.3.8 Xrdc_Ip_ErrorStateType

enum Xrdc_Ip_ErrorStateType

Enumeration listing states of access violations.

Definition at line 270 of file Xrdc_Ip_Types.h.

6.9.3.9 Xrdc_Ip_ErrorAccessType

enum Xrdc_Ip_ErrorAccessType

Enumeration listing errors occurred on a read or write access.

Definition at line 280 of file Xrdc_Ip_Types.h.

6.9.3.10 Xrdc_Ip_ErrorAttributeType

enum Xrdc_Ip_ErrorAttributeType

Enumeration listing error attributes of access violations.

Definition at line 290 of file Xrdc_Ip_Types.h.

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