4DM4 Assignment 1 RISC Scheduling of the Chacha20 Stream Cipher

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Part A

A1

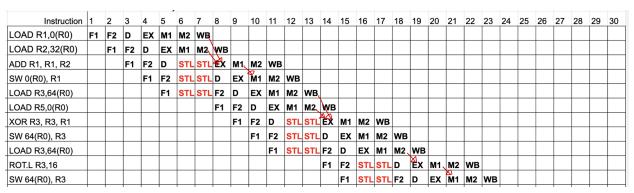
				Cloc	ck Cy	cle					
Instruction	1	2	3	4	5	6	7	8	9	10	•
LW R2,0(R0)	F1	F2	D	EX	M1	M2	WB				L
ADD R2, R2, R3		F1	F2	D	STL	STL	EX	М1	M2	WB	
											П

A2

				Cloc	k Cy	/cle						
Instruction	1	2	3	4	5	6	7	8	9	10	11	12
BNEZ, R0, loop	F1	F2	D	EX	М1	M2	WB					
NO-OP		F1	F2	D	EX	M1	M2	WB				
NO-OP			F1	. 2	D	EX	М1	M2	WB			
Next Iteration, LD				F1	F2	D	EX	M1	M2	WB		
Case2												
ADD R0,R0,R31	F1	F2	D	EX	M1	M2	WB					
BNEZ, R0, loop		F1	F2	STL	D	EX	M1	M2	WB			
NO-OP			F1	STL	D	EX	М1	M2	WB			
NO-OP					F1	F ₂	D	EX	M1	M2	WB	
Next Iteration, LD						F1	F2	D	EX	M1	M2	WE

Part B

B1



Instruction	Number of Stalls	Comments
LOAD R1,0(R0)	0	Loading 'a' into register R1 from address 0+R0
LOAD R2,32(R0)		Loading 'b' into register R2 from address 32+R0
ADD R1, R1, R2		Adding 'a' to 'b' and storing the result back to R1
SW 0(R0), R1		Saving 'a' into adress 0+R0
LOAD R3,64(R0)		Loading 'd' into register R3 from address 64+R0
LOAD R4,0(R0)	_	Loading 'a' into register R4 from address 0+R0
XOR R3, R3, R4		XORing 'a' to 'd' and storing the result back to R3
SW 64(R0), R3		Saving 'd' into adress 64+R0
LOAD R5,64(R0)		Loading 'd' into register R5 from address 64+R0
ROT.L R5,16	2	Performing a cyclic bit shift on 'd' by 16 bits
SW 64(R0), R5	2	Saving 'd' into adress 64+R0
() ()		End of first quarter round
LOAD R1,96(R0)	0	Loading 'c' into register R1 from address 96+R0
LOAD R2,64(R0)		Loading 'd' into register R2 from address 64+R0
ADD R1, R1, R2		Adding 'c' to 'd' and storing the result back to R1
SW 96(R0), R1	2	
LOAD R3,32(R0)	2	Loading 'b' into register R3 from address 32+R0
LOAD R4,96(R0)		Loading 'c' into register R4 from address 96+R0
XOR R3, R3, R4		XORing 'b' to 'c' and storing the result back to R3
SW 32(R0), R3		Saving 'b' into adress 32+R0
LOAD R5,32(R0)	2	Loading 'b' into register R5 from address 32+R0
ROT.L R5,12	2	Performing a cyclic bit shift on 'b' by 12 bits
SW 32(R0), R5	2	Saving 'b' into adress 32+R0
077 02(170), 170		End of second quarter round
LOAD R1,0(R0)	0	Loading 'a' into register R1 from address 0+R0
LOAD R2,32(R0)		Loading 'b' into register R2 from address 32+R0
ADD R1, R1, R2		Adding 'a' to 'b' and storing the result back to R1
SW 0(R0), R1	2	
LOAD R3,64(R0)		Loading 'd' into register R3 from address 64+R0
LOAD R4,0(R0)		Loading 'a' into register R4 from address 0+R0
XOR R3, R3, R4		XORing 'a' to 'd' and storing the result back to R3
SW 64(R0), R3	2	Saving 'd' into adress 64+R0
LOAD R5,64(R0)	2	Loading 'd' into register R5 from address 64+R0
ROT.L R5,16		Performing a cyclic bit shift on 'd' by 16 bits
SW 64(R0), R5	2	Saving 'd' into adress 64+R0
OVV 0+(1\0), 1\0		End of third quarter round
LOAD R1,96(R0)	0	Loading 'c' into register R1 from address 96+R0
LOAD R2,64(R0)		Loading 'd' into register R2 from address 64+R0
ADD R1, R1, R2		Adding 'c' to 'd' and storing the result back to R1
SW 96(R0), R1		Saving 'c' into adress 96+R0
LOAD R3,32(R0)		Loading 'b' into register R3 from address 32+R0
LOAD R4,96(R0)		Loading 'c' into register R4 from address 96+R0
XOR R3, R3, R4		XORing 'b' to 'c' and storing the result back to R3
SW 32(R0), R3	2	Saving 'b' into adress 32+R0
LOAD R5,32(R0)	2	Loading th' into register BE from address 33 : BO
ROT.L R5,12	2	Loading 'b' into register R5 from address 32+R0
	2	Performing a cyclic bit shift on 'b' by 12 bits
SW 32(R0), R5		Saving 'b' into adress 32+R0 End of fourth quarter round

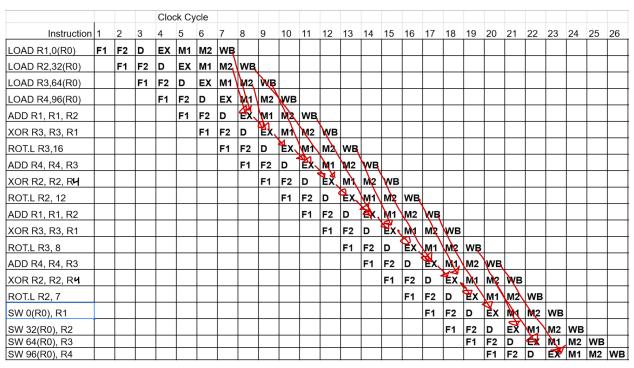
B3

It takes **92 clock cycles** to complete the quarter round operation of the Chacha20 stream cipher. The number of clock cycles is calculated by adding the number of clock cycles required to complete each of the four operations in the quarter round. Since one of the operations takes 23 clock cycles, the total number of clock cycles is 23 + 23 + 23 + 23 = 92.

B4

Assumptions

- Assume 'a' is in R2
- Assume 'b' is in R31
- Assume 'd' is in R30



As seen in the above table, it takes **26 clock cycles** to complete the quarter round operation. The number of clock cycles is calculated by adding the number of clock cycles required to complete each of the four operations in the quarter round, the loading and saving.

B5

Block of Code	Clock Cycles	Comment
Optimized Quarter Round code block from B4. A, B, D, C are loaded at the beginning of the round,		A, B, D, C are words in the first column
and are manipulated as need. Unlike in B4, they are not saved in this round. Words E, F, H, G are	Clock Cycles:26 Stall Cycles: 0	E, F, H, G are words in the second column
then loaded QR (0(R0),16(R0),32(R0),48(R0))	,	
Optimized Quarter Round code where E, F, H, G are manipulated as need. They are not saved in this round. Words I, J, L, K are then loaded QR (4(R0),20(R0),36(R0),52(R0))	Clock Cycles:22 Stall Cycles: 0	I, J, L, K are words in the third column
Optimized Quarter Round code where I, J, L, K are manipulated as need. They are not saved in this round. Words M, N, P, O are then loaded QR (8(R0),24(R0),40(R0),56(R0))	Clock Cycles:22 Stall Cycles: 0	M, N, P, O are words in the fourth column
Optimized Quarter Round code where M, N, P, O are manipulated as need. At the end of this round, all previous words (A-O) are saved to the alloted memory locations QR (12(R0),28(R0),44(R0),60(R0))	Clock Cycles:28 Stall Cycles: 0	The addresses which these words are stored too are the same ones from the previous rounds, which the words are initially read from to avoid confusion and misplacement

98 clock cycles. 0 stalls.

B6

Stall Cycles	Comment
0	Beginning of the outer loop, setting a counter to run 1023 times
0	Beginning of the inner loop, setting a counter to run 10 times
0	Using columns of the key-stream block
0	Using diagonals of the key-stream block
2*10 = 20	Ending of the inner loop. 2 stalls per loop cycle from NO-OP's
2*1024 = 2048	Ending of the outer loop. 2 stalls per loop cycle from NO-OP's
	0 0 0 0 0 2*10 = 20

Total clock cycles: 2131988

B7

Instruction Clock Cycles

104 CC - = quarter round

208 (C - quarter round

2080 CC - double round

2080 CC ×1024 - 1024 blocks

= 2129920 CC

Stall clock Cycks

2x10 - inner loop

+2 x 1024 - onter 100P

= 2068

Total CC= 2131988

2.5 G-Hz

=2.5 × 109 CC

1 second

2129920 CC x 1 Second 2.5 x 10 1 2C

- 8.52(x10-4 = 85.28 x10-3 sec = 85.2) ms