4DM4 Assignment 2 Advanced Static Pipelining

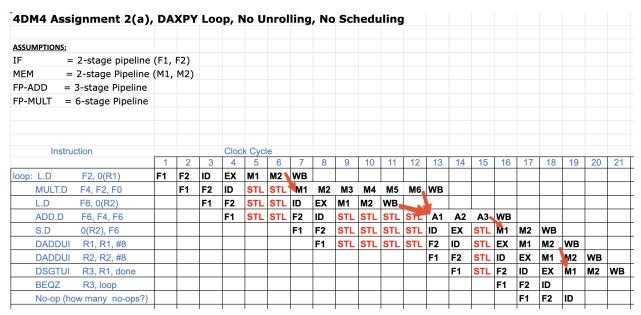
Ashpan Raskar raskara 400185326 Ahnaf Bhuiyan bhuiya3 400198359

November 9, 2022

Contents

Part (a): DAXPY Loop, No Unrolling, with No Scheduling	2
Part (b): DAXPY Loop, No Unrolling, with Scheduling	2
Part (c): DAXPY Loop, with Unrolling, with No Scheduling	3
Part (d): DAXPY Loop, with Unrolling, with Scheduling	4
Part (e): DAXPY Loop, with Unrolling, with Scheduling. On Dual-Issue	4

Part (a): DAXPY Loop, No Unrolling, with No Scheduling



Each iteration of this loop takes 23 clock cycles. The given clock speed is 3 GHz. The following equation can be used to calculate the MFLOP rating for this process.

MFLOP Rating =
$$(3\text{Ghz}) * \frac{1 \text{ FLOP}}{21 \text{ clock cycles}} = 142.9 \text{ MFLOP/s}$$
 (1)

Part (b): DAXPY Loop, No Unrolling, with Scheduling

4DM4 Assignment #2(b), Compressed Timing Table, No Unrolling with Scheduling										
Instruction Slot #	1	IF (F1,F2)	ID	EX (Int, FP)	MEM (M1,M2)	WB	Comment/Hazard			
loop: L.D	F2, 0(R1)	1,2	3	4	5,6	7				
L.D	F6, 0(R2)	2,3	4	5	6,7	8				
MULT.D	F4, F2, F0	3,4	5	6-11	12,13	14	F4 OK (No data hazard at cc 5)			
DADDUI	R2, R2, #8	4,5	6	7	8,9	10				
DADDUI	R1, R1, #8	5,6	7	8	9,10	11				
ADD.D	F6, F4, F6	6,7	8-11	12-14	15,16	17	F6 stalls from cc 9-11 F4 forwarded from EX to EX			
S.D	0(R2), F6	7-11	12	13	14,15	16	F6 Forwarded from EX to M2			
DSGTUI	R3, R1, done	8-12	13	14	14,15	16				
BEQZ	R3, loop	12,13	14	-	-	-				
loop: start next it	teration									

Each iteration of this loop takes 16 clock cycles. The given clock speed is 3 GHz. The following equation can be used to calculate the MFLOP rating for this process.

MFLOP Rating =
$$(3\text{Ghz}) * \frac{1 \text{ FLOP}}{16 \text{ clock cycles}} = 187.5 \text{ MFLOP/s}$$
 (2)

Part (c): DAXPY Loop, with Unrolling, with No Scheduling

IDM4 Assi	gnment #2	(c), Compressed T	iming Table, Un	rolled with no Schedu	ling		
nstruction Slot #	¥1	IF (F1,F2)	ID	EX (Int, FP)	MEM (M1,M2)	WB	Comment/Hazard
loop: L.D	F2, 0(R1)	1-2, 14-16, 28-30, 42-44	3, 17, 31, 45	4, 18, 32, 46	5-6, 19-20, 33-34, 47-48	7, 21, 35, 49	F2 stalled for cc 15, 29, 43
MULT.D	F4, F2, F0	2-3, 16-17, 30-31, 44-45	4, 18, 32, 46	7-12, 21-26, 35-40, 49-54	-	13, 27, 41, 55	F4 stalled for cc 5-6 Bypasses M1, M2
L.D	F6, 0(R2)	3-4, 17-18, 31-32, 45-46	7, 21, 35, 49	8, 22, 26, 50	9-10, 23-24, 37-38, 51-52	11, 25, 39, 53	Stalled at F2 for cc 5,6
ADD.D	F6, F4, F6	4-7, 18-21, 32,35, 46-49	8, 22, 36, 50	13-15, 27-29, 41-43, 55-57	-	16, 30, 44, 58	F6 stalled for cc 5,6 and cc 9-1; F4 forwared from WB to EX Bypasses M1, M2
S.D	0(R2), F6	7-8, 21-22, 35-36, 49-50	13, 28, 42, 55	14, 28, 42, 56	16-17, 30-31, 44-45, 58-59	18, 32, 46, 60	Stalled at F1 for cc 9-12, and cc F6 forwarded from EX to M2
DADDUI	R1, R1, #8	8-13, 22-27, 36-41, 50-55	14, 28, 42, 56	16, 30, 44, 58	17-18, 31-32, 45-46, 59-60	19, 33, 47, 61	R1 stalled for cc 9-12 and 15
DADDUI	R2, R2, #8	13-14, 27-28, 41-42, 55-56	16, 30, 44, 58	17, 31, 45, 59	18-19, 32-33, 46-47, 60-61	20, 34, 48, 62	R2 stalled for cc 15
DSGTUI	R3, R1, done	56-58	59	60	61-62	63	
BEQZ	R3, loop	58-59	60	-	-	-	Branch slot R3
No-Op ((how many ?)	59-60	61	-	-	-	
loop: start n	ext iteration						

Each iteration of this loop (unrolled 4 times) takes 64 clock cycles. The given clock speed is 3 GHz. The following equation can be used to calculate the MFLOP rating for this process.

MFLOP Rating =
$$(3\text{Ghz}) * \frac{1 \text{ FLOP}}{63 \text{ clock cycles}} = 47.6 \text{ MFLOP/s}$$
 (3)

Part (d): DAXPY Loop, with Unrolling, with Scheduling

4DM4 Assignment #2(d), Compressed Timing Table, DAXPY Loop, With Unrolling, and with Scheduling

Instruction Slot #1		IF (F1,F2)	ID	EX (Int, FP)	MEM (M1,M2)	WB	Comment/Hazard	
loop:	L.D	F2, 0(R1)	1-2, 8-9, 15-16, 23-24	3, 10, 17, 25	4, 11, 18, 26	5-6, 12-13, 19-20, 27-28	7, 14, 21, 29	
	L.D	F6, 0(R2)	2-3, 9-10, 16-17, 24-25	4, 11, 18, 26	5, 12, 19, 27	6-7, 13-14, 20-21, 28-29	8, 15, 22, 30	
	MULT.D	F4, F2, F0	3-4, 10-11, 17-18, 25-26	5, 12, 19, 27	6-12, 13-19, 20-26, 28-34	7-8, 14-15, 21-22, 29-30	9, 16, 23, 31	F4 OK (No hazards)
	DADDUI	R2, R2, #8	4-5, 11-12, 18-19, 26-27	6, 13, 20, 28	7, 14, 21, 29	8-9, 15-16, 22-23, 30-31	10, 17, 24, 32	
	DADDUI	R1, R1, #8	5-6, 12-13, 19-20, 27-28	7, 14, 21, 29	8, 15, 22, 30	9-10, 16-17, 23-24, 31-32	11, 18, 25, 33	
	ADD.D	F6, F4, F6	6-7, 13-14, 20-21, 28-29	8-11, 15-18, 22-25, 30-33	12-14, 19-21, 26-28, 34-36	15-16, 22-23, 29-30, 37-38	17, 24 31, 39	F6 stalled at D for 3 extra cc F4 forwarded from EX to EX
	S.D	0(R2), F6	7-11, 14-18, 21-25, 29-33	12, 19, 26, 34	13, 18, 27, 34	14-15, 19-20, 28-29, 35-36	16, 21, 30, 37	F6 forwarded from EX to M2
	DSGTUI	R3, R1, done	34-38	39	40	41-42	43	
	BEQZ	R3, loop	38-39	40	-	-	-	Branch slot R3
loop:	start next	iteration						

Each iteration of this loop (unrolled 4 times) takes 43 clock cycles. The given clock speed is 3 GHz. The following equation can be used to calculate the MFLOP rating for this process.

MFLOP Rating =
$$(3\text{Ghz}) * \frac{1 \text{ FLOP}}{43 \text{ clock cycles}} = 69.7 \text{ MFLOP/s}$$
 (4)

Part (e): DAXPY Loop, with Unrolling, with Scheduling. On Dual-Issue Machine

4DM4 Assi	gnment #2(e), C	ompressed	Timing Tab	le, DAXF	Y Loop,	With Un	rolling an	d Sched	uling. On	Dual-Iss	ue Mach	ine
							slot #1			slot #2		1
Instru	uction Slot #1	Instruction	on Slot #2	IF	ID	EX1	MEM1	WB1	EX2	MEM2	WB2	Comment/Hazard
loop: L.D	F2, 0(R1)	L.D	F6, 0(R2)	1,2	3	4	5,6	7	4	5,6	7	
L.D	F3, 8(R1)	L.D	F7, 8(R2)	2,3	4	5	6,7	8	5	6,7	8	
L.D	F4, 16(R1)	L.D	F8, 16(R2)	3,4	5	6	7,8	9	6	7,8	9	
L.D	F5, 24(R1)	L.D	F9, 24(R2)	4,5	6	7	8,9	10	7	8,9	10	
DADDUI	R2, R2, #8	MULT.D	F12, F2, F0	5,6	7	8	9,10	11	7-12	13,14	15	F12 OK (No hazards)
DADDUI	R1, R1, #8	MULT.D	F13, F3, F0	6,7	8	9	10,11	12	8-13	14,15	16	F13 OK (No hazards)
DADDUI	8(R2), 8(R2), #8	MULT.D	F14, F4, F0	7,8	9	10	11,12	13	9-14	15,16	17	F14 OK (No hazards)
DADDUI	8(R1), 8(R1), #8	MULT.D	F15, F5, F0	8,9	10	11	12,13	14	11-16	16,17	18	F15 OK (No hazards)
DADDUI	16(R2), 16(R2), #8	ADD.D	F16, F12, F6	9,10	11	12	13,14	15	12-14	15,16	17	F12 forwarded from M2 to EX
DADDUI	16(R1), 16(R1), #8	ADD.D	F17, F13, F7	10,11	12	13	14,15	16	13-15	16,17	18	F12 forwarded from M2 to EX
DADDUI	24(R2), 24(R2), #8	ADD.D	F18, F14, F8	11,12	13	14	15,16	17	14-16	17,18	19	F14 forwarded from M2 to EX
DADDUI	24(R1), 24(R1), #8	ADD.D	F19, F15, F9	12,13	14	15	16,17	18	15-17	18,19	20	F15 forwarded from M2 to EX
DSGTUI	R3, R1, done	поор										
BEQZ	R3, loop	поор										Branch slot R3
S.D	0(R2), F16	S.D	8(R2), F18	15,16	17	18	19,20	21	18	19,20	21	
S.D	16(R2), F18	S.D	24(R2), F19	16,17	18	19	20,21	22	19	20,21	22	
loop: start next	iteration											

Each iteration of this loop (unrolled 4 times) is ran using 2 seperate slots, allowing for 2 instructions to run simultaneously. The whole iteration takes 22 clock cycles. The given

clock speed is 3 GHz. The following equation can be used to calculate the MFLOP rating for this process.

MFLOP Rating =
$$(3\text{Ghz}) * \frac{1 \text{ FLOP}}{22 \text{ clock cycles}} = 136.3 \text{ MFLOP/s}$$
 (5)