4DM4 Assignment 2
Advanced Static Pipelining

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Contents

Part (a): DAXPY Loop, No Unrolling, with No Scheduling

4DM4 Assignment 2(a), DAXPY Loop, No Unrolling, No Scheduling

ASSUMPTIONS:

IF = 2-stage pipeline (F1, F2)
MEM = 2-stage Pipeline (M1, M2)
FP-ADD = 3-stage Pipeline
FP-MULT = 6-stage Pipeline

Instruction		Clock Cycle																						
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
loop: L.D	F2, 0(R1)	F1	F2	ID	EX	M1	M2	WB																	
MULT.D	F4, F2, F0		F1	F2	ID	STL	STL	FP-MULT						WB											
L.D	F6, 0(R2)			F1	F2	STL	STL	ID	EX	M1	M2	WB													
ADD.D	F6, F4, F6				F1	STL	STL	F2	STL	STL	STL	STL	STL	ID	FP-ADD			WB							
S.D	0(R2), F6					STL	STL	F1	STL	STL	STL	STL	STL	F2	ID	EX	M1	M2	WB						
DADDUI	R1, R1, #8													F1	F2	ID	EX	M1	M2	WB					
DADDUI	R2, R2, #8														F1	F2	ID	EX	M1	M2	WB				
DSGTUI	R3, R1, done															F1	F2	ID	EX	M1	M2	WB			
BEQZ	R3, loop																F1	F2	ID	EX	M1	M2	WB		
No-op (how many no-ops?)																		F1	F2	ID	EX	M1	M2	WB	

Each iteration of this loop takes 23 clock cycles. The given clock speed is 3 GHz. The following equation can be used to calculate the MFLOP rating for this process.

$$\text{MFLOP Rating} = (3\text{Ghz}) * \frac{1 \text{ FLOP}}{23 \text{ clock cycles}} = 130.4 \text{ MFLOP/s} \tag{1}$$

Part (b): DAXPY Loop, No Unrolling, with Scheduling

4DM4 Assignment #2(b), Compressed Timing Table, No Unrolling with Scheduling

Instruction Slot #1		IF (F1,F2)	ID	EX (Int, FP)	MEM (M1,M2)	WB	Comment/Hazard
loop: L.D	F2, 0(R1)	1,2	3	4	5,6	7	
L.D	F6, 0(R2)	2,3	4	5	6,7	8	
MULT.D	F4, F2, F0	3,4	5	6-11	12,13	14	F4 OK (No data hazard at cc 5)
DADDUI	R2, R2, #8	4,5	6	7	8,9	10	
DADDUI	R1, R1, #8	5,6	7	8	9,10	11	
ADD.D	F6, F4, F6	6,7	8-11	12-14	15,16	17	F6 stalls from cc 9-11 F4 forwarded from EX to EX
S.D	0(R2), F6	7-11	12	13	14,15	16	F6 Forwarded from EX to M2
DSGTUI	R3, R1, done	8-12	13	14	14,15	16	
BEQZ	R3, loop	12,13	14	-	-	-	
loop: start next iteration							

Each iteration of this loop takes 16 clock cycles. The given clock speed is 3 GHz. The following equation can be used to calculate the MFLOP rating for this process.

$$\text{MFLOP Rating} = (3\text{Ghz}) * \frac{1 \text{ FLOP}}{16 \text{ clock cycles}} = 187.5 \text{ MFLOP/s} \tag{2}$$

Part (c): DAXPY Loop, with Unrolling, with No Scheduling

4DM4 Assignment #2(c), Compressed Timing Table, Unrolled with no Scheduling

Instruction Slot #1		IF (F1,F2)	ID	EX (Int, FP)	MEM (M1,M2)	WB	Comment/Hazard
loop: L.D	F2, 0(R1)	1-2, 15-16, 29-30, 43-44	3,17,31,45	4,18,32,46	5-6, 19-20, 33-34, 47-48	7,21,35,49	
MULT.D	F4, F2, F0	2-3, 16-17, 30-31, 44-45	4,18,32,46	7-12, 21-26, 35-40, 49-54	-	13,27,41,55	F4 stalled for cc 5,6 Bypasses M1, M2
L.D	F6, 0(R2)	3-4, 17-18, 31-32, 45-46	7,21,35,49	8, 22, 36, 50	9 - 10, 23-24,37-38,51-52	11,25,39,53	Stalled at F2 for cc 5,6
ADD.D	F6, F4, F6	4-7, 18-21, 32-35, 46-49	13,27,41,55	14-16, 28-30, 42-44, 56-58	-	17,31,45,59	F6 stalled for cc 5,6 and cc 8-12 F4 forwared from WB to EX Bypasses M1, M2
S.D	0(R2), F6	7-13, 21-27, 35-41, 49-55	14,28,42,56	15, 29, 43, 57	16-17, 30-31, 44-45, 58-59	18,32,46,60	Stalled at F1 for cc 8-12 F6 forwarded from EX to M2
DADDUI	R1, R1, #8	13-14, 27-28, 41-42, 55-56	15,29,43,57	16, 30, 44, 58	17-18, 31-32, 45-46, 59-60	19, 33,47,61	
DADDUI	R2, R2, #8	14-15, 28-29, 42-43, 56-57	16,30,44,58	17, 31, 45, 59	18-19, 32-33, 46-47, 60-61	20, 34,48,62	
DSGTUI	R3, R1, done	57-58	59	60	61-62	63	
BEQZ	R3, loop	58-59	60	61	62-23	64	

Each iteration of this loop (unrolled 4 times) takes 64 clock cycles. The given clock speed is 3 GHz. The following equation can be used to calculate the MFLOP rating for this process.

$$\text{MFLOP Rating} = (3\text{Ghz}) * \frac{1 \text{ FLOP}}{64 \text{ clock cycles}} = 46.9 \text{ MFLOP/s} \tag{3}$$

Part (d): DAXPY Loop, with Unrolling, with Scheduling

Part (e): DAXPY Loop, with Unrolling, with Scheduling. On Dual-Issue Machine

Assumptions

- Assume ‘a’ is in R2
- Assume ‘b’ is in R31
- Assume ‘d’ is in R30

As seen in the above table, it takes **26 clock cycles** to complete the quarter round operation. The number of clock cycles is calculated by adding the number of clock cycles required to complete each of the four operations in the quarter round, the loading and saving. 98 clock cycles. 0 stalls. Total clock cycles: 2131988

Part (c)

Part (d)

Part (e)