ELECTRONIC PACKAGING

Assignment Report

Team Members

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Objective:

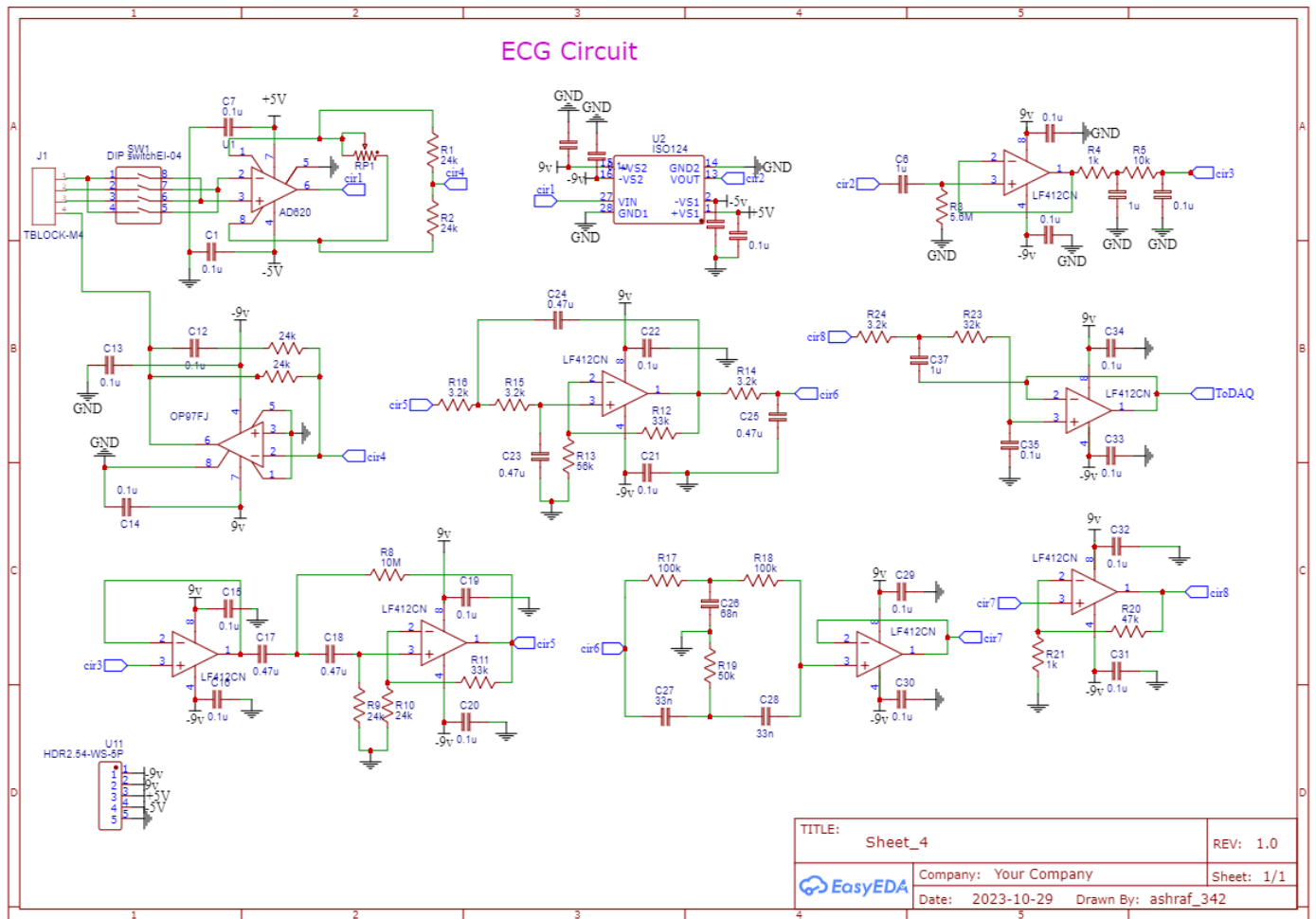Designing a Layout, Schematic and PCB of Electrocardiograph (ECG) circuit using EasyEDA and Eagle software.

Modules Required:

- – AD620 IC
- – ISO124 IC
- – LF412CN IC
- – OP97AP IC
- – Capacitors (0.1µF, 0.47 µF, 1 µF)
- – Resistors (10kΩ, 1kΩ, 50kΩ, 1kΩ, 47kΩ, 3.2kΩ, 32kΩ, 5.6MΩ, 24kΩ)
- – TBlock-M4
- – Switches (DIP switch EL04)
- – Voltage Supply pins (HDR-2.54 WS-5P)
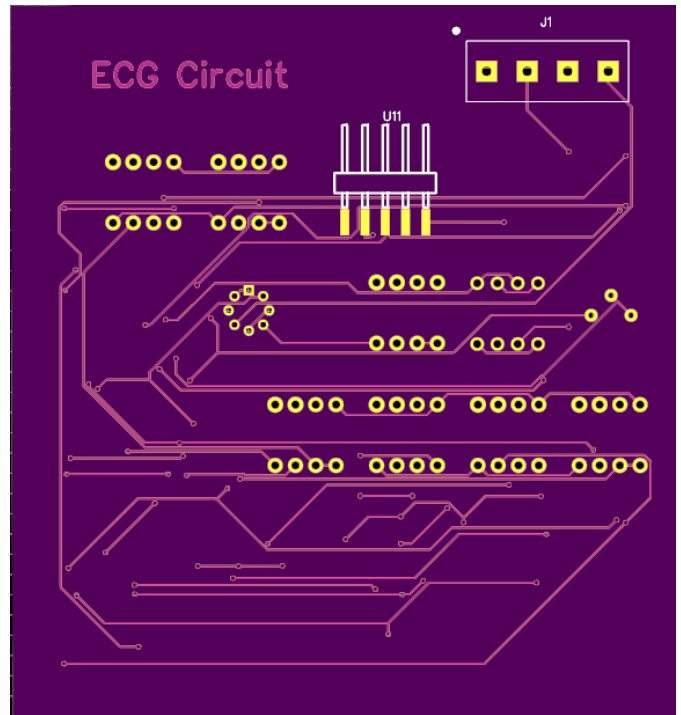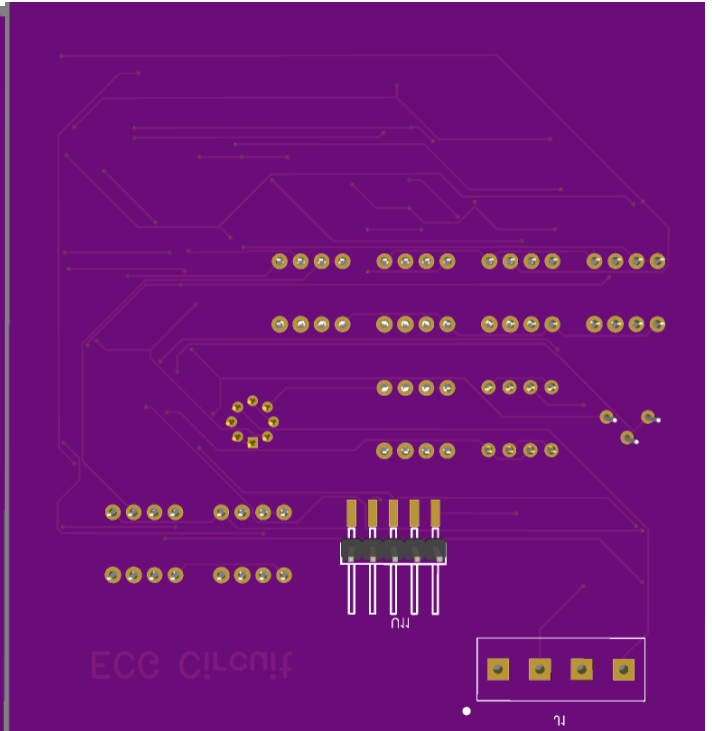
Circuit:

EasyEDA Software
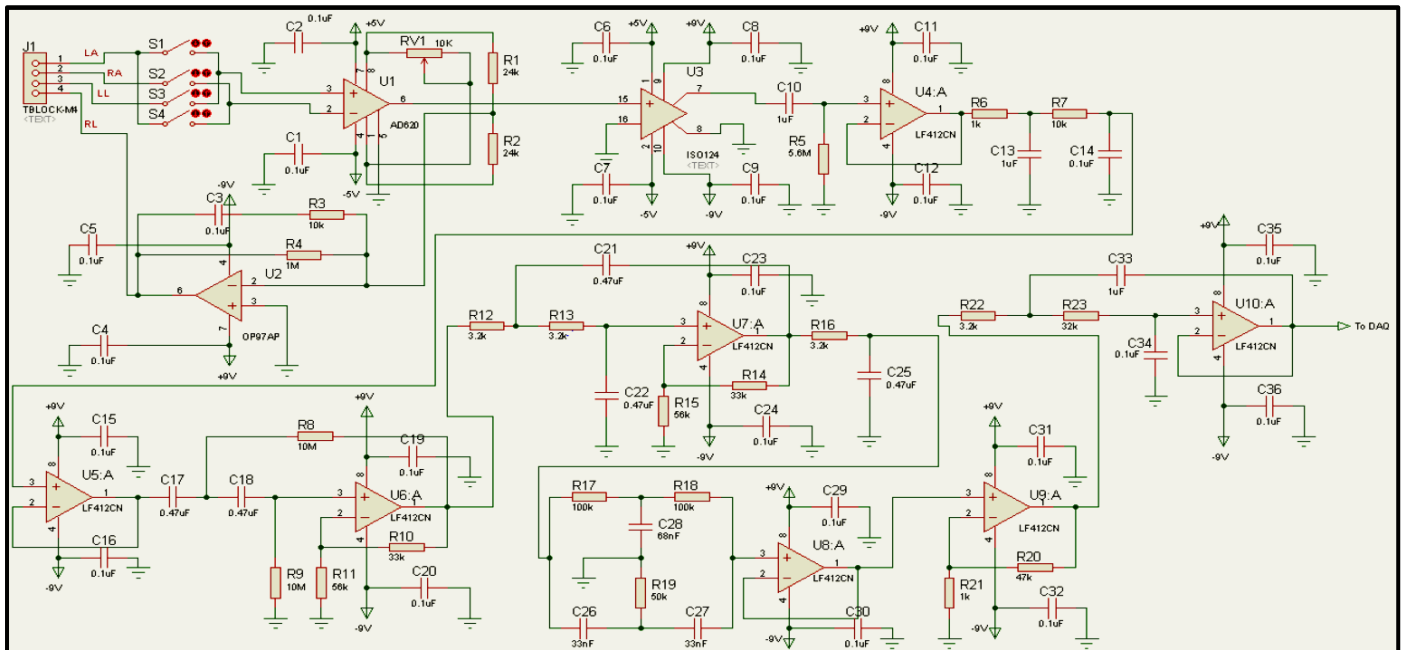
Schematic:
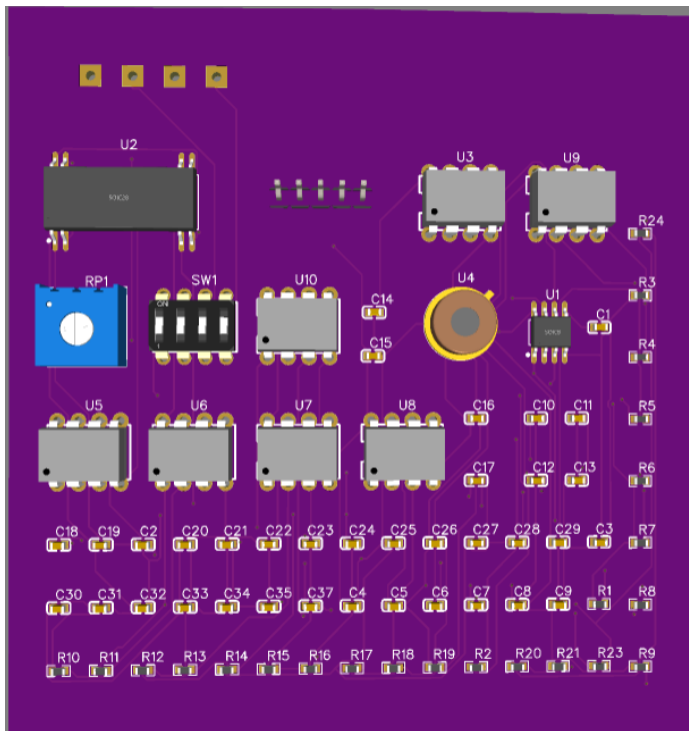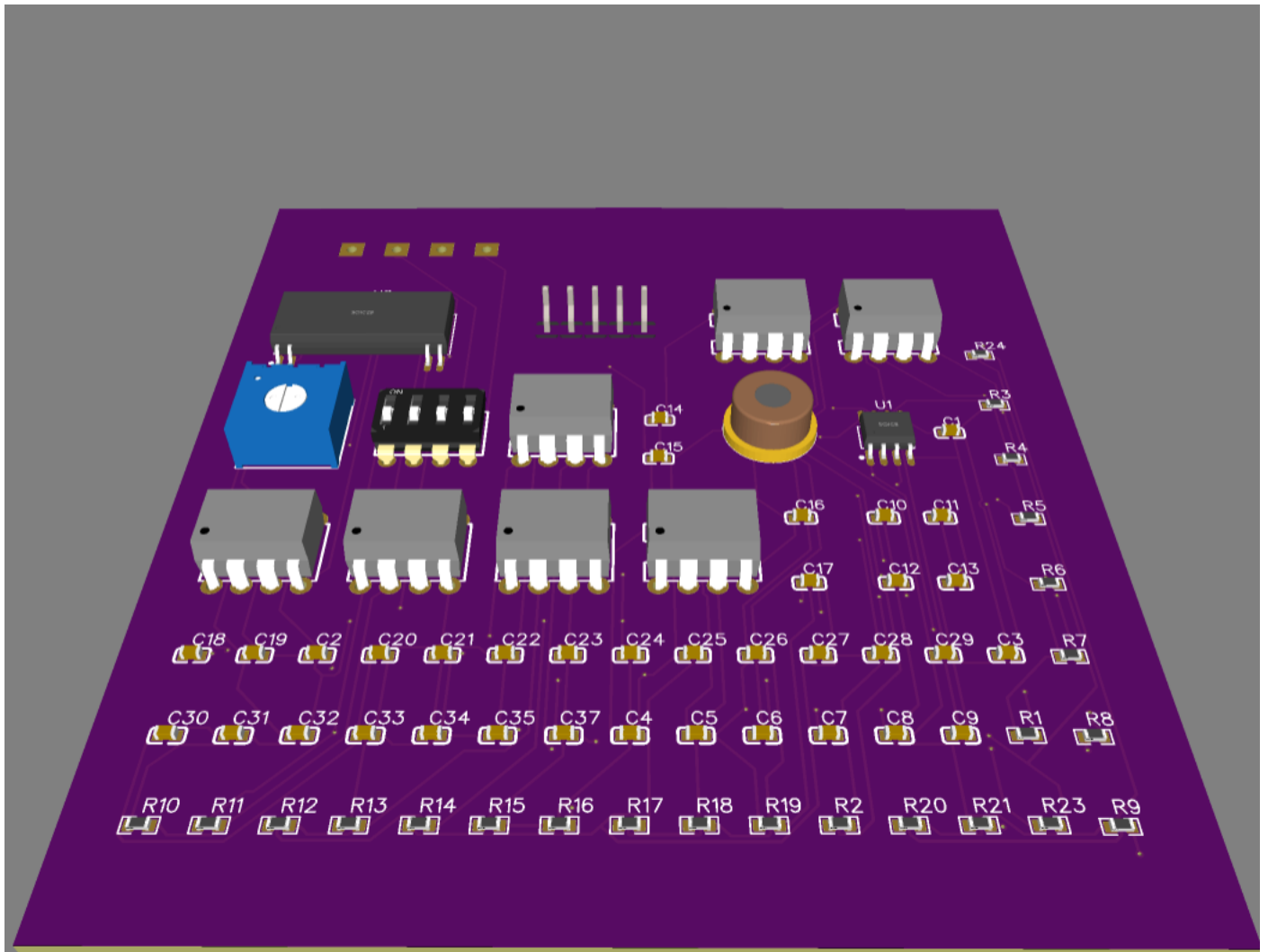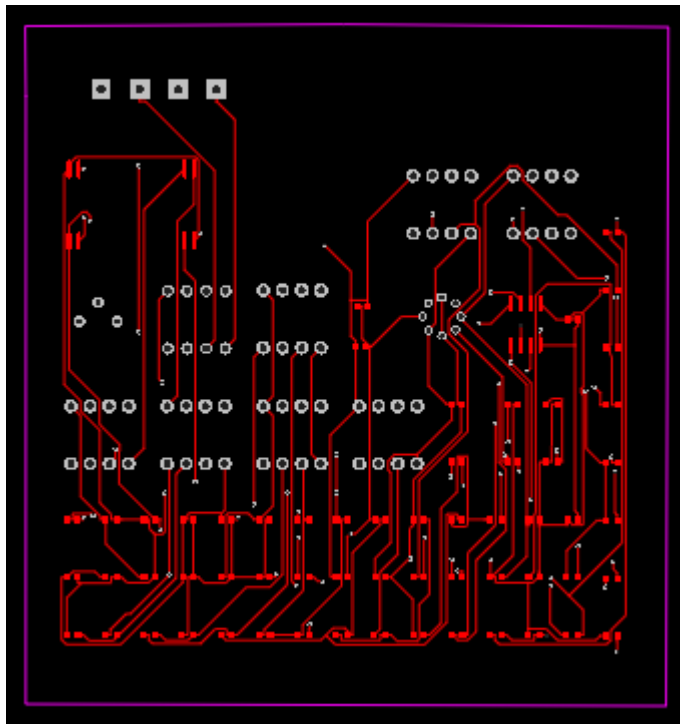
PCB Design:
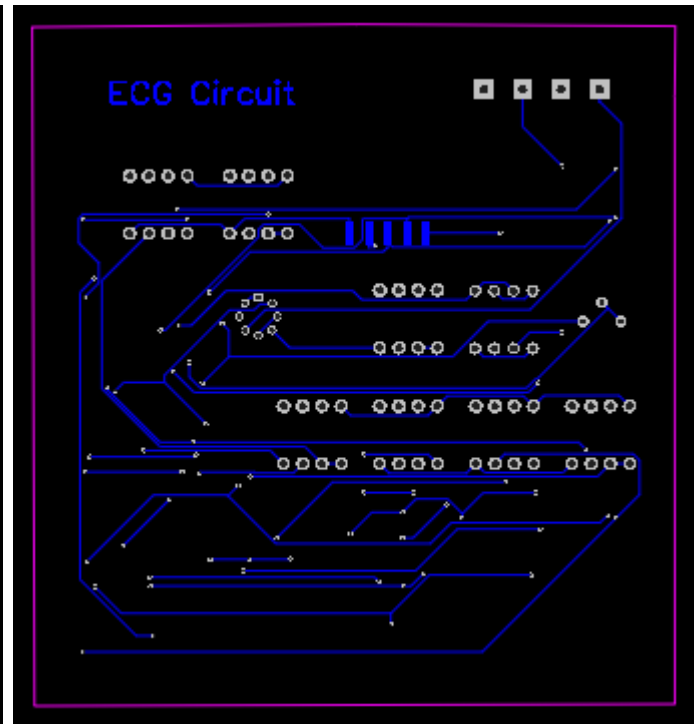
2D view
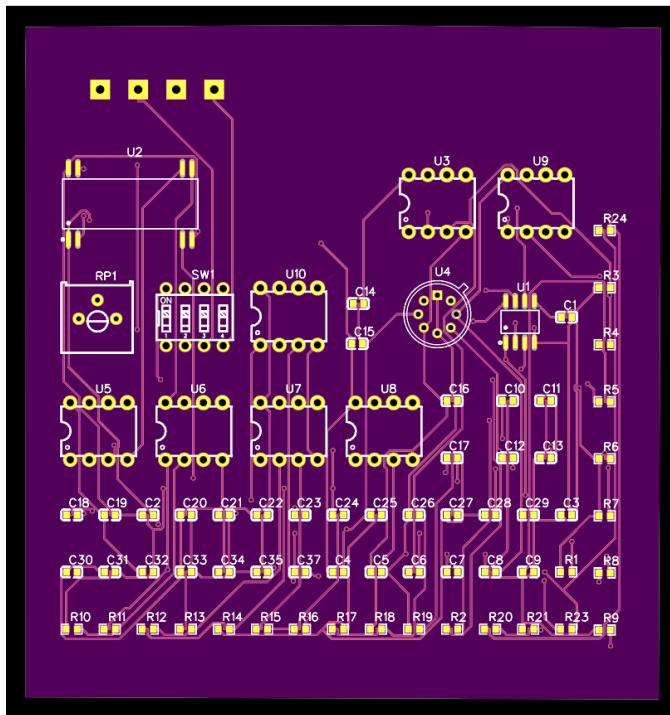
Top Layer

Bottom Layer

3D view

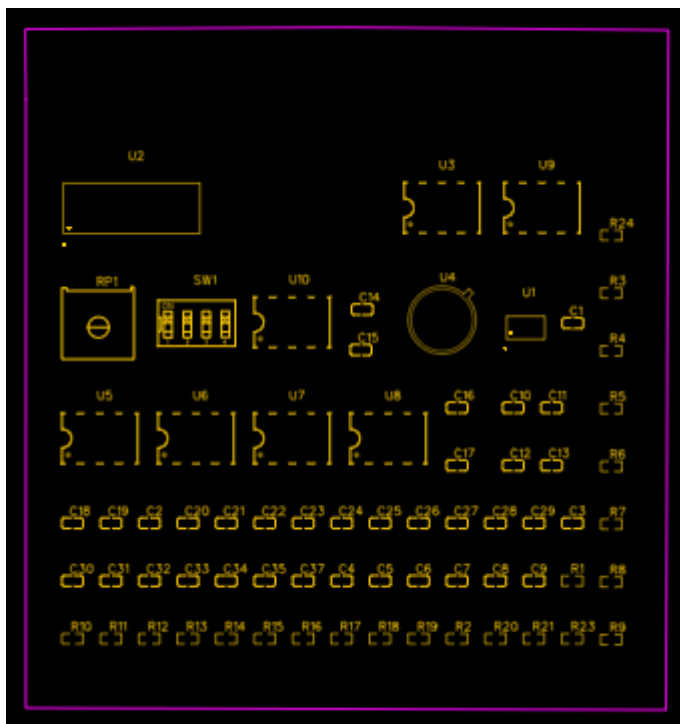Front view |Back view | cross view | Through view
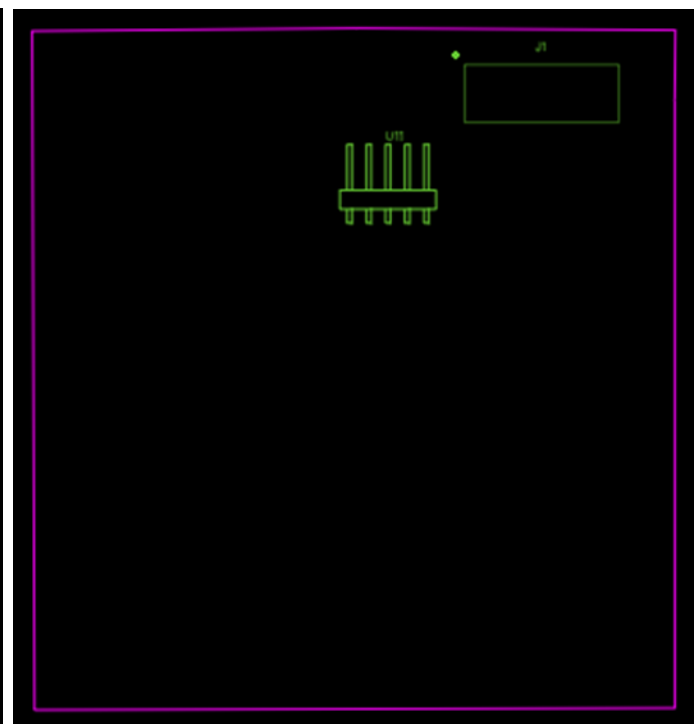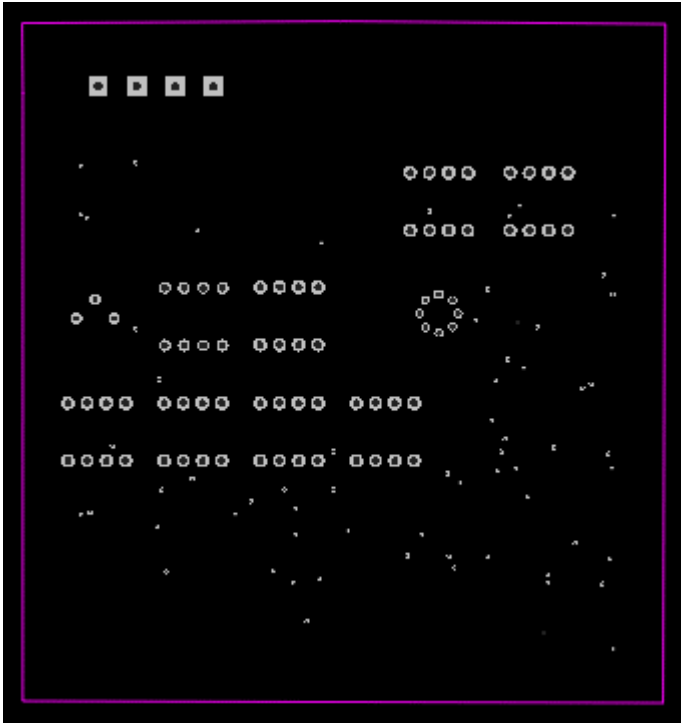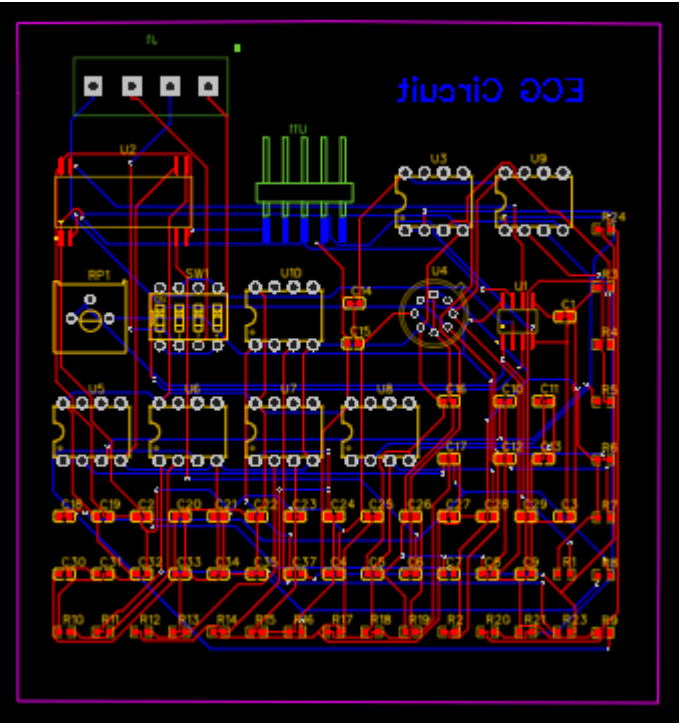
Types of common layers:
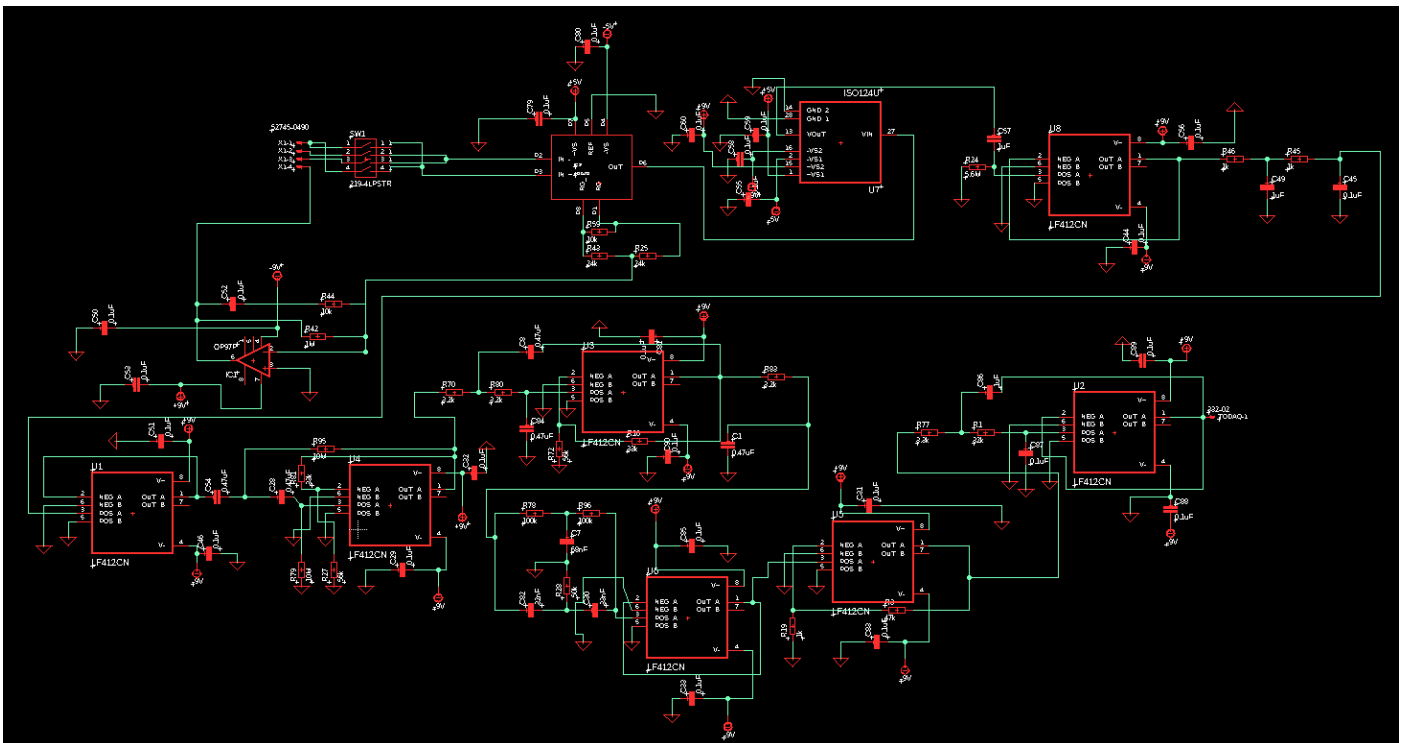

Top Layer

Bottom Layer

Top Silk Layer
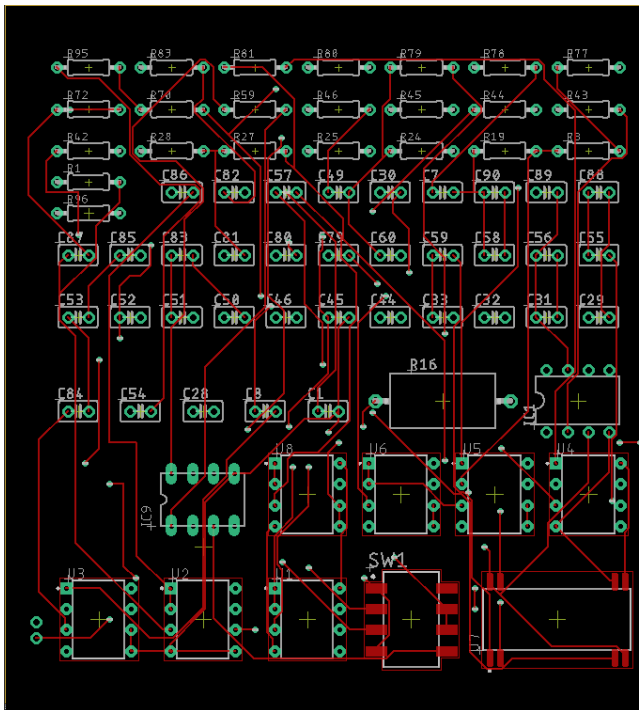

Bottom Silk Layer

Multi-Layer
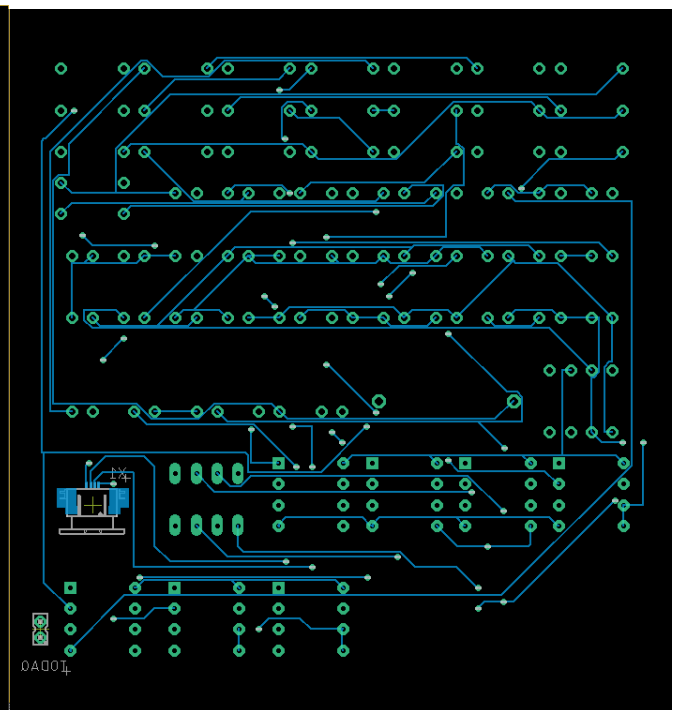

All Layers Merged

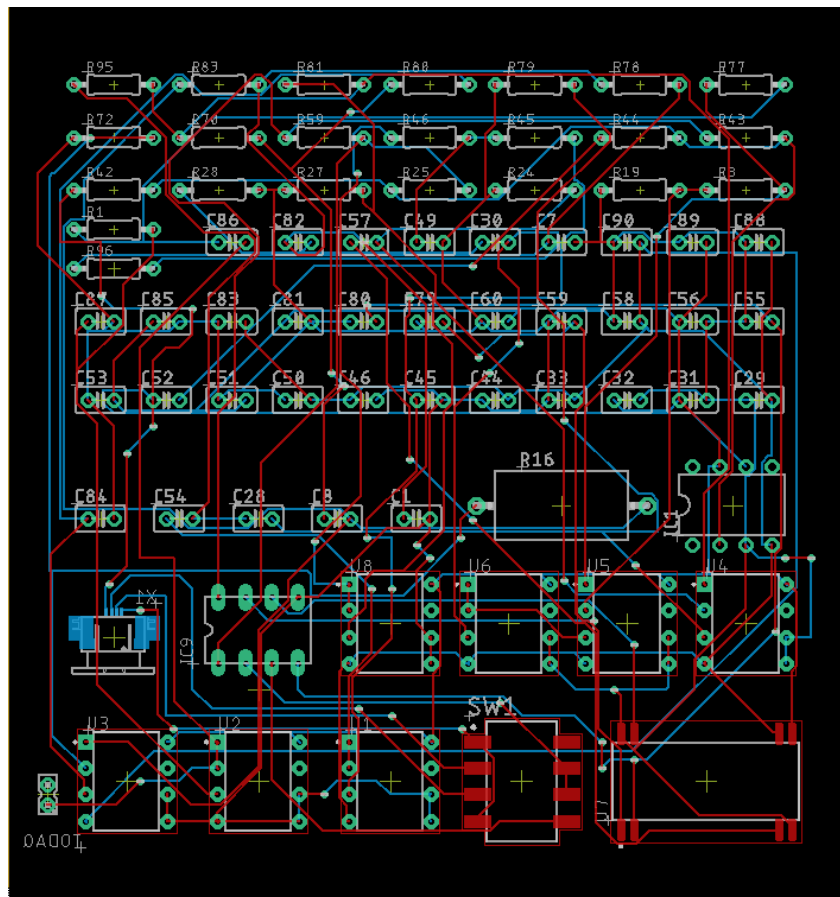# Eagle Software

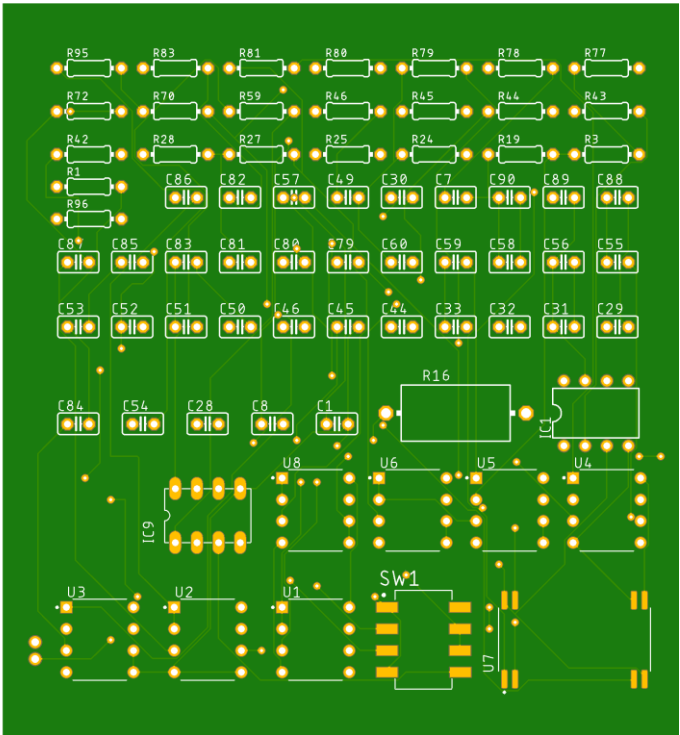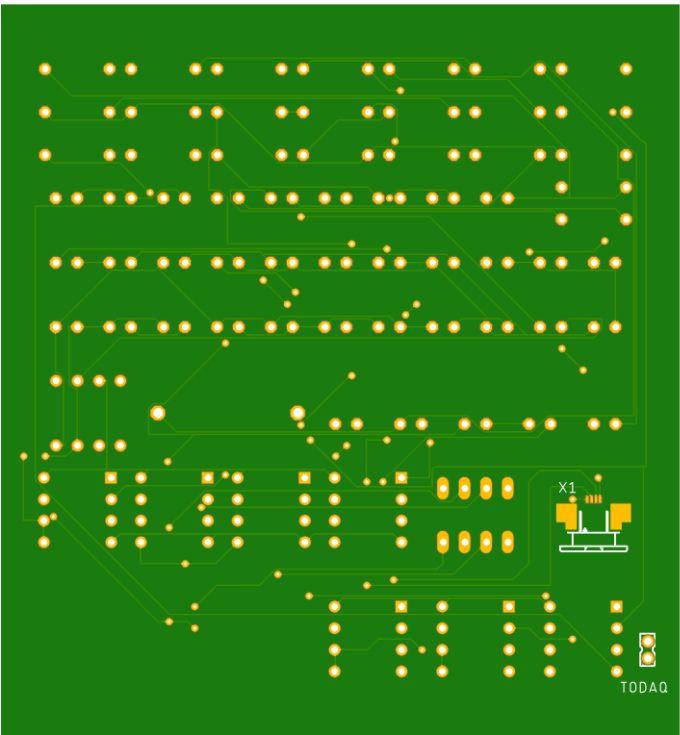## Schematic:

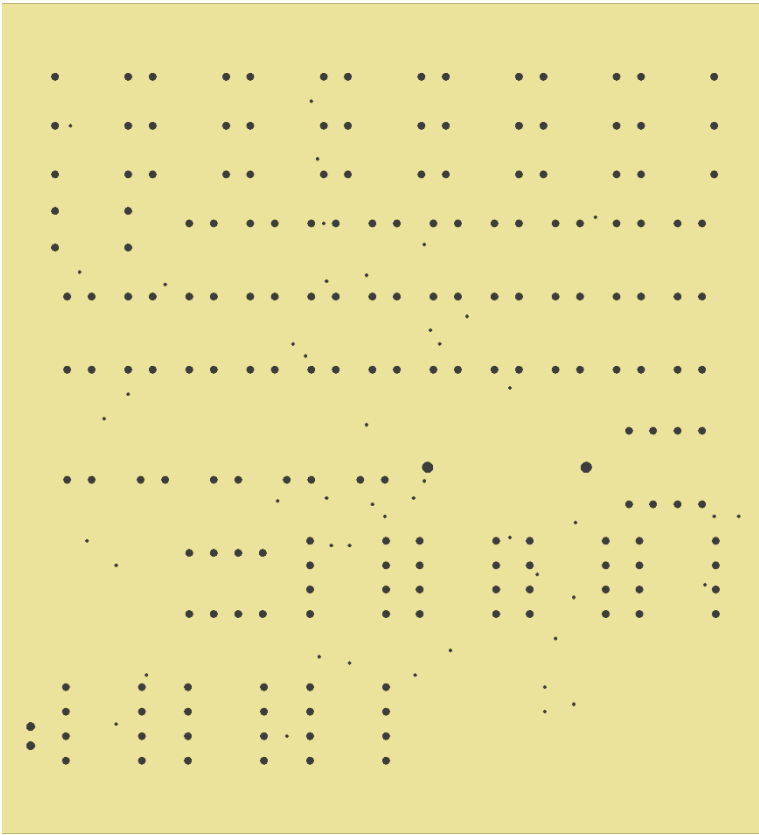# PCB Design:

Layers:

Top Layer

Bottom Layer

Merged Layer

Board Design:

Top View

Bottom View

Drill View

Measurements:

Types	EasyEDA (in mm)	Eagle (in mm)
Board Width	84.24	80.95
Board Height	90.297	86.35
Board Area	7606.62 Sq.	6990.03 Sq.
Copper Layers	2	2
Board Thickness	1.6	1.57
Via Drill Size	0.305	0.35
Min. Copper Trace Width	0.254	0.15
Max. Drill Size	1	1.10
Min. Drill Size	0.305	0.35
ERC & DRC Errors	0	0

Contributions:

Team member 1: Pamidi Mohammad Ashraf

- Designed schematic in Eagle
- Designed PCB in EasyEDA

Team member 2: Gowtham N

- Designed schematic in EasyEDA
- Designed PCB in Eagle

- In order to gain understanding in both schematic and PCB design we divided our work such that one can design schematic using one type of software while PCB design in different software and vice versa done by other member.

Concepts Used or Improvisations:

- **Use of Multilayers:** Used two layers (top layer and bottom layer) of copper and Vias are placed in order to provide the connection between the layers.
- **Double Sided PCB:** Components were placed on both sides of the PCB board in order to achieve most possible minimized circuit.

- **Level of interconnections**: Level 2 interconnections are used to provide the connections between the ICs and components.
- **Level of packaging:** The packaging involved is level 2 since single PCB board is being used.

Achievements:

- Designed PCB of zero ERC and DRC errors multilayer (two layer of copper) which is a two sided (top and bottom layer) where the connectors are invoked at the bottom.
- Gained experience on Eagle Autodesk and EasyEDA software.

Source: https://core.ac.uk/download/pdf/199199084.pdf

Thank You