Simulation Analysis of TFETs For Low Power and High-Speed Applications

A
MAJOR PROJECT REPORT

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IN
ELECTRONICS AND COMMUNICATION ENGINEERING

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(Autonomous)

(Affiliated to JNTUH, Hyderabad)
Dundigal, Hyderabad-500043
2020-2024

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that the project entitled ***"Simulation Analysis of TFETs For Low Power and High-Speed Applications"*** *is the Bonafede work done* by N. Nishanth Goud (20R21A04M8), Shaik Ashraf(20R21A04P2), M. Sai Nikitha (20R21A04M2) in partial fulfillment of the requirement for the award of the degree of B. Tech in Electronics and Communication Engineering, during the academic year 2023-24.

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ABSTRACT

This work presents simulation study of single and double gate TFETs to determine optimal device structure for the potential applications in low-power and fast switching electronic applications. 2-D Silvaco TCAD tool is used after employing appropriate physical models to analyze the effects of gate work function, intrinsic layer thickness, and gate-length on sub-threshold swing (SS) and I_{ON}/I_{OFF}. Double-gate TFETs offer enhanced electrostatic control and reduced leakage current over single gate TFET. The optimized double-gate device structure with intrinsic layer thickness of 6 nm, gate-length of 160 nm and gate work function of 4.2 eV resulted in I_{ON}/I_{OFF} of 10^{11} and SS of 30 mV/dec. Moreover, improved scalability and reduced short-channel effects make double-gate TFETs more suitable for advanced microelectronics devices.

The project focuses on the simulation analysis of both single and double gate Tunnel Field-Effect Transistors (TFETs) to identify the optimal device structure for applications requiring low-power consumption and fast switching. Utilizing a 2-D Silvaco TCAD tool and incorporating appropriate physical models, the effects of various parameters such as gate work function, intrinsic layer thickness, and oxide layer thickness on key performance metrics like sub-threshold swing (SS) and I_{ON}/I_{OFF} ratio are examined.

Overall, the findings underscore the importance of optimizing device structure and parameters in TFETs for achieving desired performance metrics. By carefully manipulating factors such as gate work function, oxide layer thickness, and intrinsic layer thickness, engineers can tailor TFET designs to meet specific requirements in low-power and fast-switching applications. These insights pave the way for further advancements in TFET technology, potentially unlocking new possibilities for energy-efficient and high-performance electronic devices.

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ACRONYMS

- TFET: Tunnel Field-Effect Transistor
- TCAD: Technology computer aided design
- SS: Sub-threshold Swing
- MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor
- ICs: Integrated Circuits

CHAPTER – 1
INTRODUCTION

1.1 OVERVIEW

This project aims to develop a system for effectively working in low power consumption devices with an accurate parameters. Double Tunneling Field Effect Transistor (TFET) has emerged as a promising candidate for next-generation semiconductor devices, owing to its potential for low power consumption and enhanced performance compared to traditional transistors. We focused on the fabrication process of Double TFET using Silvaco software, a widely utilized tool for semiconductor device simulation and design. The objective is to explore the intricacies of the fabrication process, analyze the device characteristics, and gain insights into the potential applications of Double TFET in advanced electronics.

This endeavor involves the utilization of advanced simulation tools to study and optimize device characteristics. Among these tools, Silvaco software emerges as a powerful and versatile platform for semiconductor device simulation and process development. This comprehensive investigation into Double TFET fabrication using Silvaco software delves into the intricacies of the design, simulation, and optimization processes, aiming to unlock the full potential of this cutting-edge technology.

Silvaco's suite of simulation tools stands at the forefront of innovation in semiconductor technology, offering a comprehensive platform specifically tailored for the exploration and optimization of Double Tunnel Field Effect Transistors (TFETs). Double TFETs represent a promising avenue for enhancing transistor performance, particularly in low-power applications, due to their unique structure and operational principles.

At the heart of Silvaco's offering is the integration of advanced models that accurately capture the intricate interplay of material properties, quantum mechanical effects, and process technology inherent in Double TFETs. These models provide a detailed understanding of device behavior, enabling researchers and engineers to simulate and analyze the performance of Double TFETs across a wide range of operating conditions.

From the initial stages of design parameter selection to the fine-tuning of process parameters, Silvaco's simulation capabilities serve as a critical tool for unlocking the full potential of Double TFETs. Engineers can leverage these simulations to explore various design choices, optimize device performance, and identify potential areas for improvement. Moreover, by providing insights into device behavior at the nanoscale level, Silvaco empowers users to make informed decisions throughout the development cycle, ultimately accelerating the pace of innovation in semiconductor technology.

In summary, Silvaco's suite of simulation tools plays a pivotal role in advancing the field of Double TFETs by offering a powerful platform for exploration, optimization, and innovation. By harnessing the capabilities of these tools, researchers and engineers can push the boundaries of transistor performance and pave the way for the next generation of low-power electronic devices.

1.2 MOTIVATION

The motivation behind exploring Double Tunneling Field Effect Transistor (Double TFET) fabrication with Silvaco software lies in the semiconductor industry's drive for innovation. Conventional transistors encounter issues like high power consumption and plateauing performance improvements. This research seeks solutions by leveraging the unique attributes of Double TFETs, aiming to break through these limitations and usher in a new era of energy-efficient and high-performance semiconductor devices.

Additionally, the push towards sustainability in technology motivates this research. With global concerns about energy usage and environmental impact, there is a call for semiconductor devices that are not only powerful but also environmentally friendly. The Double TFET, with its potential for superior energy efficiency, aligns with this call for greener technology. By optimizing the fabrication process through Silvaco software, we strive to make significant strides towards creating semiconductor components that minimize their ecological footprint.

1.3 EXISTING SYSTEM

The existing system is one such promising innovation is the Tunnel Field-Effect Transistor (TFET), which exhibits distinct advantages over traditional MOSFETs, such as reduced

subthreshold swing and improved energy efficiency. To harness the potential of TFETs, researchers and engineers leverage powerful simulation software, such as Silvaco, to model and simulate the intricate processes involved in their fabrication.

Silvaco software provides a comprehensive platform for semiconductor device simulation, enabling users to analyze and optimize the performance of TFETs through a systematic approach. The existing system employs Silvaco to simulate the intricate fabrication steps of TFETs, from the initial design stages to the final integration into semiconductor devices. This process involves the utilization of Silvaco's advanced modeling capabilities to accurately represent the material properties, geometries, and electrical characteristics of TFETs.

1.3.1 LIMITATIONS OF AN EXISTING SYSTEM

- **Sub-threshold swing**

The subthreshold swing refers to the rate at which the transistor switches from the OFF-state to the ON-state as the gate voltage is varied. In traditional MOSFETs, achieving a steep subthreshold slope becomes challenging as device dimensions shrink.
This limitation results in increased power consumption and decreased energy efficiency, especially in low-power applications.

- **Quantum tunneling**

Quantum tunneling occurs when charge carriers (electrons or holes) pass through a potential barrier that they would not typically have enough energy to overcome according to classical physics. In MOSFETs, as device dimensions are scaled down, the thickness of the gate oxide layer reduces, increasing the likelihood of quantum tunneling.
This phenomenon leads to increased leakage currents, causing power dissipation and compromising device performance and reliability.

- **Power consumption**

As MOSFETs are scaled down to smaller sizes, their power consumption tends to increase due to various factors, including leakage currents, gate capacitance, and resistive losses.

Leakage currents, in particular, become more pronounced at nanoscale dimensions due to quantum tunneling effects and limited control over channel conductance.

High power consumption not only affects device efficiency but also contributes to heat generation, which can degrade performance and reliability.

- **Short-channel effects**

Short-channel effects (SCEs) in MOSFETs, caused by shrinking channel lengths, elevate leakage currents, induce threshold voltage variations, and degrade switching speed. These effects compromise device reliability and energy efficiency. To counter SCEs and advance semiconductor technology, researchers explore alternative transistor designs like Tunnel Field-Effect Transistors (TFETs), which promise reduced leakage and enhanced performance, offering potential solutions for future electronic system.

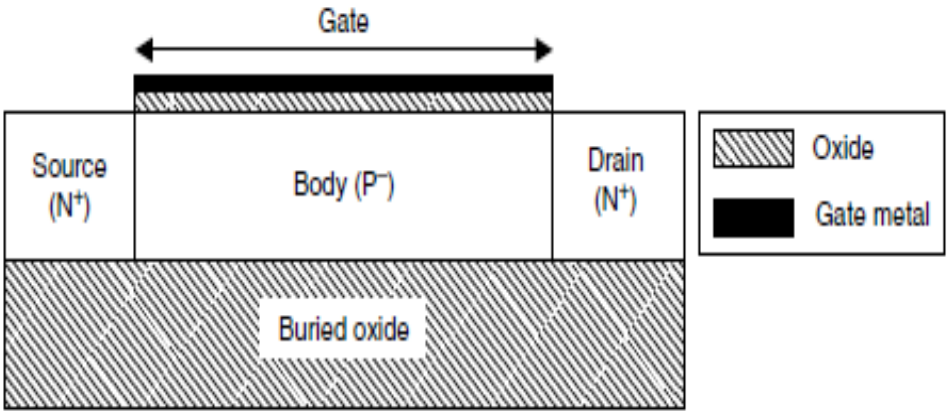

Figure 1. Structure of MOSFET

1.4 Tunnel-Field Effect Transistor (TFET)

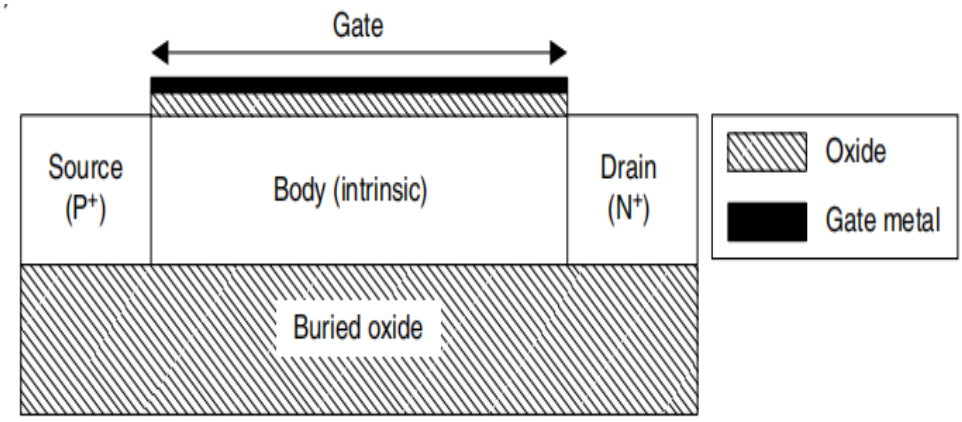

Figure 2. Structure of n-channel TFET

The Tunneling Field Effect Transistor (TFET) stands as a revolutionary semiconductor device designed to address the challenges encountered by traditional transistors, such as MOSFETs, in terms of power consumption and performance. TFETs leverage the quantum mechanical phenomenon of tunneling, allowing them to operate at lower voltages and potentially achieve better energy efficiency compared to their conventional counterparts.

The roots of TFET technology can be traced back to the early 1990s when researchers began exploring ways to overcome limitations associated with MOSFETs. MOSFETs, although immensely successful, face challenges related to power consumption, especially as devices shrink in size. TFETs emerged as a promising solution to mitigate these challenges.

The core principle behind TFET operation lies in quantum tunneling, where charge carriers pass through a thin barrier without the need for high energy levels. Unlike MOSFETs, TFETs exploit this tunneling phenomenon to control the flow of electrons or holes between the source and drain terminals, allowing for more efficient transistor operation, especially at lower supply voltages.

One of the key advantages of TFETs stems from their potential to achieve lower sub-threshold swings. This characteristic is critical in electronic devices, as it indicates how effectively a transistor can turn on and off. Lower sub-threshold swings translate to reduced power

consumption and improved energy efficiency, making TFETs an attractive option for applications where power efficiency is paramount.

Despite the promise of TFETs, there are challenges in terms of fabrication and optimization. Researchers and engineers have been actively working to overcome these obstacles to bring TFETs into mainstream semiconductor technology. Simulations using advanced software, like Silvaco, have played a crucial role in fine-tuning TFET designs and understanding the intricate interplay of quantum effects in these devices.

In conclusion, the TFET has emerged as a significant player in the evolution of semiconductor devices, with roots in the quest for improved power efficiency. From its conceptualization in the 1990s to ongoing research and development, TFETs symbolize the industry's dedication to overcoming challenges and pushing the boundaries of what is achievable in transistor technology. As advancements in fabrication techniques and simulation tools continue, the TFET holds the potential to reshape the landscape of electronic devices, offering a more energy-efficient alternative for the ever-growing demands of modern technology.

1.4.1 Why Tunnel-Field Effect Transistor (TFET)

TFETs offer several advantages over traditional MOSFETs, making them an attractive research area in semiconductor device engineering. Unlike MOSFETs, which rely on the modulation of a charge carrier channel through an electric field, TFETs exploit quantum tunneling through a thin barrier. This unique operating principle allows TFETs to achieve steeper subthreshold slope, which is beneficial for low-power applications where minimizing energy consumption is critical. Additionally, TFETs exhibit lower leakage currents compared to MOSFETs, enabling better control over power dissipation and improving overall energy efficiency. Another advantage of TFETs is their potential compatibility with new materials and fabrication techniques. As semiconductor technology advances, researchers are exploring novel materials with unique properties that could enhance transistor performance. TFETs offer a platform for integrating these materials into device structures, opening up new possibilities for optimizing transistor characteristics such as carrier mobility and bandgap engineering. Moreover, TFETs could be manufactured using existing semiconductor fabrication processes with minimal modifications, reducing the barrier to adoption in industry. In summary, TFETs present an exciting opportunity to overcome the limitations of traditional MOSFETs and drive

advancements in semiconductor technology. Their unique operating principle, coupled with potential performance benefits and compatibility with existing fabrication processes, makes them a compelling area of research. By exploring TFETs, researchers seek to push the boundaries of transistor scaling and unlock new possibilities for energy-efficient and high-performance electronic devices.

1.5 Problem Statement

As semiconductor devices continue to shrink, conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) face significant challenges, notably concerning power efficiency and leakage current. MOSFETs exhibit limitations in achieving lower sub-threshold swings and maintaining performance at reduced power supply voltages, particularly in small-scale electronic devices. This inefficiency hampers the advancement of energy-efficient electronics, necessitating the exploration of alternative transistor technologies. Tunnel Field-Effect Transistors (TFETs) emerge as promising solutions due to their potential to address MOSFET limitations. However, a comprehensive understanding of TFET advantages and limitations compared to MOSFETs is essential for their widespread adoption. The development of TFETs aims to overcome MOSFET drawbacks by offering improved subthreshold swing, enhanced I_{ON}/I_{OFF} current ratio, reduced leakage current, tighter threshold voltage control, scalability, and immunity to short-channel effects. Therefore, the investigation into TFETs' viability as MOSFET replacements is crucial for advancing energy-efficient semiconductor technologies and meeting the growing demand for low-power electronic devices.

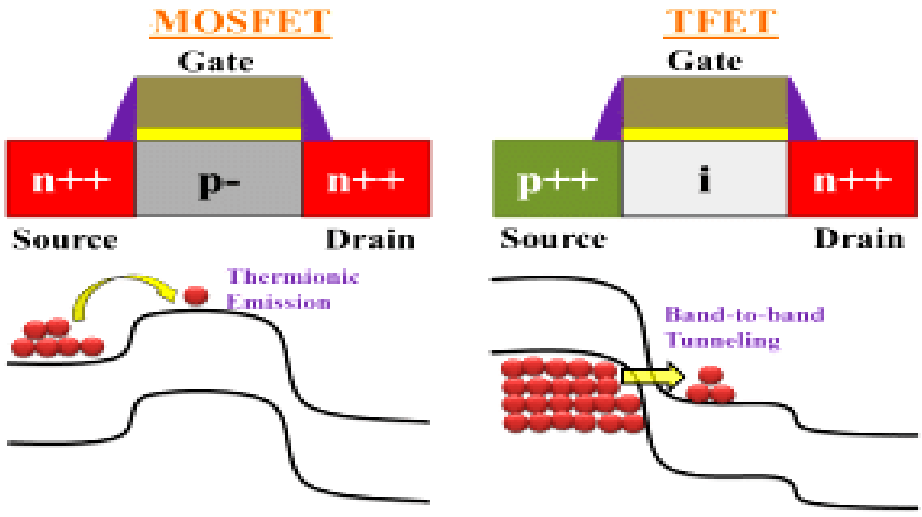

Figure 3. Comparison between MOSFET AND TFET

CHAPTER – 2
LITERATURE STUDY

[1] Sanjay Kumar, Ekta Goel, Kunal Singh, Balraj Singh, Member, IEEE, Prince Kumar Singh, Kamalaksha Baral, and Satyabrata Jit, Senior Member, IEEE 2017 "2-D Analytical Modeling of the Electrical Characteristics of Dual-Material Double- Gate TFETs With a SiO2/HfO2 Stacked Gate-Oxide Structure"

A physics-based 2-D analytical model for surface potential, electric field, drain current, subthreshold swing (SS) and threshold voltage of dual-material (DM) double-gate tunnel FETs (DG TFETs) with SiO2/HfO2 stacked gate-oxide structure has been developed in this paper. The parabolic-approximation technique, with suitable boundary conditions, has been used to solve Poisson's equation in the channel region. Channel potential model is used to develop electric field expression. The drain current expression is extracted by analytically integrating the band-to-band tunnelling generation rate over the channel thickness. Threshold voltage has been extracted by maximum transconductance method. The proposed model also demonstrates that the proper choice of work function for both the latterly contacting gate electrode (near the source and drain) materials which can give better results in terms of input-output characteristics, SS, and ION/IOFF than the conventional TFET devices. Although the proposed model has been primarily developed for Si-channel-based DM DG TFET devices, however, the model has also been shown to be applicable for other materials like SiGe (indirect bandgap) and InAs channel-based TFET structures. The results of the proposed model have been validated against the TCAD simulation results obtained by using SILVACO ATLAS device simulation software.

[2] Shashi Bala and Mamta Khosla 2018 *J. Semiconductor* "Design and simulation of nanoscale double-gate TFET/tunnel CNTFET"

A double-gate tunnel field-effect transistor (DG tunnel FET) has been designed and investigated for various channel materials such as silicon (Si), gallium arsenide (GaAs), aluminium gallium arsenide (Al*x*Ga1−*x*As) and CNT using a nano ViDES Device and TCAD SILVACO ATLAS simulator. The proposed devices are compared on the basis of inverse subthreshold slope (SS), *I*ON/*I*OFF current ratio and leakage current. Using Si as the channel material limits the property to reduce leakage current with scaling of channel, whereas the

Al*x*Ga1−*x*As based DG tunnel FET provides a better *I*ON/*I*OFF current ratio (2.51 × 106) as compared to other devices keeping the leakage current within permissible limits. The performed simulation of the CNT based channel in the double-gate tunnel field-effect transistor using the nano ViDES shows better performance for a sub-threshold slope of 29.4 mV/dec as the channel is scaled down. The proposed work shows the potential of the CNT channel based DG tunnel FET as a futuristic device for better switching and high retention time, which makes it suitable for memory based circuits.

[3] Mahdi Gholizadeh and Seyed Ebrahim Hosseini 2014 "A 2-D Analytical Model for Double-Gate Tunnel FETs"

This paper presents a 2-D analytic potential model for double-gate (DG) tunnel field effect transistors (TFETs) by solving the 2-D Poisson's equation. From the potential profile, the electric field is derived and then the drain current expression is extracted by analytically integrating the band-to-band tunnelling generation rate over the tunnelling region. The model well predicts the potential, subthreshold swing (SS), and transfer and output characteristics of DG TFETs. We analyse the dependence of the tunnelling current on the device parameters by varying the gate oxide dielectric constant, gate oxide thickness, body thickness, channel length and channel material and also demonstrate its agreement with TCAD simulation results. The SS which describes the switching behaviour of TFETs, is derived from the current expression. The comparisons show that the SS of our model well coincides with that of simulations.

[4] Samantha Lubaba Noor, Samia Safa, Md. Ziaur Rahman Khan 2016 "A silicon-based dual-material double-gate tunnel field-effect transistor with optimized performance"

The down-scaling of conventional MOSFETs has led to an impending power crisis, in which static power consumption is becoming too high. In order to improve the energy-efficiency of electronic Circuits, small swing switches are interesting candidates to replace or complement the MOSFETs used today. Tunnel FETs, which are gated p-i-n diodes who's on-current arises from band-to-band tunnelling, are attractive new devices for low-power applications due to their low off-current and their potential for a small subthreshold swing. Since Tunnel FETs are emerging devices, the most important future work will be to fabricate fully optimized n- and p-type devices, and to develop accurate compact models for their incorporation into circuits.

[5] Weixiang Zhang, Tarek Ragab, Cemal Basaran 2019 "Electrostatic Doping-Based All GNR Tunnel FET: An Energy-Efficient Design for Power Electronics"

The paper presents an Electrostatic Doping (ED)-based graphene nanoribbon (GNR) Tunneling Field-Effect Transistor (TFET) with a tri-gate design, employing the Extended Hickel (EH) semiempirical method to explore device characteristics. Notably, the GNR-TFET exhibits an exceptional ION/IOFF ratio exceeding 10^14, alongside an on-state current of approximately 103 μA/μm and a sub-60 mV/decade subthreshold swing. Through experimentation, the study identifies armchair GNRs with specific widths as optimal for achieving high ION/IOFF ratios, while longer channel lengths effectively suppress short-channel effects. Additionally, the paper delves into the scaling behavior of the ED-based GNR TFET, revealing that smaller gate-to-gate distances facilitate enhanced performance. Importantly, the study addresses the critical issue of creating a p-i-n (n-i-p) junction in the channel, crucial for TFET operation. Unlike conventional silicon based TFETs, the 2D structure of graphene necessitates more complex doping techniques. While chemical doping remains challenging, the paper proposes Electrostatic Doping (ED) as a feasible solution, utilizing an electric field to adjust the Fermi level for n-type or p-type doping. By leveraging ED, the paper bridges the gap between theoretical studies and practical applications, offering valuable insights into the design, fabrication, and scaling considerations of ED-based GNR TFETs for energy-efficient power electronics.

CHAPTER – 3
METHODOLOGY

3.1 PROPOSED SYSTEM

To simulate a Tunnel Field-Effect Transistor (TFET) for achieving low power and high-speed performance, first, we establish the device's physical structure and material properties. Then, using computer software like TCAD tools, we model the behavior of electrons as they tunnel through the transistor's thin barrier layer. We simulate various operating conditions such as voltage, temperature, and doping levels to understand how these affect TFET performance. Next, we analyze the simulation results to optimize the device design for low power consumption and high-speed operation. This involves tweaking parameters like gate voltage and channel length to enhance tunneling efficiency while minimizing leakage current. Finally, we validate our simulation by comparing the results with experimental data, ensuring our TFET design meets the desired performance criteria for low power consumption and high-speed operation.

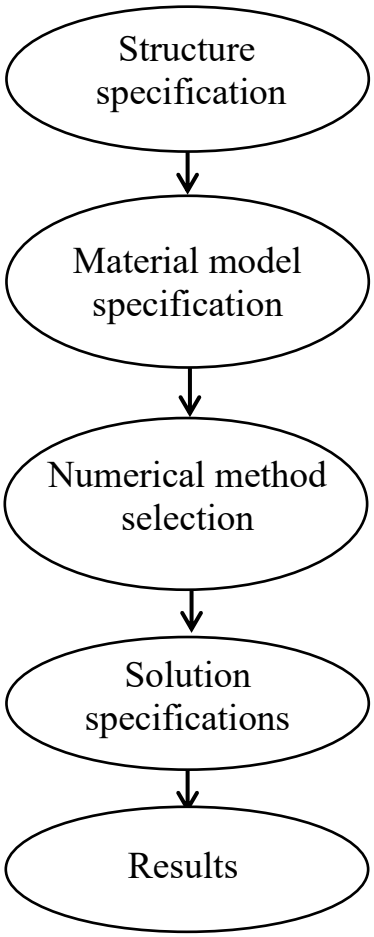

Figure 4.Proposed System Architecture

In this proposed work, researchers conducted a comprehensive study on Double-Gate Tunnel Field Effect Transistors (TFETs) to investigate their performance characteristics under varying parameters. Specifically, they explored the impact of variations in gate work function, intrinsic layer thickness, and gate length on the sub-threshold swing (SS) and the ratio of on-current (I_{ON}) to off-current (I_{OFF}), crucial metrics for evaluating transistor performance.

Firstly, the researchers varied the gate work function across a range from 3.8 to 4.6 eV in increments of 0.4 eV. They observed that as the gate work function increased, the sub-threshold swing decreased from 97.8 to 39.6 mV/dec. This trend indicates that a higher gate work function contributes to improved transistor performance by reducing the SS, which is desirable for achieving efficient transistor operation.

Secondly, they investigated the effect of varying intrinsic layer thicknesses from 4 nm to 8 nm in steps of 2 nm. Here, they found that as the intrinsic layer thickness increased, the sub-threshold swing decreased from 24 to 40 mV/dec. This suggests that thinner intrinsic layers led to better transistor performance in terms of SS, likely due to enhanced tunneling effects.

Lastly, the researchers examined the impact of gate length variations ranging from 100 nm to 160 nm in steps of 30 nm. They observed that increasing the gate length resulted in a decrease in sub-threshold swing from 64 to 30 mV/dec. This indicates that longer gate lengths contribute to improved transistor performance by reducing SS, possibly by mitigating short-channel effects.

Subsequently, the researchers analyzed the obtained values to identify the best-case scenario for I_{ON}/I_{OFF} and SS. While they achieved a minimum SS of 24.3 mV/dec, they found that the associated I_{ON}/I_{OFF} values were suboptimal at 10^{10}. However, they identified a configuration with $I_{ON}/I_{OFF} > 10^{11}$ and an associated SS of 30 mV/dec. In this configuration, the intrinsic channel thickness was 6 nm, gate length was 160 nm, and gate work function was 4.2 eV, with a constant gate-oxide thickness of 2 nm.

Overall, this study provides valuable insights into the optimization of Double-Gate TFETs by elucidating the relationships between key parameters and performance metrics, paving the way for the development of high-performance low-power electronic devices.

3.2 ADVANTAGES OF PROPOSED SYSTEM

- Low subthreshold swing
- Reduced leakage current
- Improved ON/OFF current ratio
- Potential for low power operation
- High operational speed

3.3 SYSTEM REQUIREMENT SPECIFICATIONS

3.3.1 FUNCTIONAL AND NON-FUNCTIONAL REQUIREMENTS

Requirement analysis is a very critical process that enables the success of a system or software project to be assessed. Requirements are generally split into two types: Functional and non-functional requirements.

Functional Requirements: These are the requirements that the end user specifically demands as basic facilities that the system should offer. All these functionalities need to be necessarily incorporated into the system as a part of the contract. These are represented or stated in the form of input to be given to the system, the operation performed and the output expected. They are basically the requirements stated by the user which one can see directly in the final product, unlike the non-functional requirements.

Non-Functional Requirements: These are basically the quality constraints that the system must satisfy according to the project contract. The priority or extent to which these factors are implemented varies from one project to the other. They are also called as non-behavioral requirements.

They basically deal with issues like:

- Portability
- Maintainability
- Reliability
- Scalability
- Performance
- Reusability

- Flexibility

3.3.2 HARDWARE SPECIFICATIONS

- Processor: I3/Intel Processor
- RAM: 8GB (min)
- Hard Disk: 128 GB
- Key Board: Standard Windows Keyboard
- Mouse: Two or Three Button Mouse
- Monitor: Any

3.3.3 SOFTWARE SPECIFICATIONS

- Operating System: Windows 10
- Server-side Script: Silvaco
- IDE: Silvaco
- Tools Used: TCAD TonyPlot

3.4 TECHNOLOGIES USED

3.4.1 SILVACO

Silvaco is a leading provider of electronic design automation (EDA) software, offering a comprehensive suite of tools for semiconductor device simulation, process development, and circuit design. The software is widely utilized by researchers, engineers, and designers in the semiconductor industry to model and optimize various aspects of semiconductor devices.

Silvaco software provides advanced device simulation capabilities, allowing users to model the behavior of transistors, diodes, and other semiconductor devices. It enables a detailed understanding of device characteristics, helping researchers predict and optimize performance.

In addition to device simulation, Silvaco supports process simulation, allowing users to virtually replicate the semiconductor fabrication process. Researchers can explore the impact of different fabrication parameters, materials, and technologies on device performance.

Silvaco's Technology Computer-Aided Design (TCAD) simulation tools are crucial for analyzing and optimizing semiconductor processes. TCAD tools help researchers simulate the entire fabrication process, from material deposition to device packaging, providing insights into each stage's impact on overall performance.

Beyond individual devices, Silvaco offers tools for circuit design and simulation. This allows engineers to design and test complex integrated circuits, ensuring that the individual components work seamlessly together in the final product.

Silvaco's optimization tools enable researchers and engineers to fine-tune semiconductor devices and processes for enhanced performance and yield. This is essential in the semiconductor industry, where small improvements can have a significant impact on overall device reliability and efficiency.

Silvaco software plays a crucial role in technology development, allowing semiconductor companies to explore and validate new materials, processes, and designs. This accelerates the innovation cycle by providing a virtual platform for experimentation and optimization. Silvaco's suite includes tools for reliability analysis, enabling users to assess the long-term performance and durability of semiconductor devices. This is vital for ensuring that electronic components meet industry standards and operate reliably over extended periods.

Silvaco is known for its user-friendly interface, making it accessible to both seasoned professionals and newcomers in the semiconductor field. The software's intuitive design facilitates efficient workflow, allowing users to focus on the intricacies of semiconductor design and optimization.

Silvaco software has made a significant impact on the semiconductor industry by providing a versatile and powerful platform for device and process simulation. Its contributions to the development of innovative technologies, such as Double Tunneling Field Effect Transistors (Double TFETs), exemplify how Silvaco plays a pivotal role in shaping the future of semiconductor design and fabrication. Silvaco software adheres to industry standards, ensuring compatibility with established design and manufacturing practices. This compliance is crucial for semiconductor companies working within the framework of industry norms and guidelines.

Silvaco remains at the forefront of innovation, actively researching and developing new simulation technologies. The software's commitment to pushing the boundaries of semiconductor design and fabrication reflects a forward-looking approach, anticipating and addressing emerging challenges in the ever-evolving landscape of electronic devices.

3.4.2 Origin Lab

OriginLab Corporation is a renowned provider of data analysis and graphing software solutions tailored for scientists and engineers across various disciplines. Established in 1992 by a group of engineers and scientists, including Dr. C.P. Yang and Dr. B. Huang, OriginLab has since become a leading name in the realm of data visualization and analysis. Headquartered in Northampton, Massachusetts, OriginLab has expanded its reach globally, serving a diverse clientele spanning academia, industry, and government sectors.

At the core of OriginLab's offerings is its flagship product, Origin, a comprehensive software package designed to streamline the process of data analysis and graphing. Origin provides users with a versatile platform equipped with an array of powerful tools and functionalities, empowering researchers to extract valuable insights from their data with efficiency and precision. Whether dealing with experimental data, mathematical models, or statistical analyses, Origin's intuitive interface and extensive feature set cater to the diverse needs of users across various scientific and engineering domains.

One of Origin's standout features is its robust graphing capabilities, enabling users to create publication-quality graphs and visualizations with ease. From basic line plots and scatter plots to advanced 3D surface plots and contour plots, Origin offers a plethora of graph types to suit different data visualization requirements. Moreover, Origin's customizable graph templates and extensive formatting options allow users to tailor their graphs to meet specific presentation standards or publication guidelines.

In addition to its graphing prowess, Origin excels in data analysis, offering a rich suite of statistical tools and mathematical functions. Whether performing basic descriptive statistics, hypothesis testing, or complex multivariate analysis, Origin provides users with the tools they need to explore, analyze, and interpret their data effectively. Furthermore,

Origin's integration with programming languages such as Python and LabTalk enables users to extend its functionality through custom scripts and automation, enhancing workflow efficiency and flexibility.

Over the years, OriginLab has continued to evolve its software offerings in response to emerging trends and technological advancements in data analysis and visualization. This includes the integration of advanced features such as scripting automation, interactive plotting, and cloud-based collaboration, further enhancing Origin's versatility and adaptability to changing user needs. Moreover, OriginLab's partnerships with academic institutions, research organizations, and industry partners have facilitated the development of specialized modules and add-ons tailored for specific applications and domains.

In summary, OriginLab Corporation stands as a pioneer in the field of data analysis and graphing software, providing scientists and engineers with a powerful and intuitive platform for exploring, analyzing, and visualizing their data. With its rich feature set, robust performance, and commitment to user satisfaction, Origin continues to be the software of choice for researchers and professionals seeking to unlock the full potential of their data and accelerate scientific discovery and innovation.

3.5 STAGES OF OPERATIONS

3.5.1 ON-State

The "ON state" is a critical concept across various fields, particularly in electronics, physics, and engineering. It signifies the operational condition of a device or system when it is actively conducting or performing its intended function. The ON state is essentially the opposite of the OFF state, where the device is non-conducting or inactive.

In electronics, the ON state typically refers to the condition of a transistor or switch when it allows the flow of current between its terminals. Transistors, which are fundamental components in electronic circuits, can be in either an ON or OFF state depending on the control signals applied to them. For example, in a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), the ON state occurs when a sufficient voltage is applied to the gate terminal, allowing current to flow between the source and drain terminals. This ON state enables the

transistor to amplify signals, switch currents, or perform other functions vital to electronic devices.

Moreover, the concept of the ON state extends beyond individual components to entire systems and devices. For instance, in power electronics, such as inverters or rectifiers, the ON state denotes the period during which the device conducts electricity to deliver power to a load. In this context, achieving and maintaining the ON state efficiently is crucial for the performance and reliability of power electronic systems, especially in applications like renewable energy systems, electric vehicles, and industrial drives.

Furthermore, in the realm of semiconductor devices and integrated circuits, the ON state is synonymous with the active mode of operation, where transistors are conducting and performing computational or signal processing tasks. Integrated circuits consist of millions or even billions of transistors, each transitioning between ON and OFF states rapidly to execute complex functions, such as arithmetic operations, data storage, and communication.

Beyond electronics, the concept of the ON state finds applications in diverse fields such as optics, fluid dynamics, and even social sciences. In optics, for instance, the ON state of a laser refers to the emission of coherent light when the lasing medium is appropriately stimulated. In fluid dynamics, valves and actuators have ON states when they allow fluid flow or motion through a system, regulating processes in industries like manufacturing and transportation.

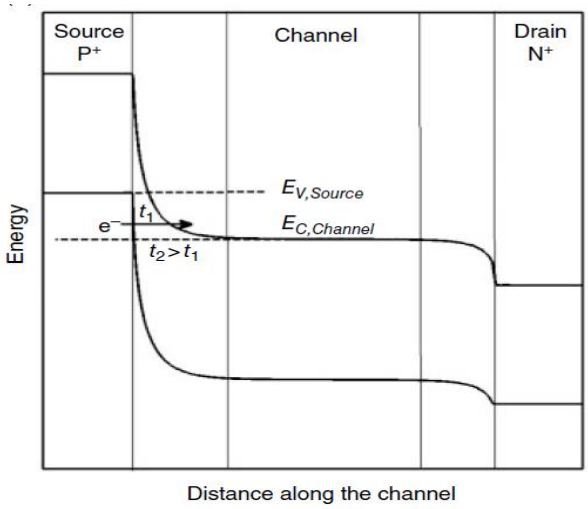

Figure 5. ON state energy band diagram TFET.

3.5.2 OFF-State

In the realm of Tunnel Field-Effect Transistors (TFETs), the "OFF state" holds paramount significance, delineating the condition when minimal or negligible current flows between the source and drain terminals. Unlike conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), TFETs leverage quantum tunneling phenomena to modulate current flow, thereby presenting distinct characteristics in their OFF-state operation. n TFETs, the OFF state is pivotal for achieving low-power operation and minimizing leakage currents, crucial factors in enhancing energy efficiency and prolonging battery life in electronic devices. Unlike MOSFETs, which rely on the formation of an induced channel between the source and drain terminals, TFETs exploit the phenomenon of band-to-band tunneling to control current flow. When the device is in its OFF state, the bandgap engineering and device architecture prevent significant carrier tunneling, effectively minimizing leakage currents and ensuring quiescent operation.

The OFF state in TFETs is intricately linked to the band structure and material properties, with careful design considerations aimed at optimizing device performance. By tailoring the bandgap and energy barriers within the semiconductor material, engineers can effectively control the tunneling probability and achieve robust OFF state characteristics, critical for achieving high-performance and reliable TFET devices.

Furthermore, in the context of TFET-based logic circuits and digital systems, the OFF state represents the state of logical "0", indicating the absence or minimal presence of current flow. This distinction is fundamental for realizing robust logic operations and ensuring proper functionality in digital circuits, where precise control of ON and OFF states is essential for computational tasks and data processing.

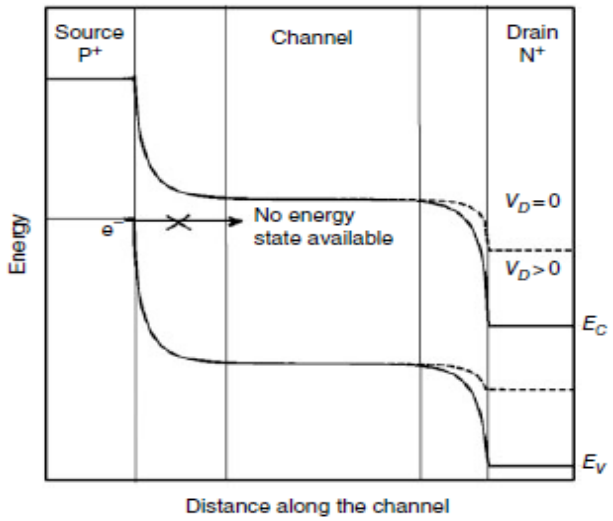

Figure 6. OFF state energy band diagram of TFET

3.7 FLOWCHART

The flowchart for simulating Tunnel Field Effect Transistors (TFETs) typically involves several key steps, each contributing to the comprehensive analysis of device behavior and performance.

In the initial steps, the meshing process is crucial for discretizing the device structure into smaller elements, facilitating numerical simulations. Following mesh generation, the device region is defined, specifying the geometric boundaries and material properties. Electrodes, including source, drain, and gate, are then identified, laying the foundation for subsequent electrical simulations. Doping profiles are established to model the distribution of charge carriers within the device, influencing its conductivity and performance characteristics. Material properties, such as bandgap and electron affinity, are assigned to accurately capture the semiconductor physics underlying TFET operation. Contact properties are defined to model the interfaces between different materials, ensuring realistic device behavior. Finally, simulation methods are selected, such as drift-diffusion or quantum transport, based on the desired level of accuracy and computational efficiency.

Once the setup is complete, the simulation process begins with logging relevant parameters and progresses through iterative solving of the device equations. After

convergence is achieved, data is loaded and analyzed, with TonyPlot serving as a powerful tool for visualizing simulation results. Finally, the extracted information is saved for further analysis or device optimization.

In summary, the flowchart for TFET simulation encompasses meshing, region and electrode definition, doping and material assignment, contact modeling, simulation method selection, iterative solving, data logging and analysis, visualization using TonyPlot, and data extraction and saving. These steps collectively enable a thorough understanding of TFET behavior and aid in the development of high-performance semiconductor devices.

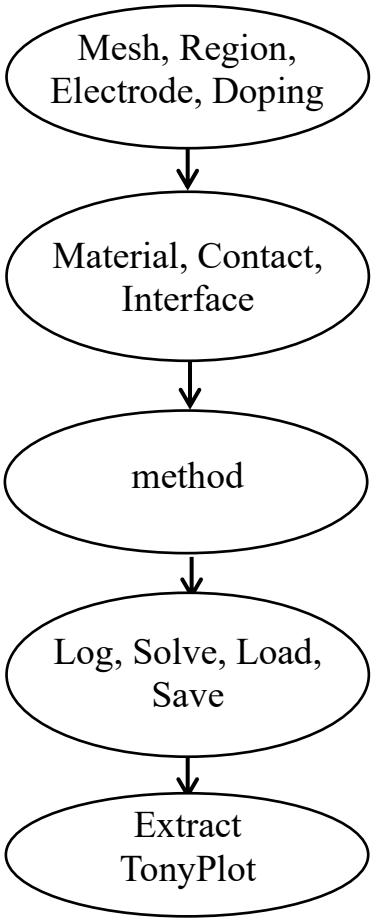

Figure 7. Flowchart of Proposed System

CHAPTER – 4

RESULTS

4.1 SINGLE GATE TFET

DEVICE STRUCTURE

The diagrams illustrating the single gate TFETs can be found in Figure 8. This device features a p+ source, an intrinsic channel and an n+ drain region. All simulations have been conducted using Silvaco's Atlas platform, employing the band-to-band tunneling model for accurate representation of device behavior.

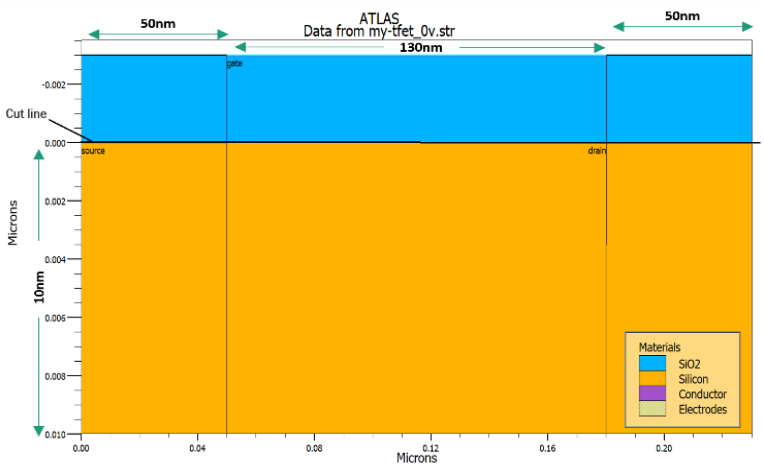

Figure 8. Schematic structure of Single gate TFET.

The schematic of the proposed device structure for single gate is shown in Figure 8. The n-channel TFET device structure has three regions named as source, intrinsic channel, and drain. TFET devices consist of intrinsic channel of silicon (Si) material and thickness of 10 nm. A doping concentrations of 10^{19} cm^{-3} (p-type) in source, 10^{15} cm^{-3} in channel, and 10^{19} cm^{-3} (n-type) in drain regions is kept. Gate contact in the TFET devices is kept as Schottky type and work function is set as 4.2 eV.

ENERGY BAND DIAGRAMS

OFF STATE

When the TFET is in off state there is no flow of charge carriers from valance band to conduction band as the formation of tunnel is absent. Because the source is p-type, there are few free electrons available. So, only a few electrons can enter the channel.

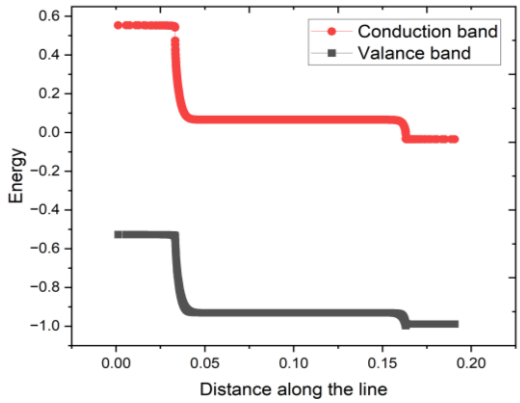

Figure 9.Energy band diagram for the single gate TFET in the OFF state.

ON STATE

As the gate voltage (VGS) increases, the valence band in the source aligns with the conduction band in the channel. However, with the alignment of the source valence band and the channel conduction band, electrons can now tunnel from valance band to conduction band.

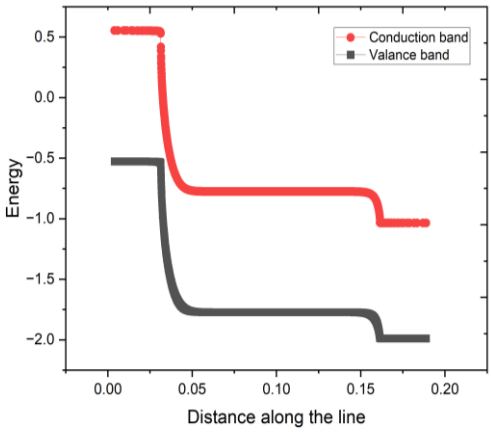

Figure 10.Energy band diagram for the single gate TFET in the ON state.

INPUT AND OUTPUT CHARECTERISTICS

Firstly gate-drain characteristics of SG-TFET is analyzed, and result is shown in Figure 11. From the SG-TFET, I_D (log) – V_{GS} characteristics it is found that device threshold voltage < 0 V. This is attributed to weak gate control which results in sub-threshold conduction.

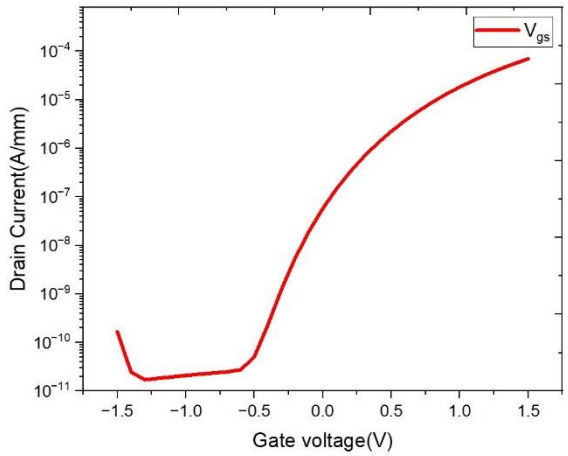

Figure 11. $I_D - V_{GS}$ characteristic in log scale of Single gate TFET, V_{DS} = 1.5 V is used.

I_{ON} / I_{OFF} value is ≈ 10^7. SG-TFET output characteristics, I_D – V_{DS} are shown in Figure 12. At higher gate voltage = 1.5 V, nonlinear increase in the drain current is found.

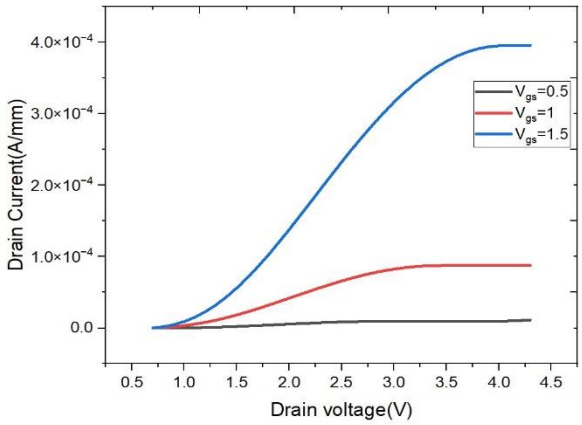

Figure 12. I_D-V_{DS} characteristic of Single gate TFET for 0.5V,1V,1.5V.

4.2 DOUBLE GATE TFET

DEVICE STRUCTURE

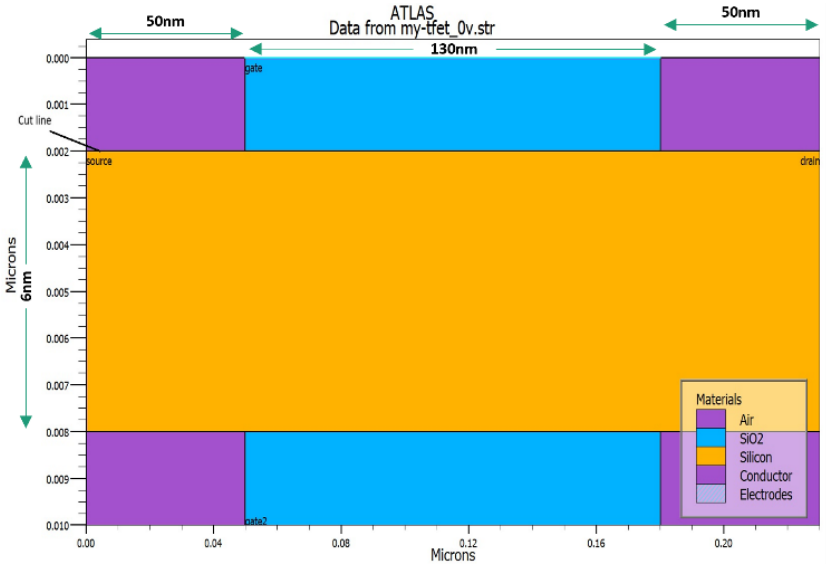

Figure 13. Schematic structure of Double gate TFET.

ENERGY BAND DIAGRAM

OFF STATE

When the TFET is in off state there is no flow of charge carriers from valance band to conduction band as the formation of tunnel is absent. Because the source is p-type, there are few free electrons available. So, only a few electrons can enter the channel, keeping the off-state current very low.

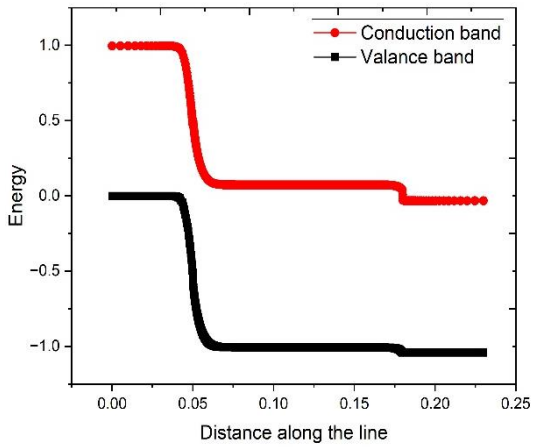

Figure 14. Energy band diagram for the double gate TFET in the OFF state.

ON STATE

As the gate voltage (VGS) increases, the valence band in the source aligns with the conduction band in the channel. However, with the alignment of the source valence band and the channel conduction band, electrons can now tunnel from valance band to conduction band.

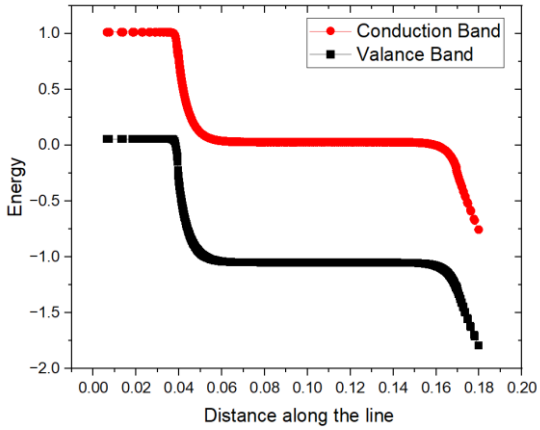

Figure 15. Energy band diagram for the Double gate TFET in the ON state.

INPUT AND OUTPUT CHARECTERISTICS

The gate-drain characteristics of DG-TFET is analyzed, and result is shown in Figure 18. From the DG-TFET, I_D (log) – V_{GS} characteristics is found.

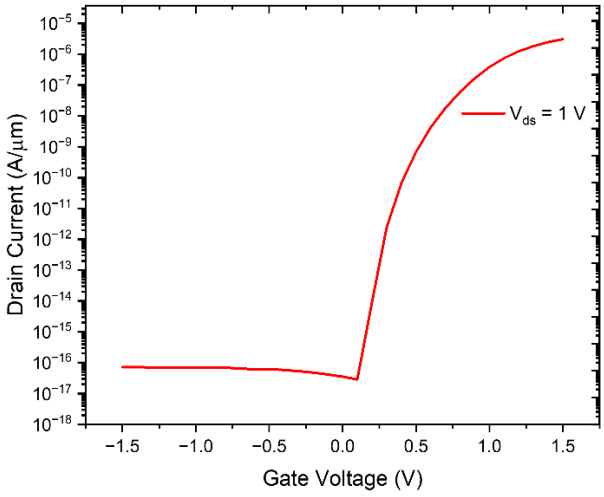

Figure 16. I_D -V_{GS} characteristic in log scale of double gate TFET.

The I_{ON} / I_{OFF} value is ≈ 10^7. SG-TFET output characteristics, $I_D - V_{DS}$ are shown in Figure 12. At higher gate voltage = 1.5 V, nonlinear increase in the drain current is found.

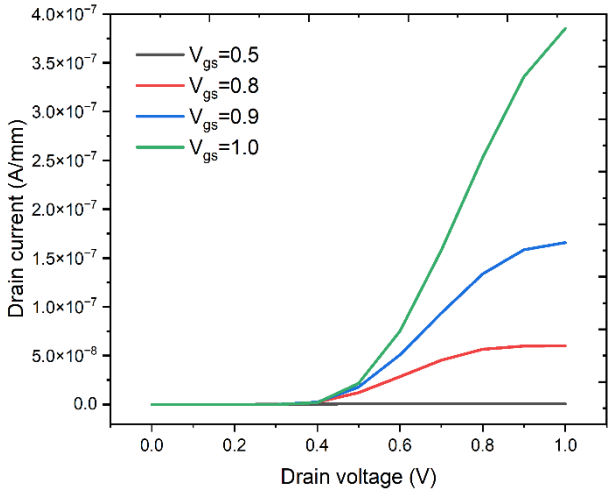

Figure 17. I_D-V_{DS} characteristic of double gate TFET

Varying work function

Gate work function varying from 3.8 to 4.6 eV exhibits sub-threshold swing (SS) values between 39 to 100 mV/dec and ION/IOFF ratio on order of $10^{10} - 10^{11}$.

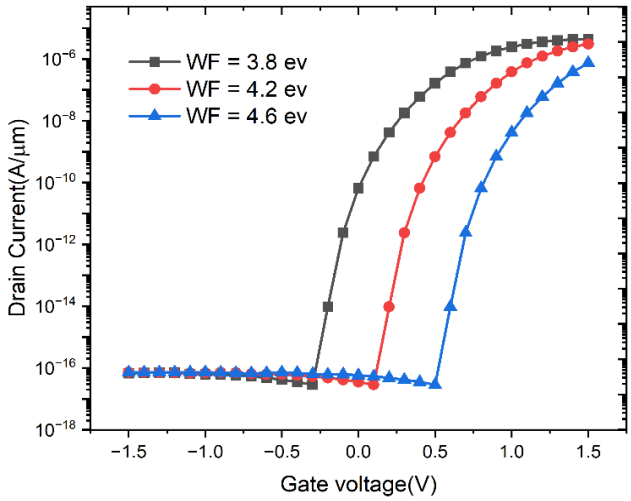

Figure 18. $I_D - V_{GS}$ characteristic of double gate TFET for 3.8ev,4.2ev,4.6ev.

Varying intrinsic layer

The intrinsic layer thickness varying from 4 nm to 8 nm exhibits sub-threshold swing (SS) between 23 - 40 mV/dec and ION/IOFF ratio on order of $10^{10} - 10^{11}$.

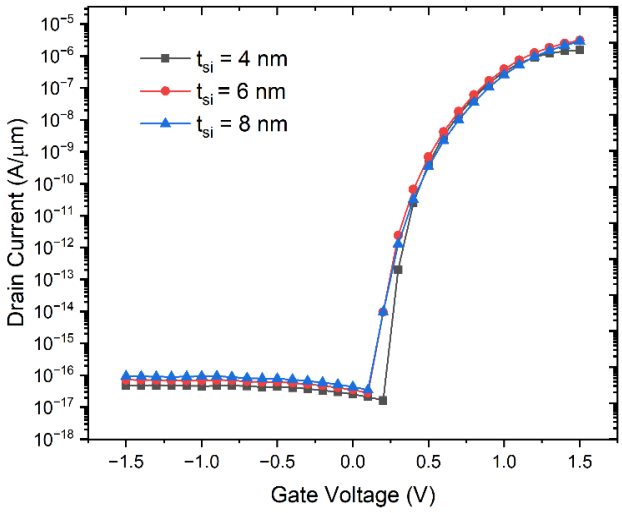

Figure 19. $I_D - V_{GS}$ characteristic of double gate TFET for 4 nm,6 nm,8 nm.

Varying gate-length

The intrinsic layer thickness varying from 100 nm to 160 nm exhibits sub-threshold swing (SS) between 30 - 64 mV/dec and ION/IOFF ratio on order of $10^{10} - 10^{11}$.

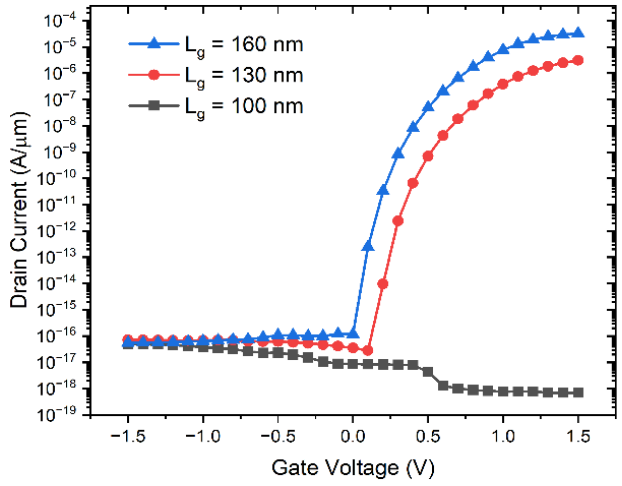

Figure 20. $I_D - V_{GS}$ characteristic of double gate TFET for 160 nm,130 nm,100 nm.

RESULTS COMPARISON

In further analysis of gate length scaling for the double gate TFET device, in ON state, I_{ON}/I_{OFF} ratio is calculated for 3 different gate lengths. As a result, the gate length of double gate TFET is directly proportional to I_{ON}/I_{OFF} ratio. Because, the probability for electrons to tunnel through the barrier is negligible, giving rise to I_{ON}/I_{OFF} ratio of 10^{11}.

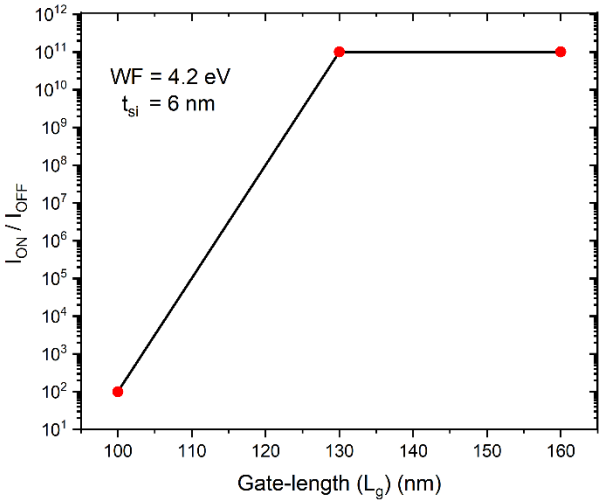

Figure 21.Variation of I_{ON} / I_{OFF} versus gate-length for fixed values of intrinsic channel thickness and gate work function.

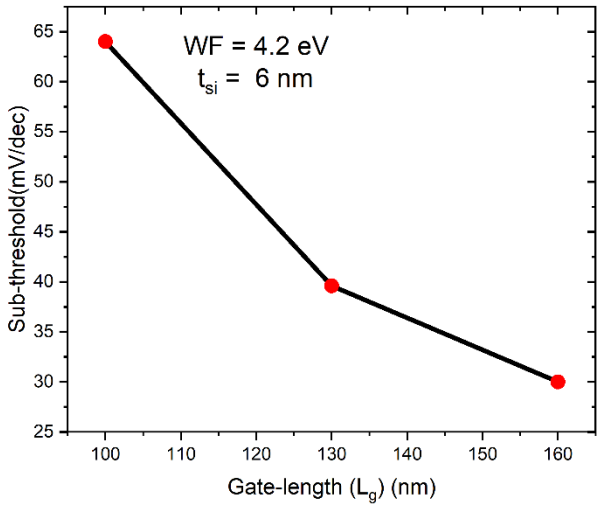

Figure 22.Variation of SS versus gate-length for fixed values of intrinsic channel thickness and gate work function.

Table 1.Values of different input work function and two output parameters (i.e SS, I_{ON}/I_{OFF}) are extracted from $I_D - V_{GS}$ curves for DG-TFETs.

S. No	Work Function (eV)	Sub-threshold Swing (mV/dec)	I_{ON}/I_{OFF}
1	3.6	97	10^{11}
2	4.2	39	10^{11}
3	4.6	39	10^{10}

From Table 1 it is observed that the direct proportionality relationship between gate work function and sub-threshold swing due to higher tunnelling between drain and channel. Varying gate work function from 3.6 to 4.6 eV there is a reduction of subthreshold swing from 97 to 39 mV/dec

Table 2.Values of different input intrinsic layer thickness and two output parameters (i.e SS, ION/IOFF) are extracted from ID – VGS curves for DG-TFETs.

S. No	Intrinsic layer thickness (nm)	Sub-threshold Swing (mV/dec)	I_{ON}/I_{OFF}
1	4	23	10^{11}
2	6	39	10^{11}
3	8	40	10^{10}

The table 2 presents data on intrinsic layer thickness, sub-threshold swing, and ION/IOFF ratio for three distinct configurations. As the layer thickness increases from 4 to 8 nm, both the sub-threshold swing and the ION/IOFF ratio display noticeable shifts. Specifically, there's increment in sub-threshold swing with increasing thickness, while the I_{ON}/I_{OFF} ratio demonstrates a variation across different thickness levels.

Table 3.Values of different input gate-length and two output parameters (i.e SS, ION/IOFF) are extracted from ID – VGS curves for DG-TFETs.

S. No	Gate-length (nm)	Sub-threshold Swing (mV/dec)	I_{ON}/I_{OFF}
1	100	64	10^2
2	130	39	10^{11}
3	160	30	10^{11}

The table 2 presents the gate-length variations with corresponding sub-threshold swing and I_{ON}/I_{OFF} ratios across three configurations. With increasing gate-length from 100 to 160 nm a notable decrease in both sub-threshold swing and I_{ON}/I_{OFF} ratio. This suggests that longer gate-lengths are associated with improved device performance.

Table 4. Values of different input parameters and two output parameters extracted from ID – VGS curves for DG-TFETs, optimized output parameters values along with respective input parameters are highlighted.

S. No	Input Parameters			Output Parameters	
	Intrinsic layer thickness (nm)	Gate-length (nm)	Work function (eV)	Sub-threshold Swing (mV/dec)	I_{ON}/I_{OFF}
1	4	130	4.2	24.3	10^{10}
2	6	160	4.2	30	10^{11}
3	6	130	4.6	39.6	10^{9}
4	6	130	4.2	39.6	10^{11}
5	8	130	4.2	40.9	10^{11}
6	6	100	4.2	64.1	10^{2}
7	6	130	3.8	97.8	10^{10}

The table offers a comprehensive overview of various input and output parameters for different transistor configurations. It includes intrinsic layer thickness, gate-length, work function, sub-threshold swing, and ION/IOFF ratio. Each row presents a unique combination of these parameters, reflecting the diverse settings under investigation. Analyzing this data can unveil insights into how different input configurations impact the resulting transistor performance, crucial for optimizing device design and functionality.

CHAPTER – 5

CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION

This study presents the simulation of single and double gate TFETs to determine optimal device structures for low-power and fast switching applications. By utilizing the 2-D Silvaco TCAD tool and appropriate physical models, multiple simulation iteration was performed. Subsequently, for double gate TFETs the effect of gate work function, intrinsic layer thickness, and gate-length on sub-threshold swing (SS) and ION/IOFF are evaluated. Single gate TFETs achieved an ION/IOFF ratio of 10^7, and for optimized double gate TFET it is measured as > 10^{11}. On the other hand, extracted value of SS for optimized double gate TFET is calculated as low as 24.3 mV/dec. It is observed that for gate-lengths of 130 and 160 nm, I_{ON} / I_{OFF} remains almost constant at 10^{11}, however, SS decreases from 39.6 to 24.3 mV/dec, at the cost of one order lower I_{ON} / I_{OFF}. After analyzing the simulation results for the double gate TFETs, the optimized values of I_{ON} / I_{OFF} = 10^{11} and SS = 30 mV/dec are selected. The device parameters associated for these values are intrinsic channel thickness t_{Si} = 6 nm, gate-length LG = 160 nm, and gate work function = 4.2 eV. The optimized double gate TFET with ION / IOFF = 10^{11} and SS = 30 mV/dec is expected to outperform single gate TFET, and would find more suitability in low-power and high-speed microelectronics applications.

TFETs, with their unique features, show great potential as a more efficient alternative to traditional transistors like MOSFETs. These simulations have acted like a window into a new world of possibilities in electronic design. By delving into the comparisons between TFETs and MOSFETs, it's evident that TFETs could be a key player in addressing issues related to energy efficiency and overall performance. It's akin to discovering a more eco-friendly and high-performing engine for our electronic devices.
The challenges and opportunities uncovered through simulations pave the way for future research, design optimizations, and practical implementations.

The collaborative efforts of academia, industry, and research communities will play a pivotal role in shaping a future where TFETs contribute significantly to the evolution of electronic devices, addressing not only the limitations of current technologies but also propelling us

toward a more sustainable and technologically advanced as we conclude this phase of simulation exploration, it is evident that TFETs hold the promise of unlocking a new paradigm in semiconductor design. The findings underscore the need for continued research and development to fine-tune TFET parameters, optimize their performance, and pave the way for their seamless integration into practical applications.

5.2 FUTURE SCOPE

Looking forward, the future holds immense promise for the practical application of TFETs in the semiconductor industry. The optimization of TFET designs based on simulation insights stands out as a priority, offering the prospect of creating transistors that not only outperform current technologies but also usher in a new era of energy-efficient electronics.

Moreover, the integration of TFETs into specific use cases, such as low-power circuits and sensors, presents exciting possibilities for diverse applications. Collaboration with industry partners becomes paramount at this juncture, facilitating the transition from simulation results to tangible implementations. The journey ahead involves addressing manufacturing challenges and ensuring that TFETs are not just theoretical marvels but practical solutions that can be mass-produced.

In essence, the conclusion of this simulation phase marks the beginning of a transformative journey. It beckons researchers, engineers, and industry stakeholders to collectively propel TFETs from simulated potential to real-world impact, shaping a future where electronic devices are not only smarter and more efficient but also more sustainable.

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CHAPTER-6

APPENDIX

6.1 Code of Single gate TFET:

```
go atlas
mesh space.mult=1.0
x.mesh loc=0.000 spac=0.01
x.mesh l=0.05 s=0.0001
x.mesh l=0.12 s=0.001
x.mesh l=0.18 s=0.0001
x.mesh loc=0.23 spac=0.01

y.mesh loc=-0.003 spac=0.0005
y.mesh loc=0.00 spac=0.0001
y.mesh loc=0.002 spac=0.0005
y.mesh loc=0.008 spac=0.0005
y.mesh loc=0.010 spac=0.0001
y.mesh loc=0.013 spac=0.0005

#Defining regions of the device
region num=1 y.max=0.000 material=Oxide
region num=2 y.min=0.000 y.max=0.010 material=Silicon
region num=3 y.min=0.010 material=Oxide

#Defining electrodes: channel length is assumed 30 nm
electrode name=gate x.min=0.05 x.max=0.18 top
electrode name=source x.max=0.05 y.min=0 y.max=0
electrode name=drain x.min=0.180 y.min=0.0 y.max=0.0
electrode name=gate2 x.min=0.05 x.max=0.18 bottom

#Defining another mesh for Band to Band tunneling
qtx.mesh loc=0.05 spac=0.0005
qtx.mesh loc=0.13 spac=0.0002
qtx.mesh loc=0.18 spac=0.0005
```

```
qty.mesh loc=0.000 spac=0.0005
qty.mesh loc=0.005 spac=0.0001
qty.mesh loc=0.010 spac=0.0005

# Defining the tunneling parameter for silicon
material material=Silicon me.tunnel=0.14 region=2

# Defining doping: The doping profile is assumed abrupt
doping uniform n.type conc=1e19 reg=2
doping uniform p.type conc=1e19 x.max=0.05 reg=2
doping uniform n.type conc=1e20 x.min=0.18 reg=2

# Defining contacts
#contact name=drain workfunction=4
contact name=gate workfunction=4
contact name=gate2 workfunction=4.5 common=gate

# Defining physical models
models bbt.nonlocal bbt.forward qtunn.dir=1 bgn consrh conmob print

#Included to improve the convergence
output val.band con.band charge e.lines

method newton
solve init
save outf=my-tfet_0v.str

# Simulating the transfer characteristics
# Id-Vgs
solve vdrain=0
solve vstep=0.1 vfinal=-0.5 name=drain
save outf=my-tfet-vd_0.5v.str
solve vstep=0.1 vfinal=1.5 name=drain
```

```
save outf=my-tfet-vd_1v.str

solve vgate=0
solve vstep=0.1 vfinal=1.6 name=gate
log outf=my-id-vgs.log
solve vstep=-0.1 vfinal=-1.5 name=gate
save outf=my-tfet-vd_1v.str
log off

# Id-VDS

solve vgate=0
solve vstep=0.1 vfinal=0.5 name=gate
log outf=id-vds-vgs_0.5.log
solve vdrain=0
solve vstep=0.1 vfinal=4.25 name=drain
log off

solve vgate=0
solve vstep=0.1 vfinal=1.0 name=gate
log outf=id-vds-vgs_1.0.log
solve vdrain=0
solve vstep=0.1 vfinal=4.25 name=drain
log off

solve vgate=0
solve vstep=0.1 vfinal=1.5 name=gate
log outf=id-vds-vgs_1.5.log
solve vdrain=0
solve vstep=0.1 vfinal=4.25 name=drain
log off

tonyplot -overlay id-vds-vgs_0.5.log id-vds-vgs_1.0.log id-vds-vgs_1.5.log
```

```
save outf=my-tfet-vd_1v.str
quit
```

6.2 Code of Double gate TFET:

```
go atlas
mesh space.mult=1.0
x.mesh loc=0.000 spac=0.01
x.mesh l=0.05 s=0.0001
x.mesh l=0.12 s=0.001
x.mesh l=0.18 s=0.0001
x.mesh loc=0.23 spac=0.01

y.mesh loc=0.000 spac=0.0005
y.mesh loc=0.002 spac=0.0001
y.mesh loc=0.006 spac=0.0001
y.mesh loc=0.008 spac=0.0001
y.mesh loc=0.010 spac=0.0005

#Defining regions of the device
region num=1 x.min=0 x.max=0.23 y.min=0.000 y.max=0.010 material=air
region num=2 x.min=0.05  x.max=0.18 y.min=0.000 y.max=0.010 material=oxide
region num=3 y.min=0.002 y.max=0.008 x.min=0.00 x.max=0.23 material= silicon

#Defining electrodes: channel legth is assumed 160 nm
electrode name=gate x.min=0.05 x.max=0.18 top
electrode name=source x.min=0.0 x.max=0.0 y.min=0.002 y.max=0.008
electrode name=drain x.min=0.23 x.max=0.23 y.min=0.002 y.max=0.008
electrode name=gate2 x.min=0.05 x.max=0.18 bottom

#Defining another mesh for Band to Band tunneling
qtx.mesh loc=0.05 spac=0.0005
qtx.mesh loc=0.115 spac=0.0001
qtx.mesh loc=0.18 spac=0.0005
```

```
qty.mesh loc=0.002 spac=0.0005
qty.mesh loc=0.005 spac=0.0001
qty.mesh loc=0.008 spac=0.0005

# Defining the tunneling parameter for silicon
material material=Silicon me.tunnel=0.14 region=3

# Defining doping : The doping profile is assumed abrupt
doping uniform n.type conc=1e15 reg=3
doping uniform p.type conc=1e20 x.max=0.05 reg=3
doping uniform n.type conc=1e18 x.min=0.18 reg=3

# Defining contacts
#contact name=drain workfunction=4
contact name=gate workfunction=4.2
contact name=gate2 workfunction=4.2 common=gate

# Defining physical models
models bbt.nonlocal bbt.forward qtunn.dir=1 bgn consrh conmob print

#Included to improve the convergence
output val.band con.band charge e.lines

method newton
solve init
save outf=my-tfet-vd_0v.str

# Simulating the transfer characteristics
# Id-Vgs
solve vdrain=0
solve vstep=0.1 vfinal=1.0 name=drain
save outf=my-tfet-vd_1.0v.str
solve vgate=0
```

```
solve vstep=0.1 vfinal=1.6 name=gate
log outf=my-id-vgs.log
solve vstep=-0.1 vfinal=-1.5 name=gate

extract init inf = "my-id-vgs.log"
extract name="nsubvt1"1.0/slope(maxslope(curve(abs(v."gate"),
log10(abs(i."drain")))))
log off

# ID-VDS

solve vgate=0
solve vstep=0.1 vfinal=0.5 name=gate
log outf=id-vds-vgs_0.5.log
solve vdrain=0
solve vstep=0.1 vfinal=1.0 name=drain
log off

solve vgate=0
solve vstep=0.1 vfinal=0.6 name=gate
log outf=id-vds-vgs_0.6.log
solve vdrain=0
solve vstep=0.1 vfinal=1.0 name=drain
log off

solve vgate=0
solve vstep=0.1 vfinal=0.7 name=gate
log outf=id-vds-vgs_0.7.log
solve vdrain=0
solve vstep=0.1 vfinal=1.0 name=drain
log off

solve vgate=0
```

```
solve vstep=0.1 vfinal=0.8 name=gate
log outf=id-vds-vgs_0.8.log
solve vdrain=0
solve vstep=0.1 vfinal=1.0 name=drain
log off

solve vgate=0
solve vstep=0.1 vfinal=0.9 name=gate
log outf=id-vds-vgs_0.9.log
solve vdrain=0
solve vstep=0.1 vfinal=1.0 name=drain
log off


solve vgate=0
solve vstep=0.1 vfinal=1.0 name=gate
log outf=id-vds-vgs_1.0.log
solve vdrain=0
solve vstep=0.1 vfinal=1.0 name=drain
log off

tonyplot -overlay id-vds-vgs_0.5.log id-vds-vgs_0.6.log id-vds-vgs_0.7.log id-vds-vgs_0.8.log id-vds-vgs_0.9.log id-vds-vgs_1.0.log
save outf=my-tfet-vd_1v.str
quit
```