Simulation Analysis of TFETs For Low Power And High-Speed Applications

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***Abstract*—This work presents simulation study of single and double gate TFETs to determine optimal device structure for the potential applications in low-power and fast switching electronic applications. 2-D Silvaco TCAD tool is used after employing appropriate physical models to analyze the effects of gate work function, intrinsic layer thickness, and gate-length on sub-threshold swing (SS) and I_{ON}/I_{OFF}. Double-gate TFETs offer enhanced electrostatic control and reduced leakage current over single gate TFET. The optimized double-gate device structure with intrinsic layer thickness of 6 nm, gate-length of 160 nm and gate work function of 4.2 eV resulted in I_{ON}/I_{OFF} of 10^{11} and SS of 30 mV/dec. Moreover, improved scalability and reduced short-channel effects make double-gate TFETs more suitable for advanced microelectronics devices.**

Keywords—Tunnel Field-Effect Transistor (TFET), doping concentration, gate work function, subthreshold swing, Silvaco ATLAS.

I. INTRODUCTION

The rapid advancement in transistor scaling and increased transistor density has led to short channel effects and significantly raised power density on chips. To maintain the same ON-current, the threshold voltage must scale proportionally with the supply voltage. However, reducing the threshold voltage leads to a sharp increase in the OFF-current and static leakage power due to the Boltzmann distribution of carriers, which limits the subthreshold swing (SS) to a minimum of 60mV/dec at room temperature. To address these challenges, new device structures like fully depleted silicon-on-insulators [1], Fin field-effect transistors (FETs) [2], and nanowire devices have been introduced [3]. Recently, there has been growing interest in exploring tunnelling-based devices for low-power applications, with Tunnel Field-Effect Transistors (TFETs) emerging as promising candidates due to their potential for steeper SS and lower OFF-current [4]-[5]. However, TFETs suffer from low ON-current and ambipolar conduction, limiting their application in digital circuits [6]-[11].Various techniques, including gate overlap/underlap [12], strained channel [13], high-k dielectric [14], and source region engineering, have been proposed to enhance the ON-current and suppress ambipolar conduction in TFETs [15]. Gate-material engineering has shown promise in improving carrier transport efficiency and suppressing short channel effects.

TFETs offer advantages in low power consumption and high-speed performance, making them suitable for applications in mobile devices, IoT devices, data processing, and telecommunications. Researchers have also proposed innovative structures like the dual-material double-gate (DMDG) TFET to improve device characteristics such as ON-current, threshold voltage, SS, and immunity against Drain Induced Barrier Lowering (DIBL) effects [16]. Ambipolarity was reduced by introducing step channel thickness in double gate TFETs (DG-TFETs) by M. Zhang et. al. However, it was done at cost of complex fabrication steps. For better switching, carbon nano tubes (CNT) channel based double gate (DG) tunnel FET was proposed by Shashi Bala and Mamta Khosla. But it provides better performance in terms of sub-threshold swing [17]. Sanjay Kumar *et. al.* proposed the work on the work functions of tunnelling and auxiliary gates of dual material (DM) double gate (DG) TFET. This results in lowest ambipolar current [18]. Based on work function, Si body thickness of dual material (DM) double gate (DG) TFET, the device performance was analysed for band profile and sub-threshold swing in [19].

While considerable research has been done on TFETs, to the best of our knowledge, there is no exclusive report regarding the impact of device physical parameters such as gate work function, intrinsic layer thickness, and gate-length on sub-threshold swing (SS) and I_{ON}/I_{OFF}. These parameters are crucial for assessing the suitability of TFETs for low-power and high-switching applications. The lack of comprehensive studies in this area serves as motivation for undertaking this project.

In this proposed work, it is found that, varying the gate work function from 3.8 to 4.6 eV (in step of 0.4 eV), the double-gate TFETs resulted sub-threshold swing (SS) of 97.8 and 39.6 mV/dec, respectively. On the other hand, when varying intrinsic layer thicknesses from 4 nm to 8 nm (in step of 2 nm), the double-gate TFETs resulted in sub-threshold swing (SS) of 24 to 40 mV/dec, respectively. Furthermore, on varying gate-length from 100 nm to 160 nm (in step of 30 nm), the double-gate TFETs resulted in sub-threshold swing (SS) values of 64 to 30 mV/dec, respectively. Subsequently, these values of input and output parameters are analyzed for best-case values of I_{ON} / I_{OFF} and SS for the proposed double gate TFET parameters. Though, minimum value of SS is found as low as 24.3 mV/dec, however, the associated I_{ON}/ I_{OFF} values equal to 10^{10}. The best-case value for I_{ON} / I_{OFF} is found > 10^{11}, and associated SS value equal to 30 mv/dec. For this particular case, associated intrinsic channel thickness was 6 nm, gate-length of 160 nm, and gate work function of 4.2 eV are found. The gate-oxide thickness was kept constant at 2 nm.

II. Device Structure And Simulation Settings

The schematic of the proposed device structure for single and double-gate is shown in Figure 1 and Figure 2. The n-channel TFET device structure has three regions named as source, intrinsic channel, and drain. Both of the TFET devices consist of intrinsic channel of silicon (Si) material and thickness of 6 nm. A doping concentrations of 10^{19} cm^{-3} (p-type) in source, 10^{15} cm^{-3} in channel, and 10^{19} cm^{-3} (n-type) in drain regions is kept. Gate contact in both of the TFET devices is kept as Schottky type and workfunction is set as 4.2 eV.

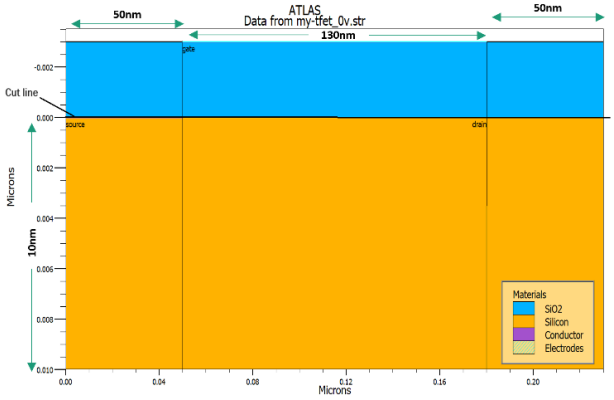

Figure 1. Schematic structure of Single gate TFET

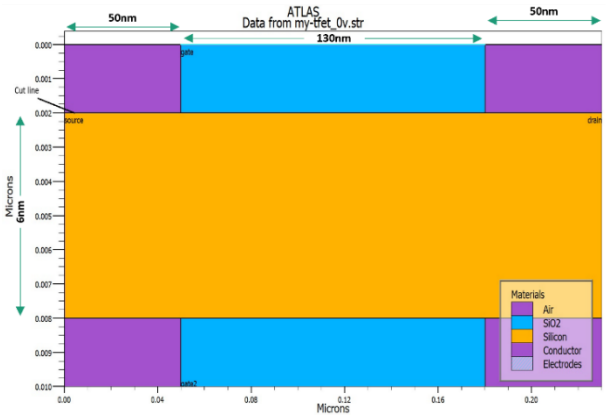

Figure 2. Schematic structure of Double gate TFET

All the characteritics analysis of the TFETs are performed using Silvaco Atlas TCAD physics-based device simulator. To capture TFET device phyiscal and electrical behaviour all appropriate models including blike Shockley-Read-Hall (SRH) for recombination, Fermi-Dirac for carrier statistics, and band-to-band tunneling model with default model parameters given in [20] are used in simulation deck. Band-to-band tunneling genartion rate is modelled using following equation.

$$G_{BBT} = D\ BB.A\ E^{(BB.\ GAMMA)}\ exp\left(-\frac{BB.B}{E}\right) \qquad (1)$$

Where, E is the electrical field magnitude, D is statistical factor, *BB.A*, *BB.B*, and *BB.GAMMA* are user defined parameters. All default values of *Si* semiconductor are used as given in [20] during all simulations. Based on the extracted energy band disgram for both single and double-gate TFETs, their ON- and OFF-state behaviour are discussed next.

A. OFF State

When the TFET is in off state there is no flow of charge carriers from valance band to conduction band as the formation of tunnel is absent. Because the source is p-type, there are few free electrons available. So, only a few electrons can enter the channel, keeping the off-state current very low.

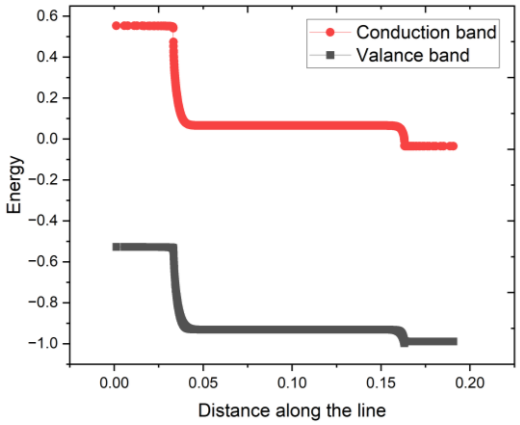

Figure 3. Energy band diagram for the single gate TFET in the OFF state.

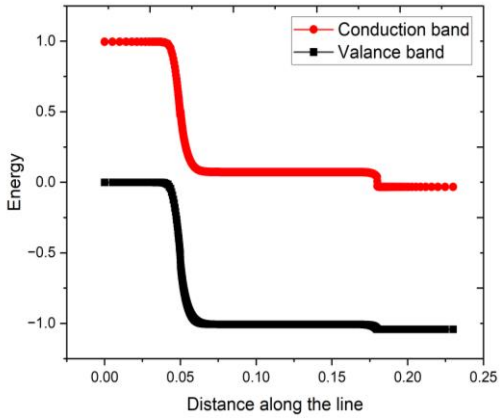

Figure 4. Energy band diagram for the double gate TFET in the OFF state.

B. ON State

As the gate voltage (V_{GS}) increases, the valence band in the source aligns with the conduction band in the channel. However, with the alignment of the source valence band and the channel conduction band, electrons can now tunnel from valance band to conduction band.

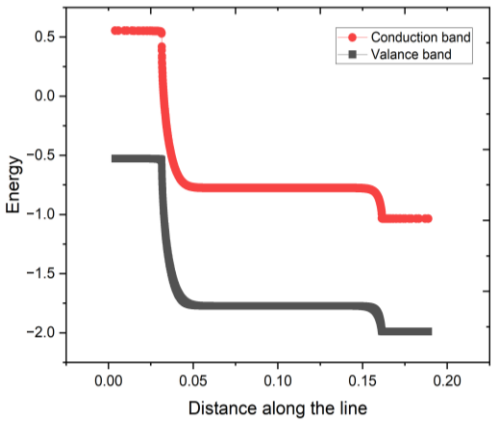

Figure 5. Energy band diagram for the single gate TFET in the ON state.

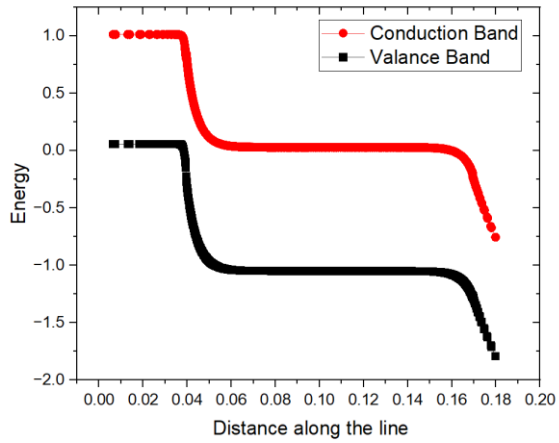

Figure 6. Energy band diagram for the double gate TFET in the ON state.

III. Resuts And Discussion

Firstly gate-drain characteristics of SG-TFET is analyzed, and result is shown in shown in Figure 7. From the SG-TFET, I_D (log) – V_{GS} characteristics it is found that device threshold voltage < 0 V. This is attributed to weak gate control which results in sub-threshold conduction. I_{ON} / I_{OFF} value is ≈ 10^7. SG-TFET output characteristics, I_D – V_{DS} are shown in Figure 2. At higher gate voltage = 1.5 V, nonlinear increase in the drain current is found.

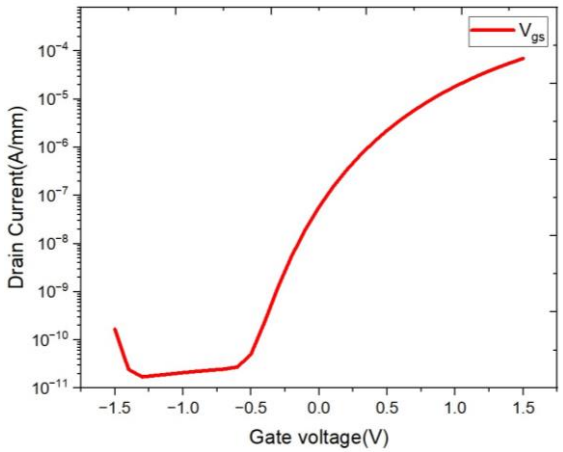

Figure 7. I_D – V_{GS} characteristic in log scale of Single gate TFET, V_{DS} = 1.5 V is used.

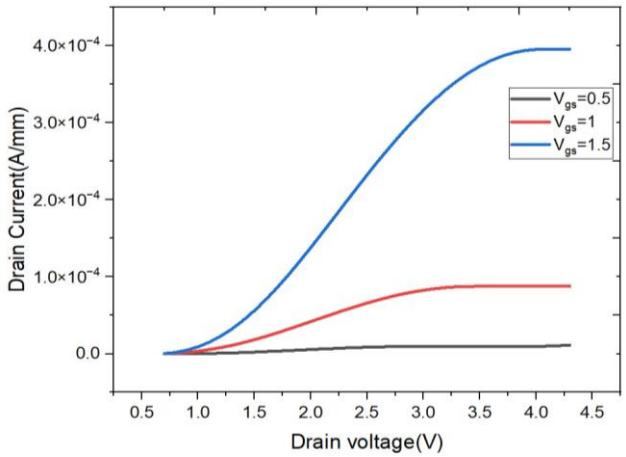

Figure 8. I_D – V_{DS} characteristic of Single gate TFET for three values of V_{GS}.

A. *Varying gate work function*

Gate work function varying from 3.8 to 4.6 eV exhibits sub-threshold swing (SS) values between 39 to 100 mV/dec and I_{ON}/I_{OFF} ratio on order of 10^{10} – 10^{11}.

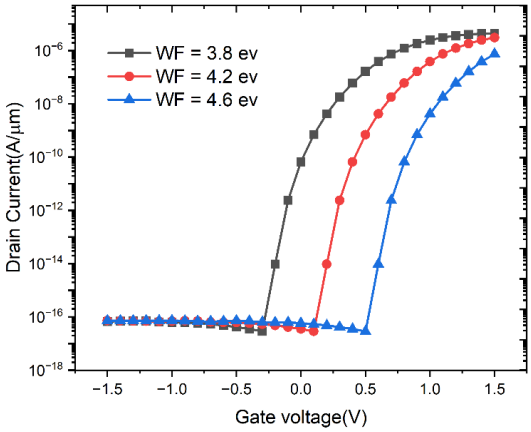

Figure 9. I_D – V_{GS} characteristic of double gate TFET for three different values of gate work functions.

B. *Varying intrinsic layer thickness*

The intrinsic layer thickness varying from 4 nm to 8 nm exhibits sub-threshold swing (SS) between 23 - 40 mv/dec and I_{ON}/I_{OFF} ratio on order of 10^{10} – 10^{12}.

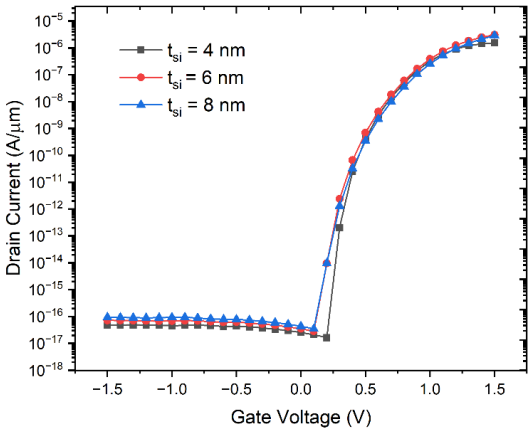

Figure 10. $I_D - V_{GS}$ characteristic of double gate TFET for 4 nm, 6 nm, and 8 nm.

C. *Varying gate-length*

The gate-length (L_G) is varying from 100 nm to 160 nm which resulted in sub-threshold swing (SS) between 30 - 64 mV/dec and I_{ON}/I_{OFF} ratio on order of 10^3 – 10^{12}.

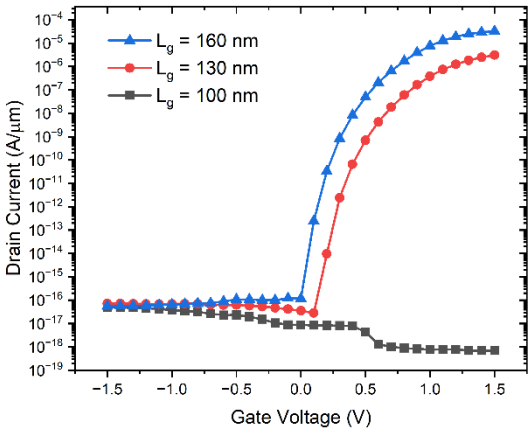

Figure 11. I_D – V_{GS} characteristic of double gate TFET for 160 nm, 130 nm, 100 nm.

To obtain the optimized values of SS and I_{ON} / I_{OFF} for the proposed DG-TFET (Figure 2), intrinsic channel thickness (t_{Si}), gate-length (L_g), and gate work function (WF) are varied. The simulation results of seven different interanimations are provided in Table 1. The highlighted row in Table 1 shows the optimized parameters for DG-TFET. Variations of I_{ON} / I_{OFF} and SS versus t_{OX} are shown in Figure 12, 13, respectively.

Table 1: Values of different input parameters and two output parameters extracted from I_D – V_{GS} curves for DG-TFETs, optimized output parameters values along with respective input parameters are highlighted.

S. No	Input Parameters			Output Parameters	
	Intrinsic layer thickness (nm)	Gate-length (nm)	Work function (eV)	Sub-threshold Swing (mV/dec)	I_{ON}/I_{OFF}
1	4	130	4.2	24.3	10^{10}
2	6	160	4.2	30	10^{11}
3	6	130	4.6	39.6	10^{9}
4	6	130	4.2	39.6	10^{11}
5	8	130	4.2	40.9	10^{11}
6	6	100	4.2	64.1	10^{2}
7	6	130	3.8	97.8	10^{10}

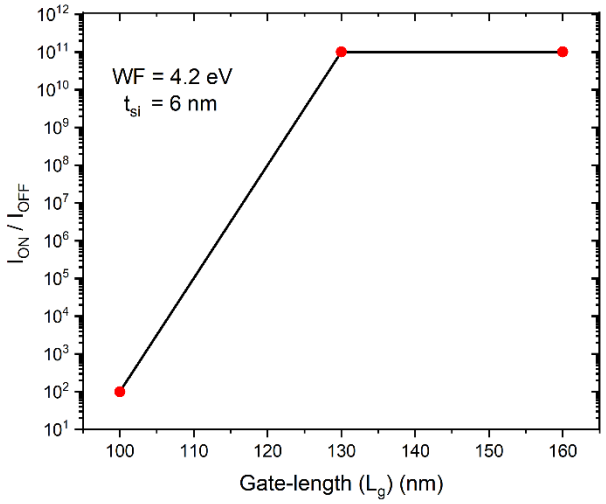

Figure 12. Variation of I_{ON} / I_{OFF} versus gate-length for fixed values of intrinsic channel thickness and gate work function.

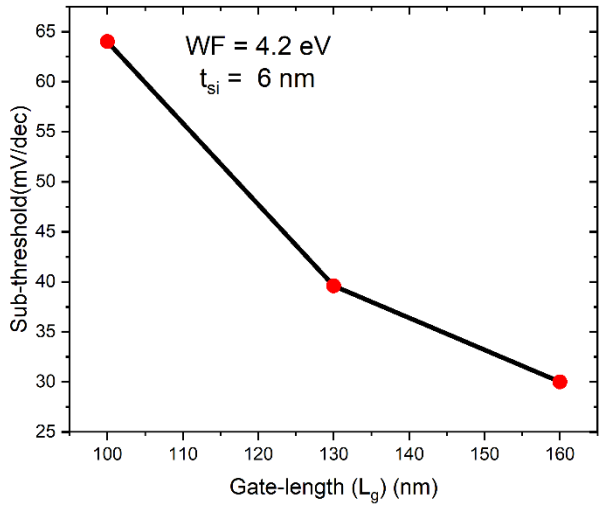

Figure 13. Variation of SS versus gate-length for fixed values of intrinsic channel thickness and gate work function.

IV. Conclusion

This study presents the simulation of single and double gate TFETs to determine optimal device structures for low-power and fast switching applications. By utilizing the 2-D Silvaco TCAD tool and appropriate physical models, multiple simulation iteration were performed. Subsequently, for double gate TFETs the effect of gate work function, intrinsic layer thickness, and gate-length on sub-threshold swing (SS) and I_{ON}/I_{OFF} are evaluated. Single gate TFETs achieved an I_{ON}/I_{OFF} ratio of 10^7, and for optimized double gate TFET it is measured as > 10^{11}. On the other hand extracted value of SS for optimized double gate TFET is calculated as low as 24.3 mV/dec. It is observed that for gate-lengths of 130 and 160 nm, I_{ON} / I_{OFF} remains almost constant at 10^{11}, however, SS decreases from 39.6 to 24.3 mV/dec, at the cost of one order lower I_{ON} / I_{OFF}. After analyzing the simulation results for the double gate TFETs, the optimized values of I_{ON} / I_{OFF} = 10^{11} and SS = 30 mV/dec are selected. The device parameters associated for these values are intrinsic channel thickness t_{Si} = 6 nm, gate-length LG = 160 nm, and gate work function = 4.2 eV. The optimized double gate TFET with I_{ON} / I_{OFF} = 10^{11} and SS = 30 mV/dec is expected to outperform single gate TFET, and would find more suitability in low-power and high-speed microelectronics applications.

Appendix

In a Tunnel Field-Effect Transistor (TFET), the subthreshold swing (SS) is a critical parameter that describes the device's ability to turn on and off efficiently at low drain currents. Unlike a MOSFET, where the SS is relatively constant over a range of gate voltages, the SS in a TFET varies with the gate voltage due to the unique tunnelling mechanism involved.

To understand the SS in TFETs, two types of subthreshold swing are typically defined:

A. Point Subthreshold Swing

The point subthreshold swing is measured at a specific gate voltage (V_{GS}). It is defined as the rate of change of drain-source voltage (V_{DS}) with respect to the natural logarithm of drain current (I_D) at that specific gate voltage. Mathematically, it is represented as:

$$SS_{point}(V_{GS}) = dlog(I_{DS}(V_{GS}))/dV_{GS} \qquad (2)$$

B. Average Subthreshold Swing

This represents the average subthreshold swing over a range of gate voltages and is given by:

$$SS_{AVG} = \frac{V_{th} - V_{off}}{\log\left(I_{DS}(V_{th}) - I_{DS}(V_{off})\right)} \qquad (3)$$

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