

An-Najah National University
Faculty of Engineering and Information Technology
Computer Engineering Department

Digital Circuit Design II (10636321)

1/12/2020

Duration: 1 Hour

Online Assignment # 2 : (ILOs: III)

Points:20

Complete the following VHDL code to implement a multiplier using repeated addition method.
(e.g. if **A=5** and **B = 4** , then the product **P** can be calculated as **5 + 5 + 5 + 5 = 20**)

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity multiplier is
    port(    CLK      : in  std_logic;
            A, B      : in  std_logic_vector(3 downto 0);
            P         : out std_logic_vector(7 downto 0));
end multiplier;
architecture behavioral of multiplier is
```

Your design should include the following pins:

1. **CLK**: (positive edge trigger input clock)
2. **A**: The first number (4 bits)
3. **B**: The Second number (4 bits)
4. **P**: The result (8 bits)

Notes:

- Use behavioral description
- The calculation should be synchronous with the clock (*the product should be calculated at the rising edge of the input clock*)

You have to submit two files:

1. A VHDL code to implement your Design.
2. A testbench file to simulate and test your design:
 - a. You have to cover all the possible cases for the input data (256 different cases)
 - b. For each case you have to:
 - Select two values for A and B.
 - Wait for two clock cycles