Digital Circuit Design II (10636321)

Due to 28/11/2020

HW1: (ILOs: **III**)	Points:**10**

Mathematically, we can define the **n-th** Fibonacci number as the sum of the **(n-1)-th** and **(n-2)-th**.

$$F(n) = \begin{cases} 0 & \text{if } n = 0 \\ 1 & \text{if } n = 1 \\ F(n-1) + F(n-2) & \text{if } n > 1 \end{cases}$$

Given the following entity declaration for a Fibonacci Calculator, complete the architecture to provide a behavioral description for the Fibonacci calculator.

```
entity Fibonacci_Calculator is
    port (   clk           : in std_logic;
             data_in       : in std_logic_vector (3 downto 0);
             load_enable   : in std_logic;
             data_out      : out std_logic_vector (9 downto 0));
end Fibonacci_Calculator;

architecture behavioral of Fibonacci_Calculator is
```

(Note: **Do not use algorithmic state machine**)

You have to submit two files:

1. A VHDL code to implement your Design.
2. A testbench file to simulate and test your design.
   a. You have to cover all the possible cases for the input data:
   b. For each case you have to:
      i. Select a test value for data_in
      ii. Activate the **load_enable** signal for at least one clock cycle.
      iii. The Fibonacci number should be calculated at the rising edge of the input clock.