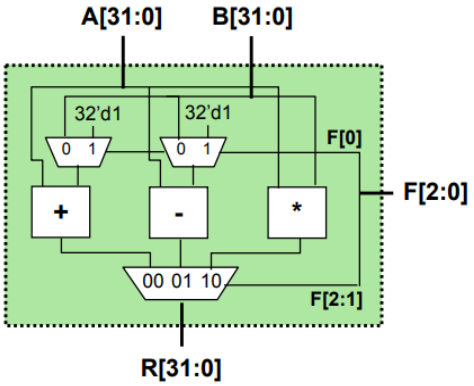
An Najah National University
Department of Computer Engineering
Digital Circuit Design
HW #2, ILO iii

Using Verilog language, design a **32 bit ALU**. The functionality and diagram of the ALU is shown below

Example: A 32-bit ALU



Function Table

F2	F1	F0	Function
0	0	0	A + B
0	0	1	A + 1
0	1	0	A - B
0	1	1	A - 1
1	0	X	A * B

You are required to implement the

- 2x1 MUX using gate level
- 3x1 MUX using behavioral level
- 32bit Adder, 32bit Subtractor, and 16bit Multiplier using dataflow level
- ALU model as gate level

Deadline: Thursday **5/12/2019**