

### 10.1. Introduction

Fig. 10.1 gives the block diagram of a superheterodyne F.M. receiver. It is similar to superheterodyne A.M. receiver. The main constituent stages of F.M. receiver are as follows :

(i) *R.F. Amplifier or Signal Frequency Amplifier.* It serves the same functions as in amplitude modulation superheterodyne receiver. Thus it serves (a) to raise the signal level appreciably before the signal is fed to the mixer and (b) to discriminate against the image signal. But in F.M. broadcast, the signal bandwidth is large being 150 kHz as against 10 kHz in A.M. broadcast. Hence the R.F. amplifier must be designed to handle this large bandwidth.

(ii) *Frequency Mixer.* It performs the usual function of mixing or heterodyning the signal frequency voltage and the local oscillator voltage to produce the difference voltage and frequency voltage which is the intermediate frequency voltage. Since F.M. broadcast takes place either in the VHF band or UHF band, single transistor frequency convertor is not used. A separate local oscillator is always used and another transistor serves as the frequency mixer. The intermediate frequency used in F.M. receivers is higher than that in A.M. receivers operating at short waves. Typical value of intermediate frequency is 12 MHz. This high intermediate frequency helps in image rejection.

(iii) *Local Oscillator.* A separate local oscillator is always used. At ultra high frequencies, it is preferred to keep the local oscillator frequency smaller than the signal frequency by an amount equal to the intermediate frequency.

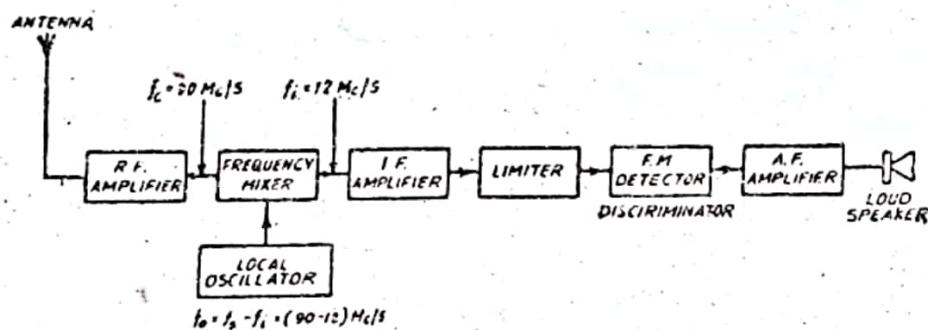


Fig. 10.1. Block diagram of superheterodyne F.M. receiver.

(iv) *I.F. Amplifier.* A multistage I.F. amplifier is used to provide large gain. Further this I.F. amplifier should be designed to have high overall bandwidth of the order of 150 kHz. Since the overall bandwidth decreases as the number of stages in cascade increases, it is necessary to design individual stages to have correspondingly higher bandwidth than the overall bandwidth desired. Double tuned circuits may be used but it is preferred, particularly at higher frequencies in the UHF range, to use stagger tuned single tuned circuit which are found to produce more gain bandwidth product than the conventional double tuned circuits.

(v) *Limiter.* The I.F. amplifier is followed by a limiter which limits the I.F. voltage to a predetermined level and thus removes all amplitude variations which may be incidentally caused due to changes in the transmission path or by man made static or natural static.

(vi) *F.M. Detector.* This extracts the original audio modulation frequency voltage from the frequency modulated carrier voltage. A discriminator is used as the F.M. detector.

(vii) *Audio Amplifier.* The output of the F.M. detector is fed to an audio frequency small signal amplifier and one or more audio frequency large-signal amplifiers. The output audio voltage is then fed to the loudspeaker. In F.M. broadcast, the maximum modulating frequency permitted is 15 kHz and hence the

audio frequency must be designed to accommodate such large bandwidth. Similarly the loudspeaker must be capable of reproducing all high frequency tones upto 15 kHz. Often two or more loudspeakers are used, each reproducing a limited range of frequencies.

### 10.2. The Limiter

The limiter removes from the carrier all amplitude variations which may be caused incidently by changes in the transmission path, by man-made static or natural static. This suppression of amplitude variation is necessary because in F.M. receivers, a very large part of the improvement in signal to noise ratio results from this. In an ideal case a limiter must remove from its output all variations in amplitude arising from variations of the amplitude of the input carrier voltage. The essential requirement of such an ideal limiter are as follows:

(i) it should function at all levels of input carrier and (ii) it should function at all rates of variation of carrier voltage. In the practical limiters, requirement (i) is not fully satisfied at low carrier levels while requirement (ii) is not met at very rapid or very slow rates of variation of carrier input. Limiters used in F.M. receivers may use one or both of the following two electrical effects : (i) leak-type bias and (ii) early (drain/collector) saturation. Often both effects are simultaneously used in the limiter circuit. The amplifier device used may be B.J.T. or F.E.T. Fig. 10.2 shows an F.E.T. amplitude limiter using both the above mentioned electrical effects.

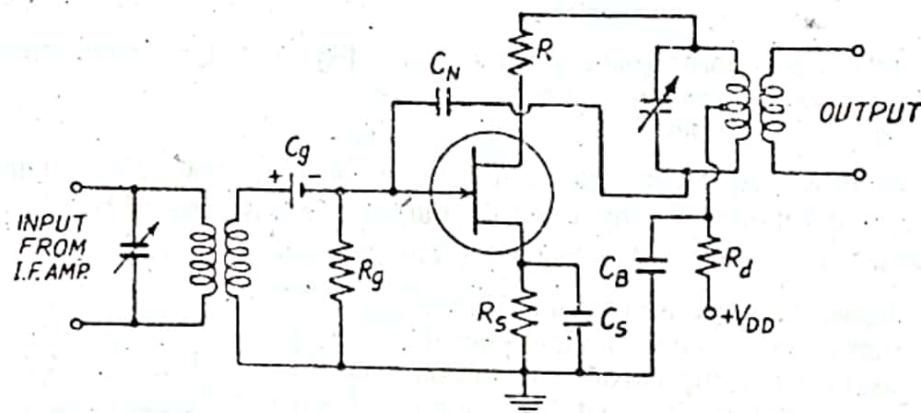


Fig. 10.2. Amplitude limiter.

This amplitude limiter is basically a tuned I.F. amplifier but has the following special features : (i) the drain supply voltage has been kept low by use of voltage dropping resistor  $R_d$  (ii) leak-type bias is provided at the gate by use of  $R_g$ - $C_g$  combination and (iii) F.E.T. has been neutralized by neutralising capacitor  $C_N$ .

**Gate Limiting Action.** Leak type bias provides limiting action. Thus as the input signal voltage rises, the current flowing through  $C_g$  increases and the negative voltage developed across capacitor  $C_g$  in the polarity shown increases. Thus as the input voltage increases, the bias on the F.E.T. increases, the gain of the amplifier reduces and the output voltage at the fundamental frequency tends to remain constant. This provides the limiting action. However effective limiting action occurs only with rather large input voltages. For small input signal, the leak bias is small and hence no limiting action takes place. Limiting action begins only when signal is large enough to produce leak bias of about  $0.6 V_{co}$ , where  $V_{co}$  is the cutoff bias.

**Drain Limiting Action.** To achieve limiting action at low values of input signal drain limiting action is utilized. This is achieved by use of a low drain supply voltage which results in saturation of the output current with low input signal voltage. In Fig. 10.2, this low drain supply voltage is achieved by using the drain dropping resistor  $R_d$ . Thus the drain supply voltage is kept about one-half of the normal d.c. drain voltage. Fig. 10.3 shows common source static drain characteristic of an n-channel FET. Low value of effective supply voltage is shown by  $V_{DD}$ . Point P gives the zero signal operating point with normal bias. Straight line  $PP_1$  gives the a.c. load line. With normal bias on the limiter, the drain voltage on the low drain voltage side is limited by the knee of the drain characteristics, i.e. the drain current becomes flat bottomed. Such a

limiting takes place at a low value of the input signal voltage namely the signal voltage corresponding to the drain voltage swing equal to  $PP_1$  in Fig. 10.3. Then as the input voltage amplitude increases, the fundamental frequency drain current becomes independent of the amplitude of the gate potential over wide ranges and hence the fundamental frequency output a.c. voltage ( $I_{D1}R_L$ ) tends to remain essentially constant as shown in Fig. 10.4. Effective limiting begins at input voltage of about 0.16 volt RMS.

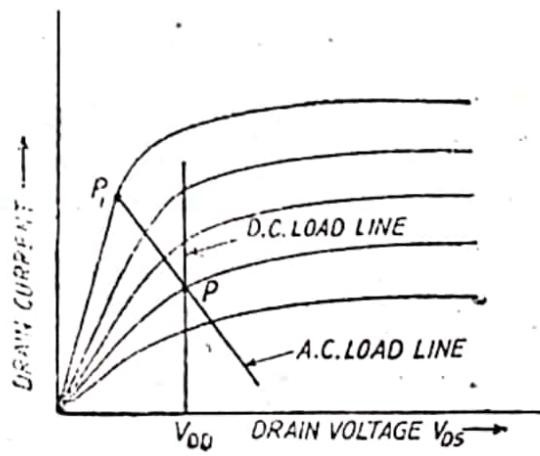


Fig. 10.3. Static drain characteristic and the load lines showing the limiting action by drain saturation.

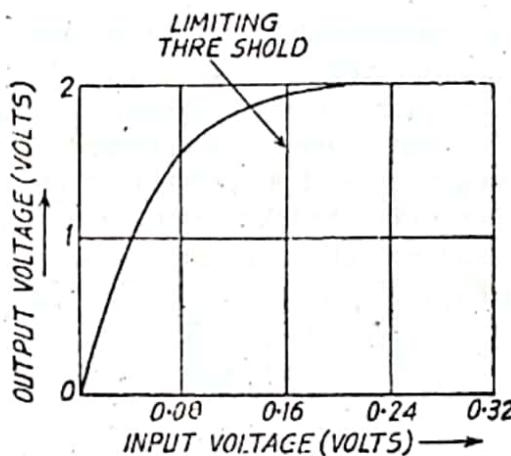


Fig. 10.4. Limiting characteristic of drain limiter.

It is possible, however, for the gate-drain section to become forward biased under saturation condition, causing a short circuit between the input and the output. This is avoided by placing a resistor  $R$  of a few hundred ohms between the drain and its tank circuit as shown in Fig. 10.2.

Fig. 10.5 shows the response characteristic of the amplitude limiter of Fig. 10.2 taking into consideration both the leak-bias limiting and drain saturation actions. It is obvious from the curve that the limiting takes place only for a certain range of input voltages. Beyond this range, the output varies with input. Thus in Fig. 10.5, for input less than about 0.16 volt, corresponding to part  $OA$  of the curve, the output increases with the increase of input, i.e. no limiting takes place. Limiting begins at point  $A$ . This point is, therefore, referred to as the *threshold of limiting*. In the range  $AB$ , as the input voltage increases from about 0.16 to 1.6 V the output current flows for progressively shorter portions of the input cycle but the fundamental component of drain current remain constant so that the output voltage remains constant. Thus proper limiting takes place in this range. The operation is similar to that of a class C amplifier, utilizing the *flywheel effect* of the tank circuit to ensure sinusoidal output voltage even though the output current is in the form of short duration pulses.

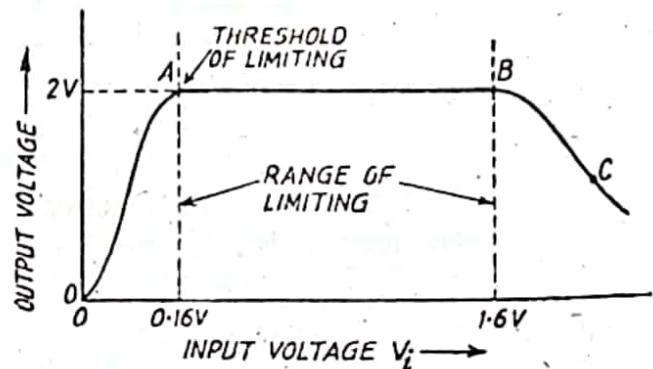


Fig. 10.5. Typical limiter response characteristic. Beyond the point  $B$  in the characteristic, the angle of output current (drain current) flow gets reduced so much that less power is fed to the output tank, resulting in reduced output voltage. Thus point  $B$  marks the upper limit of the limiting operation range. This limit has been caused by the reduced angle of drain current flow.

**Performance Limit.** We see that the range of input voltage over which limiter works satisfactorily is rather limited. Thus the lower limit of input voltage of about 0.16 volt RMS results from the FET drain characteristic while the upper limit of input voltage of about 1.6 volts RMS results from the reduced angle of output current flow. In this input voltage range from about 0.16 to 1.6 volts, the output voltage remains

almost constant at about 2 volts. In practice, therefore, we feed to this limiter an input voltage of nominal value about 0.9 volt RMS. This permits maximum range of variation of 0.7 volt RMS within which limits proper amplitude limiting takes place. This implies that any spurious amplitude variations must be quite large compared to the signal to escape being limited.

**Two Stage Amplitude Limiter.** In practical FM receivers, it is often necessary to use limiter capable of limiting action considerably beyond the maximum signal strength range obtainable by one limiter stage. Hence two stage limiter is often used.

**AGC in Amplitude Limiter.** Instead of a two stage limiter, an automatic gain control (AGC) may be used. AGC ensures that the signal fed to the limiter is within its limiting range regardless of the input signal strength. The AGC also prevents overloading of the last IF amplifier stage. In case of limiter using-leak type bias, this bias voltage varies in proportion to the input voltage and may itself be used as the AGC bias. If, however, leak type bias is not used, a separate AGC detector is used. This AGC-detector picks up a part of the output voltage of the last IF amplifier stage, rectifiers and filters it and then uses this d.c. voltage as the AGC bias for the limiter stage.

### 10.3. F.M. Detectors

The function of an FM detector is to extract the original modulating voltage from the frequency modulated voltage. This detection should be done efficiently and linearly. Further it is desirable that the detector circuit should be insensitive to amplitude changes and should not be too critical in its adjustment and operation.

The FM detector performs the detection process in two steps : (i) it converts the frequency modulated voltage into corresponding amplitude modulated voltage using one or more tuned circuits and (ii) it rectifies this amplitude modulated voltage in linear diode detectors to extract the orginal modulation frequency voltage.

These FM detectors or discriminators may be of the following types :

- (i) Single tuned Circuit Discriminator or the Slope Detector.
- (ii) Stagger Tuned Discriminator or the Balanced Slope Detector.
- (iii) Phase Difference Discriminator of the following types :
  - (a) Centre Tuned discriminator or Foster-Seeley Discriminator
  - (b) Ratio Detector.

### 10.4. Slope Detector or Single Tuned Circuits Discriminator

It makes use of a parallel tuned circuit tuned to a frequency slightly different from the centre frequency of the FM carrier, followed by a linear rectifier with filter section as shown in Fig. 10.6.

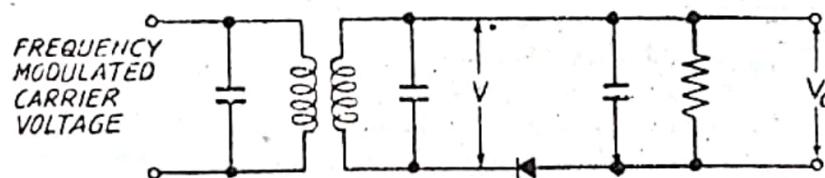


Fig. 10.6. Circuit of slope detector.

Fig. 10.7 shows the action of this slope detector in converting a frequency modulated carrier voltage into corresponding amplitude modulated carrier voltage. Thus as the instantaneous carrier frequency varies in accordance with the variation of instantaneous modulation voltage, the response of the tuned circuit varies correspondingly as shown in Fig. 10.7. The amplitude of the output voltage then varies in accordance with the variation of carrier frequency. This amplitude modulated voltage may then be rectified in diode detector to extract the modulation frequency voltage. If the response of the single tuned circuit is a straight line, then the modulation frequency voltage is identical with the original modulating voltage. But the response curve, in practice, is not linear and hence the detected output voltage gets distorted, i.e. it contains harmonic terms.

The constitutes one drawback of this discriminator. Another drawback of this circuit is that it does not reject amplitude variations. Thus if the applied input voltage is doubled, the a.c. output current and the a.c. output voltage also get doubled. An ideal discriminator should respond only to frequency variations and should not respond to amplitude variations. Because of these two basic limitations single tuned circuit discriminator is not used in practice.

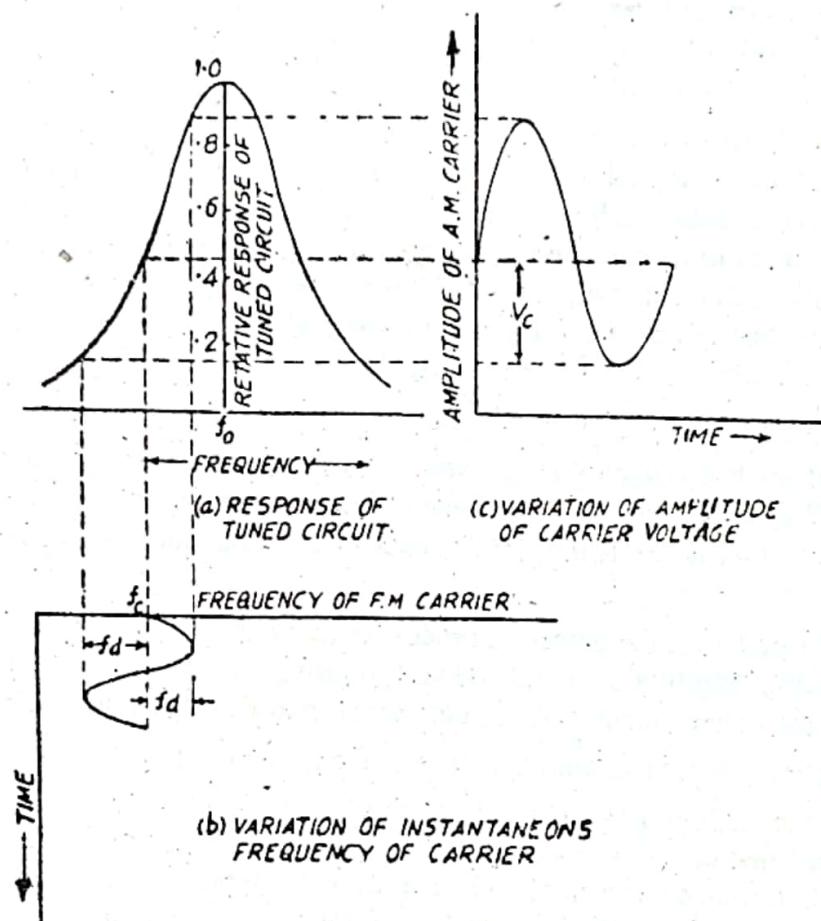


Fig. 10.7. Working of slope detector.

### 10.5. Balanced Slope Detector or Stagger Tuned Discriminator

Fig. 10.8 gives the basic circuit arrangement. It is an extension of the slope detector and eliminates the distortion present in the latter. It is fed from an input tuned circuit, tuned to the carrier centre frequency  $f_c$ . It utilizes two tuned circuits  $A$  and  $B$ , each associated with its own rectifier diode and output load circuit. This tuned circuit  $A$  is associated with rectifier diode  $D_A$  and output load circuit consisting of resistor  $R_A$  and capacitor  $C_A$  in parallel. Similarly tuned circuit  $B$  is associated with rectified diode  $D_B$  and output load circuit consisting of resistor  $R_B$  in parallel with capacitor  $C_B$ .  $R_A$  and  $R_B$  are equal and so also are  $C_A$  and  $C_B$ . Circuit  $A$  is tuned to a frequency  $f_1$  which is greater than the carrier centre frequency  $f_c$  by a small frequency interval  $\Delta f$ . On the other hand, circuit  $B$  is tuned to a frequency  $f_2$

below the carrier centre frequency  $f_c$  by the same amount  $\Delta f$ . Let  $V_A$  and  $V_B$  be the voltage responses of tuned circuits  $A$  and  $B$  respectively. These voltages  $V_A$  and  $V_B$  are rectified in diode  $D_A$  respectively and the RF components of the rectified currents are bypassed by capacitor  $C_A$  and  $C_B$  respectively. The voltage  $v_A$  and  $v_B$  developed across the load resistors  $R_A$  and  $R_B$  respectively are then nothing but the variations in the amplitudes

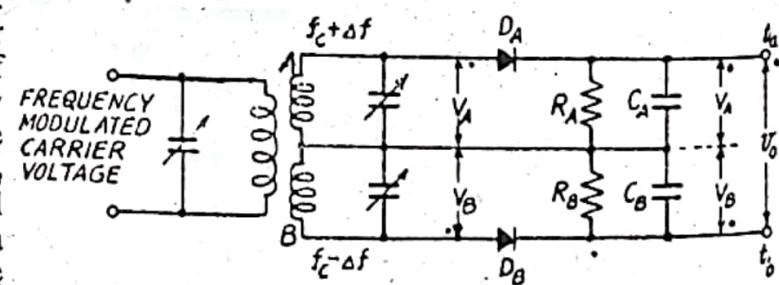


Fig. 10.8. Basic circuit of balanced slope detector.

of voltages  $V_A$  and  $V_B$ . Then the response of the tuned circuit plotted against frequency represents the detected output voltage  $v_A$  as shown in Fig. 10.9. Similarly response of tuned circuit  $B$  plotted against frequency represents the detected output voltage  $v_B$ . The circuit is so arranged that the detected voltage  $v_A$  and  $v_B$  oppose each other so that the resultant output voltage  $v_o = v_A - v_B$ . This resultant response  $v_o$  is also plotted in Fig. 10.9 by subtracting the response  $v_B$  from response  $v_A$ .

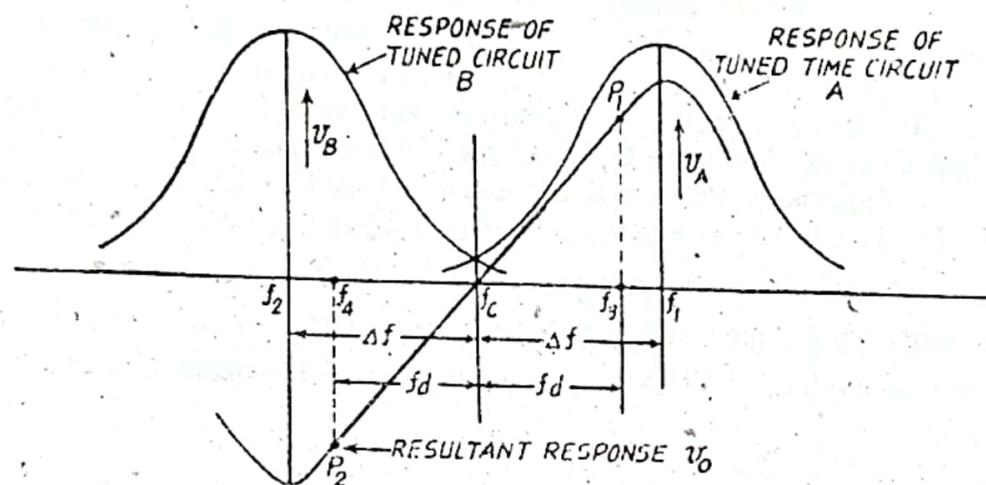


Fig. 10.9. Response of stagger tuned discriminator.

If it is seen from Fig. 10.9 that the curve of resultant output voltage  $v_o$  is almost a straight line in the range  $P_1 P_2$  and it cuts the frequency axis at the carrier centre frequency  $f_c$ .

If now a frequency modulated voltage of carrier centre frequency  $f_c$  and frequency deviation equal to or less than  $f_d$  ( $= f_3 - f_c = f_c - f_4$ ) is applied to the input of this discriminator then the rectified output voltage is proportional to the instantaneous frequency variation and hence is proportional to the instantaneous value of the modulating voltage.

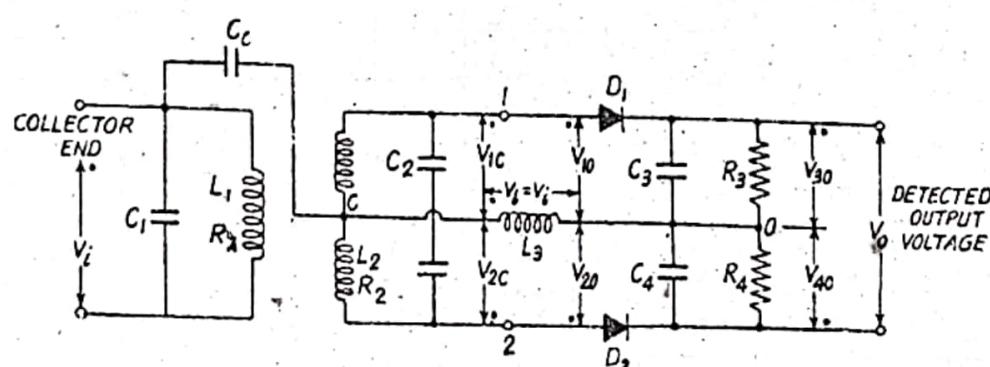


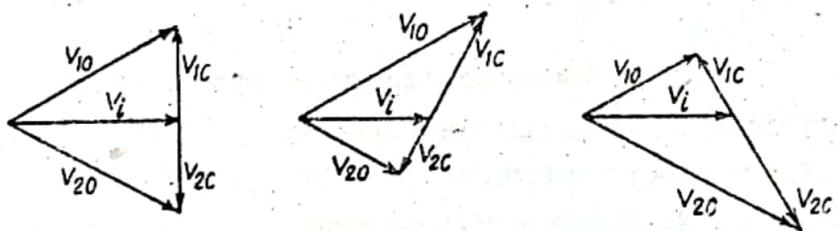
Fig. 10.10. Basic circuit of centre tuned discriminator.

#### 10.6. Centre-Tuned Discriminator or Foster-Seeley Discriminator or Phase-Shift Discriminator

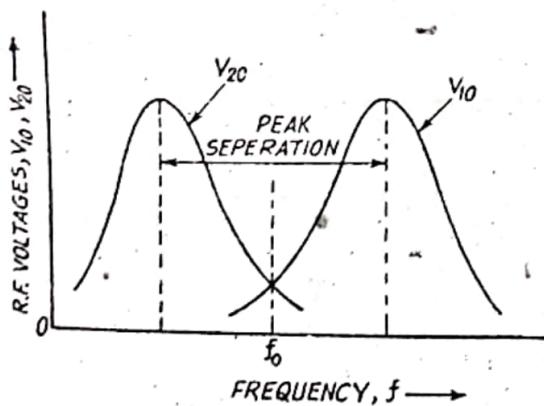
This is the commonly used form of F.M. detector. Fig. 10.10 gives the basic circuit. It uses a double tuned circuit in which both the primary and the secondary are tuned to the same frequency namely the intermediate frequency are inductively coupled. Further the centre of the secondary is connected to the collector end of the primary tuned circuit through a coupling capacitor  $C_c$ . This coupling capacitor serves another function of blocking the d.c. collector voltage from the secondary system. The R.F. choke  $L_3$  provides the return path for the d.c. component of the rectified currents of diodes  $D_1$  and  $D_2$ . Inductance of this choke  $L_3$  comes in shunt with the inductance  $L_1$  of the primary and is kept relatively much larger than  $L_1$ . The RF voltage  $V_i$  developed

across the choke  $L_3$  is very slightly less than the primary circuit voltage  $V_i$  because of the voltage drop in the coupling capacitor  $C_c$ . But since the reactance of capacitor  $C_c$  is very small in comparison with the reactance of choke  $L_3$ , voltage  $V_i$  may be put approximately equal to  $V_i$ .

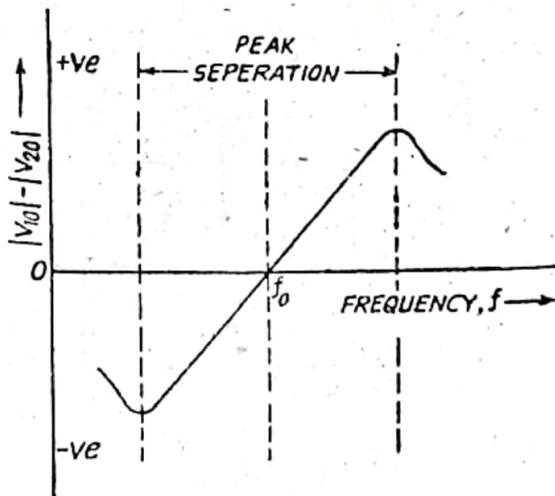
Since point C is the true electrical centre of the secondary, the R.F. voltages  $V_{1c}$  and  $V_{2c}$  as shown in Fig. 10.10 are equal in magnitude and opposite in phase. The RF voltage  $V_{10}$  applied to diode  $D_1$  is equal to  $V_i + V_{1c} \approx V_i + V_{1c}$ . Similarly RF voltage  $V_{20}$  applied to diode  $D_2$  is equal to  $V_i + V_{2c} \approx V_i + V_{2c}$ . Voltages  $V_{1c}$  and  $V_{2c}$  are not in phase with  $V_i$  and hence these have to be added vectorially to  $V_i$  to produce voltages  $V_{10}$  and  $V_{20}$ . This vectorial addition is shown in Fig. 10.11 for different values of applied RF signal frequency. Thus for applied frequency  $f$  equal to the frequency  $f_0$  of the tuned circuits, the voltages  $V_{1c}$  and  $V_{2c}$  are in phase quadrature with the voltage  $V_i$ . The voltages  $V_{10}$  and  $V_{20}$  are then equal in magnitude as shown in Fig. 10.11 (a). If, however, the applied frequency  $f$  differs from the resonant frequency of the turned circuits, the phase angles of voltages  $V_{1c}$  and  $V_{2c}$  relative to the voltage  $V_i$  differ from  $90^\circ$ . Thus if the input frequency  $f$  is higher than the resonant frequency  $f_0$ , then the phase angle of voltage  $V_{2c}$  relative to voltage  $V_i$  is say  $90^\circ - \Delta\theta$  and the phase angle of voltage  $V_{1c}$  relative to  $V_i$  is  $90^\circ + \Delta\theta$ . Accordingly the resultant voltage  $V_{10}$  is greater than the voltage  $V_{20}$  in magnitude as shown in Fig. 10.11 (a). If, on the other hand, the input frequency is below the resonant frequency  $f_0$ , the resultant voltage  $V_{10}$  is smaller than the voltage  $V_{20}$  as shown in Fig. 10.11(a). The variation of amplitude of RF voltages  $V_{10}$  and  $V_{20}$  with instantaneous frequency takes place as shown in Fig. 10.11 (b).



(a) Vector diagrams of r.f. voltages.



(b) Variation of r.f. voltages  $A_{10}$  and  $V_{20}$  with frequency  $f$ .



(c) Discriminator response characteristic.

Fig. 10.11. Centre tuned discriminator.

RF voltages  $V_{10}$  and  $V_{20}$  are separately rectified in linear detector diodes  $D_1$  and  $D_2$  respectively to produce output voltages  $V_{30}$  and  $V_{40}$  across the resistors  $R_3$  and  $R_4$ . The RF components of the rectified currents are bypassed through shunt capacitors  $C_2$  and  $C_4$  leaving only the modulation frequency component.

and the DC component to flow through resistors  $R_3$  and  $R_4$ . The output voltages  $V_{30}$  and  $V_{40}$  then represent the amplitude variations of RF voltages  $V_{10}$  and  $V_{20}$ . From Fig. 10.10, it may be seen that for the given arrangement of diodes, the output voltages oppose each other. The final output voltage  $V_o$  is then equal to the arithmetic difference  $|V_{30}| - |V_{40}|$ . This resultant rectified output voltage  $V_o$  will then vary with the instantaneous frequency of the applied signal in the same way as the difference  $|V_{10}| - |V_{20}|$  of RF voltages applied to the diodes. This is shown in Fig. 10.11 (c). The rectified output voltage  $V_o$  is then given by,

$$V_o = |V_{30}| - |V_{40}| = k[|V_{10}| - |V_{20}|]$$

where  $k$  is constant of proportionality.

This curve giving variation of rectified output voltage  $V_o$  with instantaneous frequency  $f$  is often called the *discriminator characteristic*.

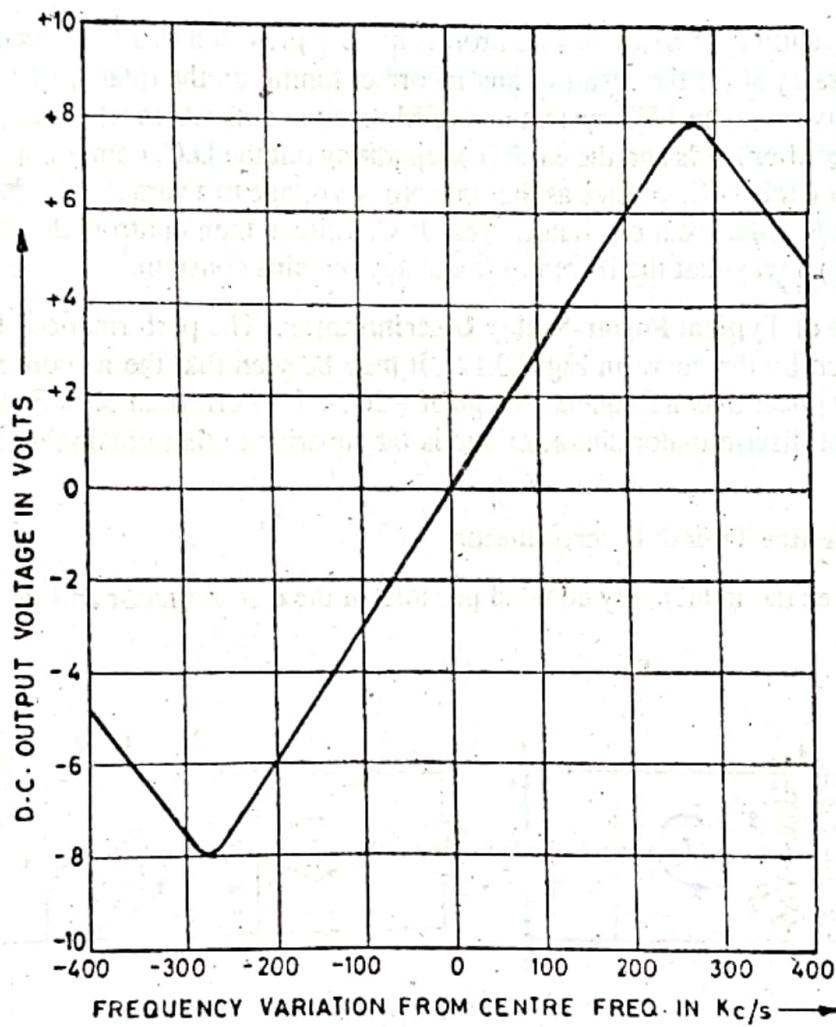


Fig. 10.12. Response characteristic of a typical Foster-Seeley discriminator (at centre frequency or 10 MHz).

Study of discriminator characteristic of Fig. 10.11 (c) reveals that at applied frequency equal to the resonant frequency, the rectified output of discriminator is zero. The zero voltage results because RF voltages  $V_{10}$  and  $V_{20}$  have equal amplitudes. At instantaneous frequency greater than the resonant frequency, the rectified output voltage  $V_o$  of discriminator is positive because RF voltage  $V_{10}$  has larger amplitude than the RF voltage  $V_{20}$ . At an instantaneous frequency less than the resonant frequency, the rectified output voltage  $V_o$  is negative because RF voltage  $V_{10}$  has smaller amplitude than the RF voltage  $V_{20}$ . It is further seen that in the frequency range between response peaks, the discriminator characteristic is essentially linear so that the instantaneous value of discriminator output voltage  $V_o$  is proportional to the variation of instantaneous

frequency from the centre value. The discriminator characteristic may thus be summarised as below : (i) discriminator output voltage  $V_o$  is zero when the applied frequency is equal to the resonant frequency (ii) at any other frequency, the output is a D.C. voltage having polarity depending on whether the instantaneous frequency is greater than or less than resonant frequency and (iii) the magnitude of the output D.C. voltage is proportional to the variation of instantaneous frequency from the resonant frequency. Thus resultant output voltage  $V_o$  accurately reproduces the variation of instantaneous frequency so long as the operation is confined to the frequency range between the response peaks. Such a discriminator, therefore, functions as an excellent FM detector provided that the resonant frequency of the discriminator tuned circuit is equal to the carrier centre frequency and provided further that the frequency deviation is confined to the true linear portion of the discriminator characteristic within the response peaks.

In all Foster-Seeley discriminators, the detected voltage is picked up from one end of the composite load while the other end is grounded.

Further AFC (automatic frequency control) is usually provided in all FM receivers. The FM receiver, AFC is highly necessary since the result of any incorrect tuning on the quality of reproduction is more pronounced in FM receivers. The AFC system in an FM receiver consists in (i) picking up the voltage between the junction of the rectifier loads and the earth (ii) separating out the D.C. component with the help of suitable filter and (iii) applying this D.C. voltage as the controlling voltage to a varactor diode which is placed in shunt with the tuned circuit of the local oscillator. This D.C. voltage then controls the local oscillator frequency automatically in such a way that the IF centre frequency remains constant.

**Performance of Typical Foster-Seeley Discriminator.** The performance of a typical Foster-Seeley discriminator is given by the curve in Fig. 10.12. It may be seen that the response curve of Foster-Seeley discriminator is very linear over a frequency range of  $\pm 200$  kHz. Performance of Foster-Seeley discriminator regarding linearity of discriminator characteristic is far superior to that obtainable for other types of phase shift discriminators.

### 10.7. Analysis of Centre Tuned Discriminator

Fig. 10.13 gives the inductively coupled portions of the discriminator and its a.c. equivalent circuit is shown in Fig. 10.14.

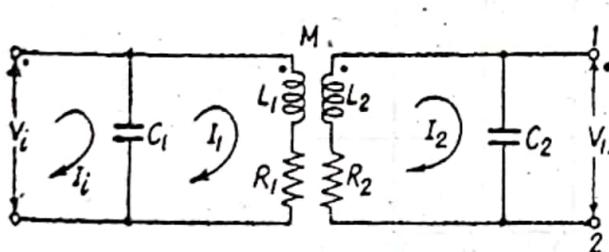


Fig. 10.13. Inductively coupled portion of centre tuned discriminator.

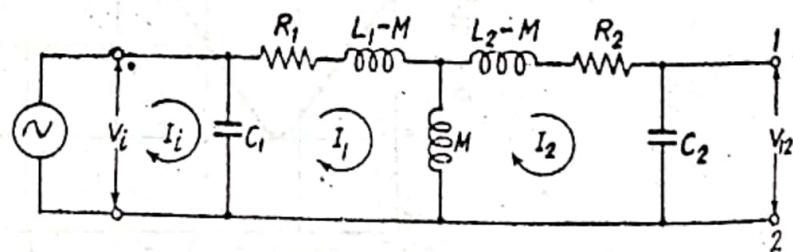


Fig. 10.14. A.C. equivalent circuit of inductively coupled portion of centre tuned discriminator.

From Fig. 10.14 we may write the following equation for the loop containing element  $C_1, R_1, M$  and  $(L_1 - M)$ :

$$j \frac{I_1}{\omega C_1} + \left[ R_1 + j \left( \omega L_1 - \frac{1}{\omega C_1} \right) \right] I_1 - j \omega M I_2 = 0 \quad \dots(10.1)$$

Similarly for loop containing elements  $R_2, C_2, M$  and  $(L_2 - M)$ , we get

$$j \omega M I_1 + \left[ R_2 + j \left( \omega L_2 - \frac{1}{\omega C_2} \right) \right] I_2 = 0 \quad \dots(10.2)$$

If the operation frequency  $\omega$  is close to centre frequency  $\omega_0$ , then fractional frequency variation  $\delta$  is given by,

$$\delta = \frac{\omega - \omega_0}{\omega_0} \quad \dots(10.3)$$

$$\omega = (1 + \delta) \omega_0 \quad \dots(10.4)$$

Hence we may write,

$$\begin{aligned} R_1 + j \left( \omega L_1 - \frac{1}{\omega C_1} \right) &= R_1 \left[ 1 + f \left\{ \frac{\omega_0 L_1}{R_1} (1 + \delta) - \frac{1}{\omega_0 C_1 R_1 (1 + \delta)} \right\} \right] \\ &= R_1 \left[ 1 + j Q_1 \left\{ (1 + \delta) - \frac{1}{1 + \delta} \right\} \right] \\ &\approx R_1 [1 + j Q_1 2 \delta] \end{aligned} \quad \dots(10.5)$$

where

$$Q_1 = \frac{\omega_0 L_1}{R_1} = \frac{1}{\omega_0 C_1 R_1} \quad \dots(10.6)$$

Similarly  $R_2 + j \left( \omega L_2 - \frac{1}{\omega C_2} \right) = R_2 (1 + j Q_2 2 \delta)$  (10.7)

where

$$Q_2 = \frac{\omega_0 L_2}{R_2} = \frac{1}{\omega_0 C_2 R_2} \quad \dots(10.8)$$

Hence Eqs. (10.1) and (10.2) may be put as,

$$R_1 (1 + j 2 \delta Q_1) I_1 - j \omega_0 M I_2 = -j \frac{1}{\omega_0 C_1} I_i \quad \dots(10.9)$$

and

$$-j \omega_0 M I_1 + R_2 (1 + j 2 \delta Q_2) I_2 = 0 \quad \dots(10.10)$$

From Eqs. (10.9) and (10.10), we get

$$I_1 = \frac{-j (1/\omega_0 C_1) . R_2 (1 + j 2 \delta Q_2)}{R_1 R_2 (1 + j 2 \delta Q_1) (1 + j 2 \delta Q_2) + (\omega_0 M)^2} I_i \quad \dots(10.11)$$

On dividing both numerator and denominator by  $R_1 R_2$ , we get

$$I_1 = \frac{-j \frac{1}{\omega_0 C_1 R_1} \cdot (1 + j 2 \delta Q_2)}{(1 + j 2 \delta Q_1) (1 + j 2 \delta Q_2) + (\omega_0 M^2 / R_1 R_2)} I_i \quad \dots(10.12)$$

$$= -j Q_1 \frac{(1 + j 2 \delta Q_2)}{(1 + j 2 \delta Q_1) (1 + j 2 \delta Q_2) + K^2 Q_1 Q_2} I_i \quad \dots(10.13)$$

From Eq. (10.13) it is clear that  $I_1 \gg I_i$  so that

$$V_i = \frac{-I_1}{j \omega_0 C_1} \quad \dots(10.14)$$

Substituting the value of  $I_1$  from Eq. (10.13) into Eq. (10.14), we get

$$V_i = \frac{(1 + j 2 \delta Q_2) Q_1}{(1 + j 2 \delta Q_1)(1 + j 2 \delta Q_2) + K^2 Q_1 Q_2} R_1 I_i \quad \dots(10.15)$$

Assuming the mutual inductance  $M$  to be small, the impedance coupled from secondary into the primary circuit may be considered to be negligibly small.

Hence

$$I_1 \approx \frac{V_i}{R_1 + j X_{L_1}} \quad \dots(10.16)$$

If  $Q$  of the primary is high, then  $R_1 \ll X_{L_1}$ , so that Eq. (10.16) becomes,

$$I_1 \approx \frac{V_i}{j X_{L_1}} = \frac{V_i}{j \omega L_1} \quad \dots(10.17)$$

Then the voltage induced in the secondary is given by,

$$V_{ind} = \pm j \omega M I_1 = \pm \frac{M}{L_1} V_i \quad \dots(10.18)$$

Neglecting the loading effects of the diode rectifiers,

$$V_{12} = \frac{-j X_{C_2} V_{ind}}{R_2 + j X_{L_2} - j X_{C_2}} = \pm \frac{-j X_{C_2} \cdot M/L_1}{R_2(1 + j 2 \delta Q_2)} V_i \quad \dots(10.19)$$

$$\text{or } \frac{V_{12}}{V_i} = \pm \frac{j X_{C_2} \cdot k \sqrt{(L_2/L_1)}}{R_2(1 + j 2 \delta Q_2)} \quad \dots(10.20)$$

Choosing the negative sign and putting  $(X_{C_2}/R_2) = Q_2$ , Eq. (10.20) becomes,

$$\frac{V_{12}}{V_i} = j \sqrt{\frac{L_2}{L_1} \cdot \frac{k Q_2}{(1 + j 2 \delta Q_2)}} \quad \dots(10.21)$$

Combining Eqs. (10.15) and (10.21), we get

$$V_{12} = j \sqrt{\frac{L_2}{L_1} \cdot \frac{k Q_2 Q_1^2}{(1 + j 2 \delta Q_1)(1 + j 2 \delta Q_2) + k^2 Q_1 Q_2}} R_1 I_i \quad \dots(10.22)$$

Ordinarily  $Q_1 = Q_2 = Q$  say. Under this condition, Eqs. (10.15) and (10.22) reduce to the following forms :

$$V_i = \frac{Q^2 (1 + j 2 \delta Q)}{(1 + j 2 \delta Q)^2 + k^2 Q^2} R_1 I_i \quad \dots(10.23)$$

and

$$V_{12} = j \sqrt{\frac{L_2}{L_1} \cdot \frac{k Q^3}{(1 + j 2 \delta Q)^2 + k^2 Q^2}} R_1 I_i \quad \dots(10.24)$$

Hence

$$\frac{V_{12}}{V_i} = j \sqrt{\frac{L_2}{L_1} \cdot \frac{k Q}{(1 + j 2 \delta Q)}} \quad \dots(10.25)$$

Thus discriminator is assumed to be driven by a constant current device such as a pentode or FET. Hence assuming  $I_i$  to be constant, from Eq. (10.23) we note that  $V_i$  is not a constant but varies with frequency.

Diodes  $D_1$  and  $D_2$  are peak diode detectors. The output D.C. potential  $V_{30}$  is proportional to the peak of the envelope of RF voltage  $V_{10}$  and similarly output D.C. potential  $V_{40}$  is proportional to the peak of the envelope of  $V_{20}$ . Then total output D.C. potential is,

$$V_o = V_{30} - V_{40} \quad \dots(10.26)$$

Further

$$V_1 = \frac{j X_{L_2} \cdot V_i}{j X_{L_1} - j (X_{C_e} + X_{C_4})} \quad \dots(10.27)$$

where  $X_{L_2}$ ,  $X_{C_e}$  and  $X_{C_4}$  are respectively the reactance of choke  $L_2$ , coupling capacitor  $C_e$  and capacitor  $C_4$ . But  $X_{L_1} \gg (X_{C_e} + X_{C_4})$ . Hence Eq. (10.27) yields,

$$V_1 \approx V_i \quad \dots(10.28)$$

Hence

$$V_{10} = V_{1c} + V_i = V_{1c} + V_i = \frac{V_{12}}{2} + V_i \quad \dots(10.29)$$

and

$$V_{20} = V_{2c} + V_i = -V_{1c} + V_i = -\frac{V_{12}}{2} + V_i \quad \dots(10.30)$$

Let  $\eta$  indicate the detector efficiency.

Then

$$\begin{aligned} V_{30} &= \eta \left| V_i + \frac{V_{12}}{2} \right| = \eta V_i \left| 1 + \frac{1}{2} \frac{V_{12}}{V_i} \right| \\ &= \eta V_i \left| 1 + j \frac{1}{2} \sqrt{\frac{L_2}{L_1}} \cdot \frac{kQ}{1 + j 2 \delta Q} \right| \end{aligned} \quad \dots(10.31)$$

and

$$\begin{aligned} V_{40} &= \eta \left| V_i - \frac{V_{12}}{2} \right| = \eta V_i \left| 1 - \frac{1}{2} \frac{V_{12}}{V_i} \right| \\ &= \eta V_i \left| 1 - j \frac{1}{2} \sqrt{\frac{L_2}{L_1}} \cdot \frac{kQ}{1 + j 2 \delta Q} \right| \end{aligned} \quad \dots(10.32)$$

Substituting the value of  $V_i$  from Eq. (10.23) into Eqs. (10.31) and (10.32), we get

$$V_{30} = \eta \left| \frac{Q^2 (1 + j 2 \delta Q)}{(1 + j 2 \delta Q)^2 + k^2 Q^2} \right| \cdot \left| 1 + j \frac{1}{2} \sqrt{\frac{L_1}{L_2}} \cdot \frac{kQ}{1 + j 2 \delta Q} \right| \cdot R_1 I_i \quad \dots(10.33)$$

and

$$V_{40} = \eta \left| \frac{Q^2 (1 + j \delta Q)}{(1 + j 2 \delta Q)^2 + k^2 Q^2} \right| \cdot \left| 1 - j \frac{1}{2} \sqrt{\frac{L_1}{L_2}} \cdot \frac{kQ}{1 + j 2 \delta Q} \right| \cdot R_1 I_i \quad \dots(10.34)$$

Hence DC output voltage  $V_o$  is given by,

$$\begin{aligned} V_o &= V_{30} - V_{40} \\ &= \eta R_1 I_i \left| \frac{Q^2 (1 + j 2 \delta Q)}{(1 + j 2 \delta Q)^2 + k^2 Q^2} \right| \cdot \left[ \left| 1 + j \frac{1}{2} \sqrt{\frac{L_2}{L_1}} \cdot \frac{kQ}{1 + j 2 \delta Q} \right| - \left| 1 - j \frac{1}{2} \sqrt{\frac{L_1}{L_2}} \cdot \frac{kQ}{1 + j 2 \delta Q} \right| \right] \end{aligned}$$

$$-\left| 1 - j \frac{1}{2} \sqrt{\frac{L_2}{L_1}} \cdot \frac{kQ}{1 + j 2\delta Q} \right| \quad \dots(10.35)$$

$V_o$  as given by Eq. (10.35) when plotted against fractional frequency deviation  $\delta$  or against instantaneous frequency gives the discriminator characteristics.

Analysis for optimum performance yields the conditions  $kQ = 1$  and  $\sqrt{L_2/L_1} = 1$ . If  $kQ$  is kept less than one i.e.  $k < 1/Q$  representing a relatively loose coupling, then the linear portion of the discriminator response curve gets reduced. On the other hand, if  $kQ > 1$ , the circuit is overcoupled and then the response curve gets distorted at the ends as shown in Fig. 10.15.

Often Foster-Seeley discriminator uses only a portion of the primary voltage to constitute the voltage  $V_i$ . Hence Eqs. (10.29) and (10.30) get modified as below :

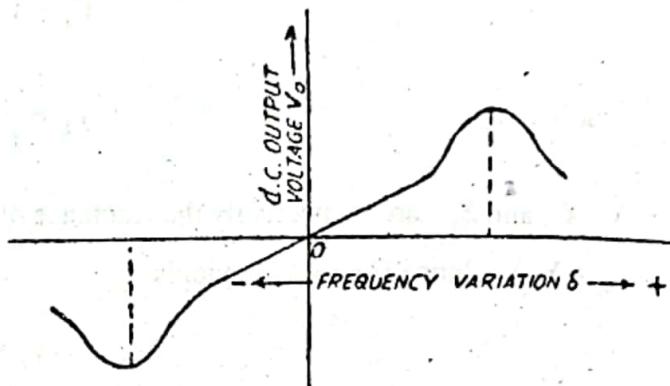


Fig. 10.15. Response of centre tuned discriminator under overcoupled conduction.

$$V_{10} = \frac{V_{12}}{2} + V_i = \frac{V_{12}}{2} + a V_i \quad \dots(10.36)$$

and

$$V_{20} = \frac{V_{12}}{2} + V_i = -\frac{V_{12}}{2} + a V_i \quad \dots(10.37)$$

where  $V_i = a V$ ,  $a$  being always less than unity.

Consequently Eqs. (10.33) and (10.34) get modified as below :

$$V_{30} = \eta \left| \frac{Q^2(1+j\delta Q)}{(1+j2\delta Q)^2+k^2Q^2} \left[ a + j \frac{1}{2} \sqrt{\frac{L_2}{L_1}} \cdot \frac{kQ}{1+j2\delta Q} \right] \right| \cdot R_1 I_i \quad \dots(10.38)$$

$$\text{and } V_{40} = \eta \left| \frac{Q^2(1+j2\delta Q)}{(1+j2\delta Q)^2+k^2Q^2} \left[ a - j \frac{1}{2} \sqrt{\frac{L_2}{L_1}} \cdot \frac{kQ}{1+j2\delta Q} \right] \right| R_1 I_i \quad \dots(10.39)$$

Finally output voltage  $V_o$  of Foster-Seeley discriminator is given by,

$$\begin{aligned} V_o &= V_{30} - V_{40} \\ &= \eta R_1 I_i \left| \frac{Q^2(1+j2\delta Q)}{(1+j2\delta Q)^2+k^2Q^2} \right| = \left| a + j \frac{1}{2} \sqrt{\frac{L_2}{L_1}} \cdot \frac{kQ}{1+j2\delta Q} \right| \\ &\quad - \left| a - j \frac{1}{2} \sqrt{\frac{L_2}{L_1}} \cdot \frac{kQ}{1+j2\delta Q} \right| \end{aligned} \quad \dots(10.40)$$

## 10.8. Design Requirements of Centre Tuned Discriminator

The discriminator must be carefully designed. Some of the significant factors are discussed below.

(a) *Centre Tap*. The centre tap on the secondary must be situated at the true electrical centre of the circuit. If the secondary is in the form of a single continuous winding, this electrical centre may be at an appreciable distance from the physical centre. To overcome this difficulty, the secondary must be wound in two equal sections, one placed at the top of the other.

(b) *Elimination of Capacity Coupling.* Design assumes that the mutual inductance  $M$  between the primary and secondary alone is used. But in practice, a small amount of capacitive coupling always takes place between the winding. Such a capacitive coupling always takes place between the windings. The capacitive coupling distorts the discriminator characteristic. In the case of coaxial winding, a simple means generally adopted to counteract this tendency consists in returning to the supply that end of the primary winding which is nearest to the secondary winding. For better result, it is necessary to place between the primary and the secondary windings, an electrostatic screen in the form of either flat spiral of wire earthed at one end or a mesh of parallel wires, all wires being joined together at one end and connected to earth.

(c) *Balancing of Loads.* The loads of the two diodes must be accurately balanced under dynamic as well as static conditions. Failing this, this signal to noise ratio deteriorates. This balanced load condition requires that the load resistances  $R_3$  and  $R_4$  be equal and so also the capacitors  $C_3$  and  $C_4$ . But in shunt with capacitors  $C_3$  and  $C_4$  come the stray capacitances which are, in general unequal. A capacitive unbalance of as small as 5 to 10  $\mu\mu F$  is enough to deteriorate the performance seriously. Another source of capacitive unbalance is the coupling capacitor  $C_c$ . This capacitor  $C_c$  effectively comes in shunt with the lower diode  $D_2$  alone. To restore dynamic balance of the two low impedances, additional capacitance should be placed across the upper diode  $D_1$ . Proper value of this balancing capacity may be found by study of oscilloscopic patterns of output voltage of the discriminator in the presence of an impulsive wave train.

(d) *Inequality of D.C. and A.C. Loads.* Another source of distortion at high depths of modulation is the inequality of the D.C. load and A.C. load of the detector. Thus as in AM detection, here also the highest depth of modulation that may be handled without distortion is equal to  $R_i/(R_i + R_s)$ , where  $R_i$  is the D.C. load resistance, output across which is coupled by a coupling capacitor  $C_c$  to another resistor  $R_1$ . But in FM detection, the trouble is further increased by the fact that the A.C. load impedance presented by the diodes at the centre frequency may differ from that at other frequencies. At the centre frequency, the detected output voltage is zero so that any load may be connected between the earth and the audio frequency take off point without affecting the load conditions at the detector diode. Under frequency modulated condition, on the other hand, additional impedance comes in shunt with the load resistor causing additional damping of the discriminator transformer. This may result in distortion of the discriminator characteristic if the changes in effective  $Q$ 's of the primary and secondary circuits so caused during the modulation cycle are appreciable.

(e) *Distortion due to de-emphasis circuit.* The de-emphasis if placed directly across the load circuit of the discriminator may cause distortion. To avoid this distortion, the de-emphasis circuit or any other circuit placed directly across the discriminator output must have impedance large as compared with the diode load impedance.

### 10.9. Ratio Detector

Ratio detector is widely used as an FM detector because of the following merits : (i) it gives an excellent noise free output (ii) unlike centre tuned discriminator, it requires no limiter (iii) relatively fewer components are required and (iv) since no limiter is required, small signal AM rejection is considerably improved and hence the input required in ratio detector for noise-free operation is considerably smaller than that in centre-tuned discriminator.

Fig. 10.16 gives the basic circuit of a ratio detector. It may be seen that the basic circuit of ratio detector is similar to the basic circuit of centred tuned discriminator of Fig. 10.10 except that the polarity of diode  $D_1$  has been reversed.

Let the potential developed across  $C_3$  be  $V_{30}$  and let it be equal to  $-V$  volts at the centre frequency. Then evidently the potential  $V_{04}$  developed across  $C_4$  must also be equal to  $-V$  volts. The total output potential  $V_o$  then, being the sum of  $V_{30}$  and  $V_{04}$  must be equal to  $-2V$  volts at the centre frequency. In the case of centre tuned discriminator, this voltage  $V_o$  at the centre frequency is zero. If the input frequency now varies slightly from the centre frequency  $f_c$ , then voltage  $V_{30}$  and  $V_{04}$  change by equal and opposite amounts. Thus if  $V_{30}$  changes to the value  $-V + \Delta V$ , then  $V_{04}$  becomes  $-V - \Delta V$ . The net output potential then remains unaltered

at the value  $-2V$ . If frequency modulated voltage is applied at the input of the discriminator, then  $\Delta E$  varies in accordance with the audio modulating voltage. The voltage  $V_{04}$  ( $= -V - \Delta E$ ) developed across  $C_4$  may be used to provide the required detected output voltage. In practice, the detected audio frequency output is taken from  $O$ , the junction of load capacitors  $C_3$  and  $C_4$ , and point  $O'$ , the centre point of load resistors which is earthed. Since voltage  $V_0$  across terminals 3 and 4 remain unaltered inspite of variations in signal frequency, the capacitor  $C$  may be made very large. Usually an electrolytic capacitor of value  $10 \mu F$  or more is used. Capacitor  $C$  has then little effect on the performance of the circuit when the input signal is free from amplitude modulation. If, however, the input signal has an AM component, this AM component produces only a very small output across capacitor  $C$ .

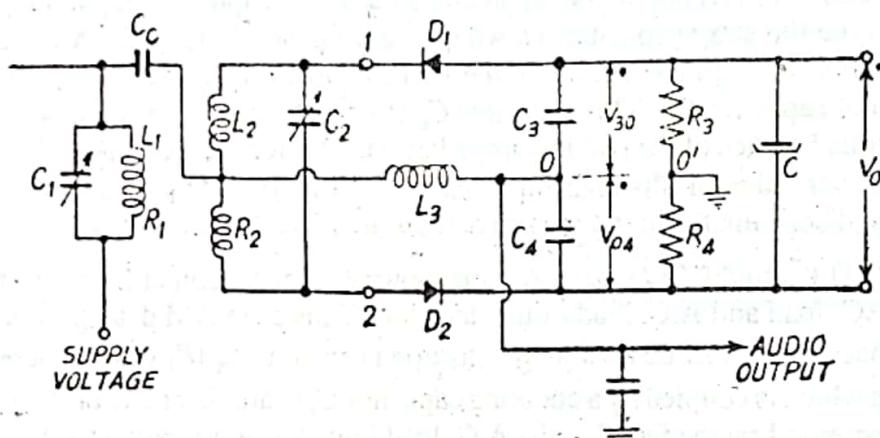


Fig. 10.16. Ratio detector.

Analysis of this ratio detector may be done in a manner similar to that used in centre tuned discriminator. The only essential difference lies in the polarity of diode  $D_1$  and hence in the polarity of voltage  $V_{30}$ . In both types of discriminators,  $V_i$  and  $V_{12}$  remain the same. Hence for ratio detector, we get

$$V_e = V_{30} + V_{04} = n [ |V_{10}| + |V_{20}| ] \quad \dots(10.41)$$

$$\begin{aligned} &= n R_1 I_1 \left| \frac{1 + j2\delta Q}{(1 + j2\delta Q)^2 + K^2 Q^2} \right| \cdot \left| 1 + j \frac{1}{2} \sqrt{\frac{L_2}{L_1}} \cdot \frac{KQ}{1 + j2\delta Q} \right| \\ &\quad + n R_1 I_1 \left| \frac{1 + j2\delta Q}{(1 + j2\delta Q)^2 + K^2 Q^2} \right| \cdot \left| 1 - j \frac{1}{2} \sqrt{\frac{L_2}{L_1}} \cdot \frac{KQ}{1 + j2\delta Q} \right| \end{aligned} \quad \dots(10.42)$$

It is clear from this expression that the total potential  $V_o$  is function of the input current  $I_i$  and hence is a function of the input signal amplitude. If, however, the frequency of the input signal varies, this voltage  $V_o$  varies very slowly and over the small frequency range of operation it is almost constant. The variation of  $V_o$  with variation of input voltage amplitude may, however, be eliminated by the use of large value capacitor  $C$ .

The ratio

$$\frac{V_{30}}{V_{04}} = \frac{1 + j \frac{1}{2} \sqrt{L_2/L_1} \cdot KQ / 1 + j2\delta Q}{1 - j \frac{1}{2} \sqrt{L_2/L_1} \cdot KQ / 1 + j2\delta Q} \quad \dots(10.43)$$

The ratio  $V_{30} / V_{04}$  is independent of the input current  $I_i$  and hence is independent of input signal amplitude.

Over the limited frequency range of operation, fractional frequency variation  $\delta$  is small so that Eq. (10.43) reduces to the following approximate form :

$$\frac{V_{30}}{V_{04}} = A_1 + A_2 \delta \quad \dots(10.44)$$

where  $A_1$  and  $A_2$  are constants.

Thus the voltage ratio  $V_{30} / V_{04}$  varies linearly with the fractional frequency variation  $\delta$ .

In practical ratio detector circuits, generally only a fraction of the primary reference voltage is introduced into the secondary through the coupling capacitor  $C_c$ .

The ratio detector has an inherent property that the degree of downward modulation which can be handled without distortion is dependent upon the degree of damping imposed under no modulation condition. The larger this damping, the greater is the downward depth of modulation which can be handled. Accordingly damping has to be kept high by keeping load resistors  $R_3$  and  $R_4$  low, of the order of 2 to 10 k $\Omega$ . Under such circumstances, it is advantageous to tap down on the primary winding. In order to secure high sensitivity and high signal level at the diodes inspite of this heavy damping, it is necessary to choose carefully this ratio  $a$  and also the coefficient to coupling of the transformer.

In the design of ratio detector, it is not practicable to adjust the coefficient of coupling  $K$  to get optimum linearity of discriminator characteristic as in the case of Foster-Seeley discriminator because here the choice of coefficient of coupling is made with a view to maximize AM rejection. The selectivity of the primary circuit of the discriminator transformer causes amplitude modulation of the signal but if good AM rejection is secured, such a selectivity will not materially affect of the audio output of the ratio detector. In this respect, ratio detector differs from the Foster-Seeley discriminator.

Regarding linearity of discriminator characteristic, ratio detector is, in general, inferior to Foster-Seeley discriminator. But the resulting distortion may be kept low by using a wide range of discriminator characteristic. The  $Q$  of the secondary should then be low; this also helps in AM rejection. Although no separate limiter is required in ratio detector AM rejection obtainable is, in general, only a little inferior to that in Foster-Seeley discriminator employing a separate limiter.

Ratio detector does not provide protection against long period variation in signal strength and hence AGC is essential with this type of detector. The D.C. voltage developed across the stabilizing capacitor  $C$  is generally used as the AGC control voltage.