North South University

Department of Electrical & Computer Engineering

LAB REPORT

Design Schematic Diagram and Layout of CMOS Circuit using Cadence Software

COURSE : CSE435

SECTION : 2

COURSE INSTRUCTOR : IQBALUR RAHMAN ROKON (IQR)

LAB INSTRUCTOR : SARIAH TUL QARIM

SUMBITTED BY :

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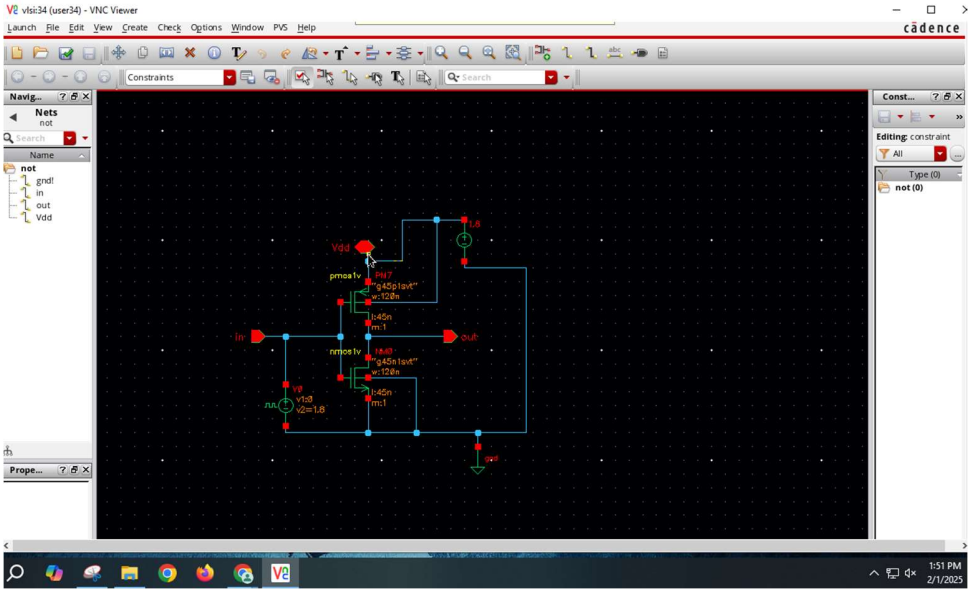
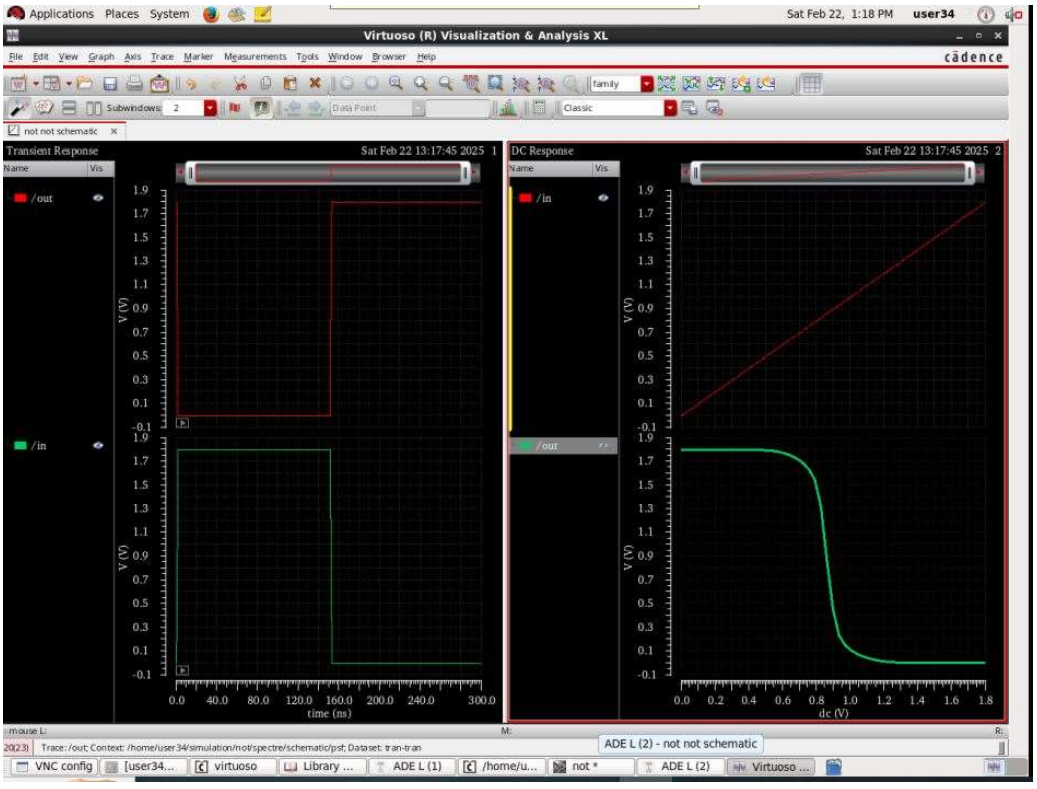
ID :2131081642
SEC : 02

CADENCE ID : USER 34

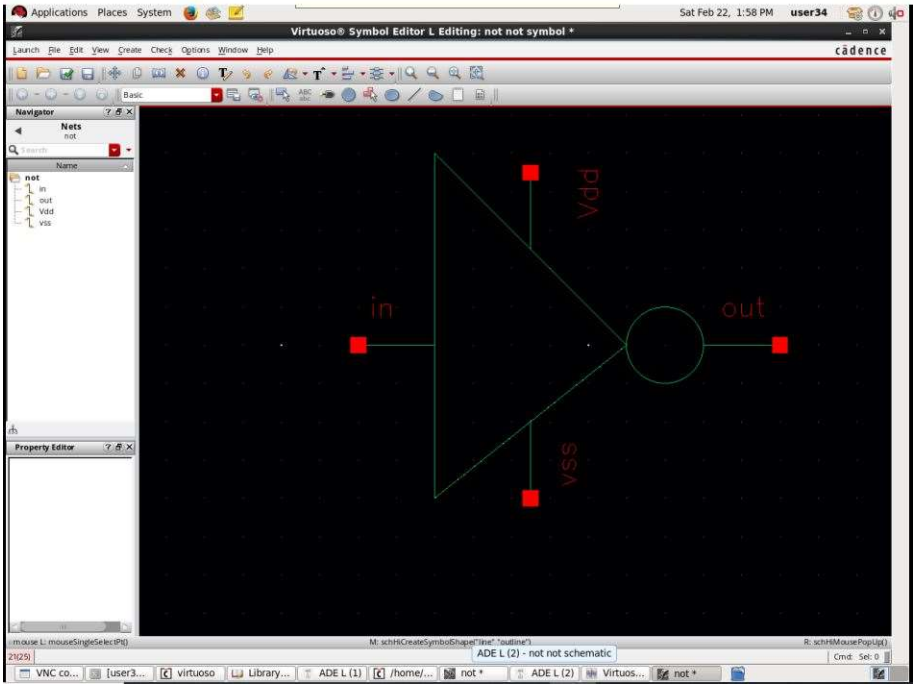
NOT GATE USING CMOS :



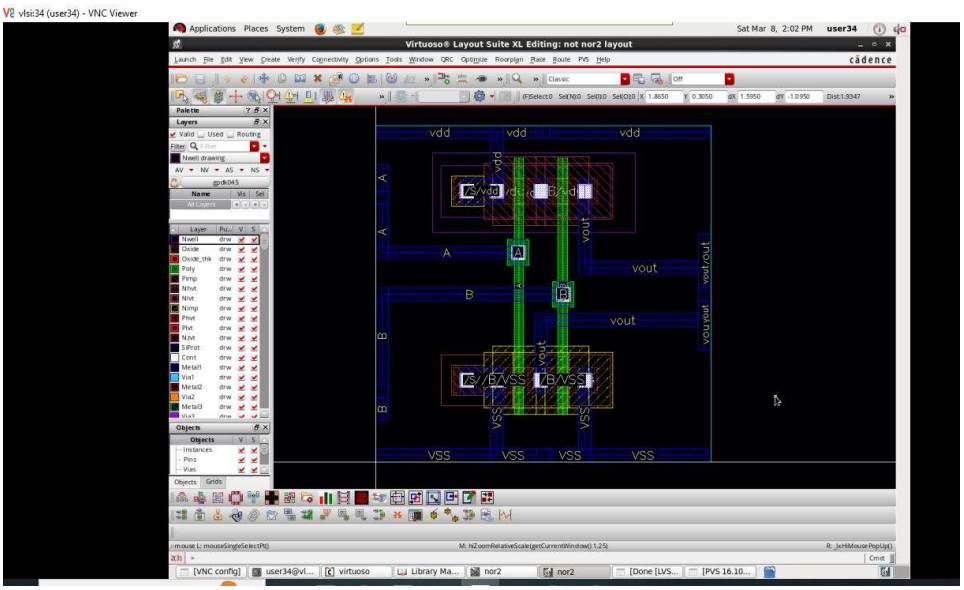
TIMING DIAGRAM (DC ANALYSIS):



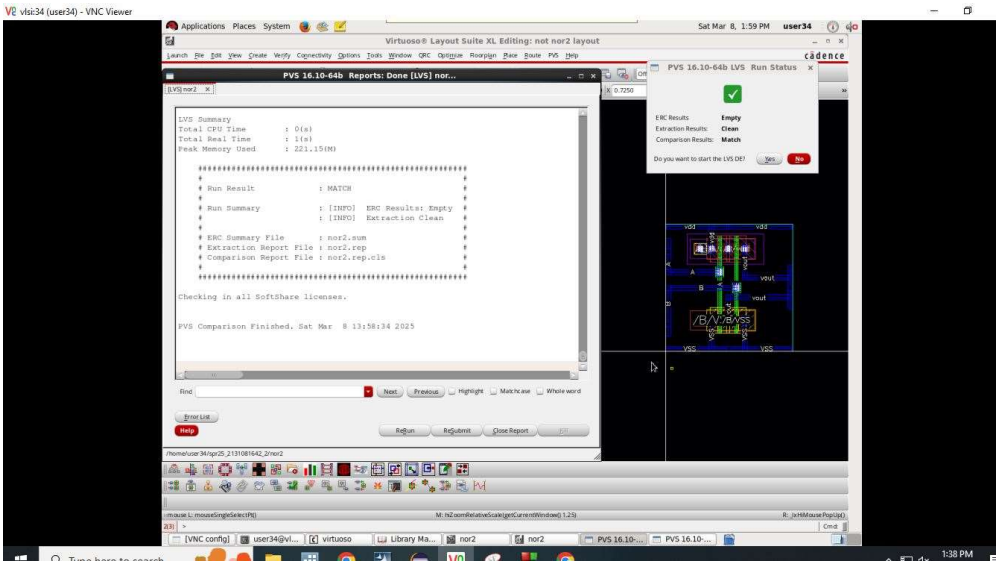
PIN DIAGRAM(NOT SYMBOL) :



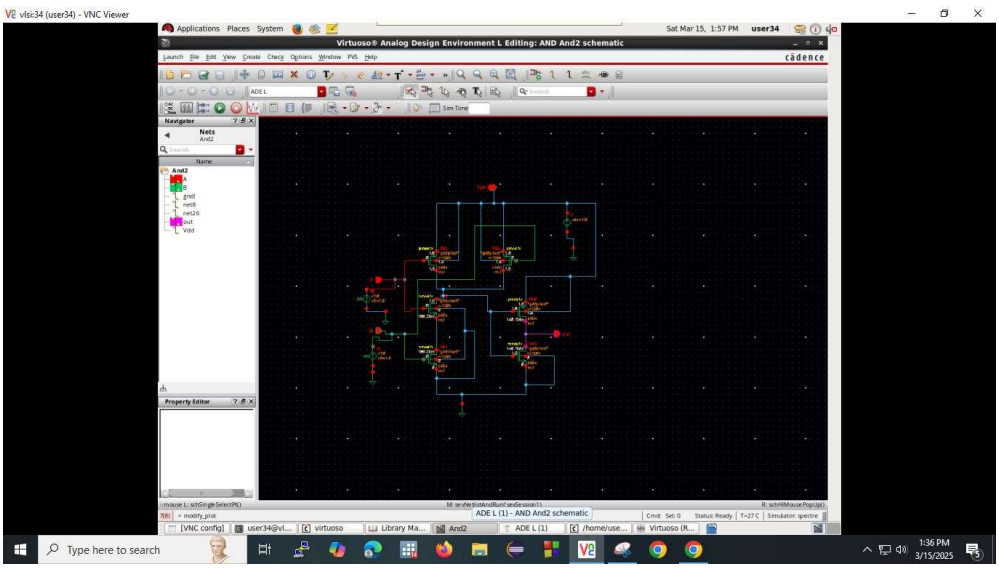
LAYOUT:



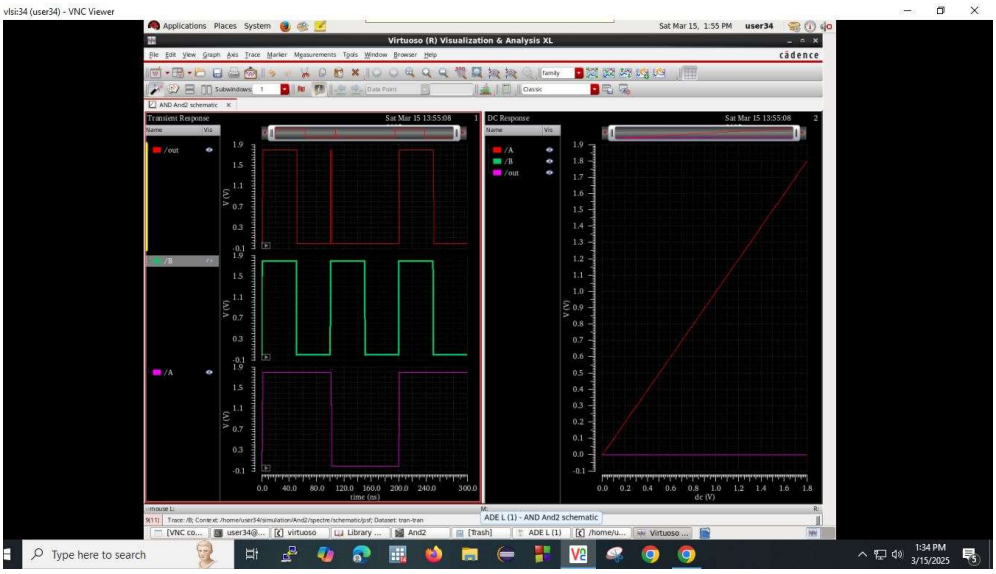
LVS MATCH :



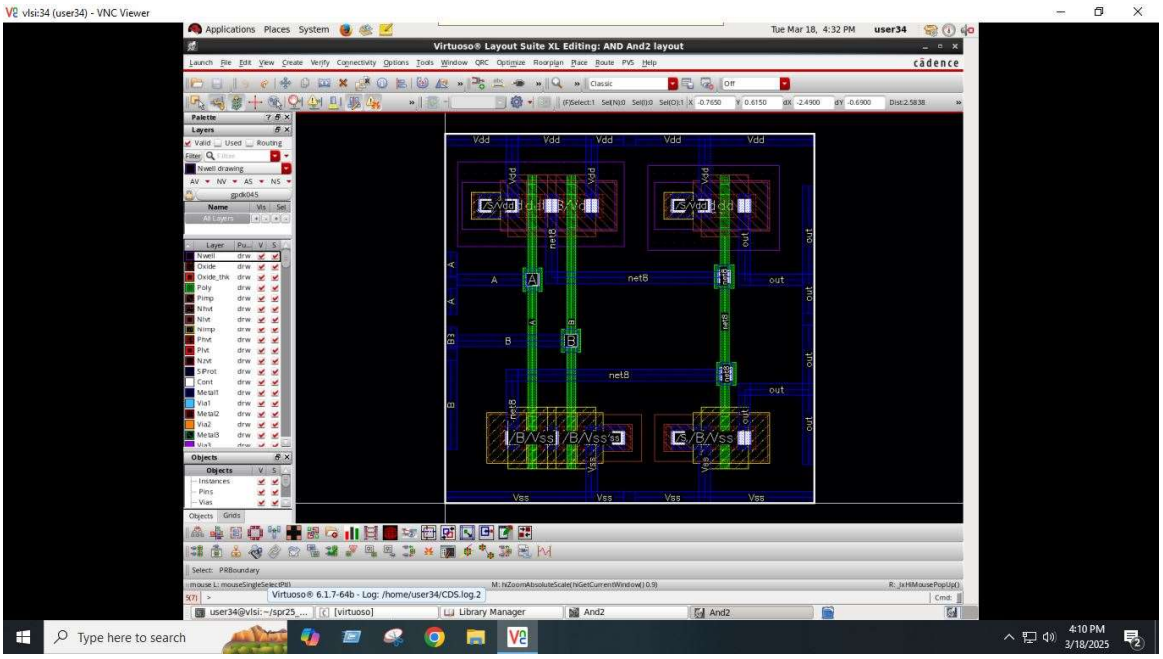
PROJECT (AND2) :



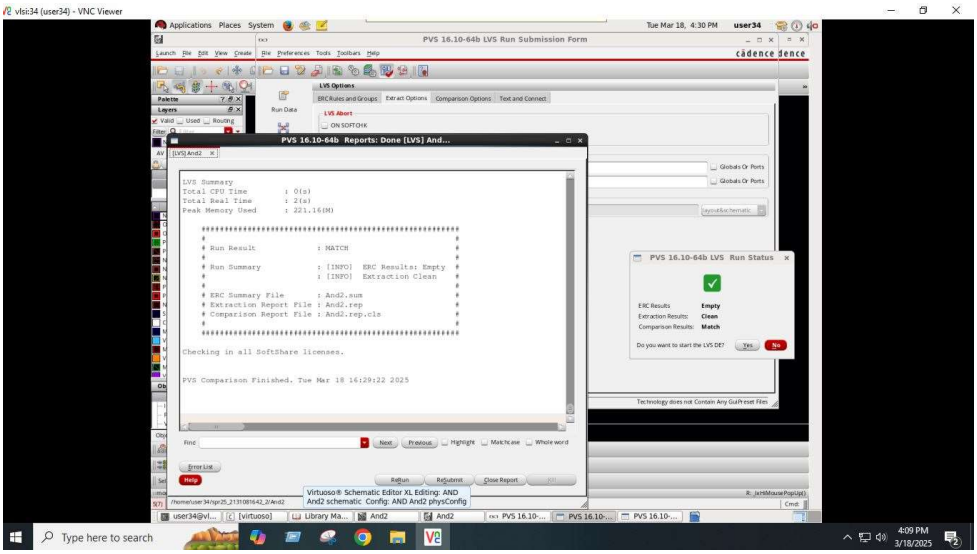
DC ANALYSIS :



LAYOUT :



LVS MATCH :


vlsi34 (user34) - VNC Viewer
Applications Places System
Tue Mar 18, 4:30 PM user34
PVS 16.10-64b LVS Run Submission Form
cadence
PVS 16.10-64b Reports: Done [LVS] And...
LVS Summary
Total CPU Time : 0(s)
Total Real Time : 2(s)
Peak Memory Used : 221.16(M)
Run Result : MATCH
Run Summary : [INFO] ERC Results: Empty
: [INFO] Extraction Clean
ERC Summary File : And2.sum
Extraction Report File : And2.rep
Comparison Report File : And2.rep.cls
Checking in all SoftShare licenses.
PVS Comparison Finished. Tue Mar 18 16:29:22 2025
PVS 16.10-64b LVS Run Status
ERC Results: Empty
Extraction Results: Clean
Comparison Results: Match
Do you want to start the LVS DE?
Yes
No
Virtuoso® Schematic Editor XL Editing: AND
And2 schematic Config: AND And2 physConfig
Type here to search
4:09 PM
3/18/2025