NORTH SOUTH UNIVERSITY

DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

EEE413L/CSE413L/ETE419L: Verilog HDL: Modeling, Simulation & Synthesis

PROJECT

Instruction

- Write your name, ID, and section.
- Two designing problems are given. Simulate and synthesis both problems using ModelSim, Xilinx and Cadence.
- Attach screenshots for each problem.
- Save the file in pdf format.
- Print and submit the hardcopy of your assignment. **[Online submission is strictly prohibited]**

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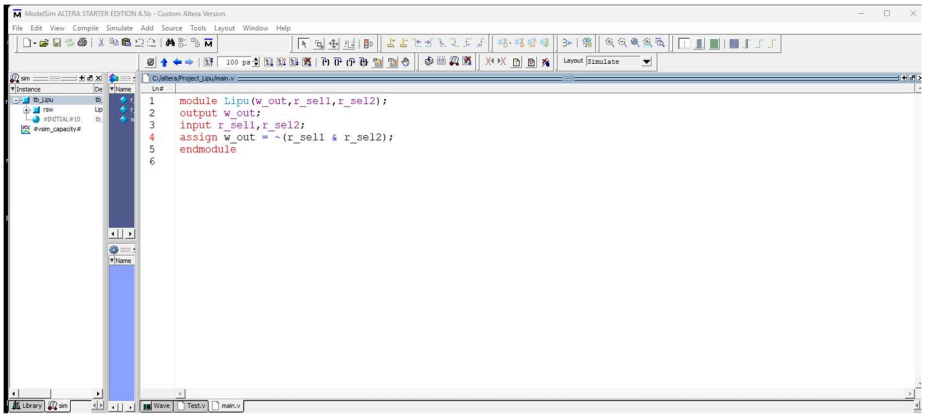
Problem 1

Consider the truth table below. The truth table shows a **2-bit input** truth table. Here **r_Sel[1]** and **r_Sel[0]** are **1-bit inputs** and **w_Out** is **1-bit output**. You need to know the value of both **r_Sel[1]** and **r_Sel[0]** to determine the value of the output **w_Out** using conditional operation of data flow modeling. Simulate and synthesis your design.

r_Sel[1]	r_Sel[0]	w_Out
0	0	1
0	1	1
1	0	1
1	1	0

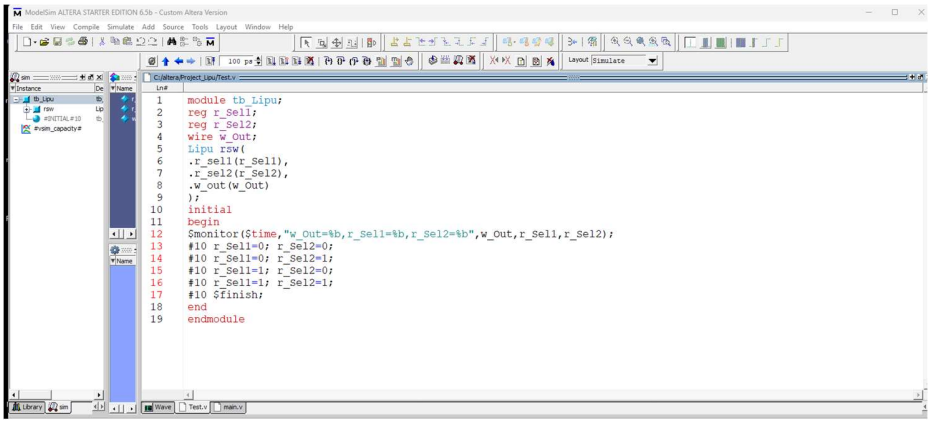
Attach screenshots of the following parts.

1. Main module.



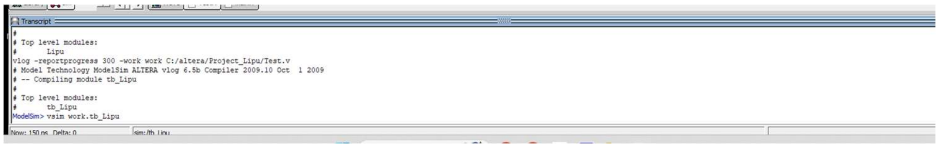
```
module Lipu(w_out,r_sel1,r_sel2);
output w_out;
input r_sel1,r_sel2;
assign w_out = ~(r_sel1 & r_sel2);
endmodule
```

2. Testbench.



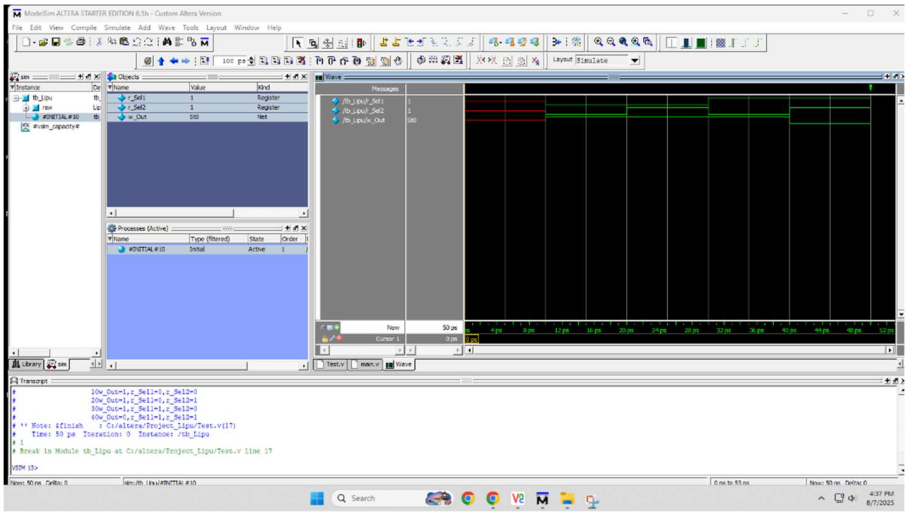
```
module tb_Lipu;
reg r_Sel1;
reg r_Sel2;
wire w_Out;
Lipu rsw(
.r_sel1(r_Sel1),
.r_sel2(r_Sel2),
.w_out(w_Out)
);
initial
begin
$monitor($time,"w_Out=%b,r_Sel1=%b,r_Sel2=%b",w_Out,r_Sel1,r_Sel2);
#10 r_Sel1=0; r_Sel2=0;
#10 r_Sel1=0; r_Sel2=1;
#10 r_Sel1=1; r_Sel2=0;
#10 r_Sel1=1; r_Sel2=1;
#10 $finish;
end
endmodule
```

3. Transcript after compiling using ModelSim.

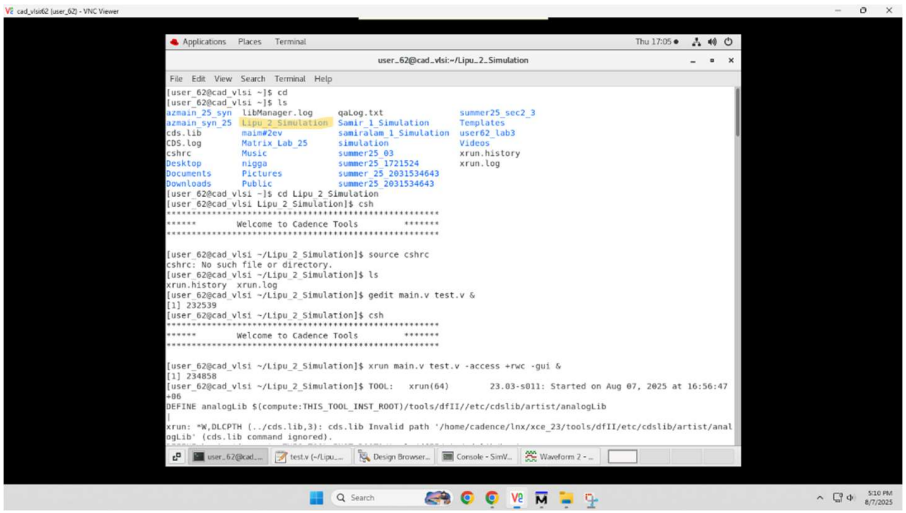


```
# Top level modules:
#       Lipu
vlog -reportprogress 300 -work work C:/altera/Project_Lipu/Test.v
# Model Technology ModelSim ALTERA vlog 6.5b Compiler 2009.10 Oct  1 2009
# -- Compiling module tb_Lipu
#
# Top level modules:
#       tb_Lipu
ModelSim> vsim work.tb_Lipu
```

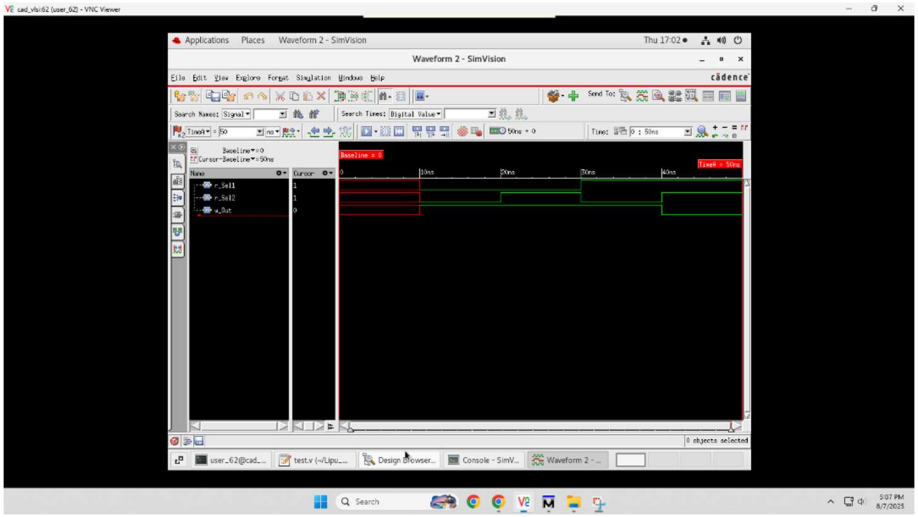
4. Waveforms after complete simulation using ModelSim.



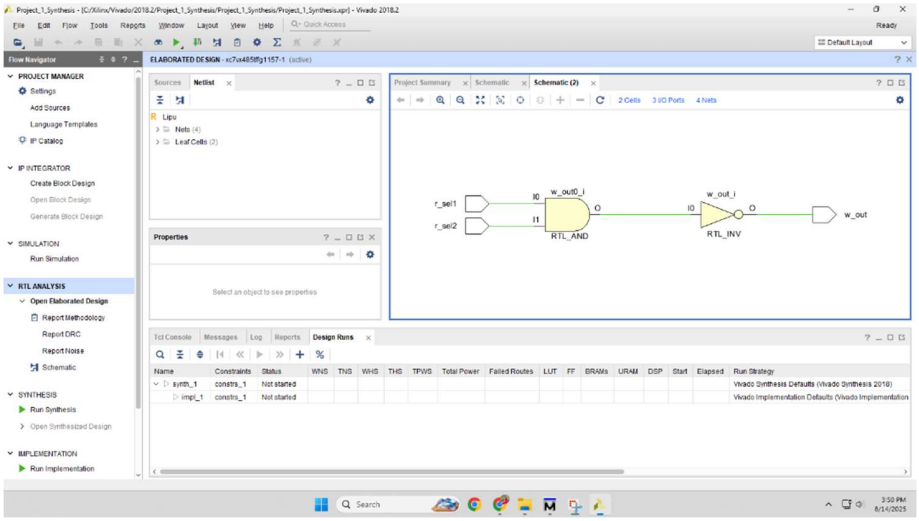
5. Using VNC viewer, make a directory in the form **'Name_Section_Simulation'** [eg. Oshin_1_Simulation], save the main module and testbench in that directory, and take a screenshot of that directory.



6. Waveform after complete simulation using Cadence.

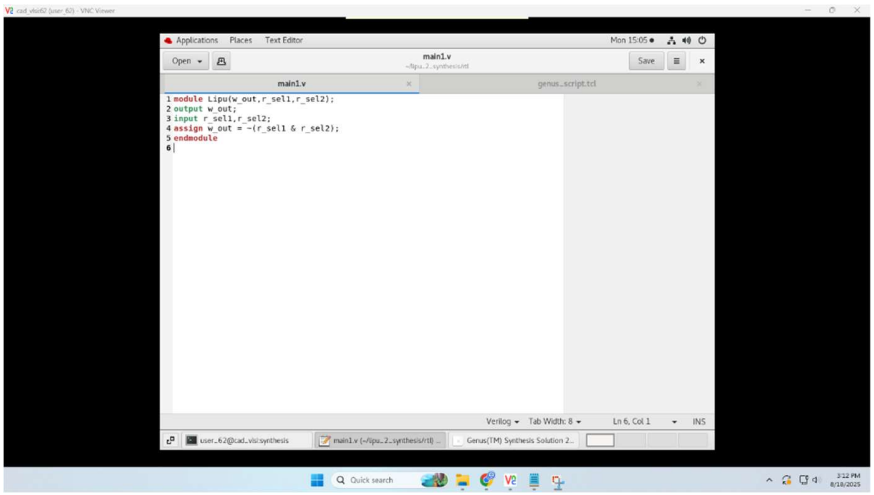


7. RTL Schematic after synthesis using Xilinx.

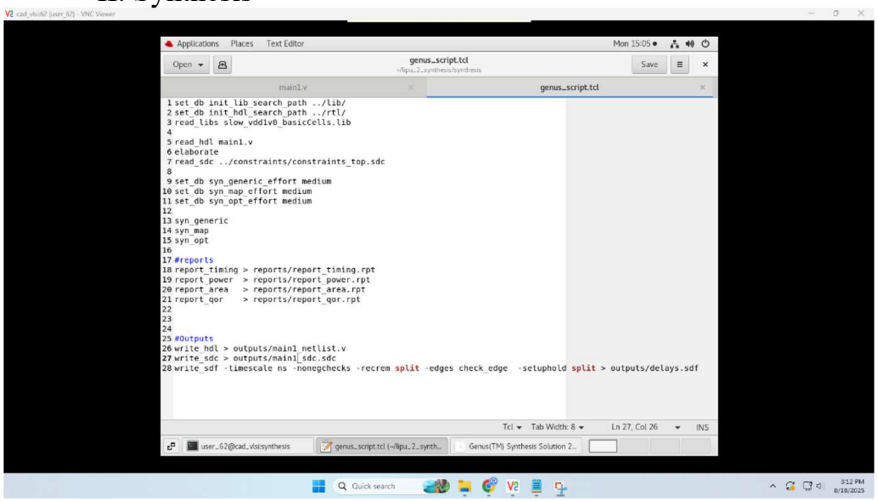


8. Using VNC viewer, make a directory in the form **'Name_Section_Synthesis'** [eg. Oshin_1_Synthesis], make the four directories [constraints, lib, rtl, synthesis] inside that directory, save the main module inside rtl and take screenshots changing directory to

I. rtl

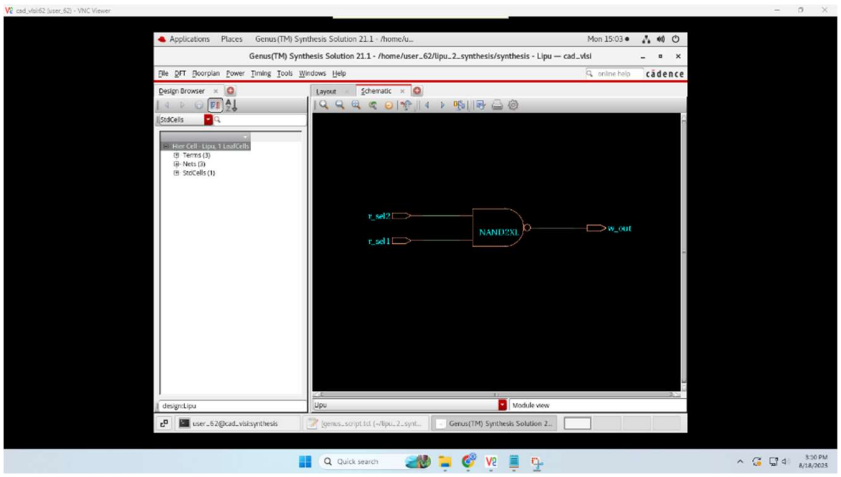


II. Synthesis



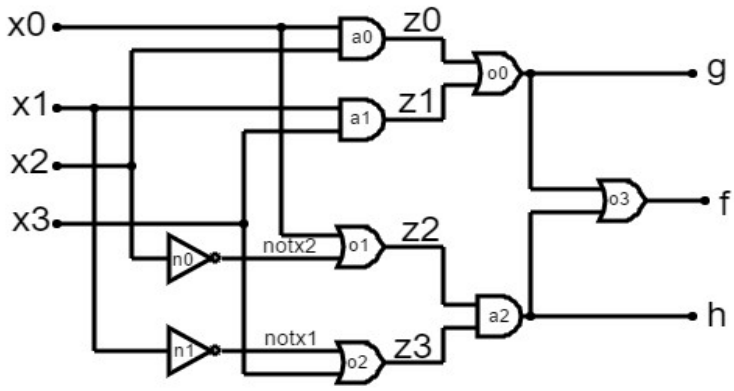
[*Note:Take screenshots after copying necessary files from root for synthesis*]

9. Schematic after synthesis using Cadence.



Problem 2

A simple logic gates circuit is given below where **x0, x1, x2, x3** are **1-bit inputs** and **g, f, h** are **1-bit outputs.** Simulate and synthesis your design.



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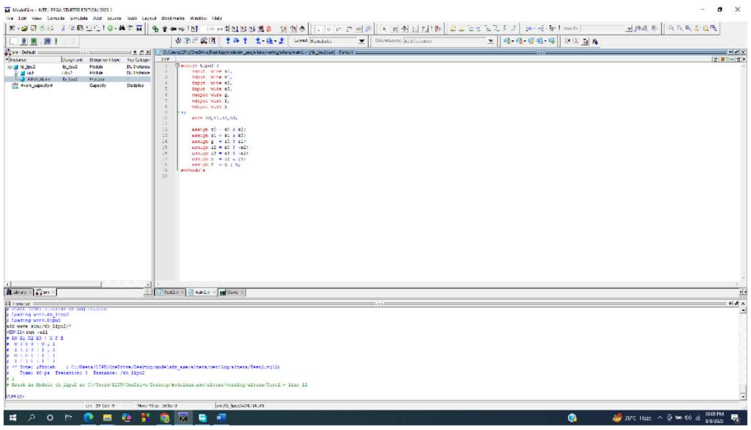
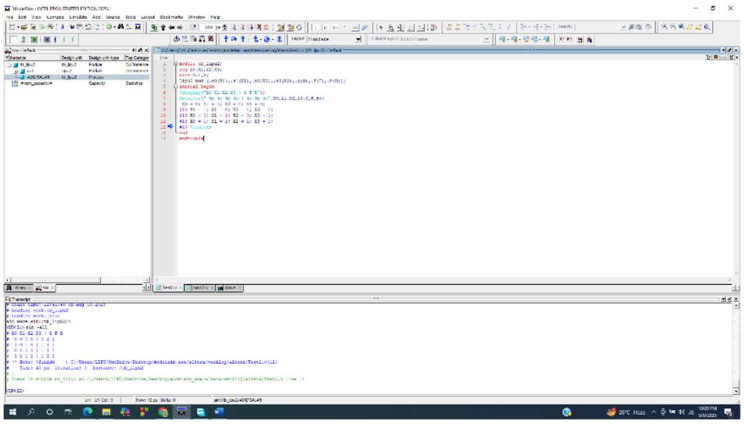
1. Main module.



2. Testbench.



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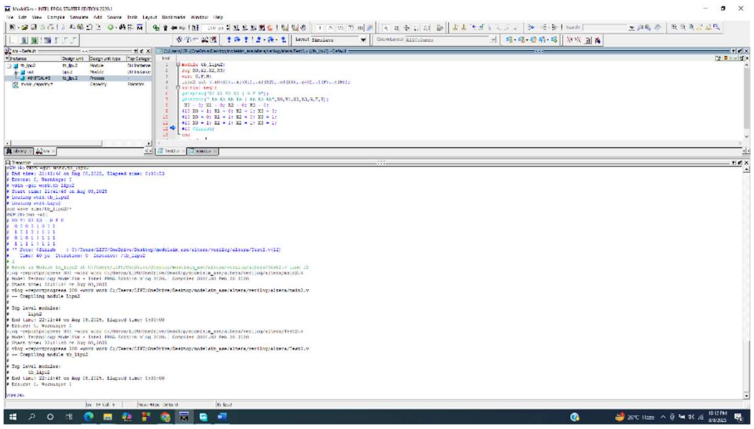
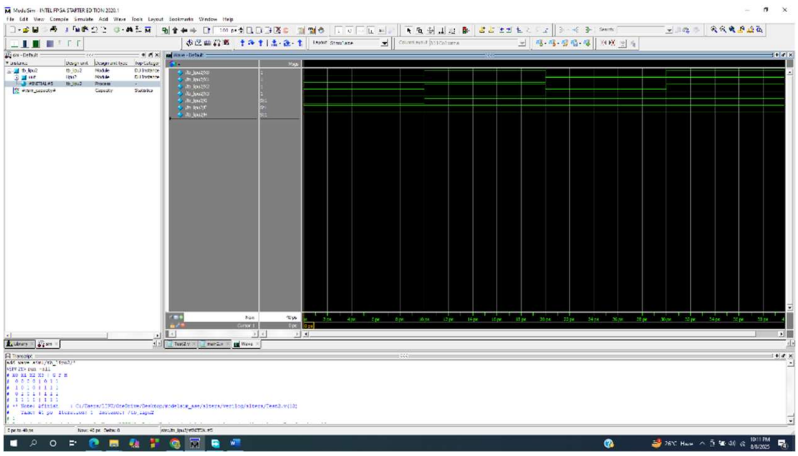


4. Waveforms after complete simulation using ModelSim.



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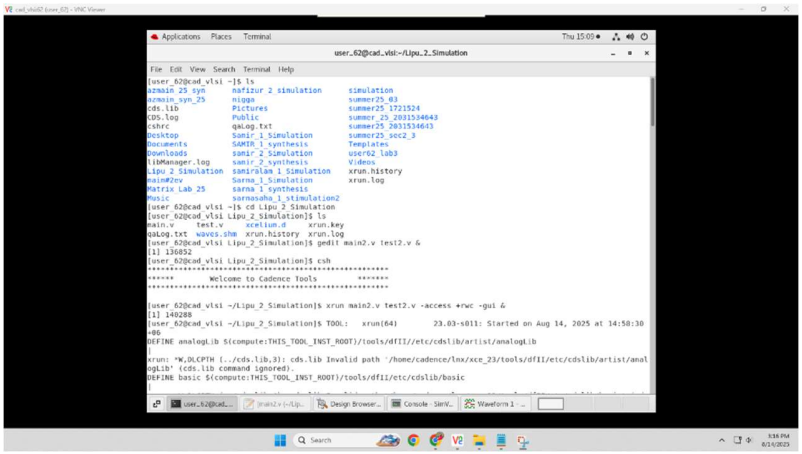

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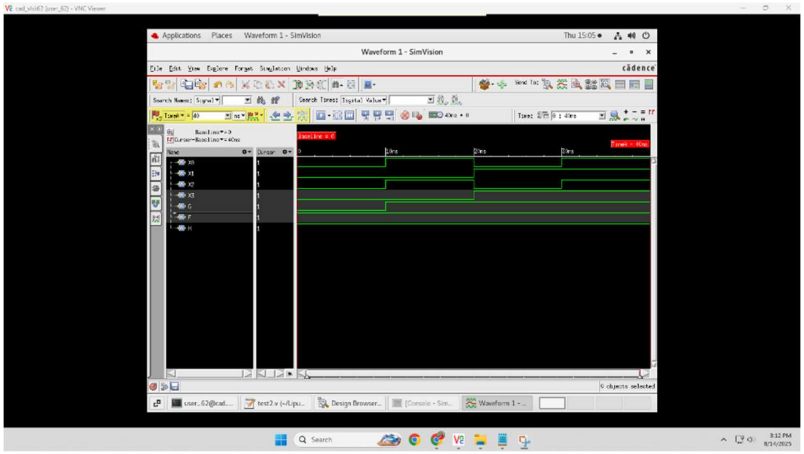

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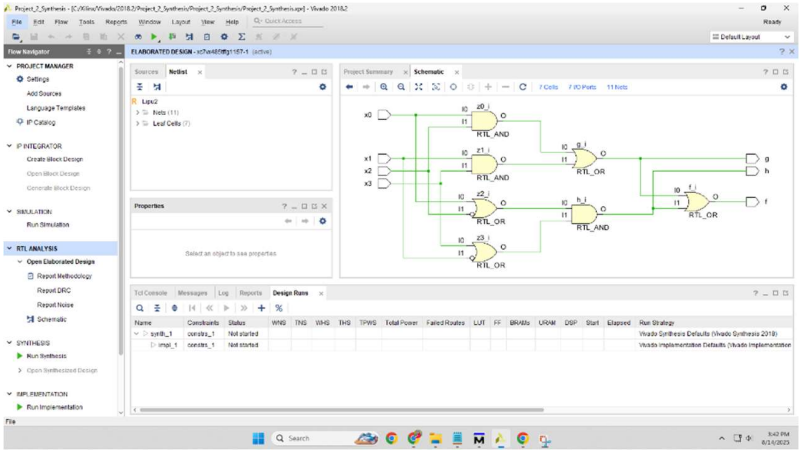

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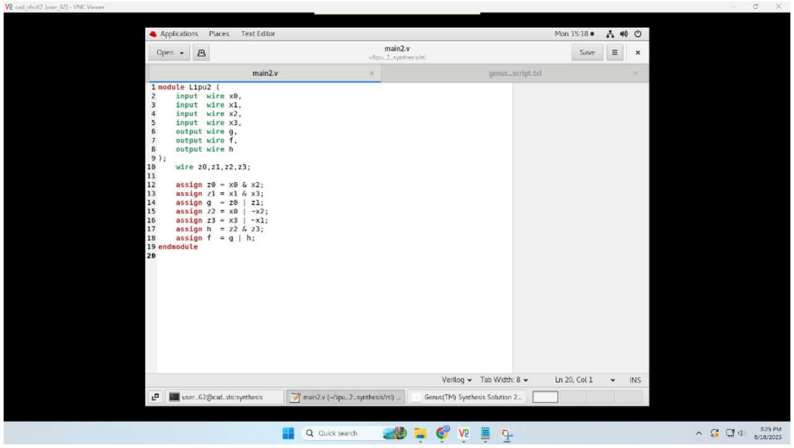

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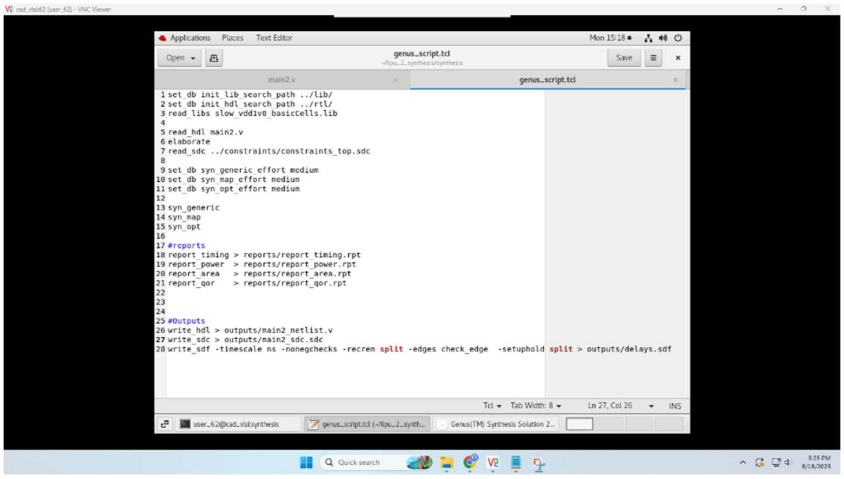

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