PROJECT ON 2 – BIT ASYNCHRONOUS DOWN COUNTER USING CADENCE

Submitted for requirements for the practical coursework

of

M Tech (VDN)

by

ASHRETA SAHAY

Roll no 2302102033

DISCIPLINE OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

15th Nov

INDIAN INSTITUTE OF TECHNOLOGY INDORE

I hereby certify that the work which is being presented in the report entitled **Project on 2 bit asynchronous down counter using Cadence** submitted for requirements of the practical coursework of **M Tech (VDN)** and submitted in the Discipline of Electrical Engineering**, Indian Institute of Technology Indore**, is an authentic record of my work carried out during the time period from Aug2023 to Nov 2023 under the supervision of Dr. Santosh Kumar Vishwakarma. The matter presented in this report has been cited properly wherever necessary.

(Ashreta Sahay)

This is to certify that the above statement made by the candidate is correct to the best of my/our knowledge.

(Dr. Santosh Kumar Vishvakarma)

ACKNOWLEDGEMENTS

First of all, I would like to thank my Supervisor Dr. Santosh Kumar Vishwakarma whose constant motivation, guidance and suggestion helped me to accomplish the task. I would also like to thank him for providing Cadence software resources associated with Nanoscale Devices, VLSI Circuit and System Design (NSDCS) Lab. I Would Like to Thank NSDCS PhD Scholar Mr. Shashank, Mr. Sonu, Mr. Vikas, Mr. Mukul, Ms. Vasundhara, Mr. Sagar, Mr. Radheshyam, Ms. Komal and Ms. Neha Maheshwari for guidance and support and fellow MTech VDN student for constant motivation towards achieving the task.

SYNOPSIS

A **Counter** is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit.

This project includes making schematic and layout of 2-bit asynchronous down counter using T flipflop. Model library SCL 180nm has been used to make schematic and layout. Pmos18 and Nmos18 have been used from model library to design. Analog library has been used for voltage source and ground.

Further, verification of the schematic and layout has been carried out to verify the functionality of the counter by doing schematic simulation. For layout verification , Design Rule Check (DRC) , Layout v/s Schematic Check (LVS) has been carried out. Post layout simulation has been done to verify the pre-layout simulation results.

LIST OF FIGURES

TABLE OF CONTENTS

1.INTRODUCTION

A **Counter** is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit. For example, in up counter a counter increases count for every rising edge of clock. Not only counting, a counter can follow the certain sequence based on our design like any random sequence 0,1,3,2…. They can also be designed with the help of flip flops. They are used as frequency dividers where the frequency of given pulse waveform is divided. Counters are sequential circuit that count the number of pulses can be either in binary code or BCD form. The main properties of a counter are timing, sequencing, and counting.

Counter works in two modes :

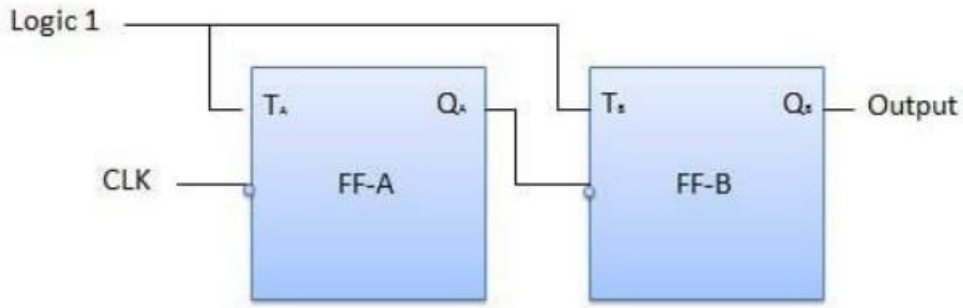
- Up counter - Counts in ascending order
- Down counter – Counts in descending order

Counters are broadly divided into two categories :

- Asynchronous counter
- Synchronous counter

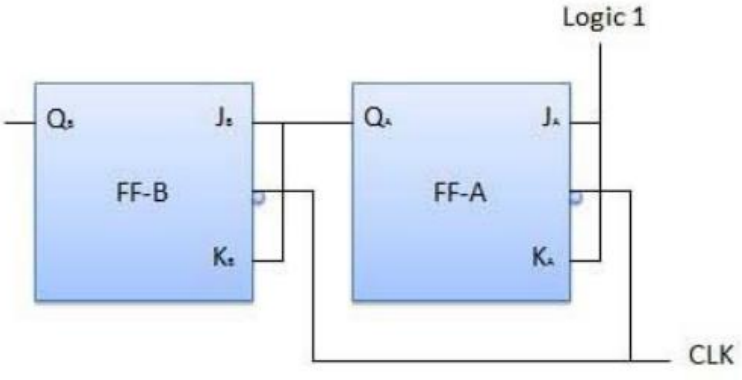
1. Asynchronous Counter

In asynchronous counter we don't use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following flip flop is driven by output of previous flip flops. Ripples are generated through outputs of each flip flop, hence it is also called **"RIPPLE"** counter and serial counter. A ripple counter is a cascaded arrangement of flip flops where the output of one flip flop drives the clock input of the following flip flop.



2. Synchronous Counter

Unlike the asynchronous counter, synchronous counter has one global clock which drives each flip flop so output changes in parallel. The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of same clock is given to each flip flop. It is also called as parallel counter.

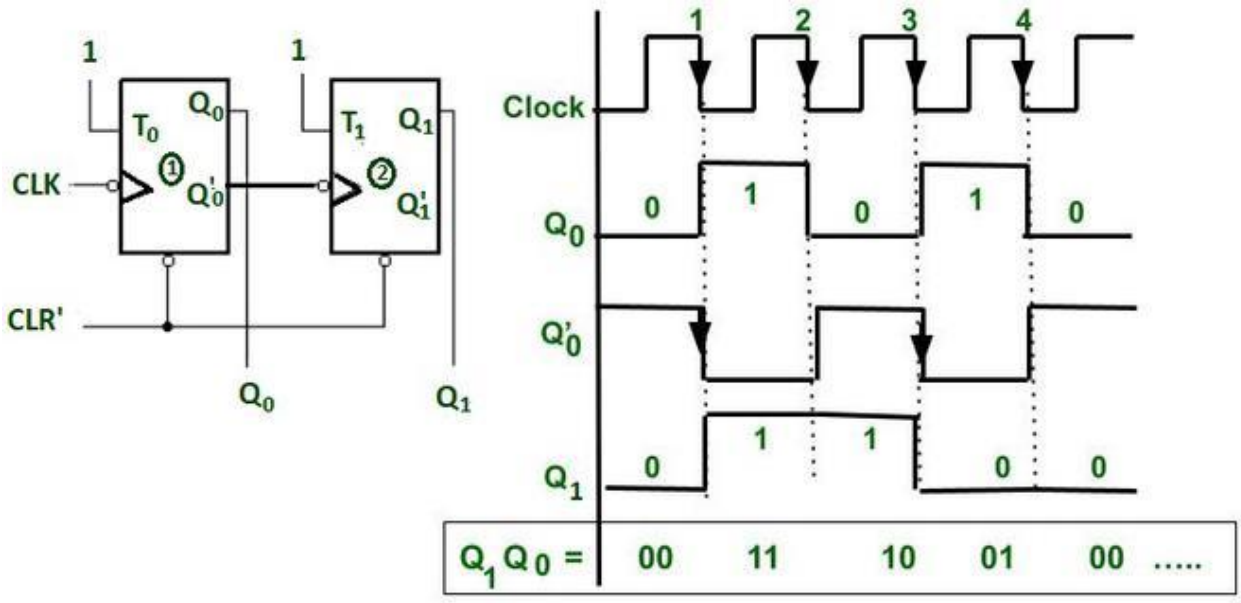


2. THEORY

2.1 2 – bit asynchronous counter

In asynchronous/ripple counter output of the first flip-flop is provided as the clock to the second flip-flop i.e flip-flop(FF) are not clocked simultaneously. Circuit is simpler, but speed is slow. We have designed down counter using T flip flop.

When the complemented output state (i.e. **Q'**) of previous FF is feed as clock to next FF then the counter will perform down counting as you seen below(i.e. 3 2 1 0). After 4th -ve edge clock pulse the sequence will repeat.



2-bit asynchronous down counter

We required 2 T- flip flops for our counter as depicted in above diagram.

2.2 T – FLIPFLOP

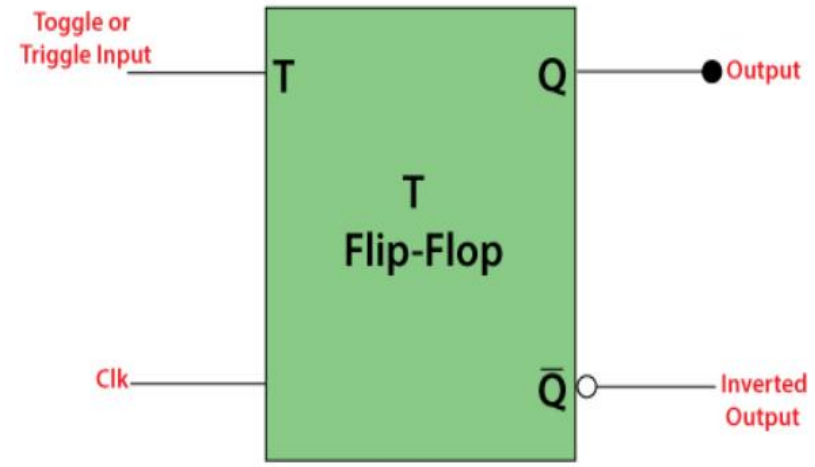
In T flip flop, "T" defines the term "Toggle". In SR Flip Flop, we provide only a single input called "Toggle" or "Trigger" input to avoid an intermediate state occurrence. Now, this flip-flop work as a Toggle switch. The next output state is changed with the complement of the present state output. This process is known as "Toggling"'.

We can construct the "T Flip Flop" by making changes in the "JK Flip Flop". The "T Flip Flop" has only one input, which is constructed by connecting the input of JK flip flop. This single input is called T. In simple words, we can construct the "T Flip Flop" by converting a "JK Flip Flop". Sometimes the "T Flip Flop" is referred to as single input "JK Flip Flop".

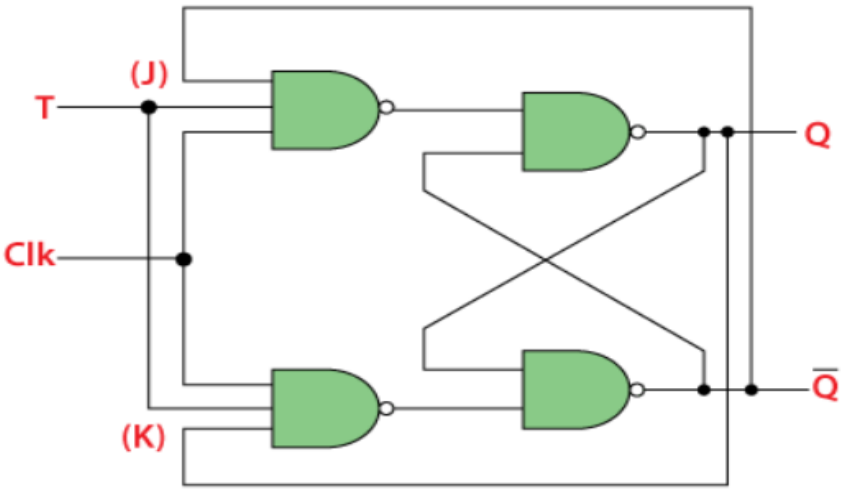
- Truth Table of T Flip Flop :

	Previous		Next	
T	Q	Q′	Q	Q′
0	0	1	0	1
0	1	0	1	0
1	0	1	1	0
1	1	0	0	1

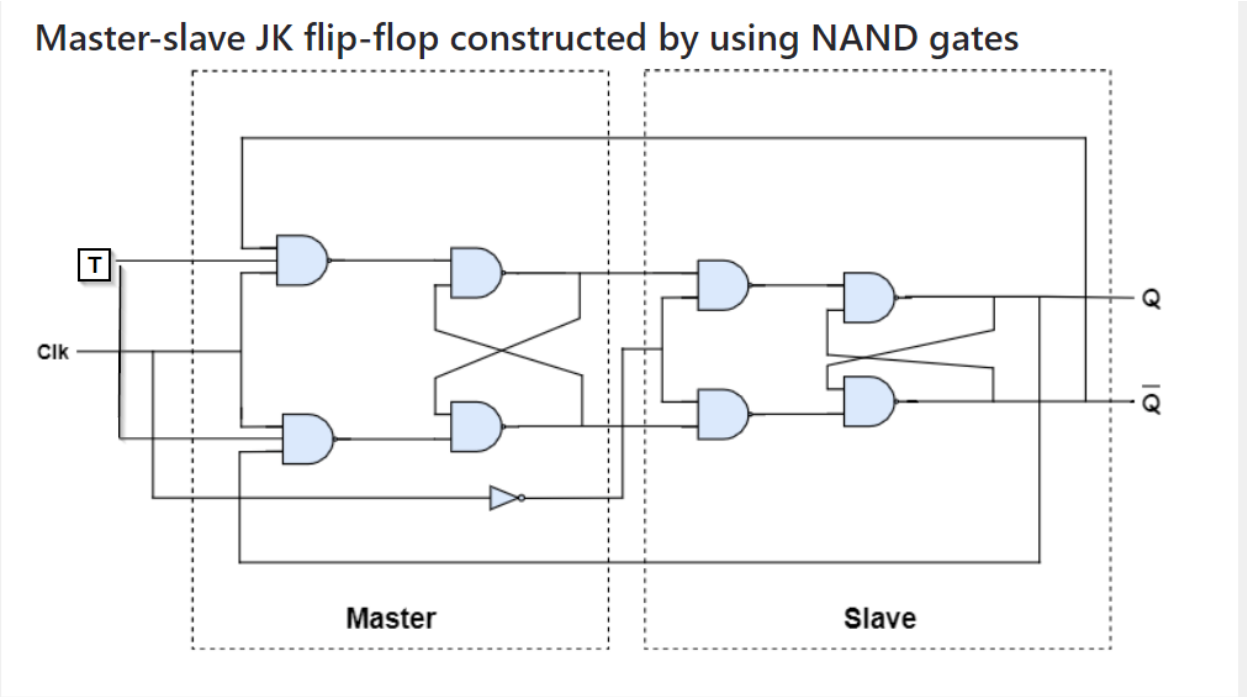
- T Flip Flop Representation



- **NAND implementation of T flip flop**



We have used master slave configuration for counter to invoke edge triggering so as to eliminate race around condition, as follows:



3. CADENCE – SCHEMATIC

3.1 SCHEMATIC :

- 2 input NAND gate :

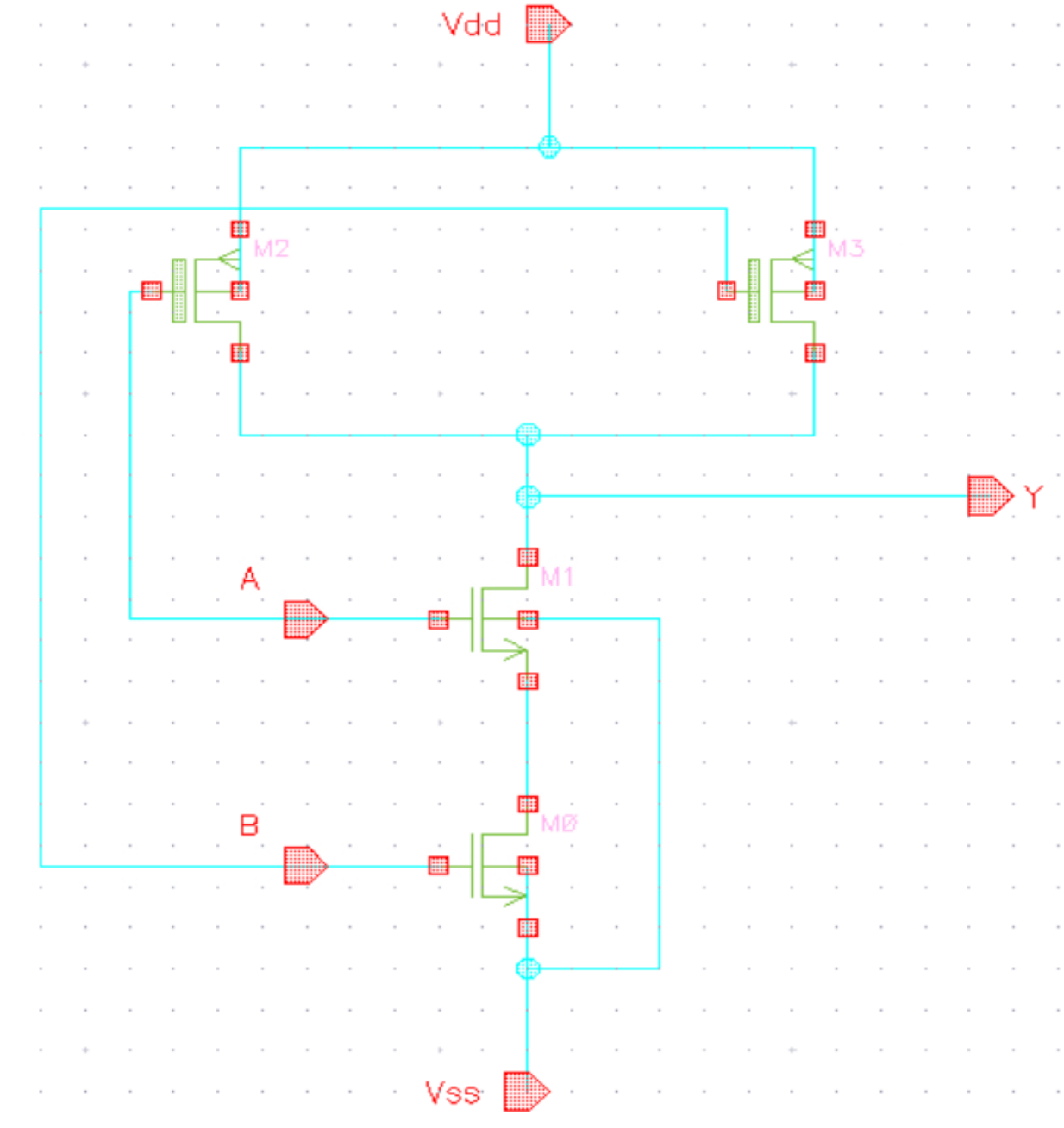


Fig. 1

- 3 input NAND gate:

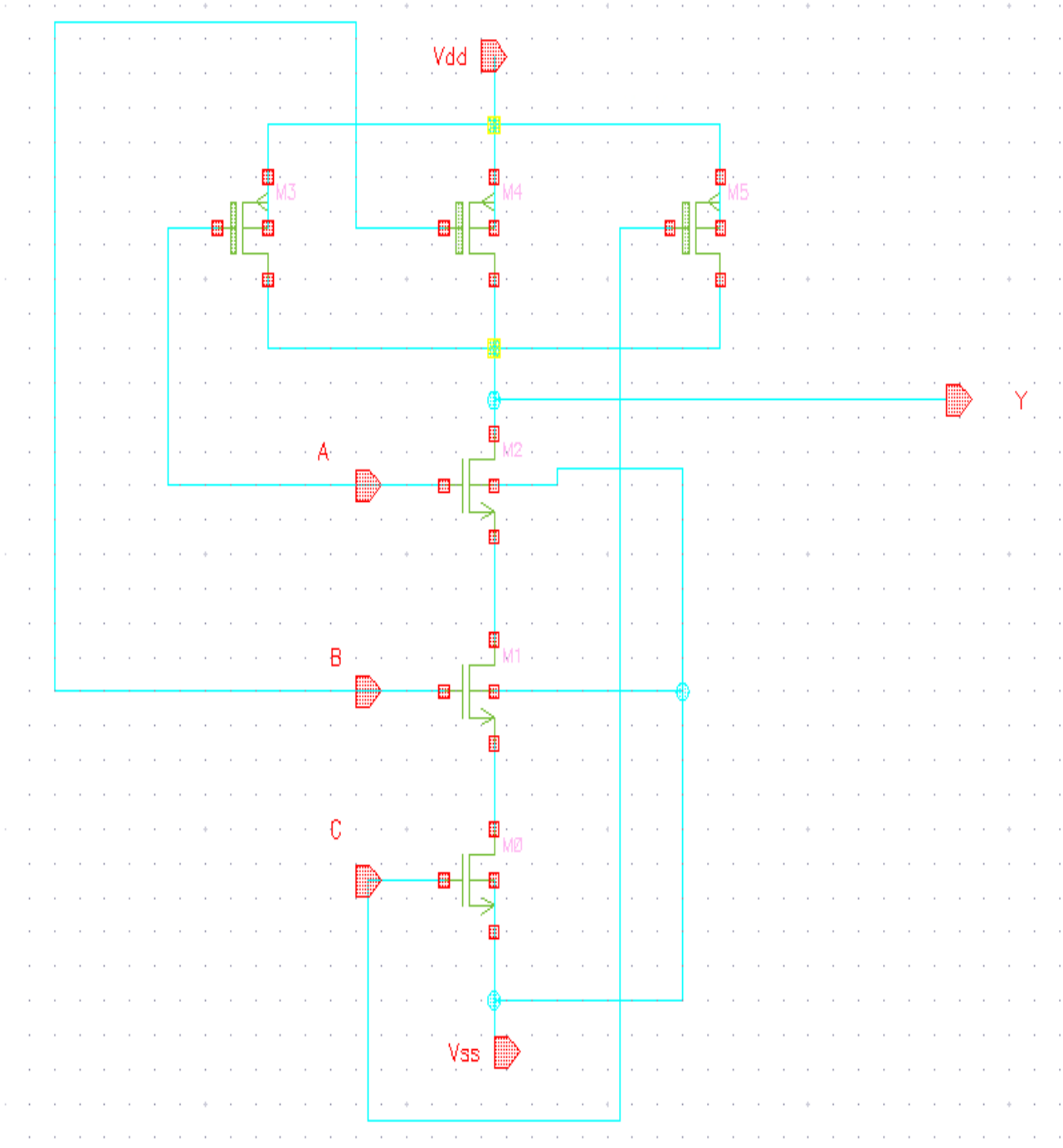


Fig. 2

- CMOS Inverter

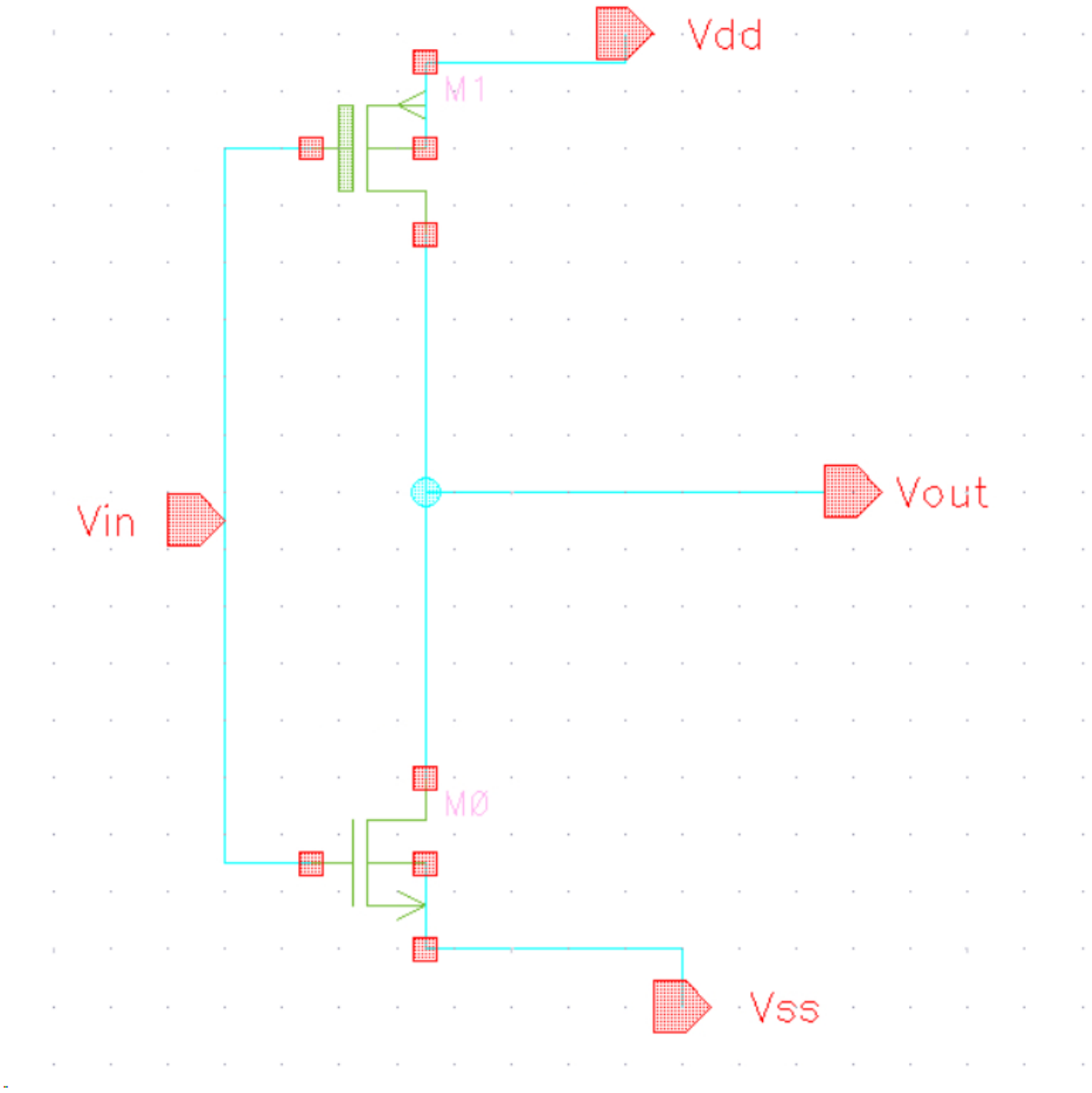


Fig. 3

- Master Slave T Flip flop

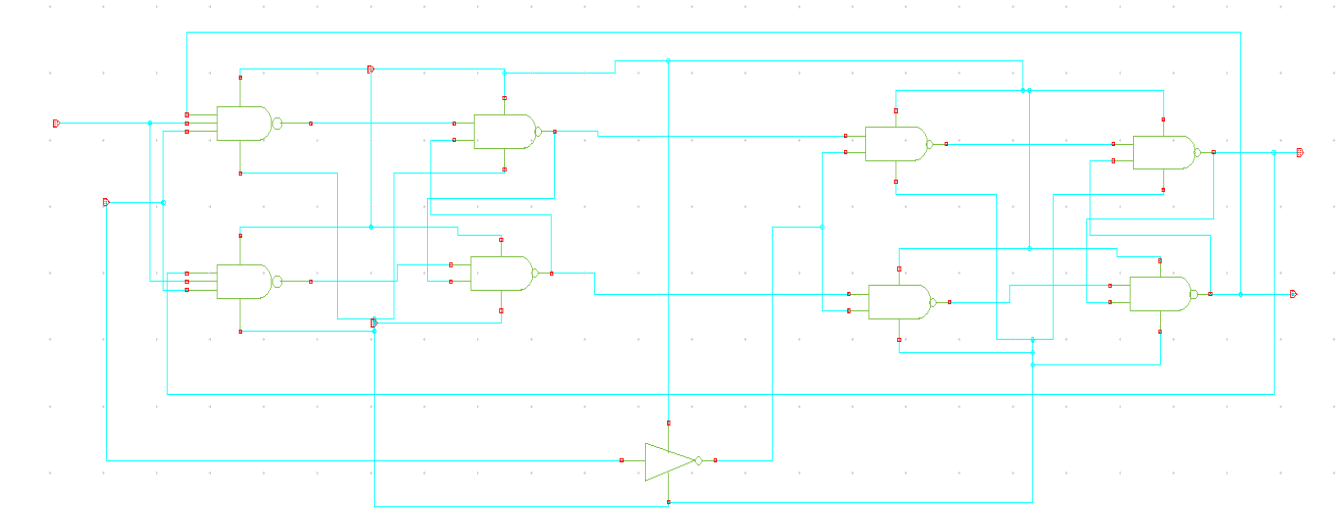


Fig. 4

- 2 – bit asynchronous down counter

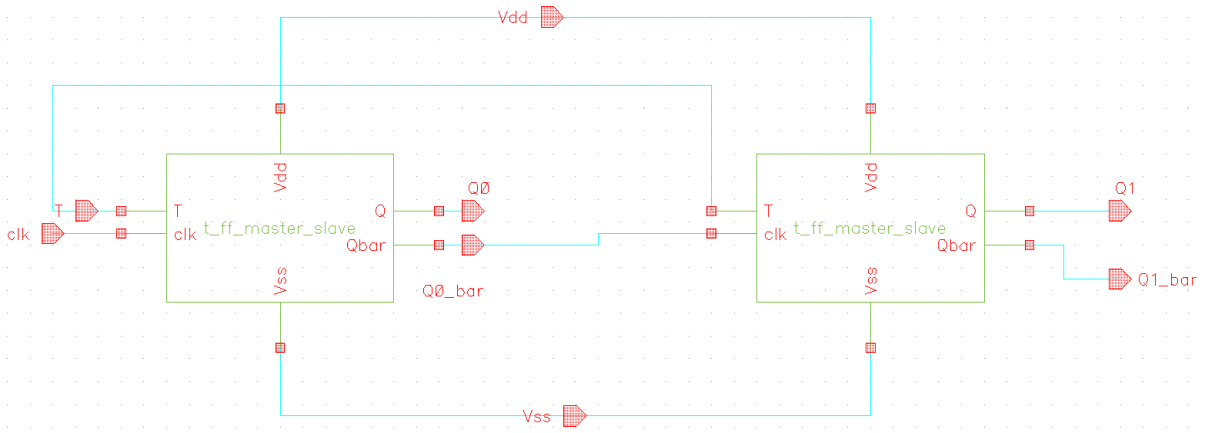


Fig. 5

3.2 SYMBOL

- 2 – input NAND

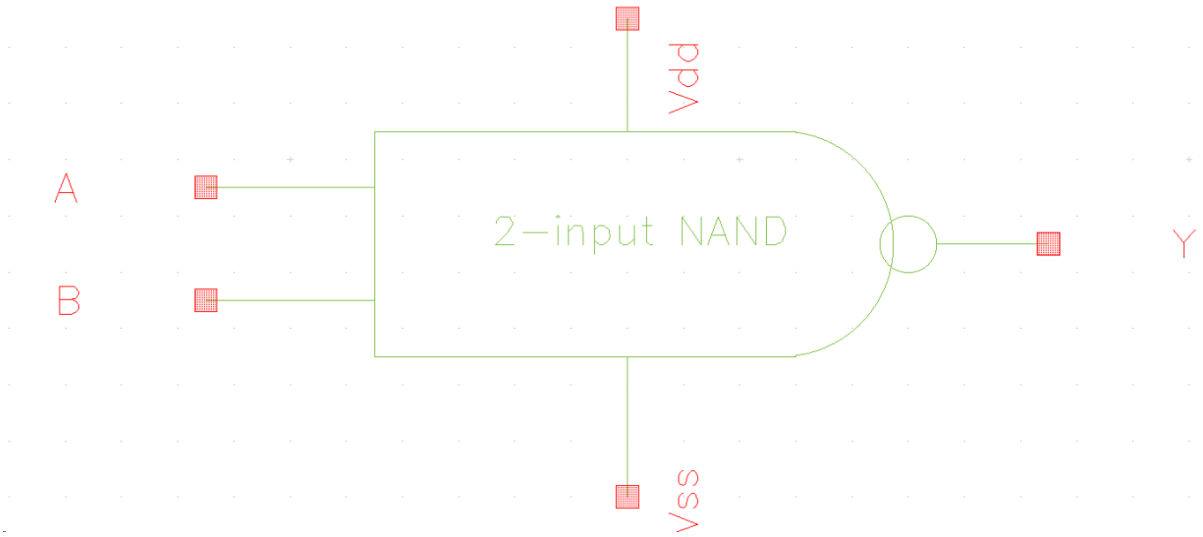


Fig. 6

- 3 – input NAND

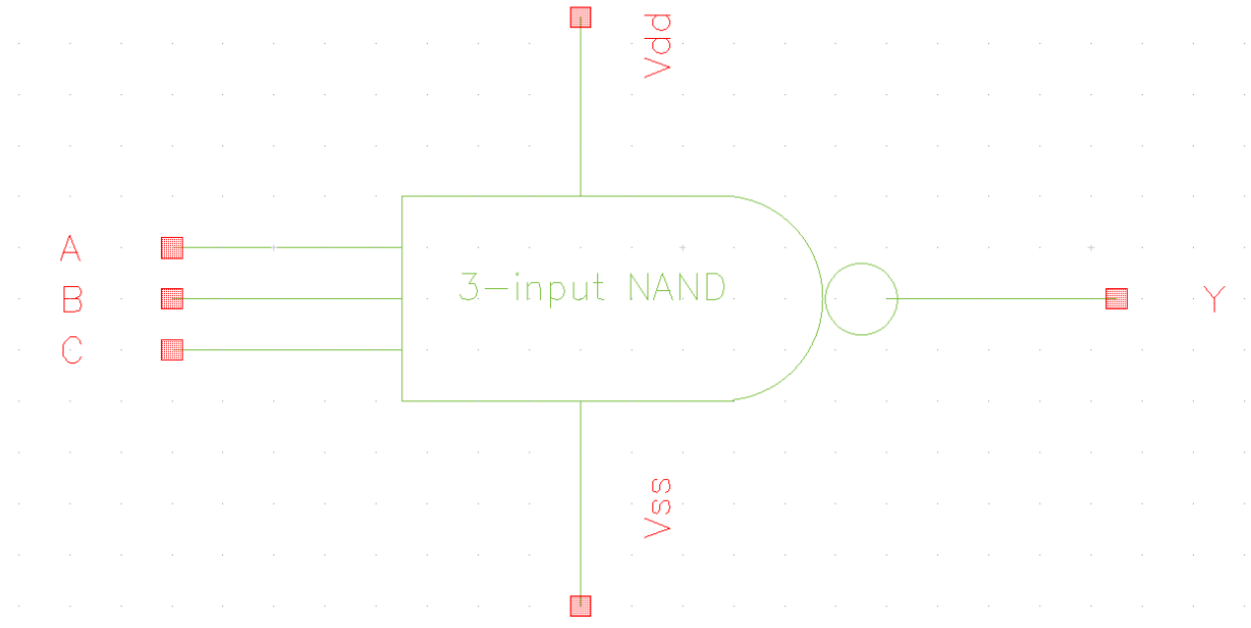


Fig. 7

- CMOS Inverter

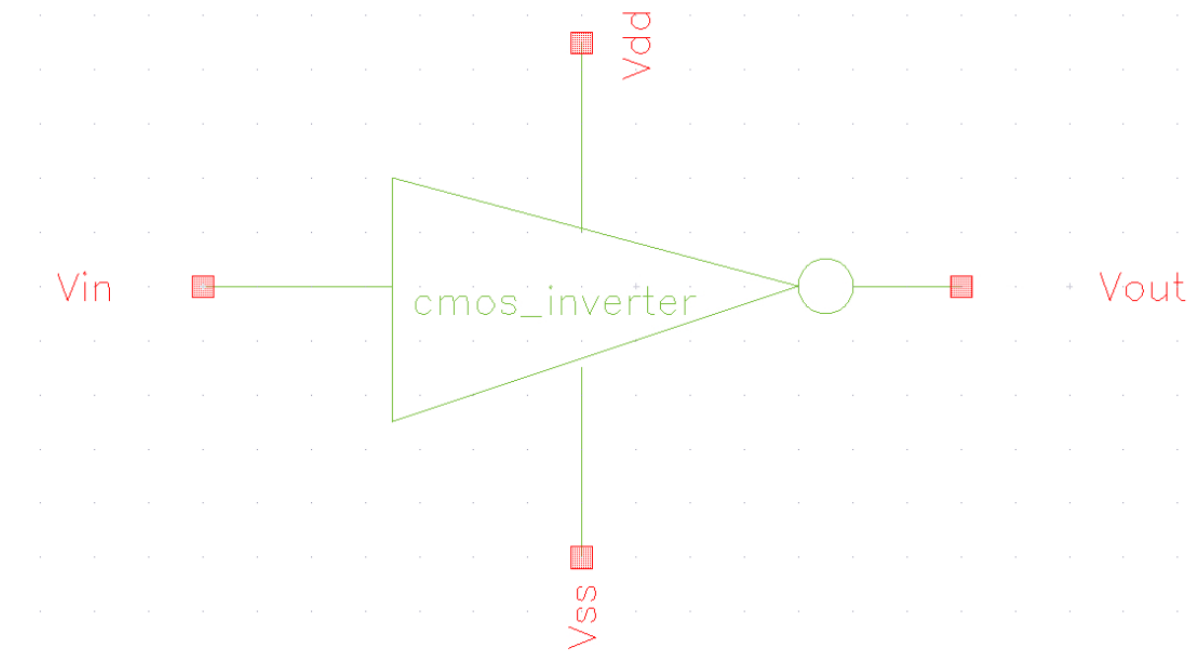


Fig. 8

- Master – slave T Flipflop

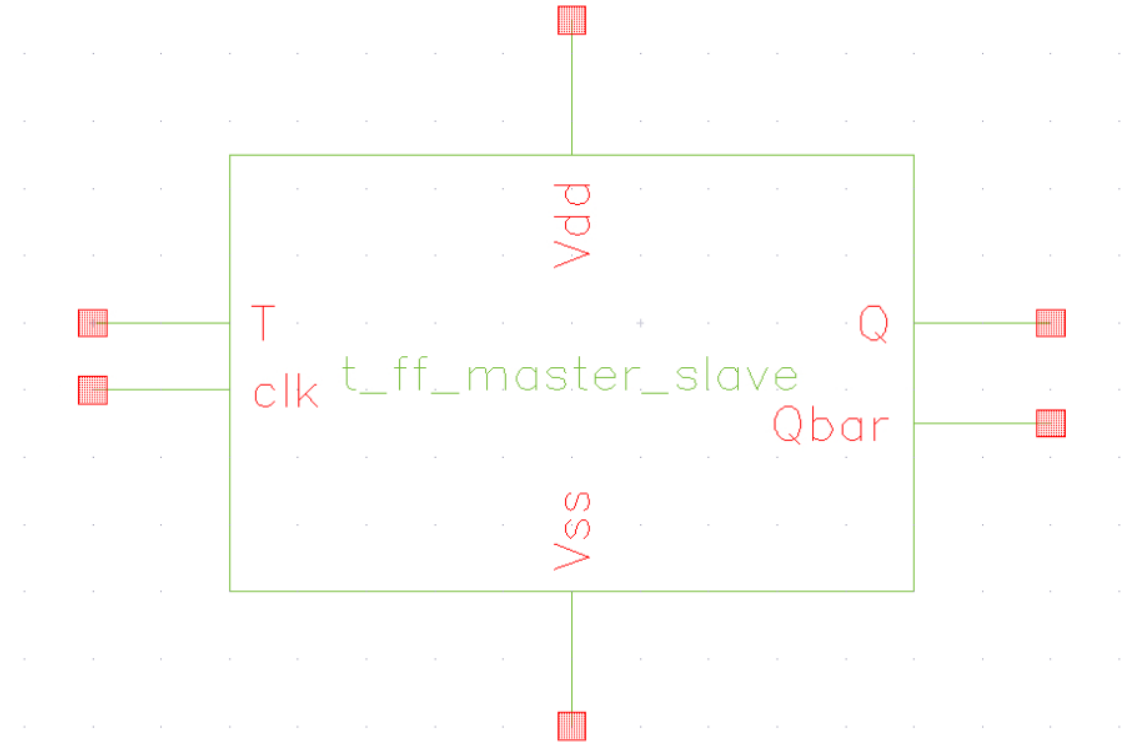


Fig. 9

3.3 TESTBENCH

- Test Bench of 2-bit asynchronous down counter

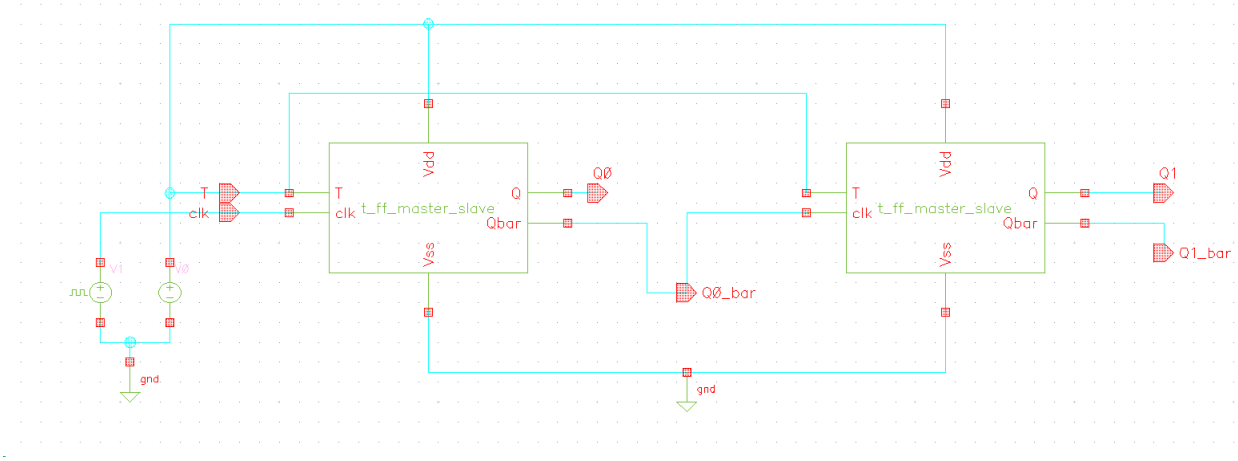


Fig. 10

3.4 ADE L window

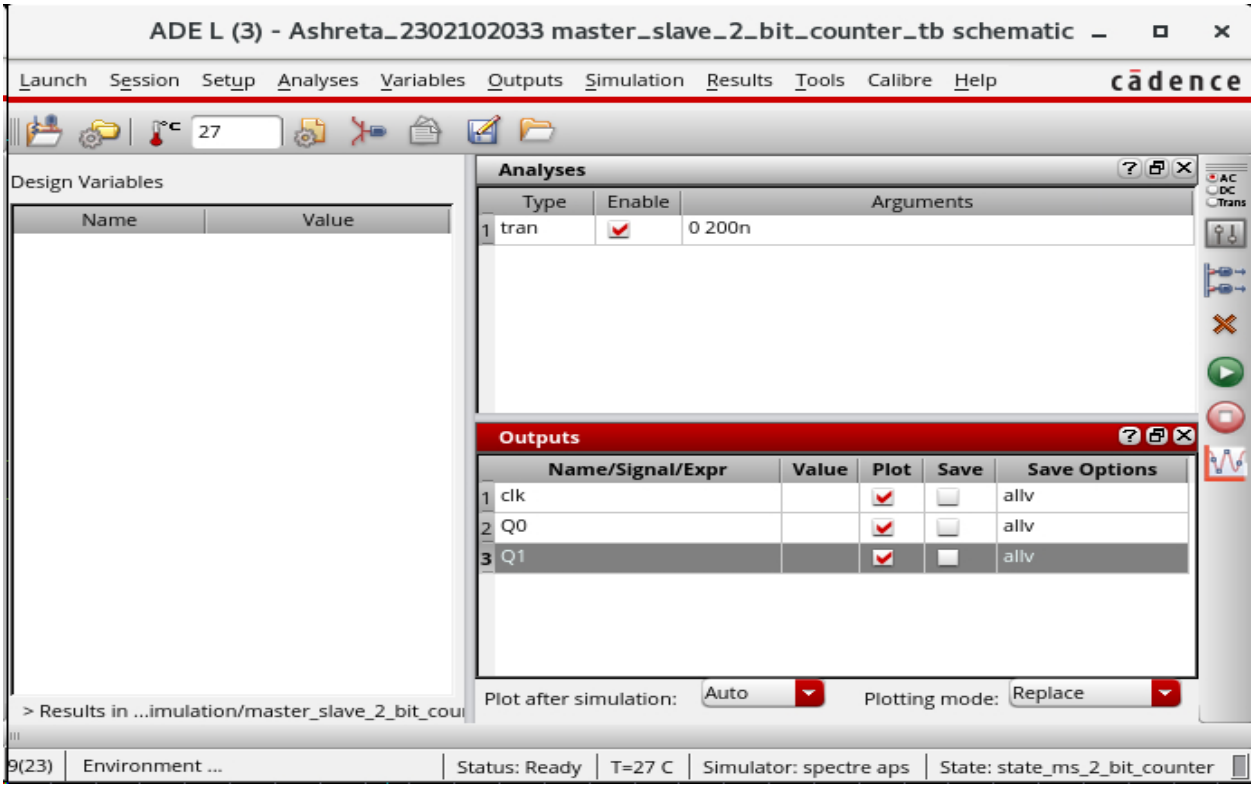


Fig. 11

3.5 Transient analysis waveform

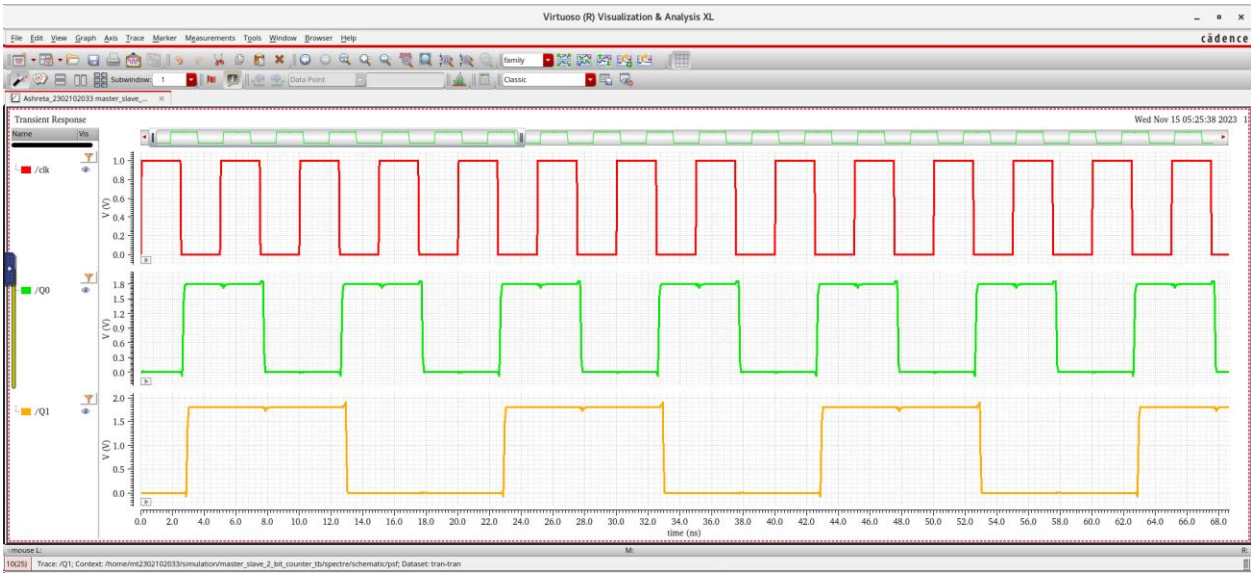


Fig. 12

Result: In above waveform we are able to see that it is negative edge triggered down counter.

4. CADENCE – LAYOUT

4.1 LAYOUT

- 2 – input NAND :

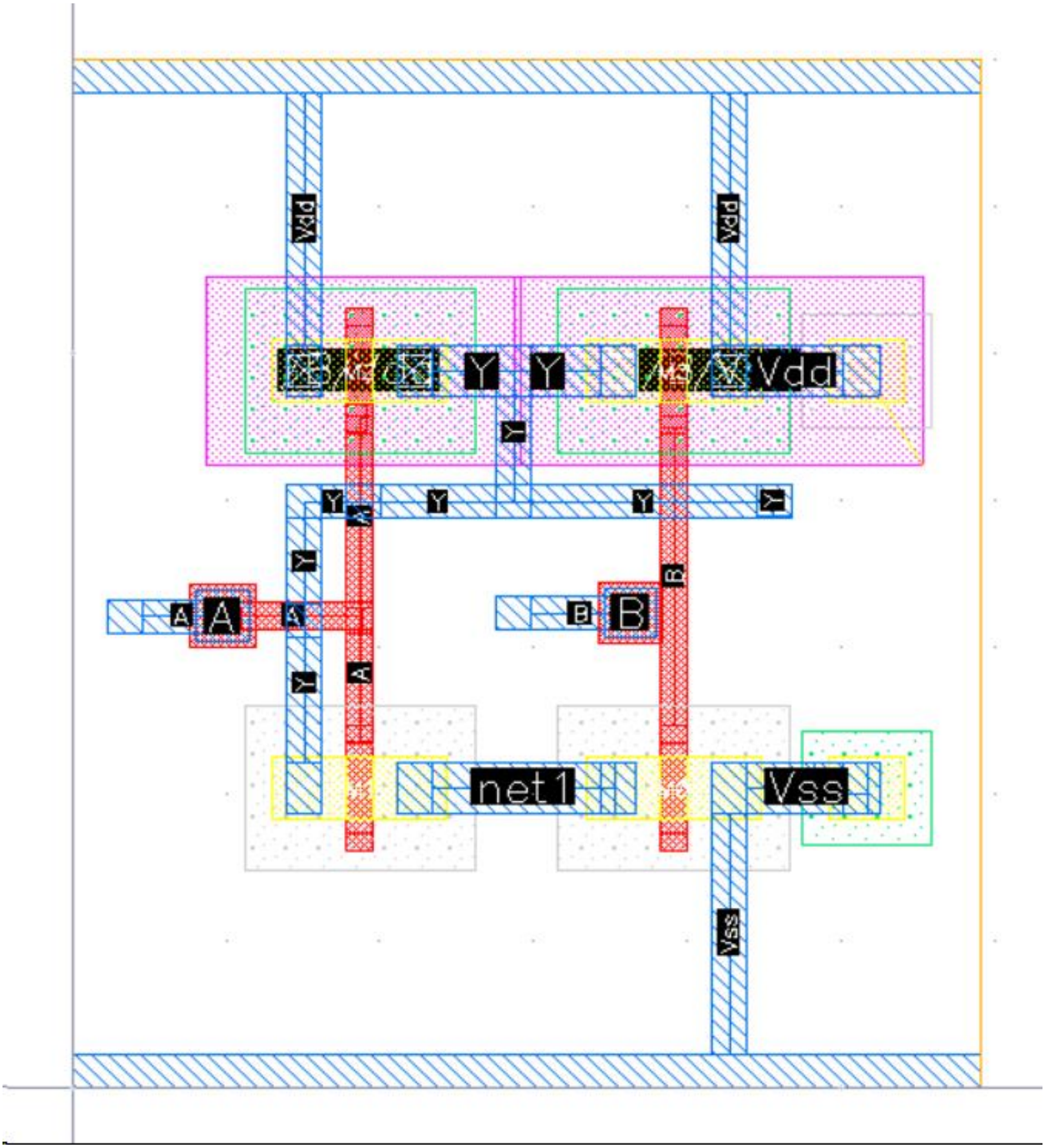


Fig. 13

- 3-Input NAND :

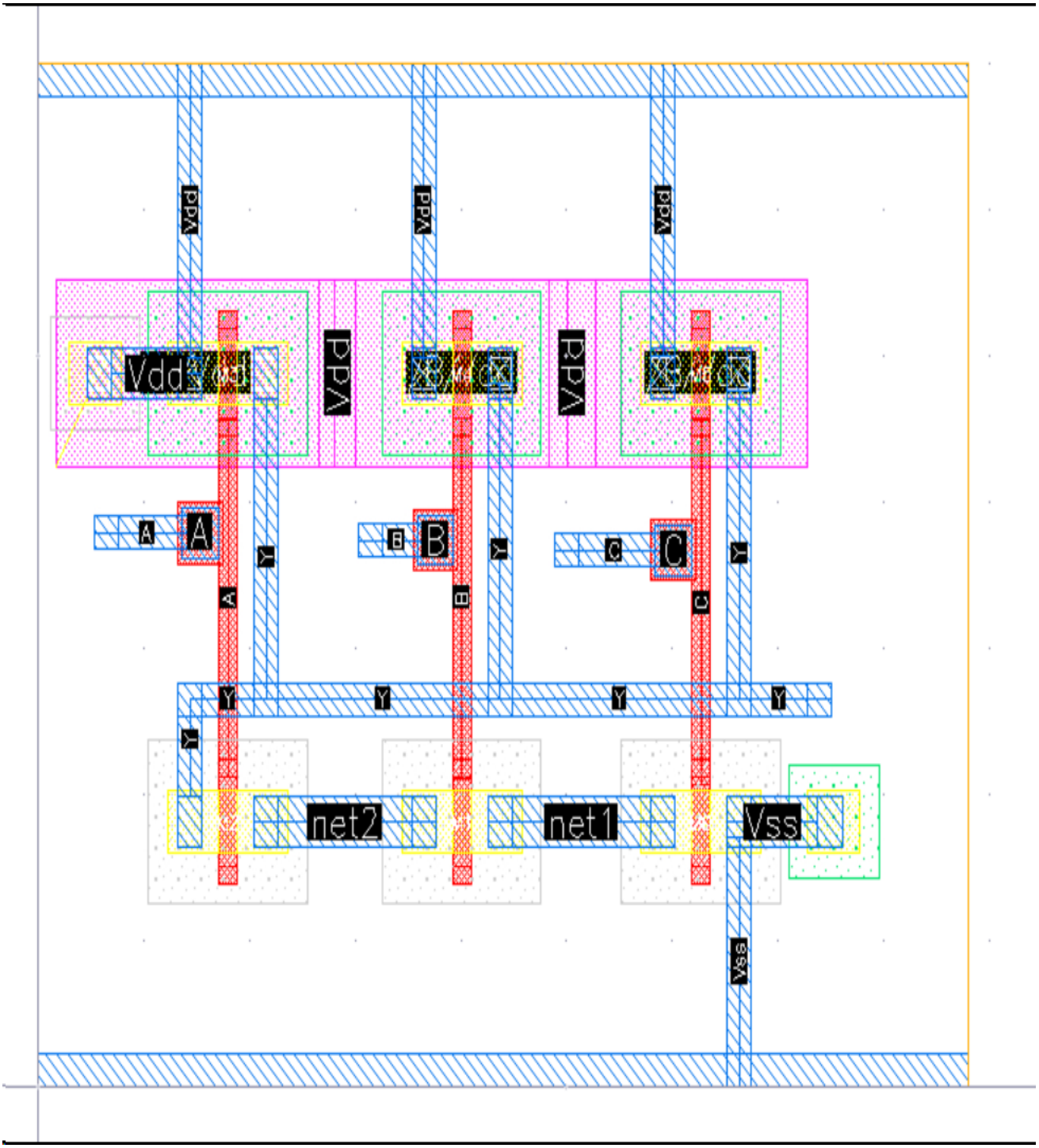


Fig. 14

- CMOS Inverter

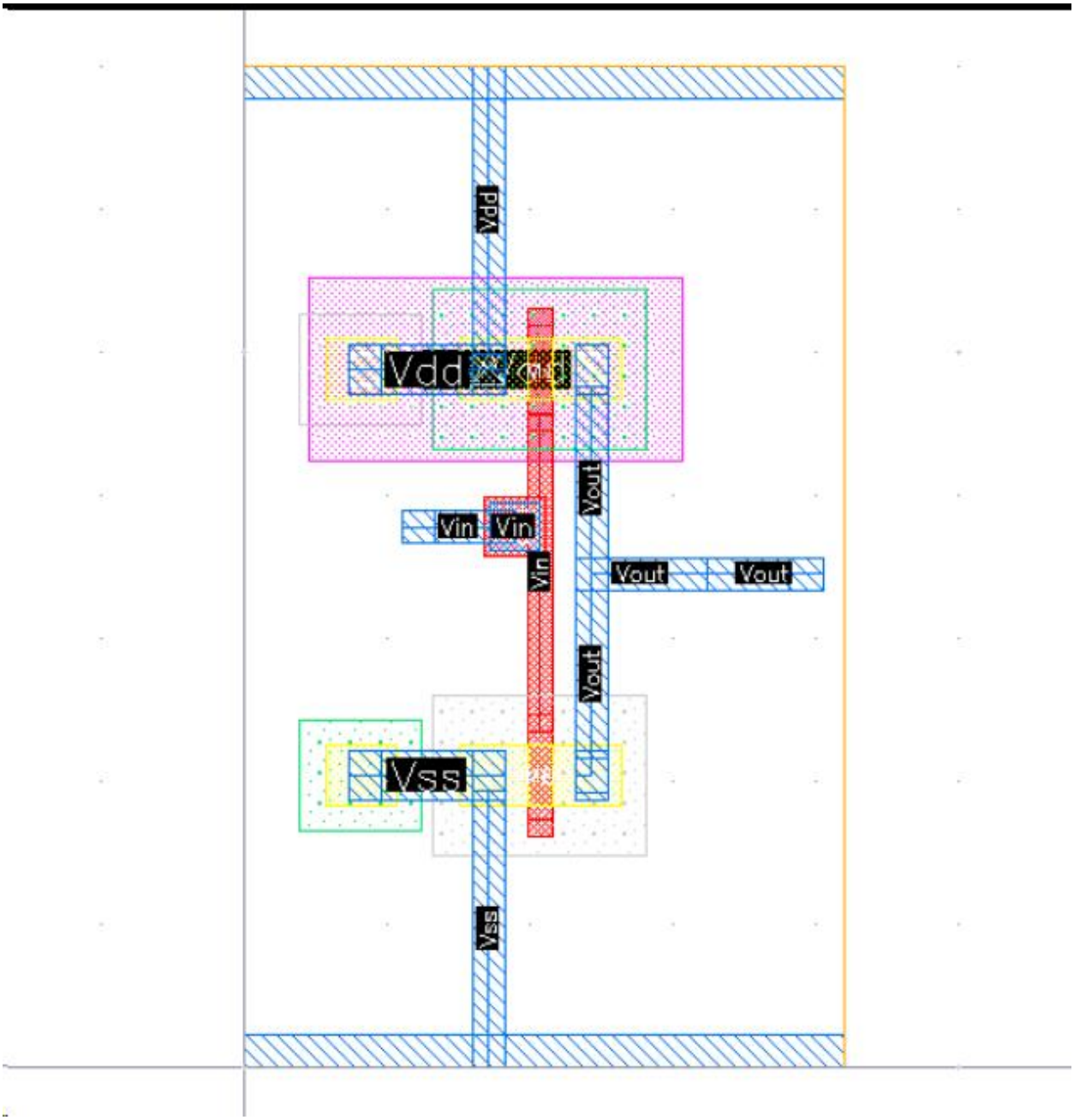


Fig. 15

- **Master – slave T Flipflop**

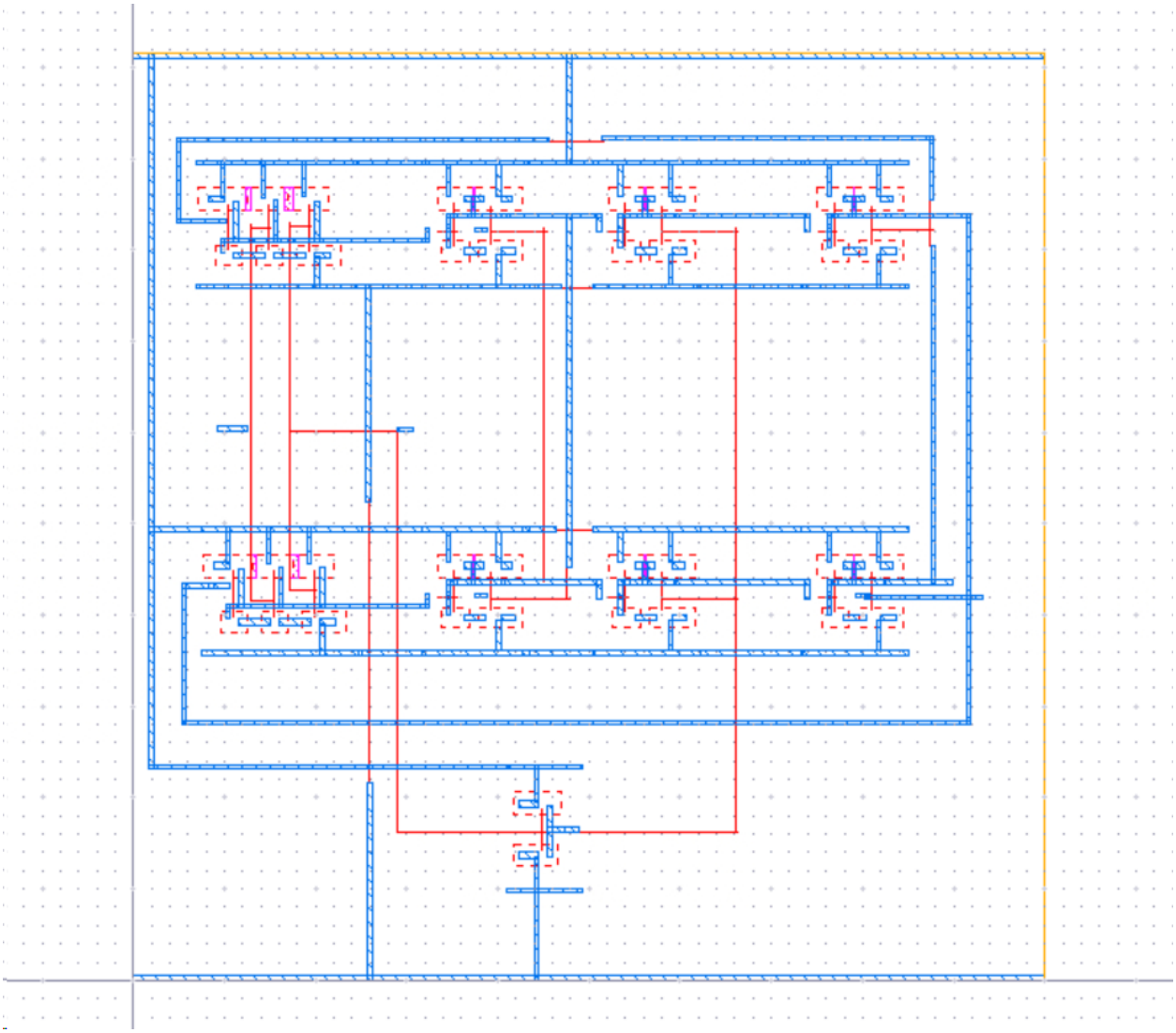


Fig. 16

- 2 – bit asynchronous down counter

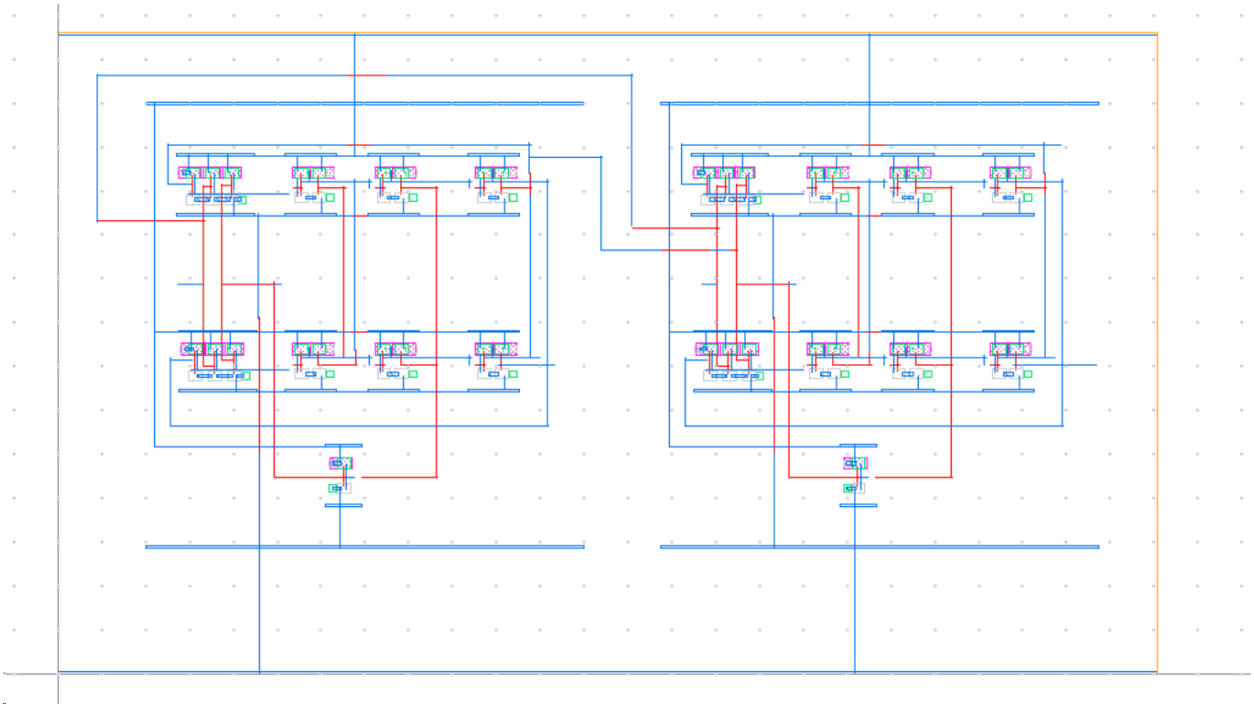


Fig. 17

4.2 DESIGN VERIFICATION

a) Design Rule Check (DRC) using nmDRC tool in Calibre software

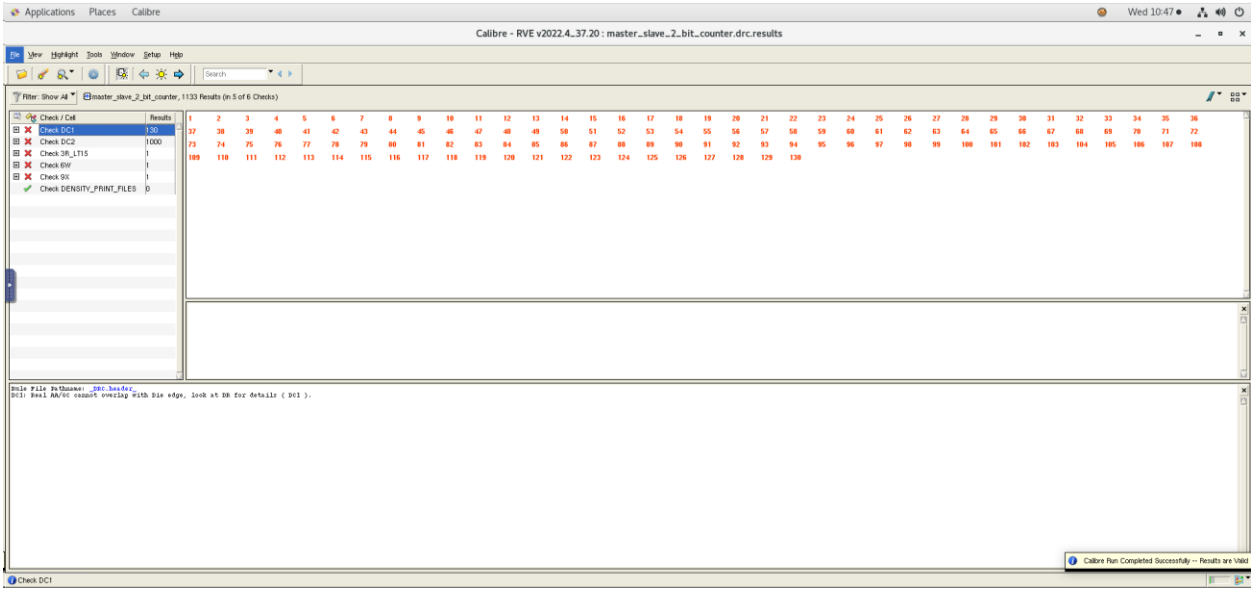


Fig. 18

b) Layout Vs Schematic (LVS) using nmLVS tool in Calibre software

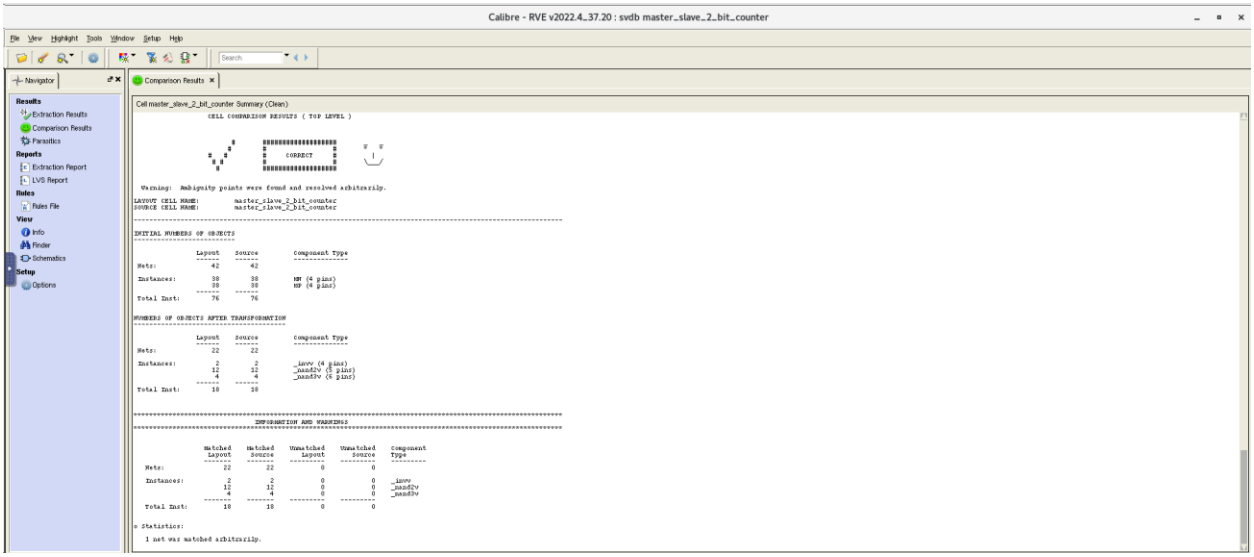


Fig. 19

c) Parasitic extraction (PEX) using Calibre software

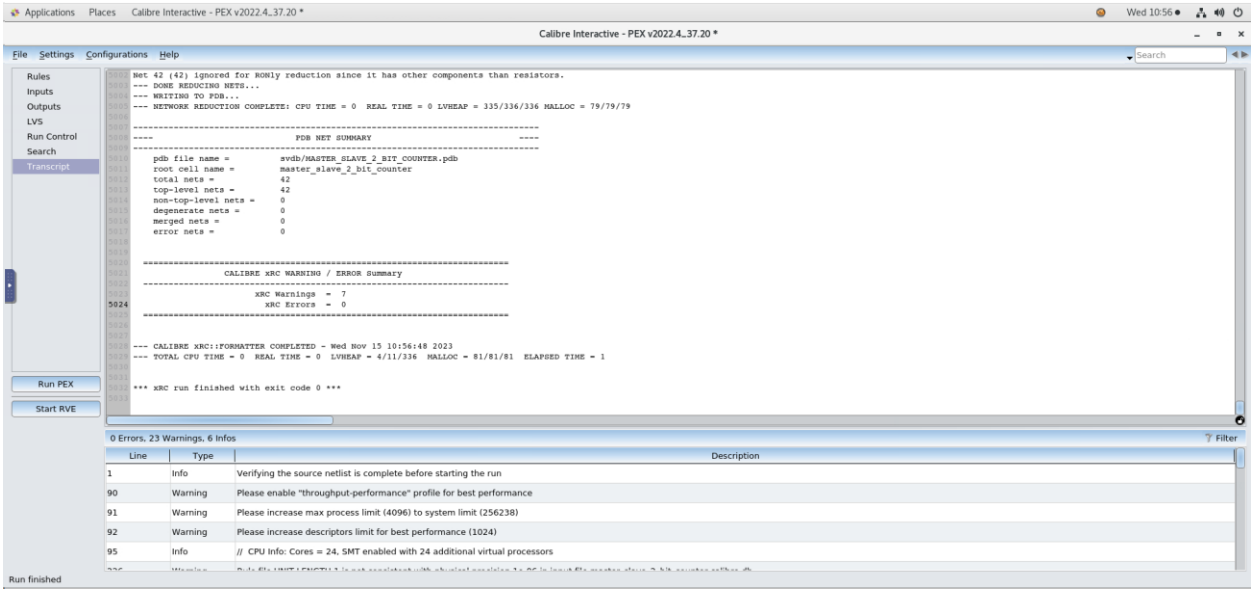


Fig. 20

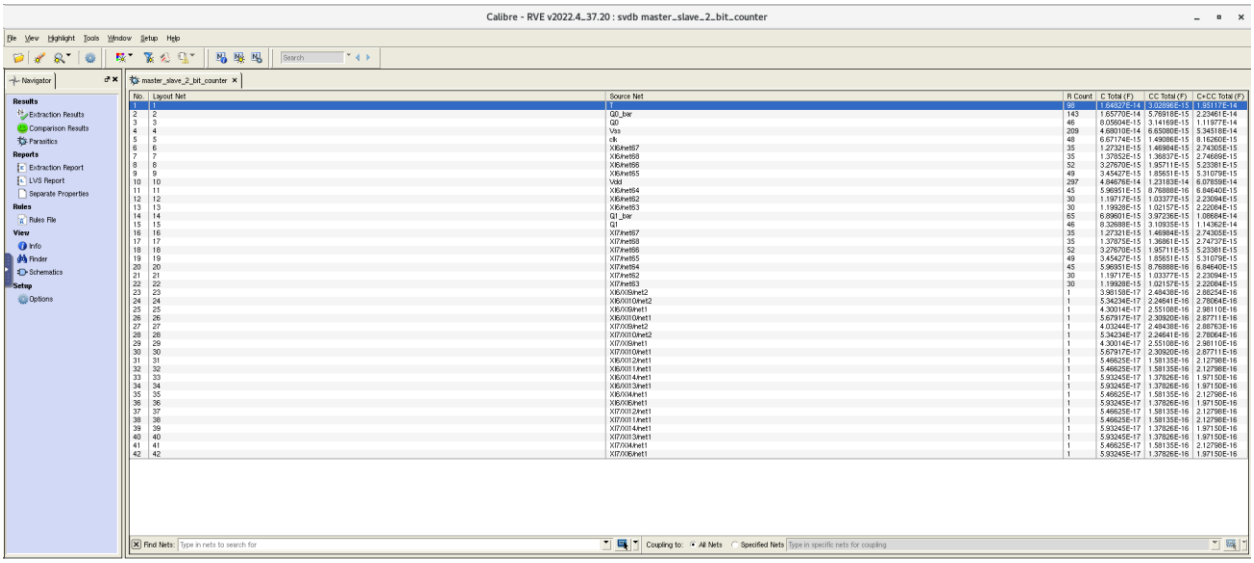

Calibre - RVE v2022.4_37.20 : svdb master_slave_2_bit_counter
File View Highlight Tools Window Setup Help
Navigator
master_slave_2_bit_counter
Results
Extraction Results
Comparison Results
Parasitics
Reports
Extraction Report
LVS Report
Separate Properties
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
No. Layout Net Source Net R Count C Total (F) CC Total (F) C+CC Total (F)
1 1 1 53 1.68327E-14 3.10366E-15 1.99363E-14
2 2 Q0_bar 143 1.65770E-14 5.76918E-15 2.23461E-14
3 3 Q0 46 0.05604E-15 3.14169E-15 1.11977E-14
4 4 Vss 209 4.69810E-14 6.63080E-15 5.34518E-14
5 5 clk 48 6.67174E-15 1.49086E-15 8.16260E-15
6 6 XI6/net87 35 1.27321E-15 1.46984E-15 2.74305E-15
7 7 XI6/net88 35 1.37852E-15 1.36837E-15 2.74689E-15
8 8 XI6/net86 52 3.27670E-15 1.97511E-15 5.23381E-15
9 9 XI6/net85 49 3.45427E-15 1.85631E-15 5.31059E-15
10 10 Vdd 297 4.84676E-14 1.23183E-14 6.07859E-14
11 11 XI6/net84 45 5.96951E-15 8.76888E-16 6.84640E-15
12 12 XI6/net82 30 1.19717E-15 1.03377E-15 2.23094E-15
13 13 XI6/net83 30 1.19928E-15 1.02157E-15 2.22084E-15
14 14 Q1_bar 65 6.89801E-15 3.97236E-15 1.08684E-14
15 15 Q1 46 8.32688E-15 3.10935E-15 1.14362E-14
16 16 XI7/net87 35 1.27321E-15 1.46984E-15 2.74305E-15
17 17 XI7/net88 35 1.37875E-15 1.36861E-15 2.74737E-15
18 18 XI7/net86 52 3.27670E-15 1.97511E-15 5.23381E-15
19 19 XI7/net85 49 3.45427E-15 1.85631E-15 5.31059E-15
20 20 XI7/net84 45 5.96951E-15 8.76888E-16 6.84640E-15
21 21 XI7/net82 30 1.19717E-15 1.03377E-15 2.23094E-15
22 22 XI7/net83 30 1.19928E-15 1.02157E-15 2.22084E-15
23 23 XI6/XI0/net2 1 3.98158E-17 2.49439E-16 2.88254E-16
24 24 XI6/XI10/net32 1 5.34234E-17 2.24641E-16 2.78084E-16
25 25 XI6/XI09/net1 1 4.30014E-17 2.55108E-16 2.98110E-16
26 26 XI6/XI10/net1 1 5.67917E-17 2.30920E-16 2.87711E-16
27 27 XI7/XI8/net2 1 4.03244E-17 2.49439E-16 2.89763E-16
28 28 XI7/XI10/net2 1 5.34234E-17 2.24641E-16 2.78084E-16
29 29 XI7/XI8/net1 1 4.30014E-17 2.55108E-16 2.98110E-16
30 30 XI7/XI10/net1 1 5.67917E-17 2.30920E-16 2.87711E-16
31 31 XI6/XI12/net1 1 5.46625E-17 1.58135E-16 2.12798E-16
32 32 XI6/XI11/net1 1 5.46625E-17 1.58135E-16 2.12798E-16
33 33 XI6/XI14/net1 1 5.93245E-17 1.37826E-16 1.97150E-16
34 34 XI6/XI13/net1 1 5.93245E-17 1.37826E-16 1.97150E-16
35 35 XI6/XI04/net1 1 5.46625E-17 1.58135E-16 2.12798E-16
36 36 XI6/XI05/net1 1 5.93245E-17 1.37826E-16 1.97150E-16
37 37 XI7/XI12/net1 1 5.46625E-17 1.58135E-16 2.12798E-16
38 38 XI7/XI11/net1 1 5.46625E-17 1.58135E-16 2.12798E-16
39 39 XI7/XI14/net1 1 5.93245E-17 1.37826E-16 1.97150E-16
40 40 XI7/XI13/net1 1 5.93245E-17 1.37826E-16 1.97150E-16
41 41 XI7/XI04/net1 1 5.46625E-17 1.58135E-16 2.12798E-16
42 42 XI7/XI05/net1 1 5.93245E-17 1.37826E-16 1.97150E-16
Find Nets:
Coupling to: All Nets Specified Nets

Fig. 21

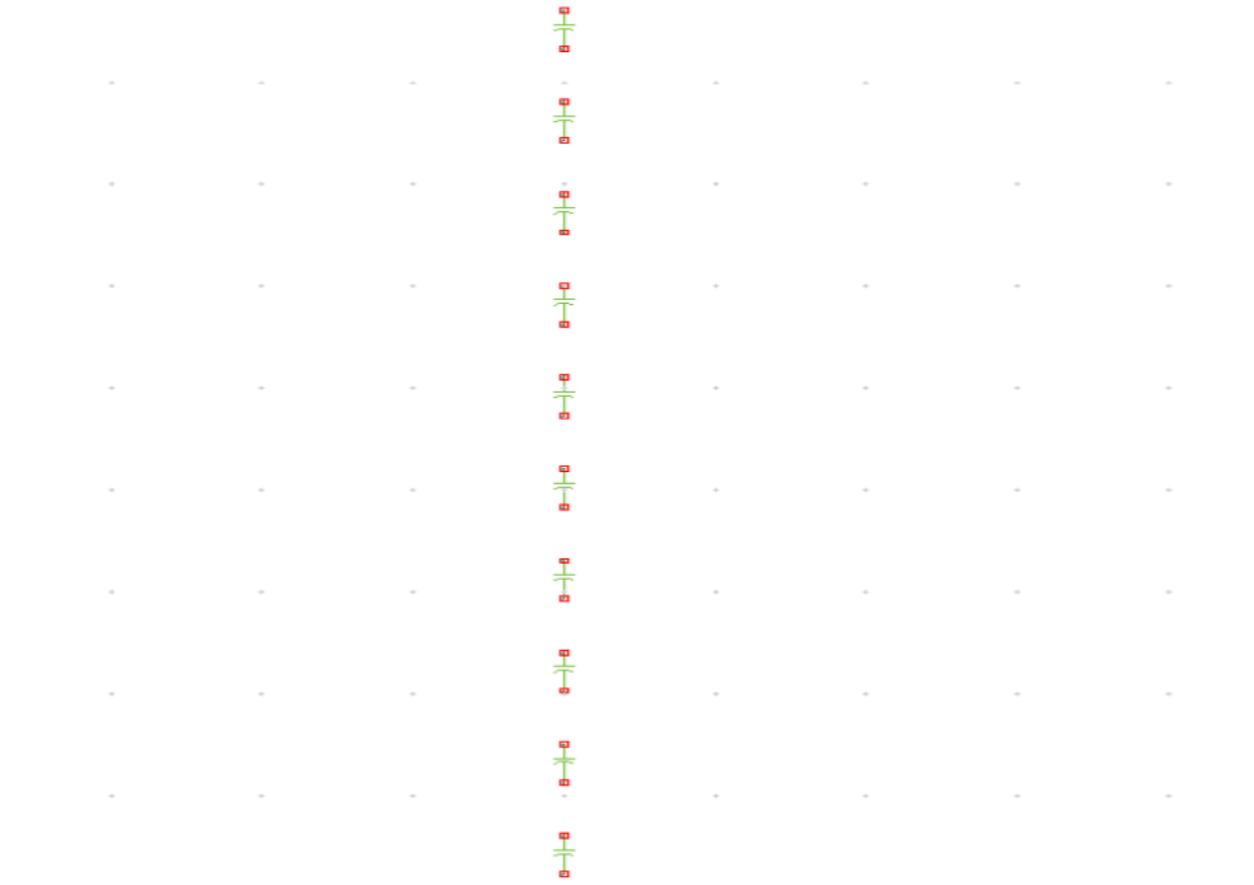


Fig. 22

4.3 POST – LAYOUT SIMULATION

Fig. 23

5. CONCLUSION

In this report, we have implemented 2 bit asynchronous down counter that is capable to count 4 different states.