TCD is Tessent core description file , it is a new format
When you read the memlib files into the Tessent tool with Tessent shell flow the memlib files are automatically translated into the TCD files.
So we need not to do anything specific to generate the TCD Files.

The main important prerequisite is memlibs which would be generated by memory compiler tool.
This is required when we are going to insert MBIST to test all the memories for which memlibs are present.
High performance 3rd party IP with embedded memories will instead sometimes provide a Shared Memory Bus for MBIST testing.Additional TCD files must be created when using a shared memory bus. One cluster memory
Cluster memory TCD file defines the shared memory bus interface and its mapping to the logical memories. And
a logical memory TCD file for each logical memory defines the logical to physical memory
instance mappings.

There is one semi-automated flow which you need to consider while using the shared bus interface.
This is necessary for creating the Cluster TCD and Logical TCD.
First, if the IP provides an MBIF (MBIST Information File), which is a text file format describing the interface and its mapping to the logical memories, the cluster
memory TCD and stubs for the logical memory TCDs can be automatically created using a utility
provided by Tessent called memlibGenerate.

Logical memories Stubs would be created since the IP provider does not know how the logical memories
would be implemented as physical memories.

There is another flow which is caaed automated shared bus learning flow .
This is used to create the final logical memory TCDs with logical to physical mappping .
It does by reading the cluster TCD , logical memory TCD Stubs , physical memory TCDs and the design to trace the connections
between interface and physical memory instrances .

Library Requirements
Three memory library files are required:
Memory Cluster Tessent Core Description

Associated with each Shared Bus memory cluster module

Describes Shared Bus interface pins

Lists all logical memories contained within the Shared Bus memory cluster module

Describes pin mappings between logical memories and the Shared Bus interface

Logical Memory Tessent Core Description

Associated with each logical memory in the Shared Bus memory cluster module

Created or modified by the user based on physical memories used

References library files of individual physical memories making up the logical memory

Physical Memory Tessent Core Description

Associated with each physical memory

Used in the standard Tessent MemoryBIST flow

Does not need modifications if generated by a memory compiler

Guideline for Memory grouping

Tessent tool will automatically identify the Non excluded memories (which you dont want to test) , it will
create a default mbist architecture for the core/chip and the information is written into file called DefaultMemorybist_.dft_spec file

This file is a configuration file which included the number of mbist controllers required and which memory instances are
tested in parallel vs serial.
You can manually edit this file based on your discreation how the memories need to be tested.

RAMs and ROMS cant be tested by the same controller
MBIST Controller and the memoires it tests much be clocked synchronously therefore memories
in different clock domains require difference mbist controllers .
RAMs tester through a shared memory bus have their own mbist controller.

Each MBIST Controller implements steps , A step is a group of memory instances tested in parallel
which each step is serialized.