```
read_file inputs/dig_top.v -format verilog
 set current_design dig_top
 link
 set_scan_configuration -style multiplexed_flip_flop
set_dft_configuration -clock_controller enable

create_port -dir in ATE_CLKIN
create_port -dir in pll_bypass
create_port -dir in pll_reset
create_port -dir in occ_testmode
create_port -dir in SCAN_EN
set_dft_signal -view exist -type Oscillator -port clkin -timing [list 40 60]
set_dft_signal -view exist -type scanclock -port clkin -timing [list 40 60]
set_dft_signal -view exist -type Oscillator -port clk_500khz -timing [list 40 60]
set_dft_signal -view exist -type scanclock -port clk_500khz -timing [list 40 60]
set_dft_signal -view spec -type ScanClock -port ATE_CLKIN
set_dft_signal -view spec -type pll_bypass -port pll_bypass
set_dft_signal -view spec -type pll_reset -port pll_reset
set_dft_signal -view spec -type testmode -port occ_testmode
set_dft_signal -view spec -type ScanEnable -port SCAN_EN

set_scan_configuration -chain 10 -clock_mix mix_clocks
set_dft_clock_controller -cell_name OCC_1 -design snps_clk_mux -cycles_per_clock 2 -test_mode
occ_testmode -chain_count 1 -pllclock clkin -ateclock ATE_CLKIN
set_dft_clock_controller -cell_name OCC_2 -design snps_clk_mux -cycles_per_clock 2 -test_mode
occ_testmode -chain_count 1 -pllclock clk_500khz -ateclock ATE_CLKIN
 create_test_protocol
dft_drc
preview_dft -show all
insert_dft
write_file -output occ_inserted_netlist.v -format verilog –hierarchy
```

LAB 3A

```
##read_file input/dig_top.v -format verilog
read_file input/dig_top_scan_mapped.v -format verilog
set current_design dig_top
link
set_scan_configuration -style multiplexed_flip_flop
#compile -scan
#write_file -format verilog -hierarchy -output output/dig_top_scan_mapped.v
set_dft_configuration -scan_compression enable
set_dft_signal -view existing_dft -type ScanClock -port  clkin -timing [list 40 60]
set_dft_signal -view existing_dft -type ScanClock -port  clk_500khz -timing [list 40 60]
set_dft_signal -view existing_dft -type Reset -port reset_n -active_state 0
set_dft_signal -view existing_dft -type TestMode -port test_override -active_state 1
create_port COMPRESS_MODE -dir IN
set_dft_signal -view spec -type TestMode -port COMPRESS_MODE -active_state 1

create_port SCAN_EN -dir IN
create_port SCAN_IN1 -dir IN
create_port SCAN_IN2 -dir IN
create_port SCAN_OUT1 -dir OUT
create_port SCAN_OUT2 -dir OUT
set_dft_signal -view spec -type ScanEnable -port SCAN_EN
set_dft_signal -view spec -type ScanDataIn -port SCAN_IN1
set_dft_signal -view spec -type ScanDataIn -port SCAN_IN2
set_dft_signal -view spec -type ScanDataOut -port SCAN_OUT1
set_dft_signal -view spec -type ScanDataOut -port SCAN_OUT2
#The number of ext scan chains/channels to build
set_scan_configuration -chain_count 2
# The number of compressed scan chains to build
set_scan_compression_configuration -chain_count 20
create_test_protocol
```

```
dft_drc

dft_drc -verbose > reports/drc.rpt

preview_dft -test_points all

insert_dft

write_file -format verilog -hierarchy -output output/dig_top_compr.v

write_test_protocol -output output/dig_top_scan.spf -test_mode Internal_scan

write_test_protocol -output output/dig_top_compress.spf -test_mode ScanCompression_mode

report_scan_path -test_mode all > reports/scan_cells_compress.rpt

report_scan_compression_configuration > reports/scan_compress_conf.rpt
```

LAB 3B-

```
read_file input/dig_top_scan_mapped.v -format verilog
set current_design dig_top
link
#set_scan_configuration -style multiplexed_flip_flop
#compile -scan
set_dft_configuration -scan_compression enable
set_dft_signal -view existing_dft -type ScanClock -port  clkin -timing [list 40 60]
set_dft_signal -view existing_dft -type ScanClock -port  clk_500khz -timing [list 40 60]
set_dft_signal -view existing_dft -type Reset -port reset_n -active_state 0
set_dft_signal -view existing_dft -type TestMode -port test_override -active_state 1
create_port COMPRESS_MODE -dir IN
set_dft_signal -view spec -type TestMode -port COMPRESS_MODE -active_state 1
create_port SCAN_EN -dir IN
set_dft_signal -view spec -type ScanEnable -port SCAN_EN

for {set i 1} {$i <= 4} {incr i 1} {
create_port -dir in SCAN_IN[$i]
create_port -dir out SCAN_OUT[$i]
set_dft_signal -view spec -type ScanDataIn -port SCAN_IN[$i] -test_mode all
set_dft_signal -view spec -type ScanDataOut -port SCAN_OUT[$i] -test_mode all
}
#The number of ext scan chains/channels to build
set_scan_configuration -chain_count 4
set_scan_compression_configuration -max_length 300
create_test_protocol
dft_drc
preview_dft
insert_dft
write_file -format verilog -hierarchy -output output/dig_top_compr.v
```

```
write_test_protocol -output output/dig_top_scan.spf -test_mode Internal_scan
write_test_protocol -output output/dig_top_compress.spf -test_mode ScanCompression_mode
report_scan_path -test_mode all > reports/scan_cells_compress.rpt
report_scan_compression_configuration > reports/scan_compress_conf.rpt
report_dft_configuration > reports/dft_conf.rpt
report_scan_configuration > reports/scan_conf.rpt
report_dft_signal > reports/dft_signal.rpt
```

LAB-2

```
read_file inputs/counter.vs -format verilog
 set current_design up_down_counter

 link

 set_scan_configuration -style multiplexed_flip_flop
 compile -scan
 write_file -format verilog -output outputs/compile_scan.v

 set_dft_signal -view existing_dft -type ScanClock -port clk -timing [list 40 60]
 set_dft_signal -view existing_dft -type reset -port reset -active_state 0

create_port -dir in TestMode
 set_dft_signal -view existing_dft -type TestMode -port TestMode -active_state 1

 create_port -dir in SCAN_EN
 set_dft_signal -view spec -type ScanEnable -port SCAN_EN

 create_port -dir in SCAN_IN
 set_dft_signal -view spec -type ScanDataIn -port SCAN_IN


 create_port -dir out SCAN_OUT
 set_dft_signal -view spec -type ScanDataOut -port SCAN_OUT

 set_scan_path chain1 -view spec -scan_data_in SCAN_IN -scan_data_out SCAN_OUT
 set_scan_configuration -chain_count 1
```

```
create_test_protocol
dft_drc -verbose > reports/drc.rpt
dft_drc
# fix the DRC

set_dft_configuration -fix_clock enable
set_dft_signal -view spec -type TestData -port clk
set_dft_signal -view spec -type TestMode -port TestMode -active_state 1
set_autofix_configuration -type clock -control TestMode -test_data clk

set_dft_configuration -fix_reset enable
set_dft_signal -view spec -type TestData -port reset
set_autofix_configuration -type reset -control TestMode -test_data reset

preview_dft
insert_dft

write_file -format verilog -output outputs/scan_inserted.v
write_test_protocol -output outputs/scan_inserted.spf

report_scan_path -chain all > reports/scan_cells.rpt
report_scan_chain > reports/scan_chain.rpt
write_test_model -format ddc -output outputs/scan_inserted.ddc
write_test_model -format ctl -output outputs/scan_inserted.ctl
```

LAB 4D

```
read_file inputs/dig_top_scan_mapped.v -format sverilog

set current_design dig_top
link

set_scan_configuration -style multiplexed_flip_flop
set_dft_signal -view existing_dft -type ScanClock -port  clkin -timing [list 40 60]
set_dft_signal -view existing_dft -type ScanClock -port  clk_500khz -timing [list 40 60]
set_dft_signal -view existing_dft -type Reset -port reset_n -active_state 0
set_dft_signal -view existing_dft -type TestMode -port test_override -active_state 1
set_dft_signal -view existing_dft -type Constant -port test_override -active_state 1

create_port SCAN_EN -dir IN
set_dft_signal -view spec -type ScanEnable -port SCAN_EN

set_scan_configuration -max_length 50
create_test_protocol

dft_drc -verbose

set_dft_signal -view spec -type TestMode -port test_override -active_state 1
set_dft_configuration -fix_clock enable
set_dft_signal -view spec -type TestData -port clkin
set_autofix_configuration -type clock -control test_override -test_data clkin
preview_dft -test_points all
insert_dft

write_file -format verilog -hierarchy -output outputs/dig_top_scan.v
report_scan_path  -chain all > reports/Scan_chains.rpt
report_scan_path  -cell all > reports/Scan_cells.rpt
```