VLSI DESIGN FLOW: RTL TO GDS

Lecture 31
DFT: Basic Concepts

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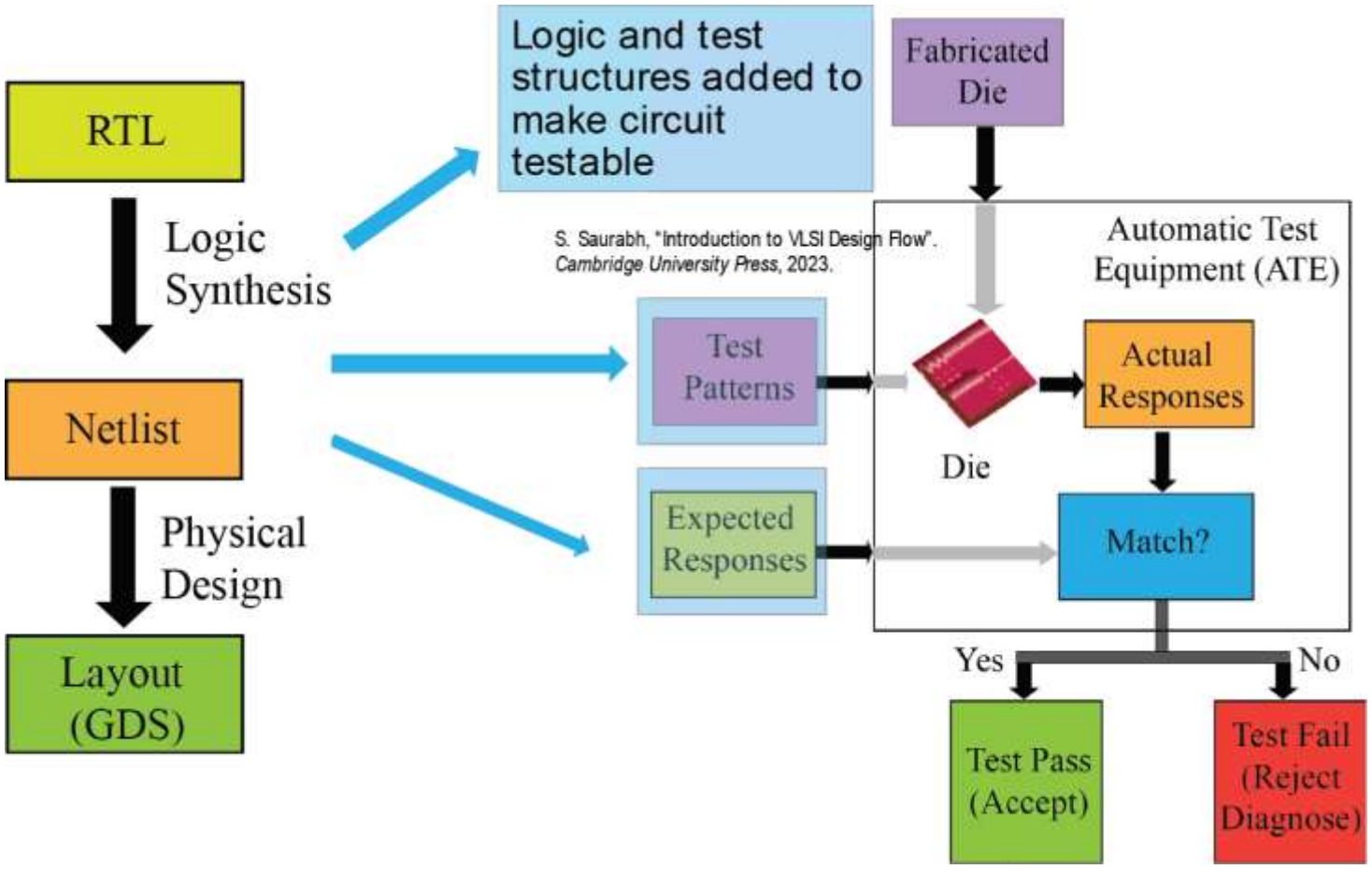
Lecture Plan



- Basic Concepts related to DFT

Structural Testing

Consider a circuit that implements a Boolean function with N inputs.
How to test the fabricated circuit?

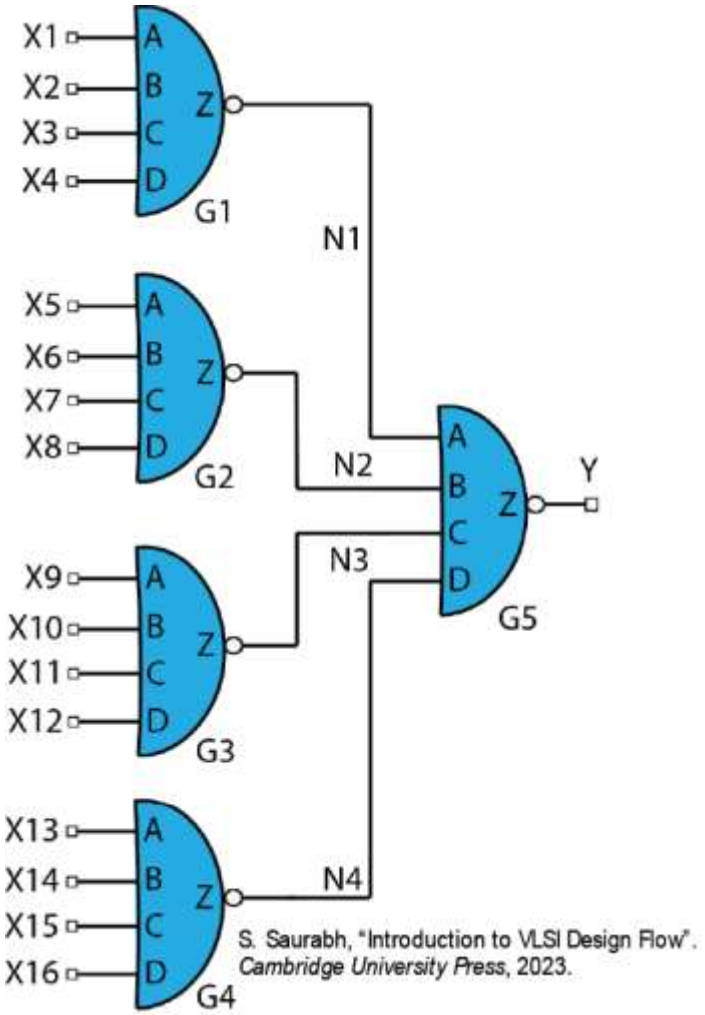
Functional Testing:

- Apply all possible 2^N input combinations and check output
- Becomes infeasible for large N (say 50 or 100)

Structural Testing:

- Test the components that implements a logic function rather than testing the input–output functionality
- The paradigm of structural testing is widely employed
  - ➢ It reduces the number of test patterns required for good test quality

Functional Testing vs. Structural Testing



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Functional Testing

- Will require $2^{16} = 65536$ input combinations

Structural Testing

- Test individual components of the circuit (*G1*, *G2*, *G3*, *G4*, and *G5*)
- Each gate will require $2^4 = 16$ input combinations (total 80)

Assumptions

- Can observe the output pins for all the components
- Can write any value at the input pins of all the components
- There could be a problem in the integration of components (need to tackle that also).

DFT techniques tries to make structural testing more effective by ensuring the above assumptions.

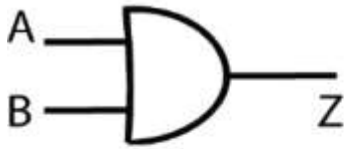
Fault Models

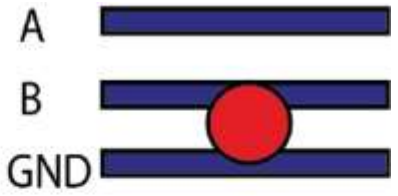
Fault Model

- Represents a defect using a logical or electrical model

Why do we use a Fault Model?

- Allows us to analyze the impact of a defect using logic or circuit analysis techniques
- Allows deriving test patterns algorithmically for detecting a given fault
  - ➢ Quantitative assessment of testing effectiveness using fault coverage
- Transforms the problem of defect detection to the problem of fault detection





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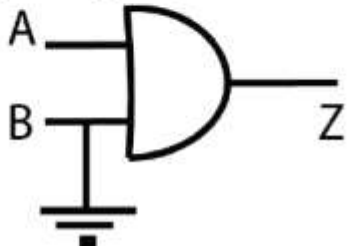


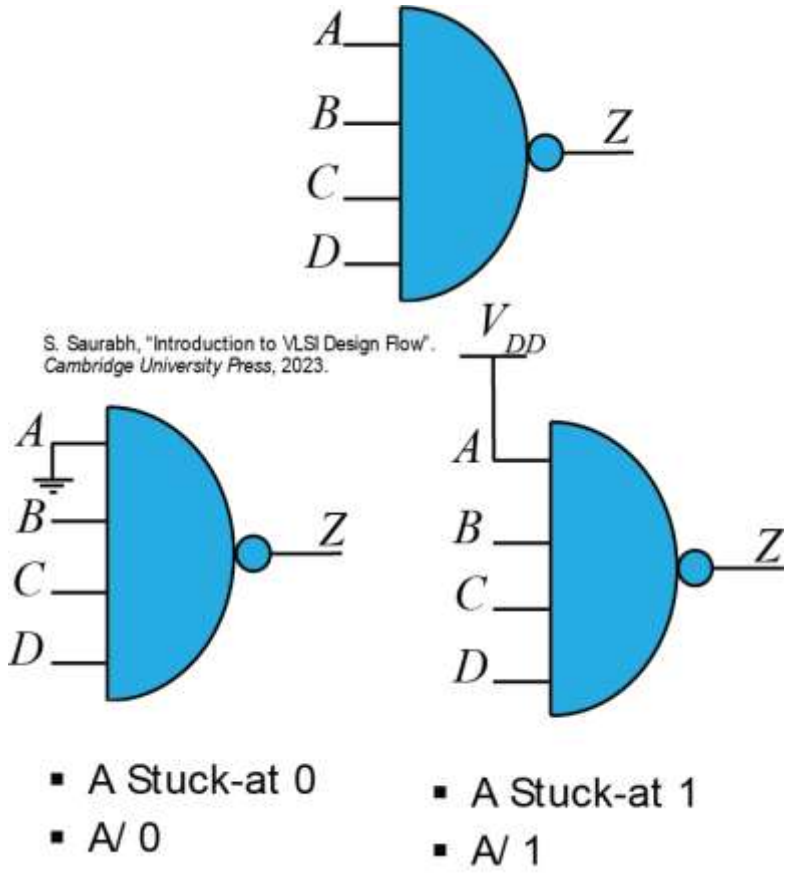
Stuck-at Fault Models

Stuck-at Fault Model

- Assumes that defects cause the signal to be permanently stuck at a constant logic
- Transforms defects to a logical fault model
- Two types:
  - Stuck at logic “0”: stuck-at-0 or SA0 fault
  - Stuck at logic “1”: stuck-at-1 or SA1 fault

Single Stuck-at Fault Model

- Assumes that there is only one fault active at a time
- Reduces the complexity of test pattern generation significantly



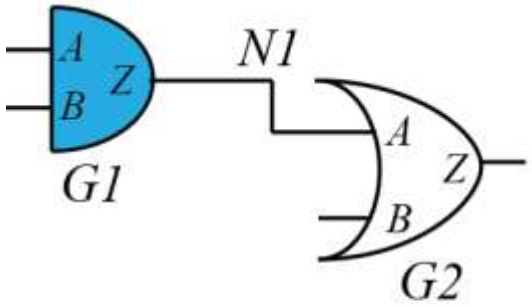
- A Stuck-at 0
- A/ 0

- A Stuck-at 1
- A/ 1

Stuck-at Faults: Fault-site

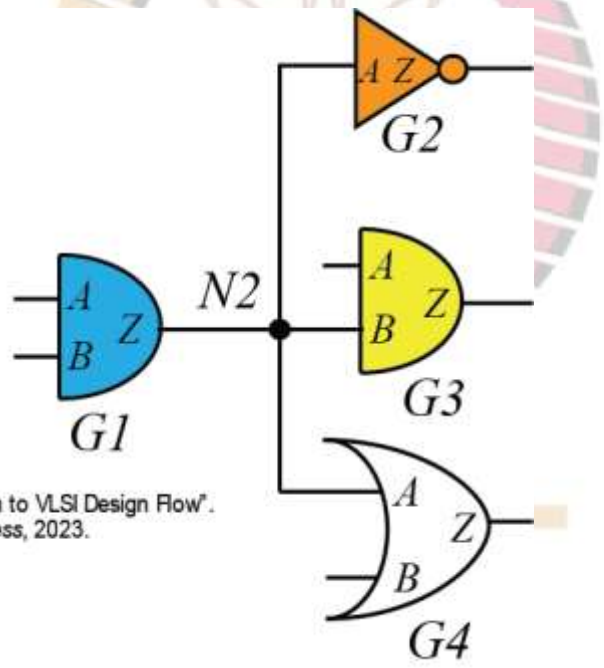
Fault-site:

- The point where a fault exists or we assume it to exist
- Emulate a stuck-at fault by first disconnecting the corresponding signal source.
  - Tie it to the constant logic (either 0 or 1 depending on the fault type)



Fanout-free net:

- **1** fault site



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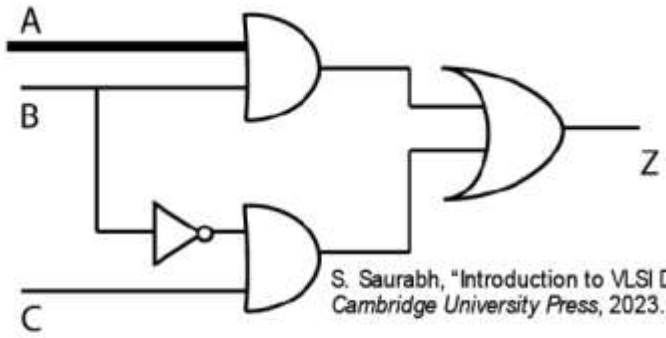
Multi-fanout net (N>1):

- (N+1) fault sites

Possible Stuck-at Faults: Illustration

- Consider the circuit alongside
- How many single stuck-at (0/1) faults are possible in this circuit?



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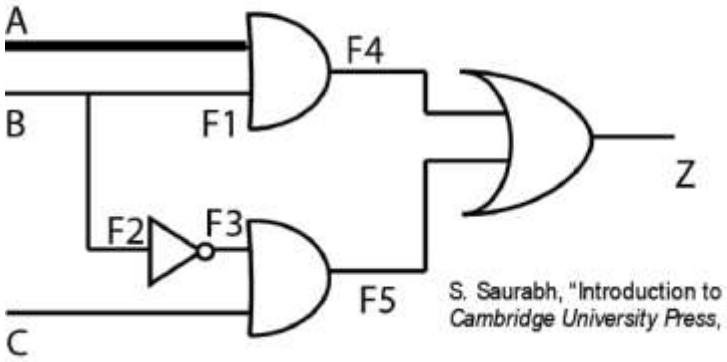

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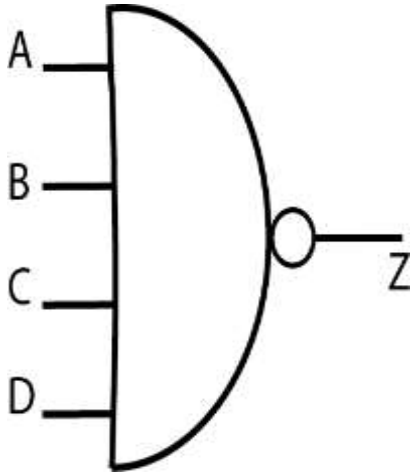
Answer: 18

Detecting a Fault: Test Vectors

Test Vectors

- Any input pattern, or sequence of input patterns, that produces a different output response for a faulty circuit and a fault-free circuit

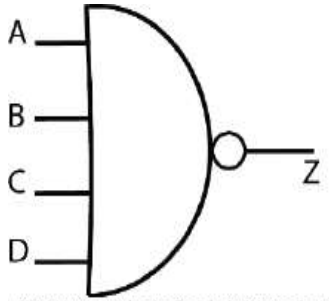


Exhaustive Testing for functionality

- Exponential number of test vectors required (2^N) to test the functionality

Single stuck-at fault model makes the number of fault linear in the number of circuit elements

Design for Testability: Test Vectors



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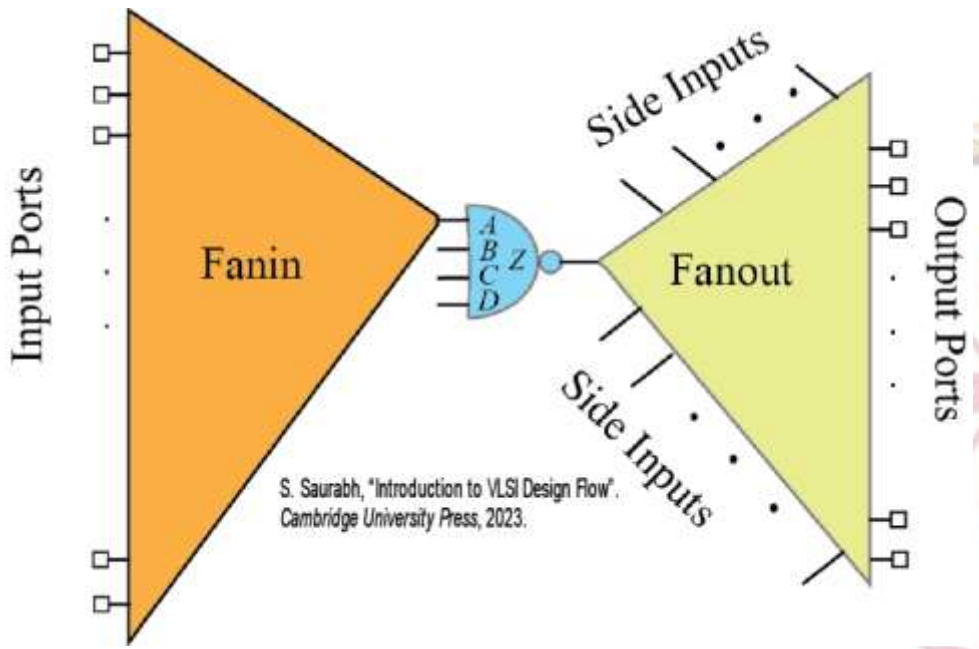
Test Vectors

- 1111 (A/0, B/0, C/0, D/0, Z/1)
- 0111 (A/1, Z/0)
- 1011 (B/1, Z/0)
- 1101 (C/1, Z/0)
- 1110 (D/1, Z/0)

$$Number\ of\ test\ vectors = n + 1$$

					Stuck-at 0					Stuck-at 1				
A	B	C	D	Z	A/0	B/0	C/0	D/0	Z/0	A/1	B/1	C/1	D/1	Z/1
0	0	0	0	1	1	1	1	1	0	1	1	1	1	1
0	0	0	1	1	1	1	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	1	1	0	1	1	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	1	1	1	1	1	1	1	0	0	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1	1
1	0	0	1	1	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	1	1	0	1	0	1	1	1
1	1	0	0	1	1	1	1	1	0	1	1	1	1	1
1	1	0	1	1	1	1	1	1	0	1	1	0	1	1
1	1	1	0	1	1	1	1	1	0	1	1	1	0	1
1	1	1	1	0	1	1	1	1	0	0	0	0	0	1

Combinational Circuit: Controllability and Observability



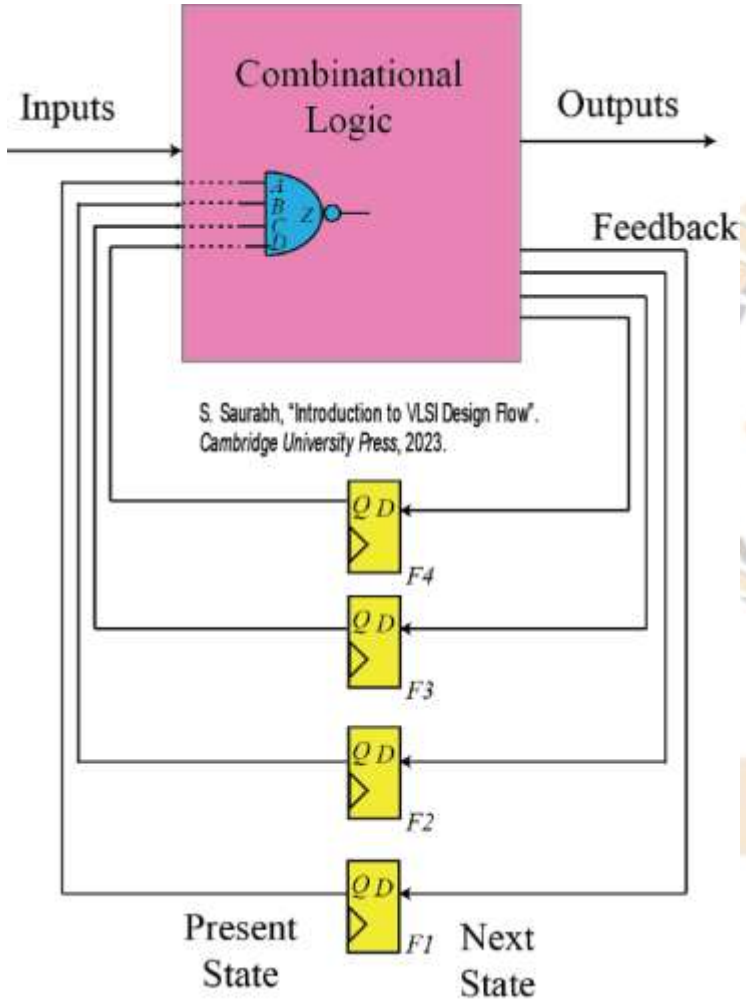
- If the NAND gate was lying too deep in a circuit, it is difficult to apply the required test vectors at the inputs

Controllability: ability to set any desired value (0 or 1) on the internal signals of a circuit by applying an appropriate test-vector to the primary inputs.

- Similarly the output of NAND gate will be difficult to observe at any primary output if the NAND gate is lying too deep in circuit

Observability: ability to examine any internal signal by propagating its value to a primary output by applying appropriate test vector to the primary inputs.

Sequential Circuit: Controllability and Observability



Problem of controllability

- Setting a particular value at any pin in a sequential circuit is more difficult
  - Several cycles may be required to write a particular value
  - State traversal required
  - Finding such a test sequence is time consuming by sequential ATPG tool

Problem of observability

- Similar difficulty in examining the value at a particular pin in the sequential circuit (requires state traversal)

References

- M. Bushnell and V. Agrawal, “Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits”, *Springer Science & Business Media*, 2004.
- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.