# Verilog Gate-Level Netlists and SDC

1. Is the netlist “vorca.v” hierarchical or flat? If hierarchical, how many hierarchical modules are there in the netlist, and what are they called?

2. How many flip-flops are in the netlist? How many of these flip-flops are connected to the clock port “clk” and how many are not?

3. Draw a schematic of the fanout cone of the flip-flop “f32_mux_1_data_reg_5_”. How many endpoints are there in this fanout cone? What types of endpoints are they?

4. Take one of the endpoints of the fanout cone above and trace its entire fan-in cone. How many startpoints are in this fan-in cone? List all the startpoints, and indicate what type of startpoint they are. Are any startpoints input ports?

5. There is a three-bit input bus called `i_hb_sup”. Trace the fanout cone of bit [1] of this bus and list all endpoints. Submit a schematic of the fanout cone.

6. The clock pins of many flip-flops are not connected to the “clk” port. Where does the clock to these flip-flops come from?

7. The RAK library does not have an integrated clock gating cell. The vorca netlist, however, contains several instances of a clock gater, “ICG”. Create a netlist for ICG with instantiations of actual standard cells and append it to the vorca netlist.

8. Write an SDC for vorca with clock definitions and with input and output delays set at half the clock period. Parameterize the clock period in the SDC, and set its value such that the clock frequency is 1 GHz.