VLSI DESIGN FLOW: RTL TO GDS

Lecture 32
Scan Design Flow

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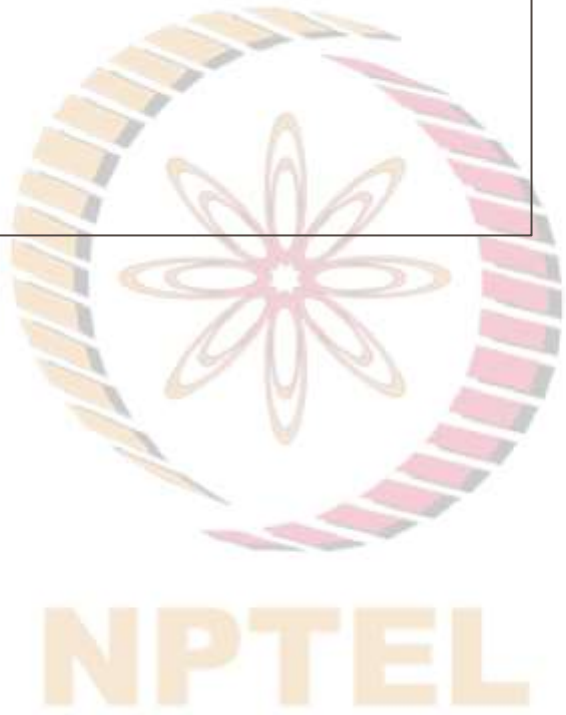
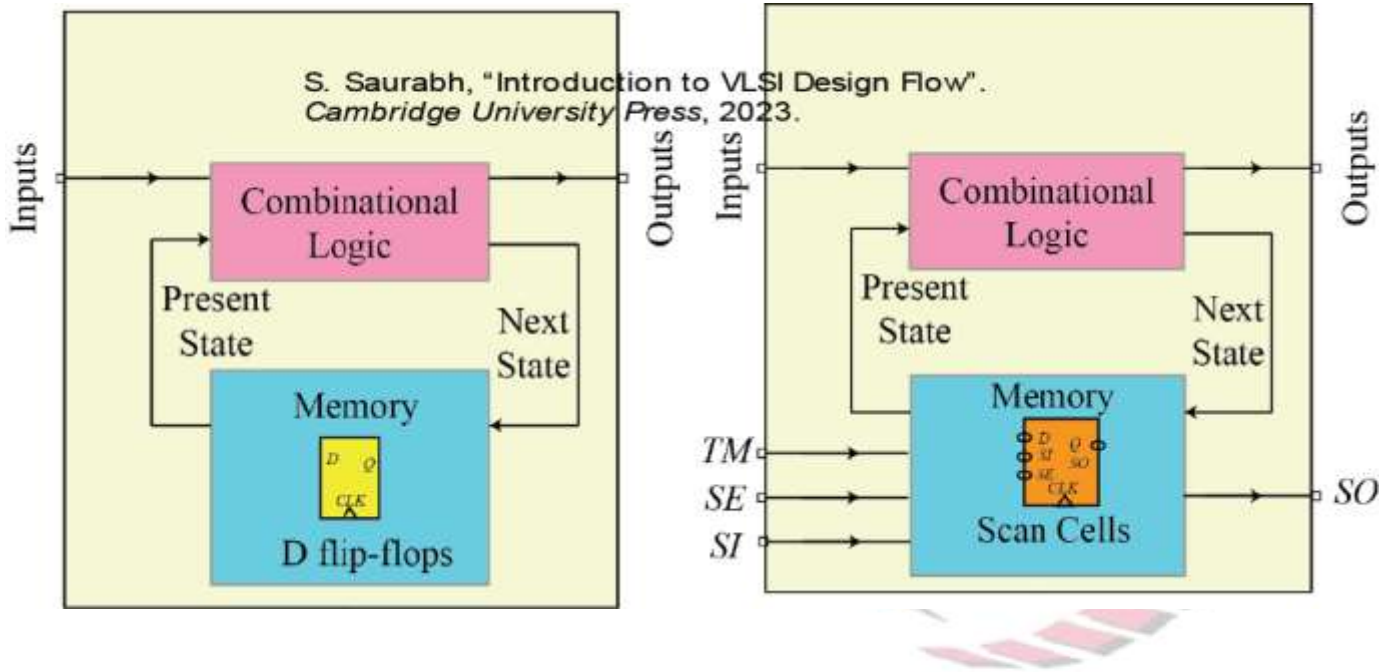
Lecture Plan

Scan Design Flow

- Design Modifications
- Mechanism of Testing
- Tasks



Scan Design Flow: Design Modifications

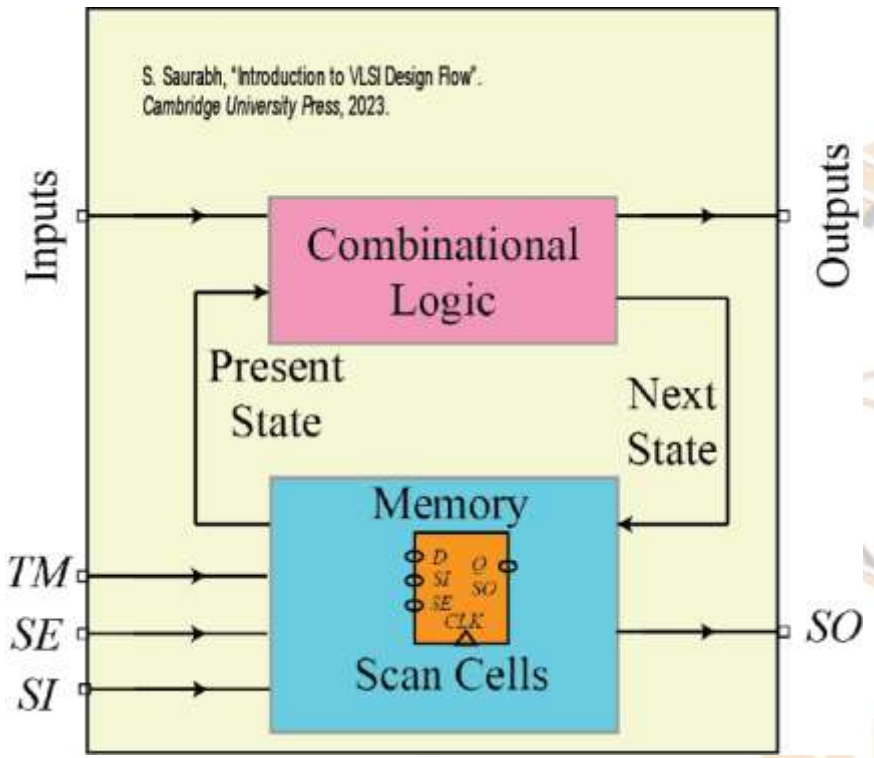


- Extra primary ports added
  - TM (Test Mode)
  - SE (Scan Enable)
  - SI (Scan In)
  - SO (Scan Out)
- D flip-flops replaced with another memory elements (**scan cells**)
- Scan cells are reconnected to form shift register (**scan chain**)

Effect

- Dramatically improve *controllability* and *observability* of memory elements (flip-flop) in a sequential circuit

Scan Design Flow: Different Modes



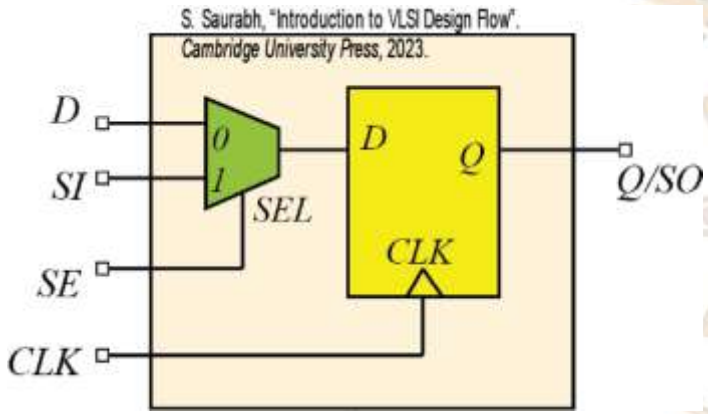
Design works in three modes:

1. Normal Mode: functional mode in which chip works
2. Shift Mode:
   - Memory elements (i.e. scan cells) work as shift registers
   - Test vectors are shifted-in and responses are shifted-out
3. Capture Mode: response of the fabricated circuit is captured during testing

Mode	TM	SE
Normal	0	0
Shift	1	1
Capture	1	0

Scan Cells

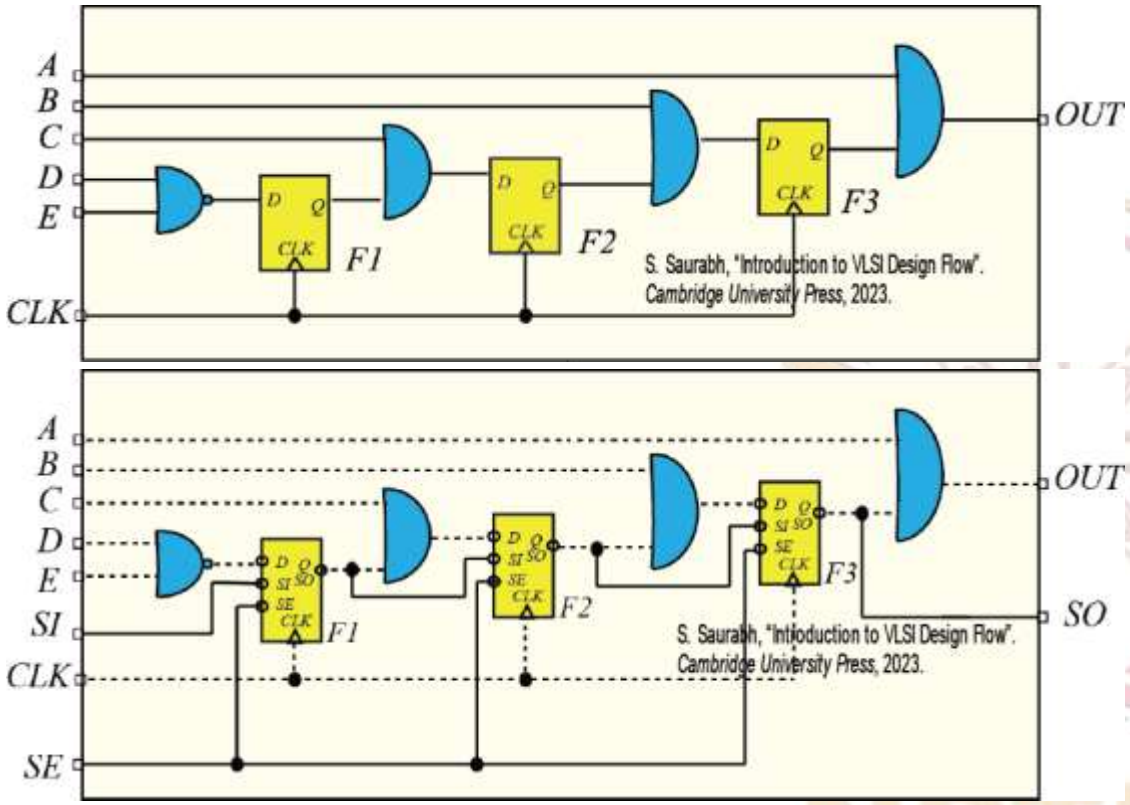
- Different kinds of scan cell can be used
- Most popular is MUXED-D Scan Cell



- D, CLK, Q similar to D flip-flop
- SI ≡ scan input
- SE ≡ scan enable
- Q also works as SO≡ scan out

- The multiplexer selects data between D and SI using the value at SE pin
- In the normal/capture mode: SE=0
  - ➢ Value at D is latched
- In the shift mode, SE=1
  - ➢ Value at SI is latched
- ➢ Output pin produces the content of D flip-flop
  - ➢ Next State could be of D-pin or SI-pin

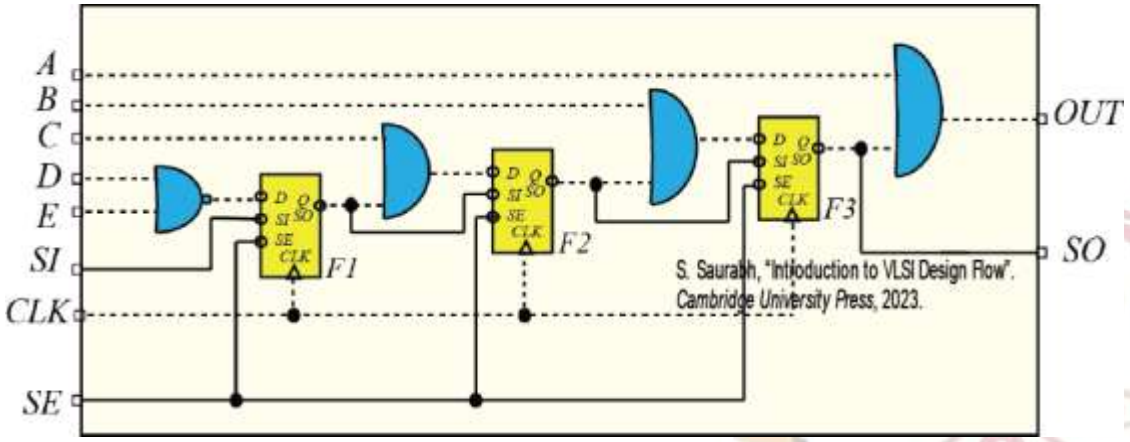
Scan Design Flow: Forming Scan Chain (Example)



- No changes made to the previous connections of D, Q and CLK pins

- The SI pin of the first scan cell is connected to the SI port
- Q/SO pin of one cell is connected to SI pin of the next cell to form a chain
- Q/SO pin of the last scan cell is connected to the SO port
- All SE pins of scan cells are connected to the SE port
- Form a scan chain consisting of N scan cells
- Any test vector can be shifted-in from SI port in N clock cycles
- Any test response can be shifted-out to SO port in N clock cycles
- Without scan chain, it could take exponential number of cycles

Scan Design: Sequential to Combinational Circuit Testing

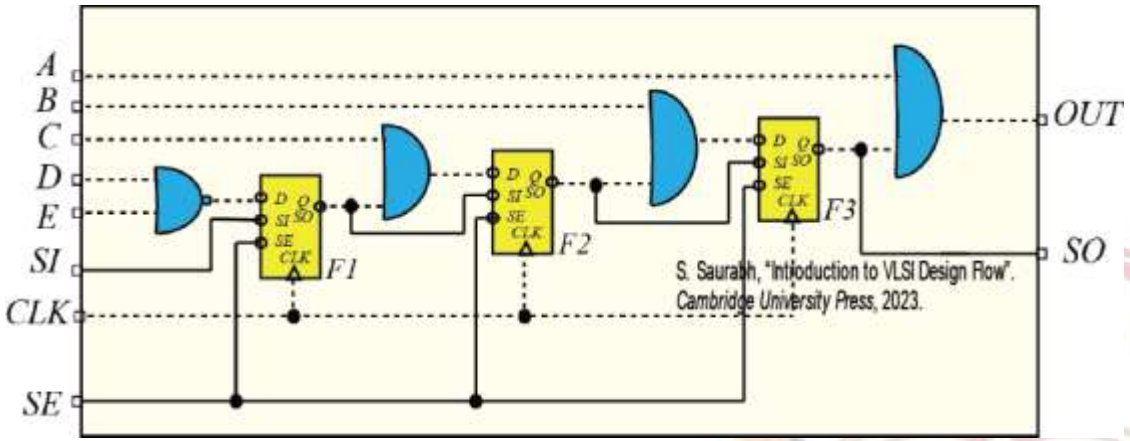


- Pins of a flip-flop becomes controllable/observable from primary input/output
  - Q-pin can be treated as pseudo-primary input (PPI)
  - D-pin can be treated as pseudo-primary output (PPO)

Scan design eases of testing:

- Effectively transforms the problem of sequential circuit testing to combinational circuit testing
- Automatic test pattern generation (ATPG) problem effectively changes from sequential to combinational

Scan Design Flow: Mechanism



Shift Mode: set SE=1.

- Shift in the desired test vector using port SI to the scan cells F1, F2, F3.
- Apply the required test vector at input port also.

Capture Mode: set SE=0 for 1 clock cycle.

- If there was a fault for which test vector was applied, scan cells will capture the result of fault and receive "fault" output

Shift Mode: switch back to shift mode (SE=1)

- Shift out the captured result to the port SO.
- The result is compared with the expected response
- Simultaneously, apply next test vector at port SI and allow it to scan-in through the scan chain.

Scan Design Flow: Tasks

Design Preparation: Design becomes testable

- Guidelines that must be followed during designing such that scan design flow can be used effectively

Scan Synthesis: Design becomes Scan Design

- **Scan Configuration** (During Synthesis)
  - Decide number of scan chains, scan cells to be used, exclude certain elements from being converted to scan cells
- **Scan Replacement** (During Synthesis)
  - Replace Flip-Flops with Scan Cells
- **Scan Reordering and Stitching** (During Physical Design)
  - Reorder scan cells based on physical location so that routing becomes easier

- **Test Vector Generation**
- **Scan Verification**
  - Scan Shift/Capture Operation using logic simulator
  - Verify Timing (STA): Hold Violations

Scan Design Flow: Cost

- Area Overhead: Scan Cell, Routing resource
- IO Pin Cost
- Performance degradation: added delay of multiplexor
- Design Effort Cost

References

- M. Bushnell and V. Agrawal, “Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits”, *Springer Science & Business Media*, 2004.
- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.