# VLSI DESIGN FLOW: RTL TO GDS

Lecture 34
Built-in Self-test (BIST)


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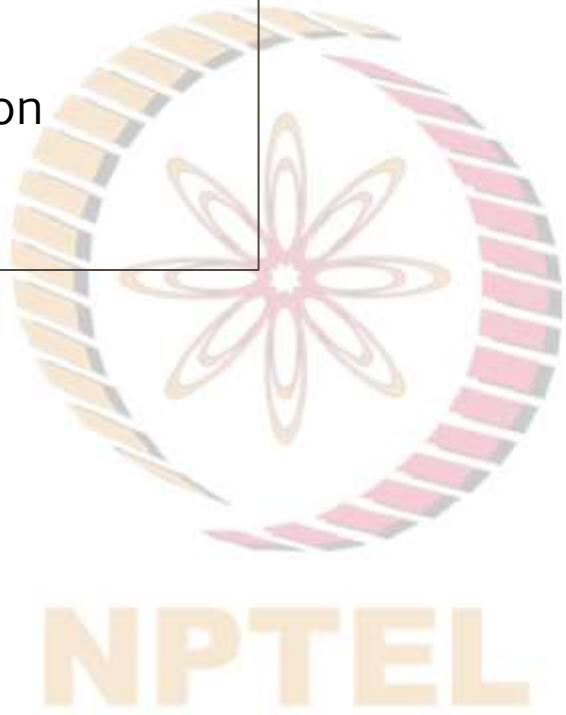
# Lecture Plan

- Distinguishing Features
- Architecture
- Random Test Pattern Generation
- Test Response Analyser



# Built-in Self Test (BIST)

**Drawbacks of ATE-based testing:**

- Cost of testing high
  - ATE cost
  - Voluminous test data: increase test time
- Can be done only in production test environment
  - Lacks capability of field testing
- At-speed test difficult
  - Probe's inductance/capacitance bottleneck

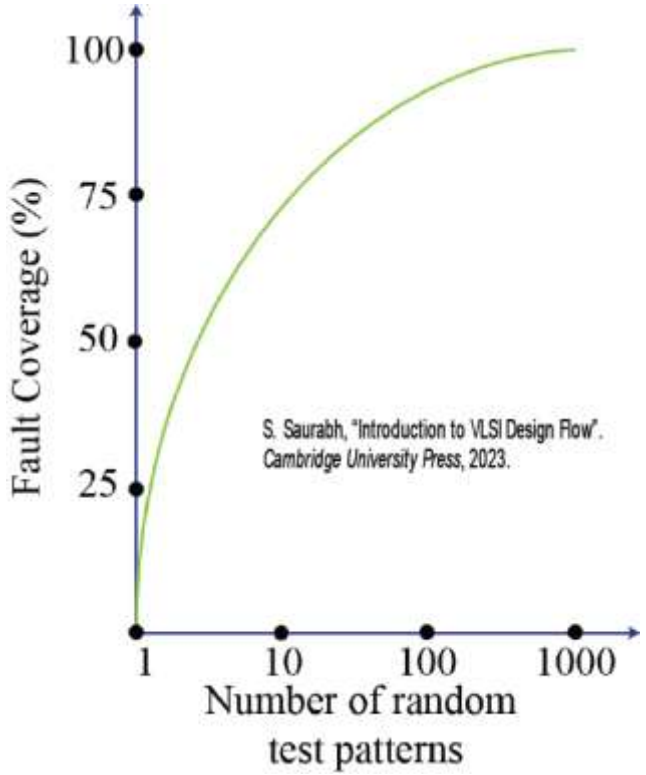
**BIST as a solution:**

- Test-oriented additional hardware and software features **inside a given IC**
- Allows IC to test their own operation
- Reducing dependence on an external ATE for testing
  - Repair in the field possible

# Built-in Self Test (BIST): Distinguishing Features

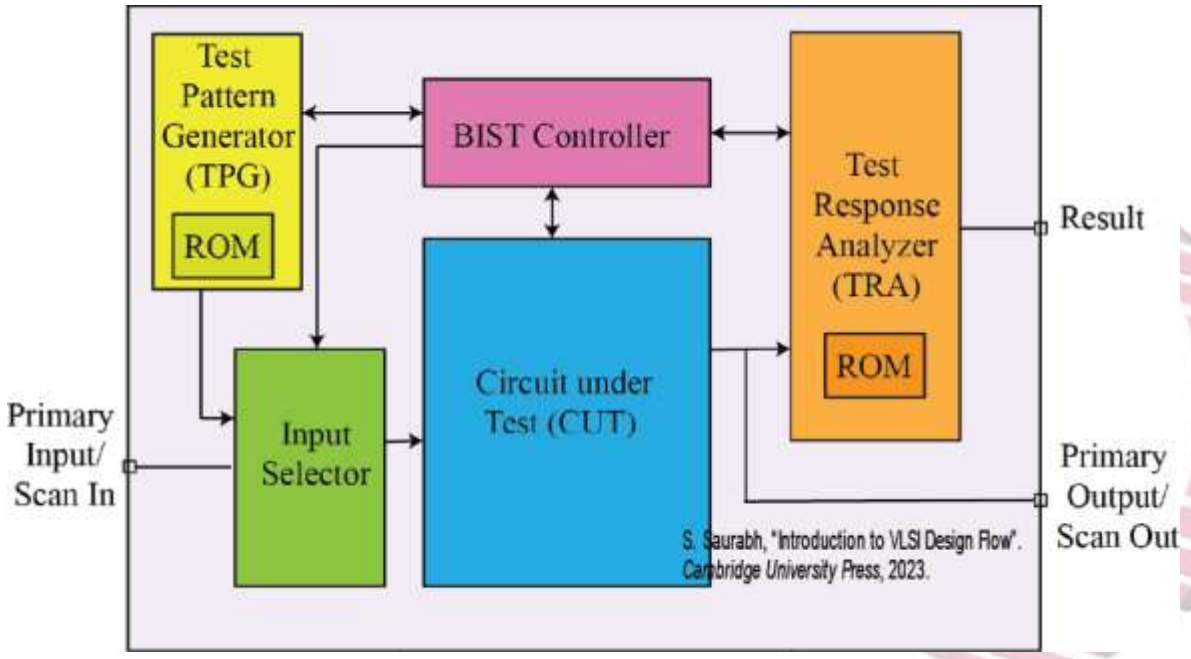
1. Contains *Pseudo-random pattern generator* inside the chip
   - Provides test vectors dynamically
   - Avoids storing voluminous test vectors
2. Performs *signature analysis* for detecting failures
   - Does not perform comparison of exact response
   - Avoids storing voluminous expected response inside the chip

# Testability: Fault Coverage vs. Random Test Pattern Count




- Stuck-At Fault coverage rises to 100% logarithmically
- Reaching 90% coverage is easy using random patterns

# BIST: Architecture

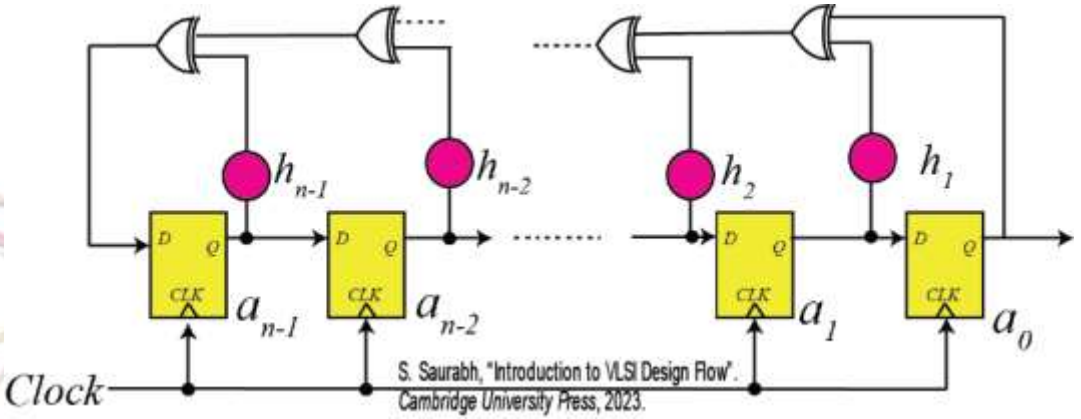



- **Test Pattern Generator (TPG)**
  - Generates pattern for testing
  - Can contain ROM
- **Test Response Analyzer (TRA)**
  - Generates signature for the test response and compare
  - ROM stores golden signature
  - Compares test signature with the golden signature
- **Test Controller**
  - Controls all the operations of BIST
  - Strategy for overall test control is most difficult part of BIST

# BIST: Test Pattern Generator

- **Pseudo-Random Pattern Generator**
  - Linear Feedback Shift Register (LFSR)
  - Repeatable
  - Small hardware can produce large number of “random” test patterns

- We can tap the output of any flip-flop to provide feedback.
- If we tap the output $a_i$ of the i-th flip-flop, then $h_i$ is taken as 1, else it is taken as 0.




$$a_0^{k+1} = a_1^k$$

$$a_1^{k+1} = a_2^k$$

....

$$a_{n-2}^{k+1} = a_{n-1}^k$$

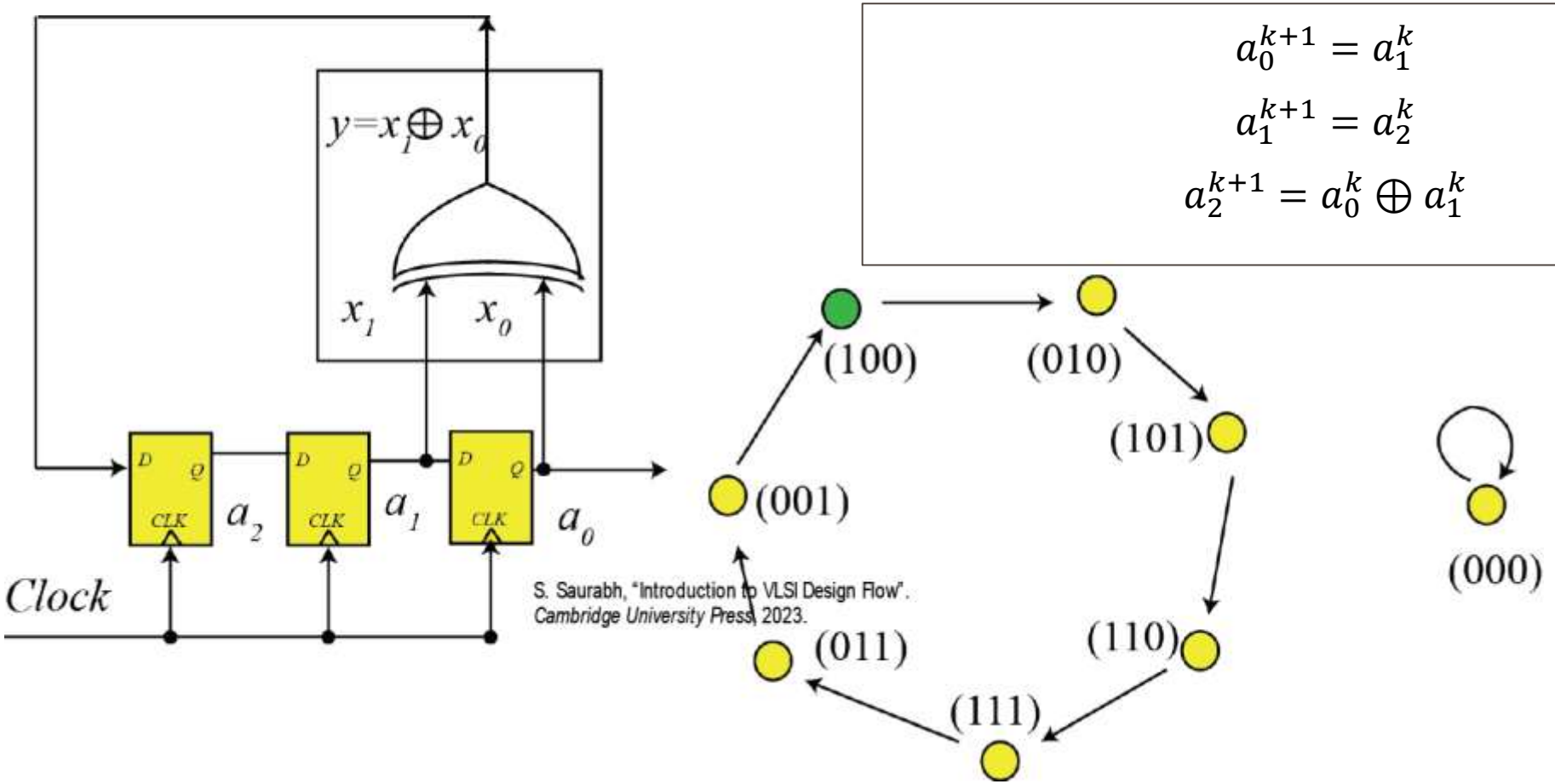
$$a_{n-1}^{k+1} = a_0^k \oplus h_1 a_1^k \oplus h_2 a_2^k \oplus \ldots \oplus h_{n-1}\, a_{n-1}^k$$

# Pattern Generator: Illustration

$$a_0^{k+1} = a_1^k$$

$$a_1^{k+1} = a_2^k$$

$$a_2^{k+1} = a_0^k \oplus a_1^k$$



# Pattern Generator: Considerations

- **LFSR**
  - Test patterns generated by an LFSR have most of the properties of random numbers
  - Desirable to have long sequence so that good fault coverage is achieved

- Some faults may be not covered by random pattern generator
  - Use ATPG to get deterministic test-vector and put those test-vectors in **ROM**
  - Helps achieve high fault coverage with small number of test vectors

# BIST: Test Response Analyzer (1)

- No. of test patterns can be large (e.g. 1 million) and there can be many outputs (e.g. 100)
  - Too **voluminous** data to store in ROM (100 million bits)

- **Compaction**: method of reducing the number of bits in the circuit response

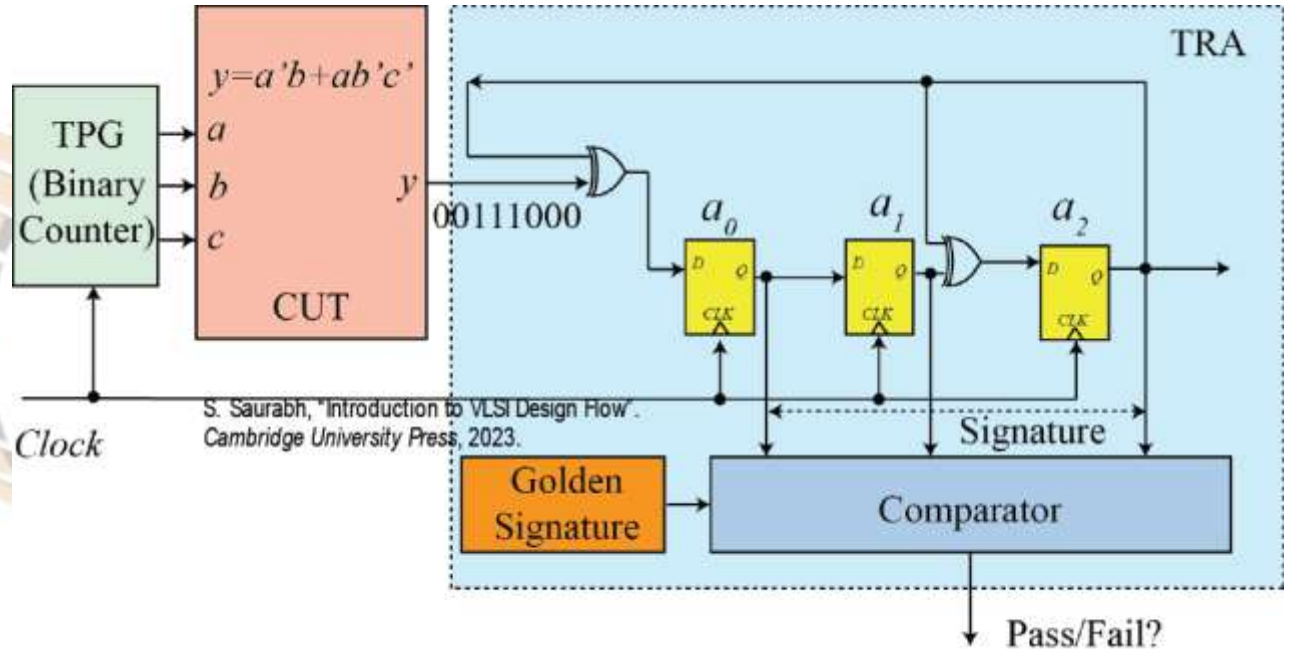
- **Signature**: a statistical property of a circuit, usually a number computed for a circuit from its responses

- **Signature Analysis**: signature of a good circuit ("golden signature" ) compared with the signature of a "potentially" faulty circuit ("test signature")
  - If "golden signature" matches "test signature" then the circuit is assumed to be good, else faulty
  - Desirable: signature of a good circuit and faulty circuits are different

- **Aliasing**: During testing, it is possible that the signature of "good" circuit and "faulty" circuit match
  - Due to information loss during compaction

# BIST: Test Response Analyzer

- Techniques to compute Signature
  - ➢ **Ones Counting**: count number of ones across all circuit responses
    - ❑ Different permutations can yield same signature
  - ➢ **Modular LFSR**: Extra XOR gate at the input
    - ❑ Single Input Signature Register (SISR)
    - ❑ Need to start with a *seed value*



# Built-in Self Test (BIST)

## Advantages

- Lower cost of test, since the need for external electrical testing using an ATE will be reduced
- No need to store test patterns
- At-speed test can be done
- Capability to perform tests outside the production electrical testing environment

## Disadvantages

- Additional silicon area
  - Yield and Reliability decrease
- Performance loss
  - Extra delays
- Additional pin (and possibly bigger package size) requirements

# References


- M. Bushnell and V. Agrawal, “Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits”, *Springer Science & Business Media*, 2004.
- S. Saurabh, “Introduction to VLSI Design Flow”. Cambridge: *Cambridge University Press*, 2023.