Verification of Truth Table for Digital Logic gates

Experiment no.1 Date:

<u>Aim:</u> To study the working of logic gates and to verify their truth tables using LTSPICE software.

Software Required: LTSPICE software

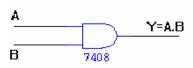
Theory and Circuit Diagram:

Logic gates are one of the fundamental building blocks of digital systems. Most of the functions in a computer, with the exception of certain types of memory, are implemented with logic gates used on a very large scale. For example, a microprocessor, which is the main part of a computer, is made up of hundreds of thousands or even millions of logic gates. The term gate is used to describe a circuit that performs a basic logic operation. The following section describes the different types of logical gates used in digital circuits.

AND Gate:

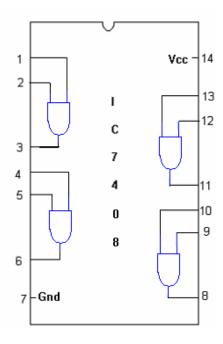
The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

SYMBOL: PIN DIAGRAM:



TRUTH TABLE

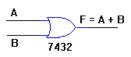
А	В	A.B	
0	0	0	
0	1	0	
1	0	0	
1	1	1	



OR Gate:

The OR gate performs a logical addition commonly known as the OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low. The circuit symbol, pin diagram of IC7432 implementing logical OR operation and the truth table are given below

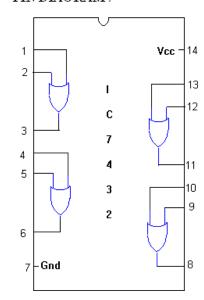
SYMBOL:



TRUTH TABLE

В	A+B
0	0
1	1
0	1
1	1
	0

PIN DIAGRAM:



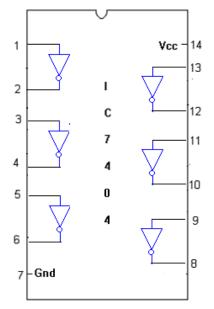
NOT GATE:

The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high. The circuit symbol with the pin diagram of IC7404 implementing not operation is shown below





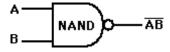
Α	A
0	1
1	0

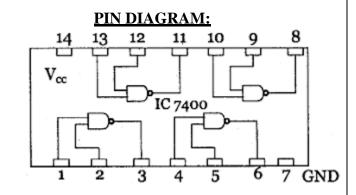


NAND GATE:

The NAND gate is a combination of AND-NOT. The output is high when both inputs are low and any one of the inputs is low. The output is low level when both inputs are high. The circuit symbol, pin diagram of IC 7400 and the corresponding truth table are given below.

SYMBOL:





TRUTH TABLE

Input A	Input B	Output
0	0	1
0	1	1
1	0	1
1	1	0

NOR GATE:

The NOR gate is a combination of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high. The circuit symbol, PIN diagram of IC7432 with the truth table are given below.

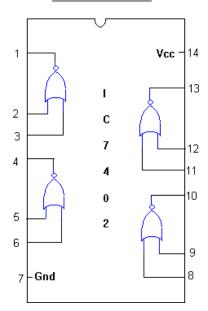
TRUTH TABLE

Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	0

SYMBOL :

$$\frac{A}{B} \frac{F = \overline{A + B}}{7402}$$

PIN DIAGRAM:



Ex-XOR GATE:

The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

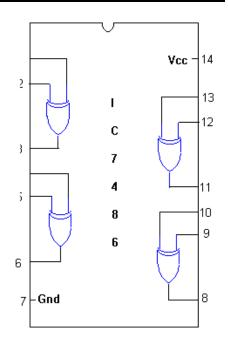
CIRCUIT SYMBOL

PIN DIAGRAM:



TRUTH TABLE:

А	В	AB + AB
0	0	0
0	1	1
1	0	1
1	1	0



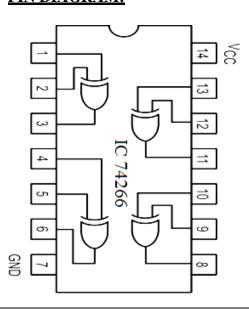
EX-NOR gate

SYMBOL:

TRUTH TABLE

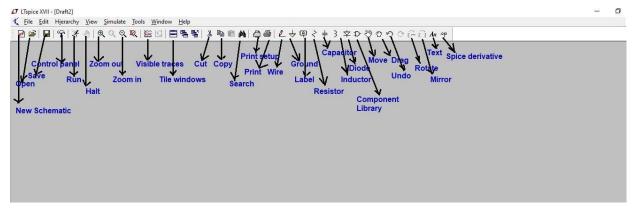
Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	1

PIN DIAGRAM:



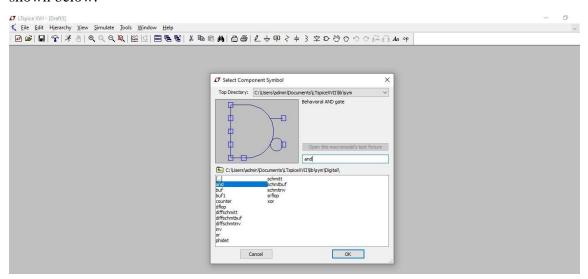
Procedure, Observation Table, and Waveforms:

Step 1: Open LTspice software.



Step 2: Go to File→ New schematic

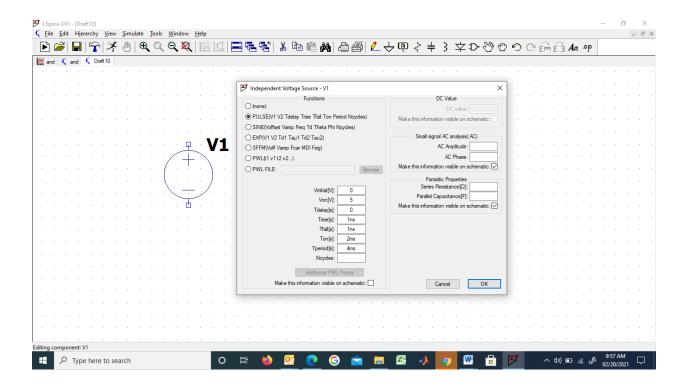
Step 3: Once new schematic file is created, go to component library and choose AND gate as shown below.



Step 4: Similarly, choose the voltage in the library and press the advanced option.

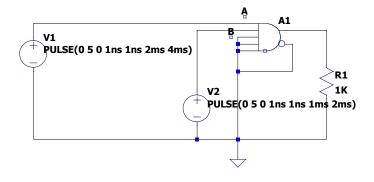
Choose pulse and enter the given values as shown in the figure. The second voltage source may be chosen with on time as 2ms and total time period as 4ms





/T Edit Cina	ulation Com					
L) Edit Sim	iulation Com	mand				
Transient	AC Analysis	DC sweep	Noise	DC Transfer	DC op pnt	
	Perfo	rm a non-line	ear, time	-domain simula	tion.	
				Stop time:	4ms	
		Time	to start	saving data:		
			Maximu	m Timestep:		
	Start ex	cternal DC su	apply vol	tages at 0V:		
Stop simulating if steady state is detected:						
0	on't reset T=	0 when stead	dy state	is detected:		
		Step the	load cur	rent source: [
	Sk	kip initial ope	rating po	int solution:		
Syntax: .tr	an <tstop> [-</tstop>	<option> [<</option>	option>]]		
.tran 4ms						
	Car	ncel		C	DK .	

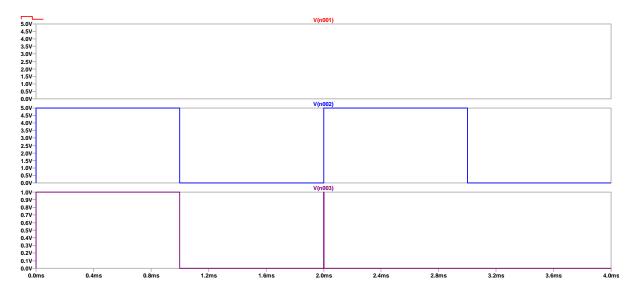
Step 6: As shown in the figure given below, for the AND gate element, if the output is directly taken, it will give you AND logic. Otherwise, if the output is taken from the inverted element (with a circle), it is the NAND logic as shown in figure



.tran 4ms

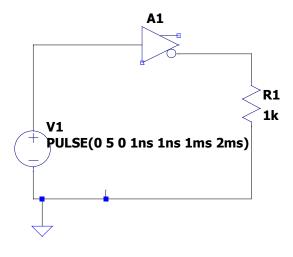
Input and Output Voltage Waveforms:

The plot of the two inputs (Vn001, Vn002) and the output voltages are given in the figure below. From the output voltages it can be observed that the output voltage goes high only when both inputs are high.



NOT Gate Implementation:

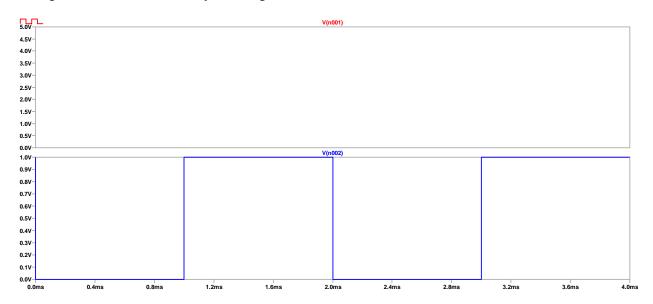
Make use of the inverting buffer in the LTSPICE library for emulating the NOT gate



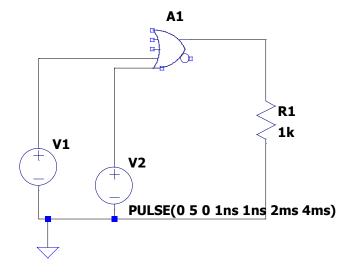
.tran 4ms

Input and Output Voltage waveforms:

From the input and the output voltage waveforms it can be observed that the output voltage is inverted is inverted by the not gate.



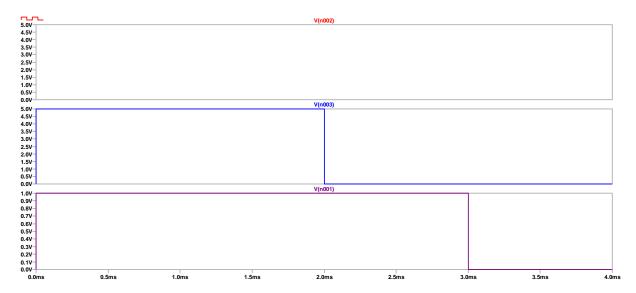
OR Gate implementation:



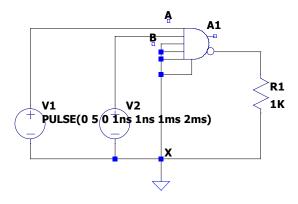
.tran 4ms

Input and Output Voltage Waveforms:

From the results it can be observed that the output of the OR gate stays high when at least one of the logical inputs are in the active high state.



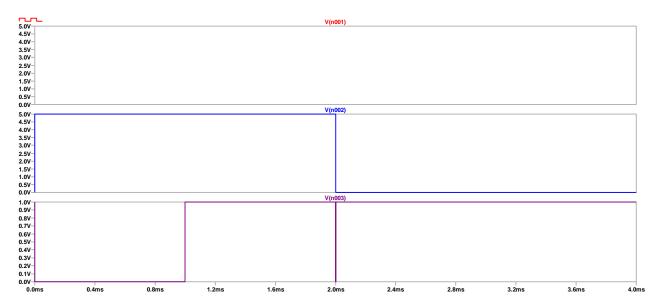
NAND Gate Implementation:



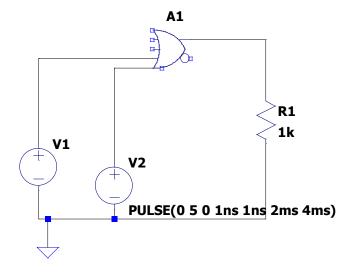
.tran 4ms

Input and Output Voltage Waveforms:

From the plot of output voltage (V003) it can be observed that the output of the NAND gate stays low when both the inputs (Vn001, Vn002) stay high.

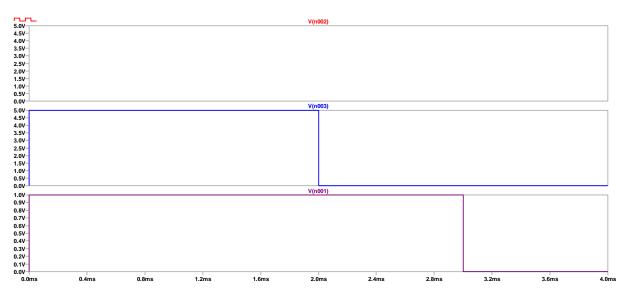


NOR Gate Implementation:

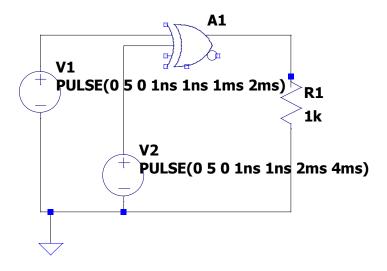


.tran 4ms

Input and Output Voltage waveforms:



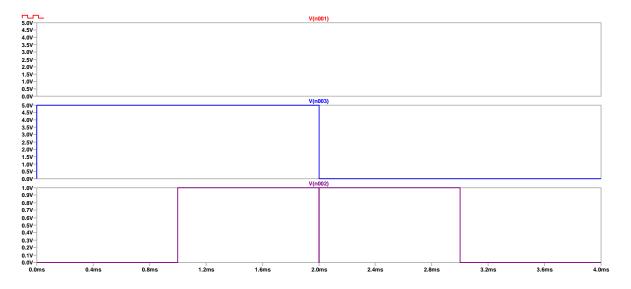
EXOR Gate Implementation:



.tran 4ms

Input and Output Voltage waveforms:

From the plot of output voltage (Vn002) it can be observed that the output of the Ex-OR gate stays low when both the inputs (Vn001,Vn003) remains the same.



Result

The working of logic gates is verified with truth tables using LTSPICE software.