Design of Decoder and Encoder

Experiment no. **Date:**

Aim:

To design and implement Decoder and Encoder using logic gates

Software Required: LTspice software

Theory

DECODER:

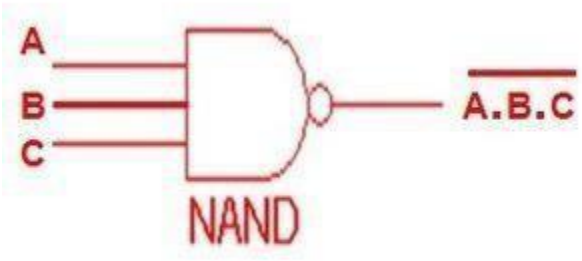
A decoder is a digital circuit that detects the presence of a specified combination of bits (code) on its inputs and indicates the presence of that code by a specified output level. The input code generally has fewer bits than the output code. In its general form, a decoder has n input lines to handle n bits and from one to 2^n output lines to indicate the presence of one or more

n bit combinations. In the block diagram of decoder circuit the encoded information is present as n input producing 2^n possible outputs. 2^n output values are from 0 through out 2^n – 1.

ENCODER:

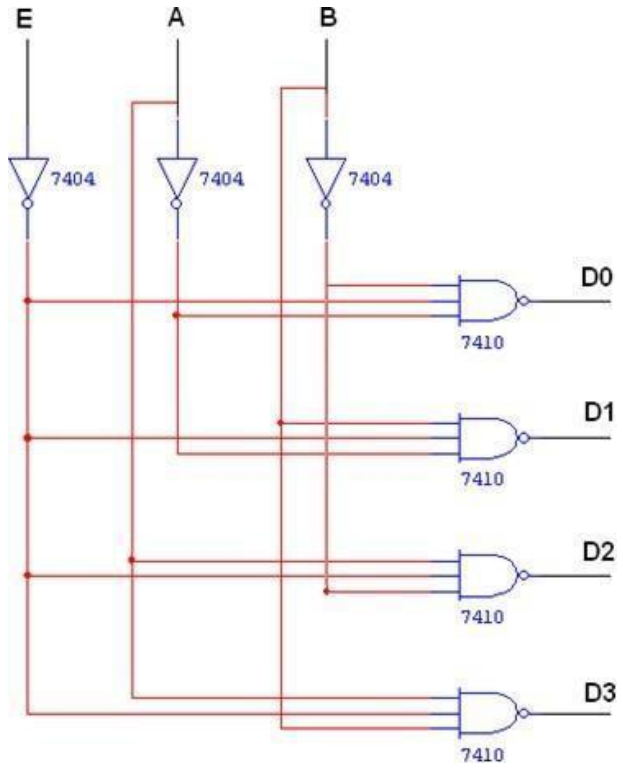
An encoder is a digital circuit that performs the inverse operation of a decoder. An encoder has 2^n (or fewer) input lines and *n* output lines. The output lines, as an aggregate, generate the binary code corresponding to the input value.

LOGIC DIAGRAM OF DECODER:



3 input NAND gate				
A	B	C	A.B.C	$\overline{A.B.C}$
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

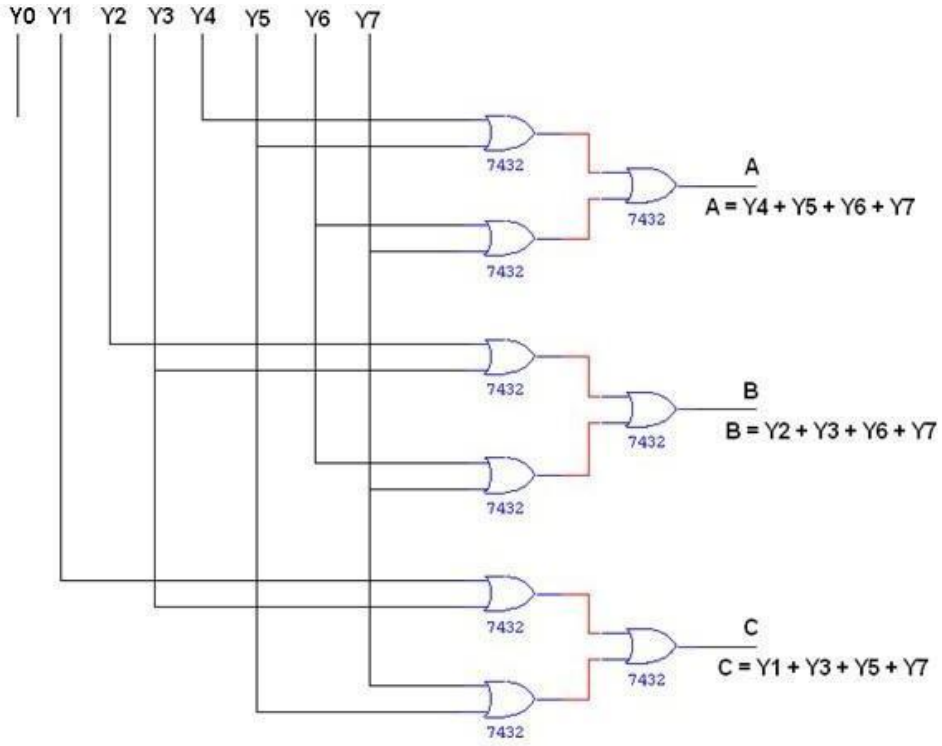
EQUIVALENT LOGIC DIAGRAM OF DECODER:



TRUTH TABLE:

INPUT			OUTPUT			
E	A	B	D0	D1	D2	D3
1	0	0	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

LOGIC DIAGRAM OF ENCODER:

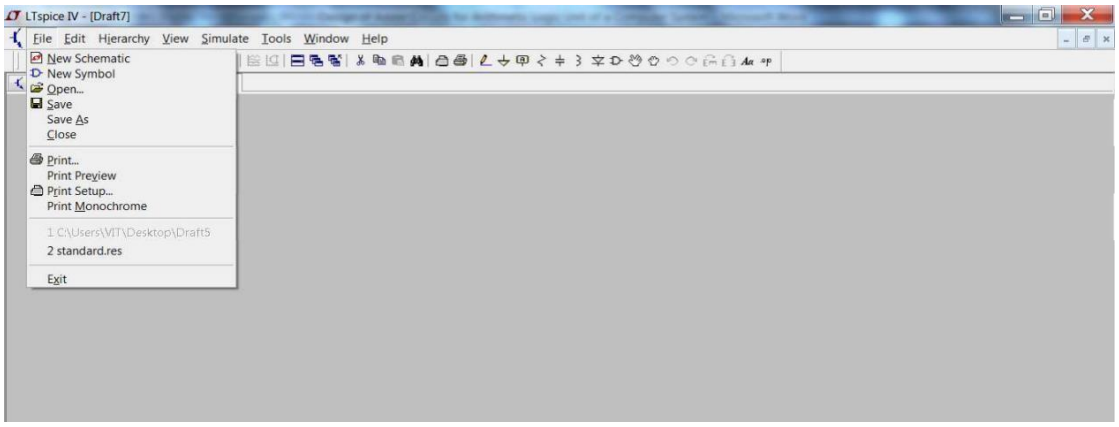


TRUTH TABLE:ENCODER

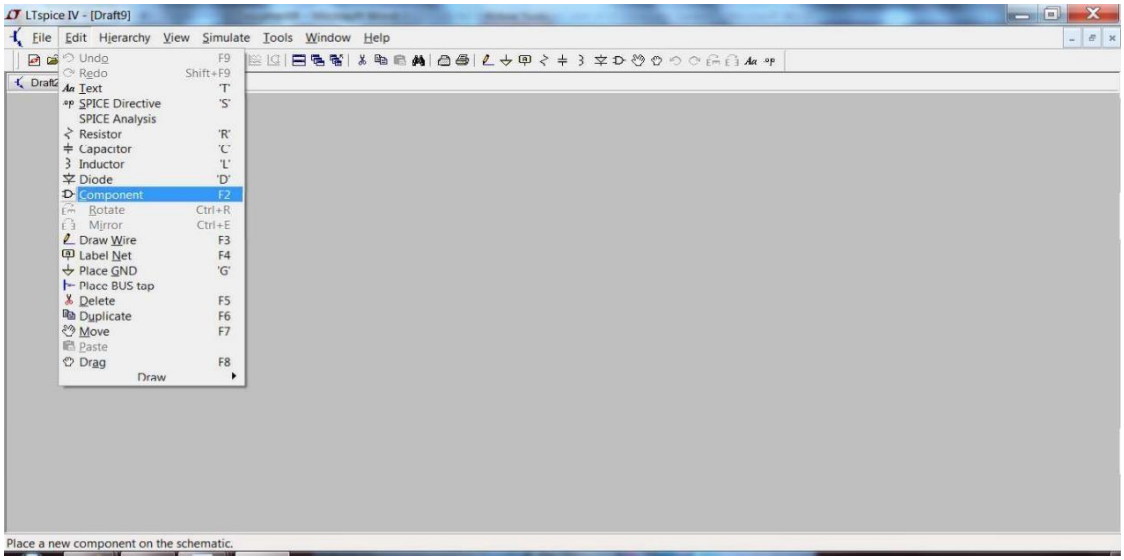
INPUT								OUTPUT		
Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	A	B	C
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Procedure for Simulation:

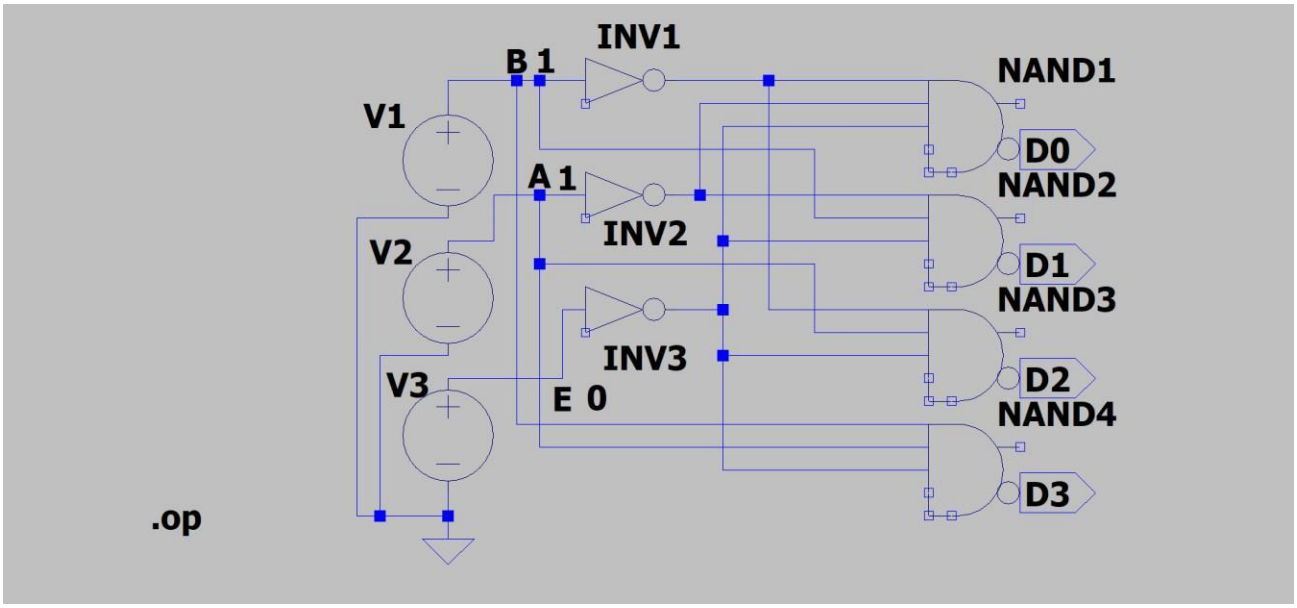
1. Open LTspice. Go to File⁓ New Schematic.



2. On the File Menu, click on Edit ⁓ Component.

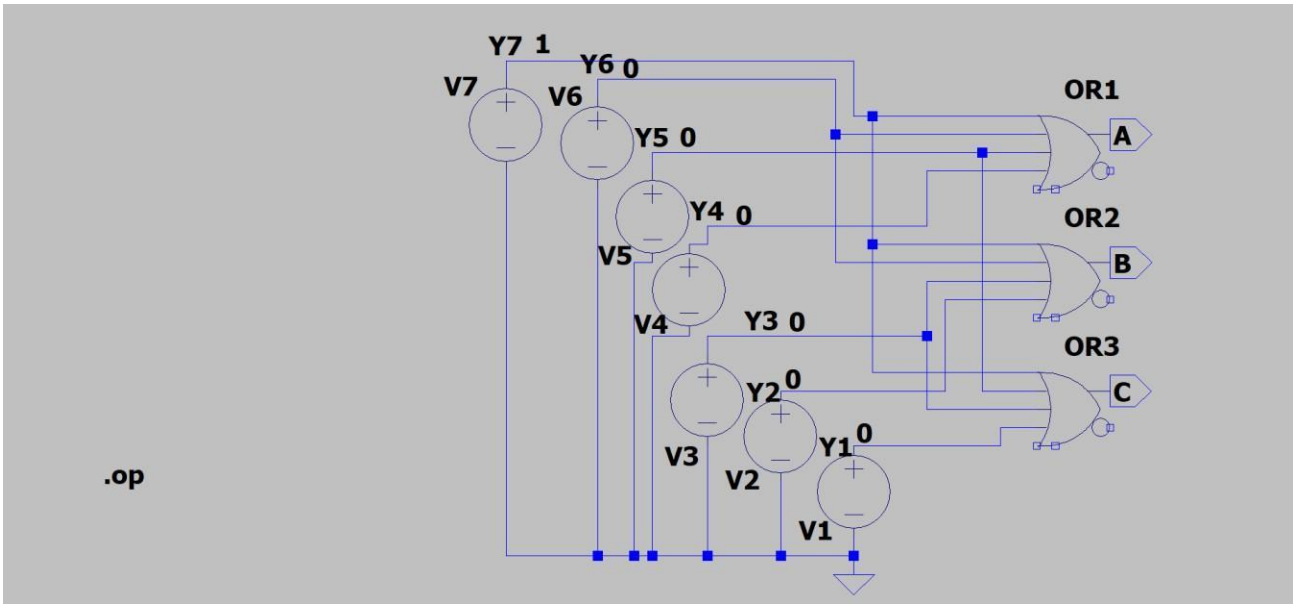


3. **For Decoder**: Place the voltage sources, NOT gate, NAND gate, and ground on to schematic and make necessary connections as shown in the Figure.



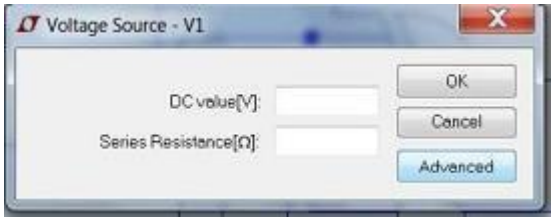
Decoder

For Encoder: Place the voltage sources, OR gates and ground on to schematic and make necessary connections as shown in the Figure .



Encoder

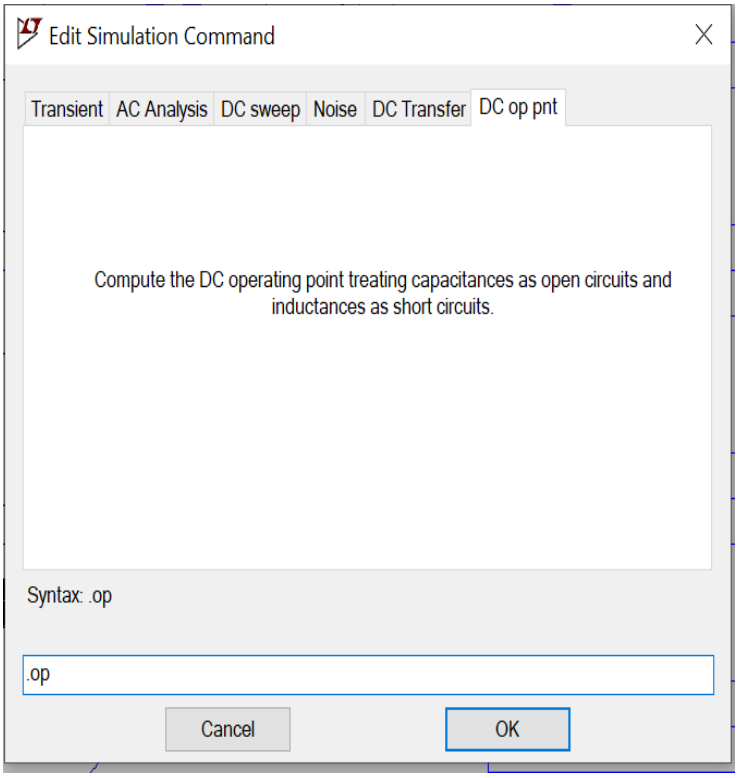
4. As shown in the figures below, For Decoder
   Right click on the voltage sources V1 and then Enter DC Value 1 and then click OK option.
   Right click on the voltage sources V2 and then Enter DC Value 1 and then click OK option.
   Right click on the voltage sources V3 and then Enter DC Value 0 and then click OK option.



For Encoder,
Right click on the voltage sources V7 and then Enter DC Value 1 and then click OK option.
Right click on the voltage sources V6 and then Enter DC Value 0 and then click OK option.
Right click on the voltage sources V5 and then Enter DC Value 0 and then click OK option.
Right click on the voltage sources V4 and then Enter DC Value 0 and then click OK option.
Right click on the voltage sources V3 and then Enter DC Value 0 and then click OK option.
Right click on the voltage sources V2 and then Enter DC Value 0 and then click OK option.
Right click on the voltage sources V1 and then Enter DC Value 0 and then click OK option.

6. Go to Edit → SPICE analysis.

   For both Decoder and Encoder: Select “DC op pnt” tab and Click “OK” and Press run symbol on menu bar.



7. Observe the values and verify the truth table of both decoder and encoder. Results are shown below for the Last case of Truth Table for both decoder and encoder.

Results for Decoder:

```
        --- Operating Point ---

V(n001):        0               voltage
V(n002):        0               voltage
V(n003):        1               voltage
V(d0):          1               voltage
V(b):           1               voltage
V(d1):          1               voltage
V(a):           1               voltage
V(d2):          1               voltage
V(d3):          0               voltage
V(e):           0               voltage
I(V3):          0               device_current
I(V2):          0               device_current
I(V1):          0               device_current
I8(Inv3):       -0              device_current
I7(Inv3):       0               device_current
I6(Inv3):       0               device_current
I2(Inv3):       0               device_current
I8(Inv2):       -0              device_current
I7(Inv2):       0               device_current
I6(Inv2):       0               device_current
I2(Inv2):       0               device_current
I8(Inv1):       -0              device_current
I7(Inv1):       0               device_current
I6(Inv1):       0               device_current
I2(Inv1):       0               device_current
I8(Nand4):      -0              device_current
I7(Nand4):      0               device_current
I6(Nand4):      0               device_current
```

Results for Encoder:

--- Operating Point ---

V(y7):	1	voltage
V(y6):	0	voltage
V(y5):	0	voltage
V(y4):	0	voltage
V(a):	1	voltage
V(y3):	0	voltage
V(y2):	0	voltage
V(b):	1	voltage
V(y1):	0	voltage
V(c):	1	voltage
I(V7):	0	device_current
I(V6):	0	device_current
I(V5):	0	device_current
I(V4):	0	device_current
I(V3):	0	device_current
I(V2):	0	device_current
I(V1):	0	device_current
I8(Or3):	-0	device_current
I7(Or3):	0	device_current
I6(Or3):	0	device_current
I2(Or3):	0	device_current
I8(Or2):	-0	device_current
I7(Or2):	0	device_current
I6(Or2):	0	device_current
I2(Or2):	0	device_current
I8(Or1):	-0	device_current
I7(Or1):	0	device_current
I6(Or1):	0	device_current

8. Similarly, Verify the Decoder and Encoder Circuits for all other cases of truth table and present the results.

RESULT:

Thus , the decoder and encoder circuits were implemented using logic gates in LTspice software and verified.