Verification of all gates using UNIVERSAL GATES

Experiment no. 2 **Date:**

AIM:

To study and verify the all logic gates using UNIVERAL Gate NAND using LTspice.

APPARATUS REQUIRED:

Logic gates (IC) trainer kit.
Connecting patch chords or wires.
IC 7400

THEORY:

NAND gate is actually a combination of two logic gates: AND gate followed by NOT gate. So its output is complement of the output of an AND gate. This gate can have minimum two inputs, output is always one. By using only NAND gates, we can realize all logic functions: AND, OR, NOT, X-OR, X-NOR, NOR. So this gate is also called universal gate.

(1). NAND gates as NOT gate

A NOT produces complement of the input. It can have only one input, tie the inputs of a NAND gate together. Now it will work as a NOT gate. Its output is

$$Y = (A.A)'$$

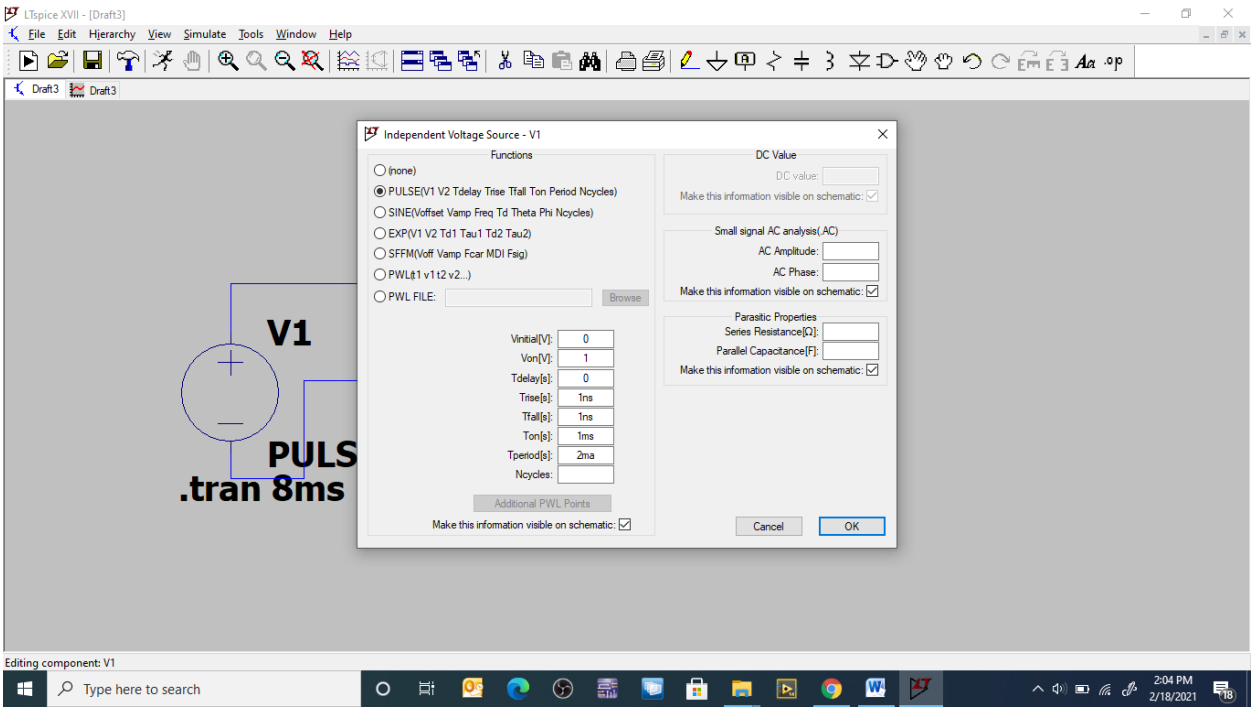
=> $$Y = (A)'$$

NOT Gate diagram

NOT (inverter)

NOT Truth table

Input	Output
A	Y=A'
0	1
1	0


LTspice XVII - [Draft3]
File Edit Hierarchy View Simulate Tools Window Help
Draft3 Draft3
Independent Voltage Source - V1
Functions
(none)
PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles)
SINE(Voffset Vamp Freq Td Theta Phi Ncycles)
EXP(V1 V2 Td1 Tau1 Td2 Tau2)
SFFM(Voff Vamp Fcar MDI Fsig)
PWL(t1 v1 t2 v2...)
PWL FILE:
Browse
Vinitial[V]: 0
Von[V]: 1
Tdelay[s]: 0
Trise[s]: 1ns
Tfall[s]: 1ns
Ton[s]: 1ms
Tperiod[s]: 2ma
Ncycles:
Additional PWL Points
Make this infomation visible on schematic:
DC Value
DC value:
Make this information visible on schematic:
Small signal AC analysis(.AC)
AC Amplitude:
AC Phase:
Make this information visible on schematic:
Parasitic Properties
Series Resistance[Ω]:
Parallel Capacitance[F]:
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Cancel
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V1
PULS
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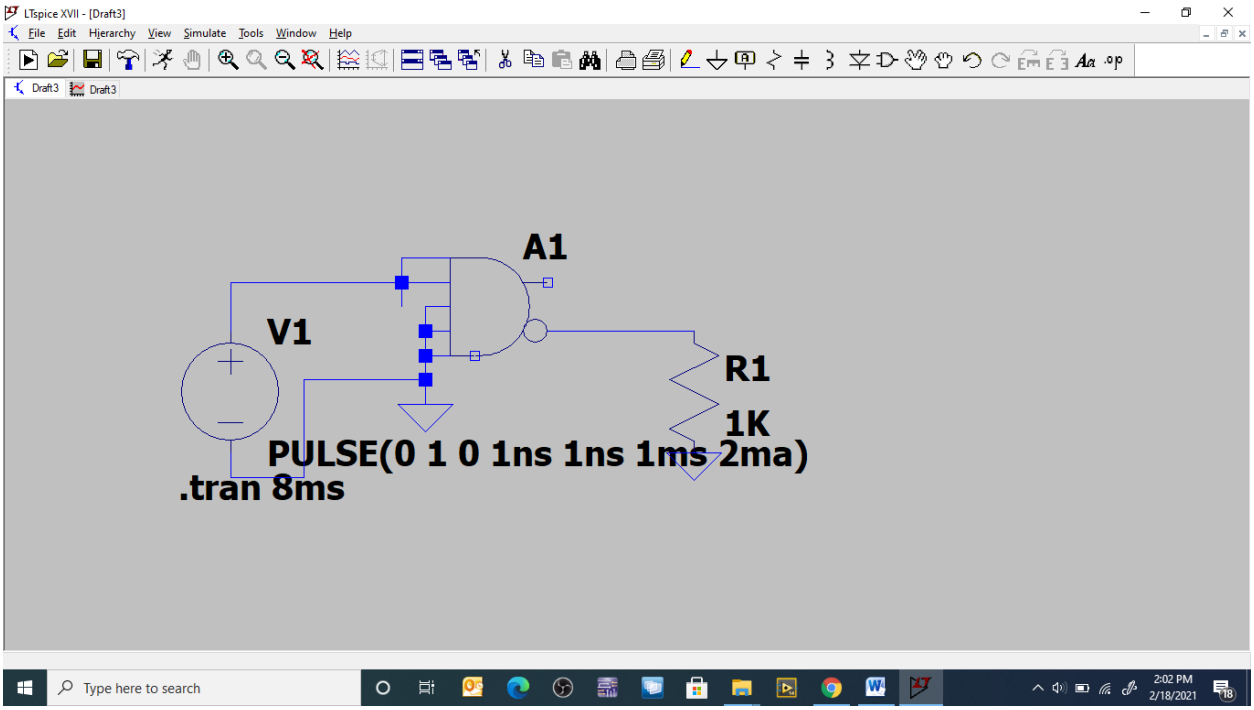
2/18/2021


LTspice XVII - [Draft3]
File Edit Hierarchy View Simulate Tools Window Help
Draft3 Draft3
A1
V1
R1
1K
PULSE(0 1 0 1ns 1ns 1ms 2ma)
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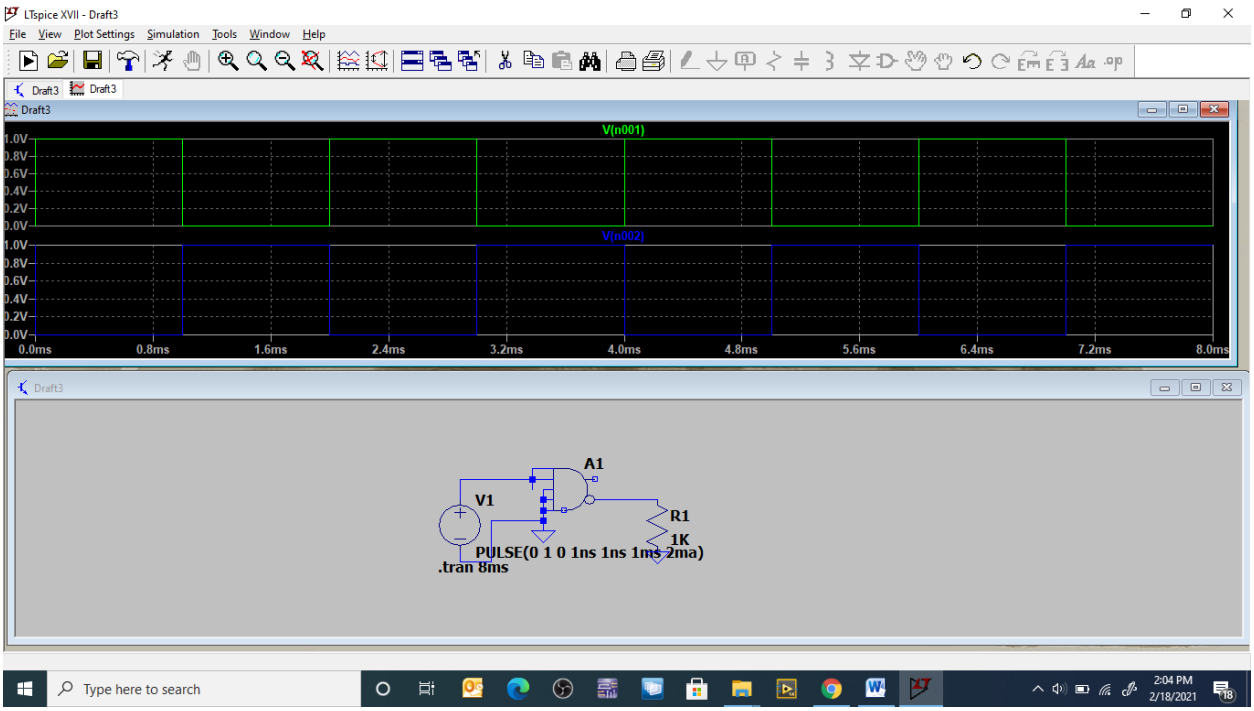


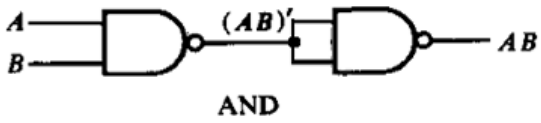
(2). NAND gates as AND gate

A NAND produces complement of AND gate. So, if the output of a NAND gate is inverted, overall output will be that of an AND gate.

$$Y = ((A.B)')'$$

$$\Rightarrow \quad Y = (A.B)$$

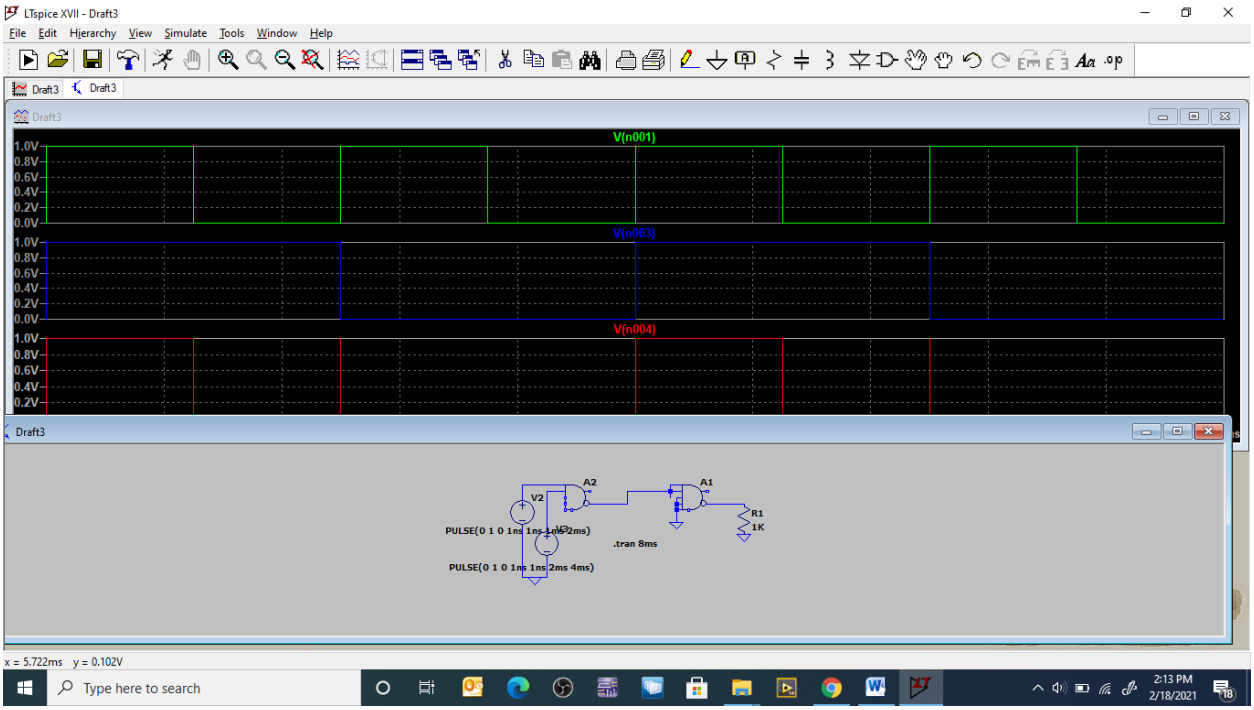
AND Gate diagram

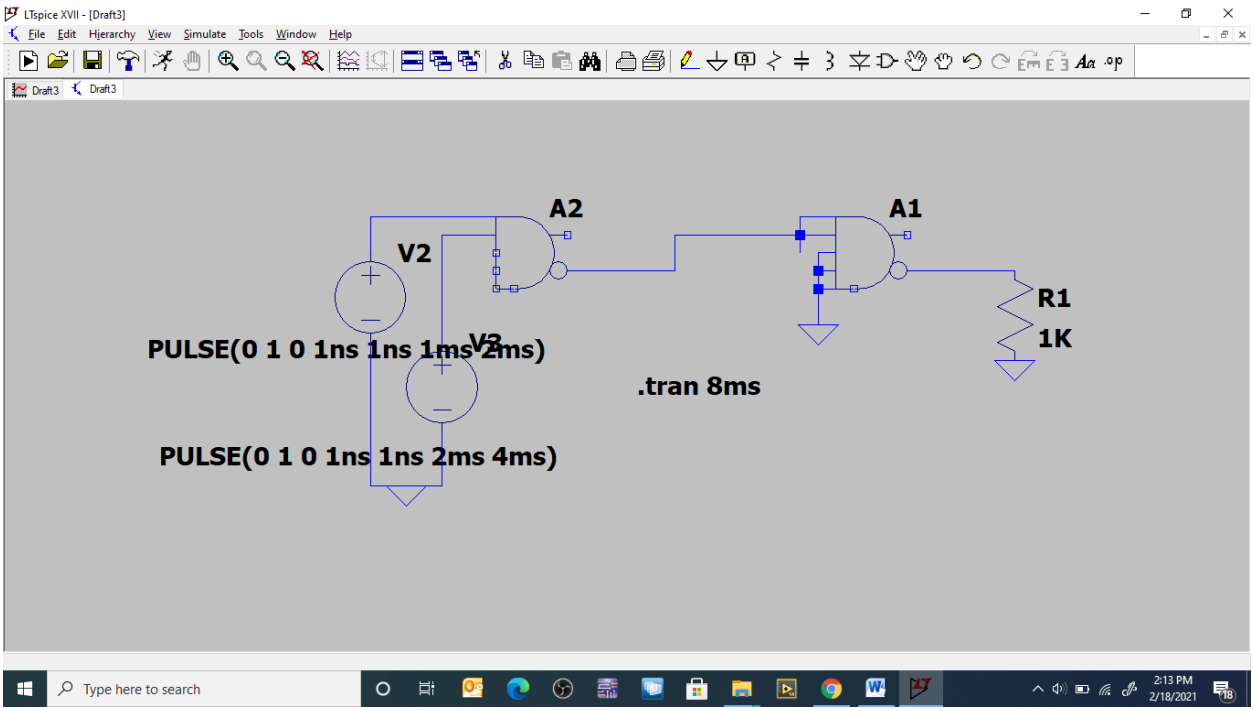


AND

AND Gate Truth table

Input		Output
A	B	C=A.B
0	0	0
0	1	0
1	0	0
1	1	1





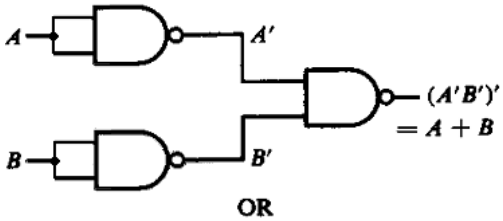
(3) NAND gates as OR gate

From De-Morgan's theorems: (A.B)' = A' + B'

=> (A'.B')' = A'' + B'' = A + B

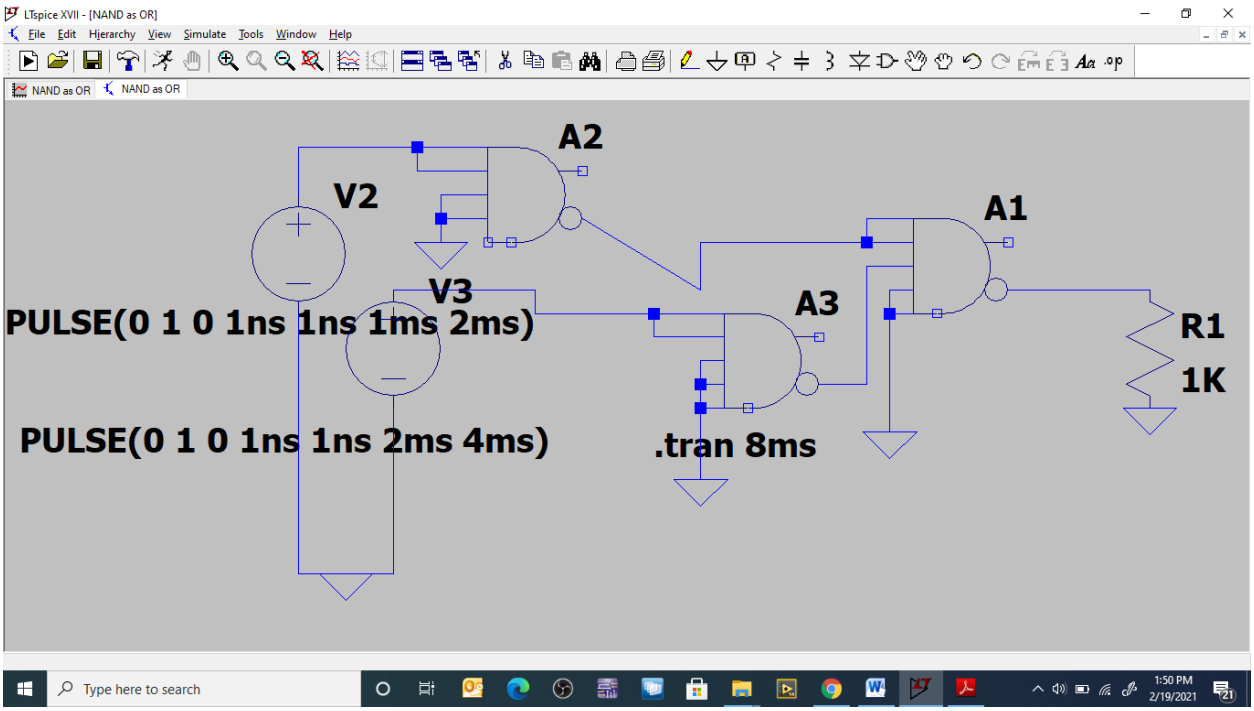
So, give the inverted inputs to a NAND gate, obtain OR operation at output.

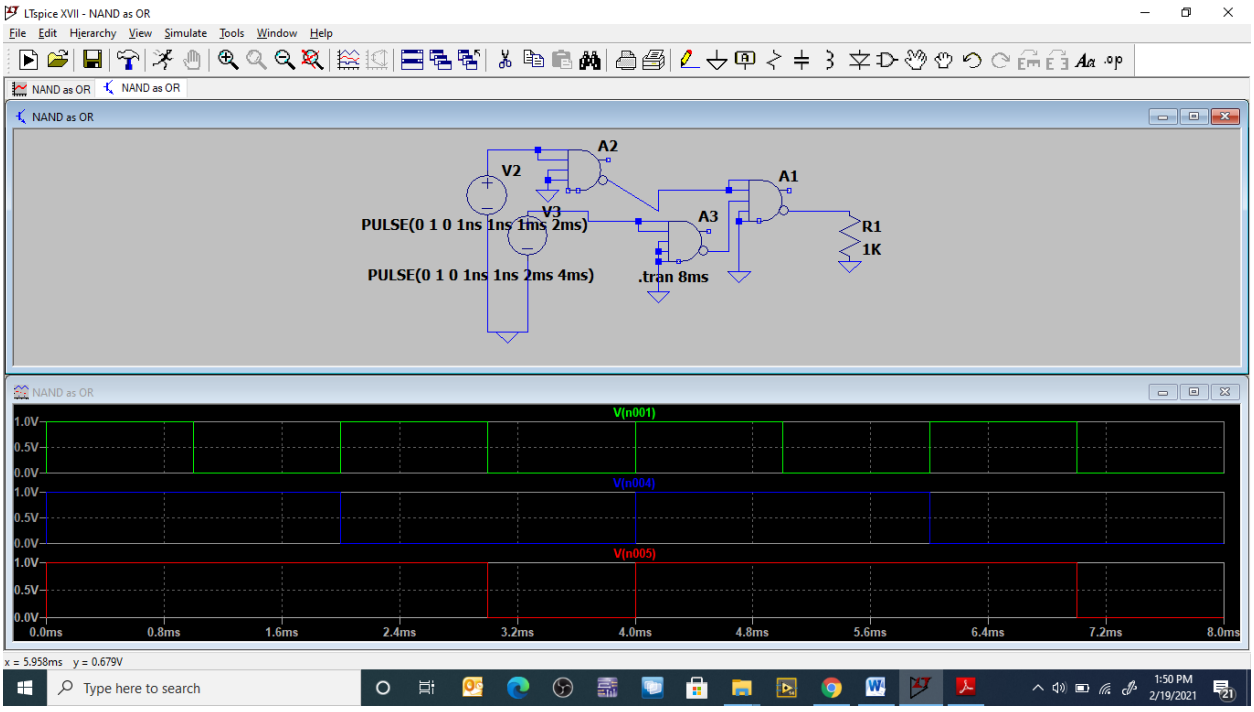
OR Gate diagram



OR Gate Truth table

Input		Output
A	B	C=A+B
0	0	0
0	1	1
1	0	1
1	1	1

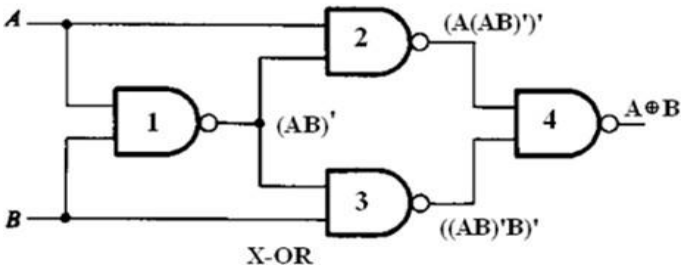




(4) NAND gates as X-OR gate

The output of a two input X-OR gate is shown by: Y = A'B + AB'. This can be achieved with the logic diagram shown in the left side.

Ex- OR Gate diagram



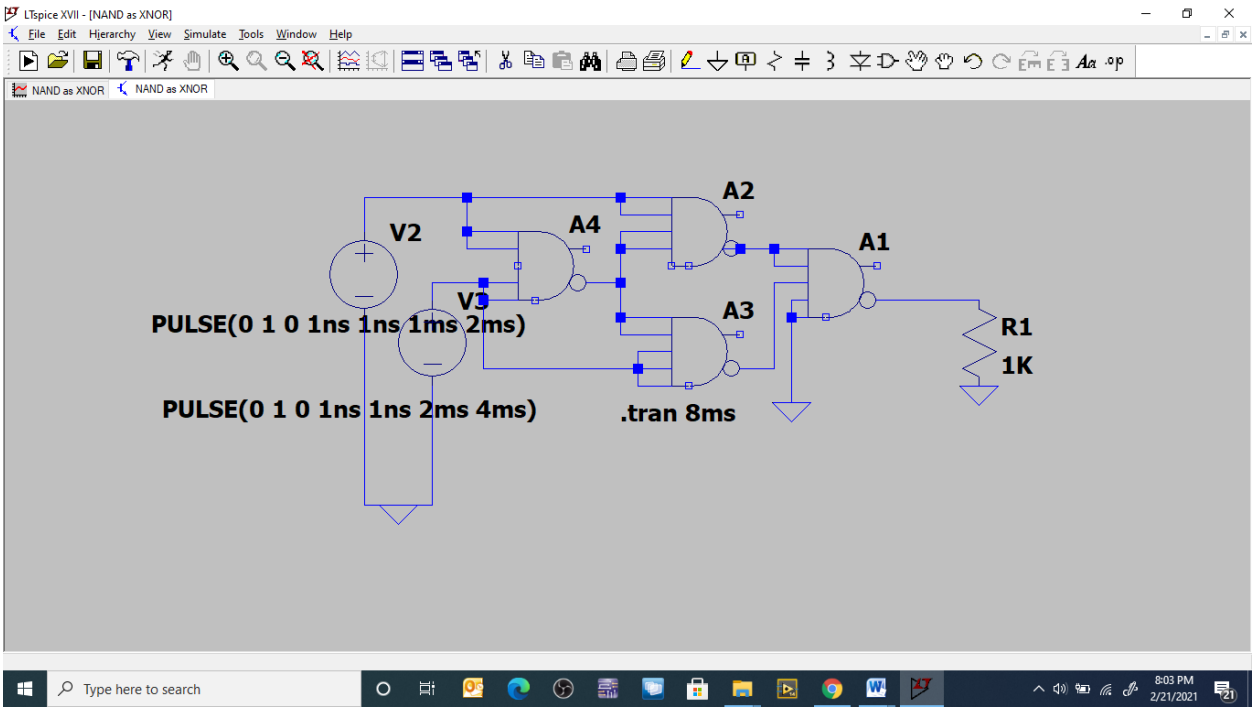
Inputs		Outputs
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

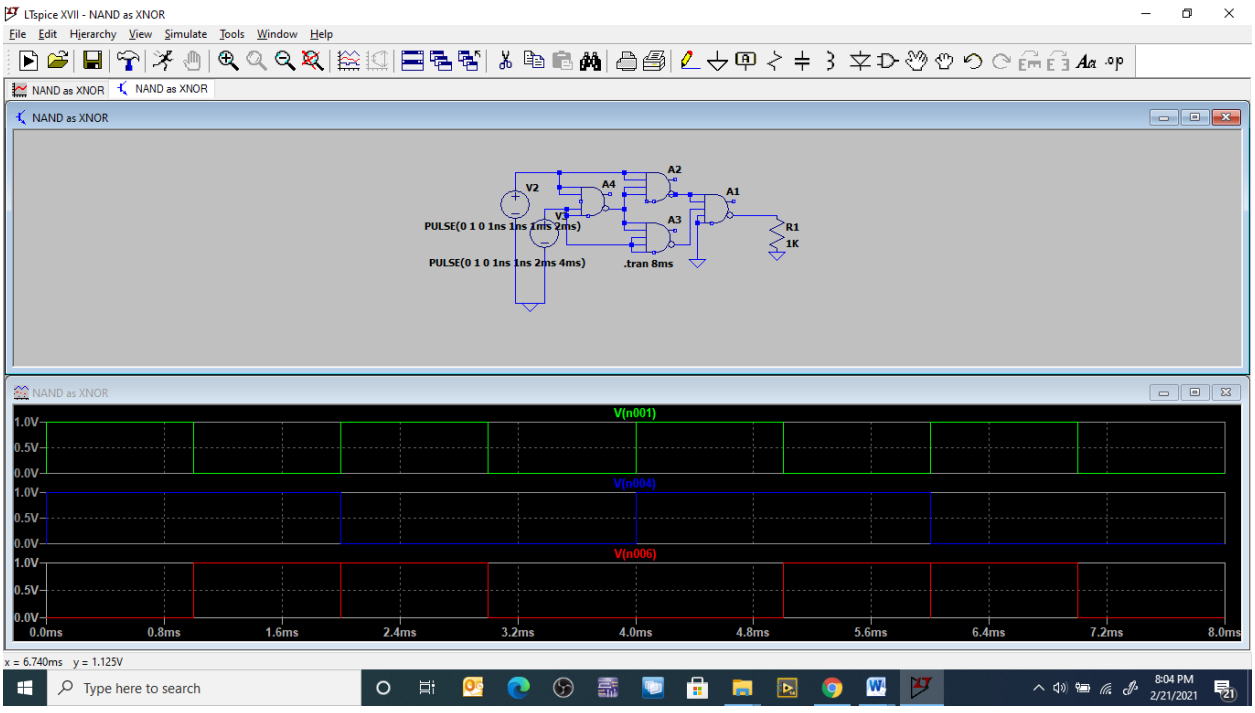
Gate No.	Inputs	Output
1	A, B	(AB)’
2	A, (AB)’	(A (AB)’)’
3	(AB)’, B	(B (AB)’)’
4	(A (AB)’)’, (B (AB)’)’	A’B + AB’

Now the output from gate no. 4 is the overall output of the configuration.

$$Y = ((A\,(AB)')'\,(B\,(AB)')')'$$
$$= (A(AB)'')'' + (B(AB)'')''$$
$$= (A(AB)') + (B(AB)')$$
$$= (A(A' + B)') + (B(A' + B'))$$
$$= (AA' + AB') + (BA' + BB')$$
$$= (\,0 + AB' + BA' + 0\,)$$
$$= AB' + BA'$$

=> $Y = AB' + A'B$

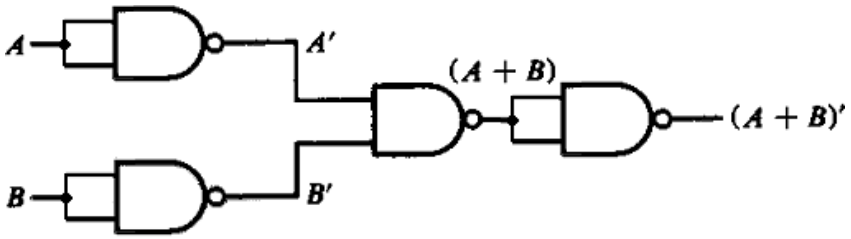




(5) NAND gates as NOR gate

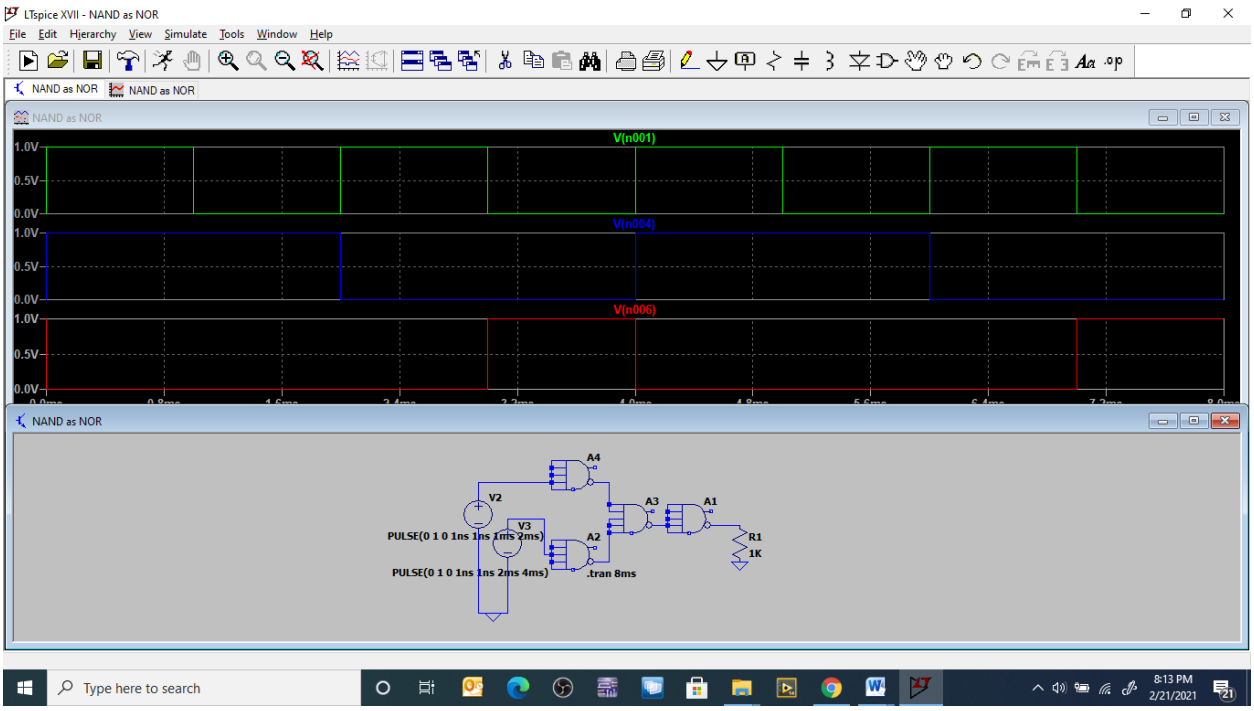
A NOR gate is an OR gate followed by NOT gate. So connect the output of OR gate to a NOT gate, overall output is that of a NOR gate.

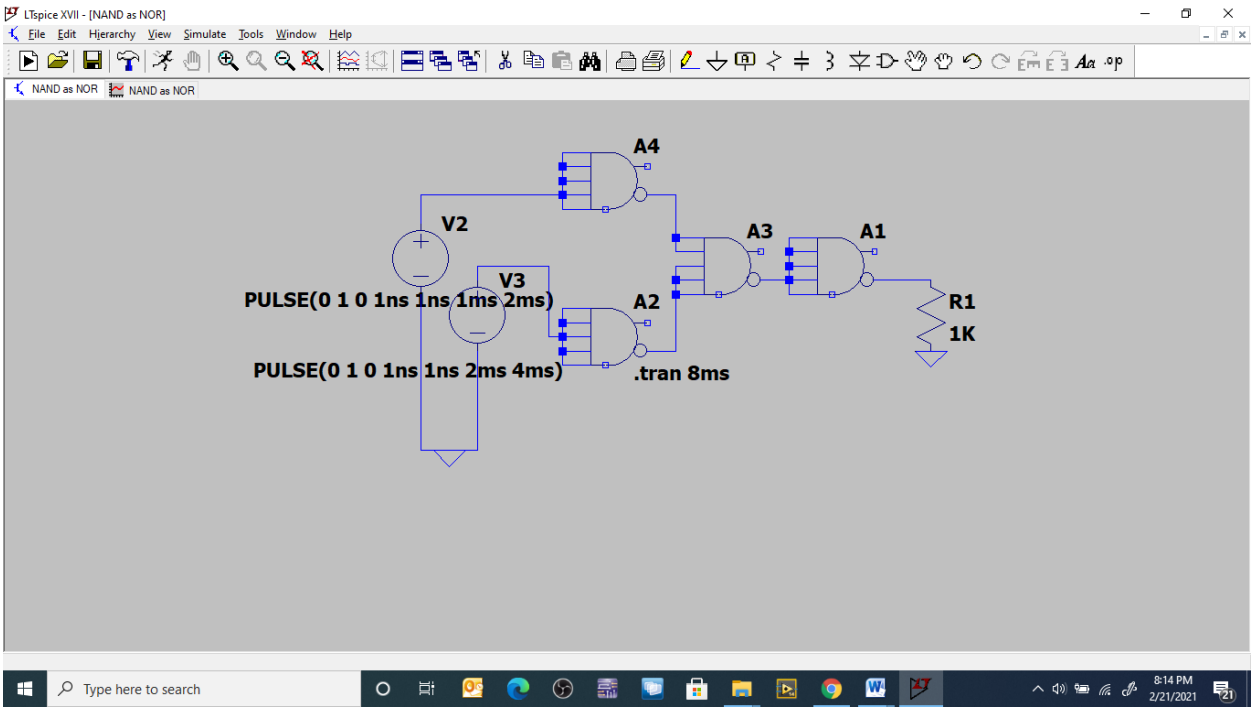
Y = (A + B)'

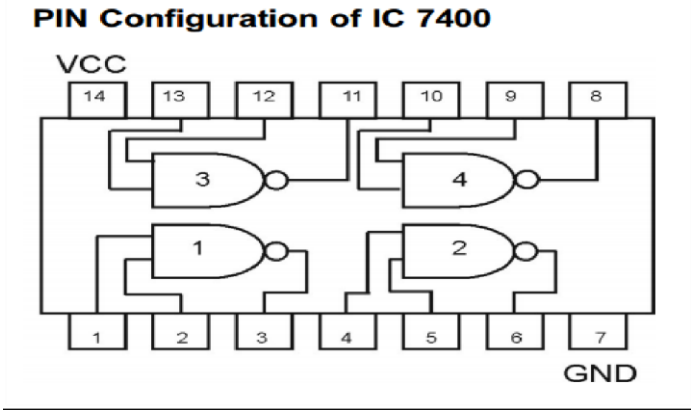


NOR

2 Input NOR gate		
A	B	A+B
0	0	1
0	1	0
1	0	0
1	1	0







Procedure:

1. Connect the trainer kit to ac power supply.
2. Connect the NAND gates for any of the logic functions to be realized.
3. Connect the inputs of first stage to logic sources and output of the last gate to logic indicator.
4. Apply various input combinations and observe output for each one.
5. Verify the truth table for each input/ output combination.
6. Repeat the process for all logic functions.
7. Switch off the ac power supply.

RESULT:

Thus all the gates are verified using NAND gates using LTspice