Design of Arithmetic Logic Circuit using IC's- Half Adder and Full Adder

(Data Processing in Micro-controller Applications)

Aim:

To design, simulate, and verify a half adder and a full adder used in the Arithmetic logic circuit, using ICs.

Software required:

LTspice software

1. Half adder

Theory for Half adder:

Adders form a core component of the Arithmetic Logic Unit (ALU) and play a major role in calculating memory addresses, table indices, etc.

A half adder is the simplest digital adder. It is a combinational circuit that performs the addition of two binary digits. It takes in two input bits, A (addend) and B (augend), and produces two output bits, the sum, and the carry. The truth table for adding two binary digits A and B is shown below:

Truth Table for Half Adder:

A	***B***	***SUM***	***CARRY***
0	*0*	*0*	*0*
0	*1*	*1*	*0*
1	*0*	*1*	*0*
1	*1*	*0*	*1*

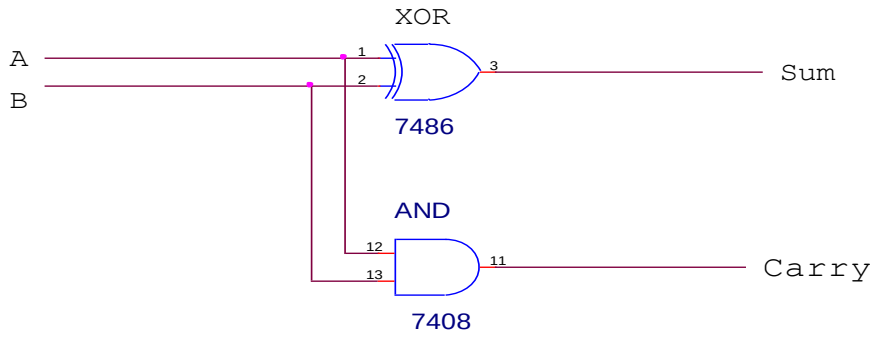
The simplified Boolean functions from the truth table are:

$$SUM = \overline{A}B + A\overline{B}$$

$$CARRY = AB$$

Boolean expressions can be implemented in different ways. Below example shows the implementation of Half Adder using EX-OR and AND logic gates:

Implementation of Half Adder using EX-OR and AND logic gates



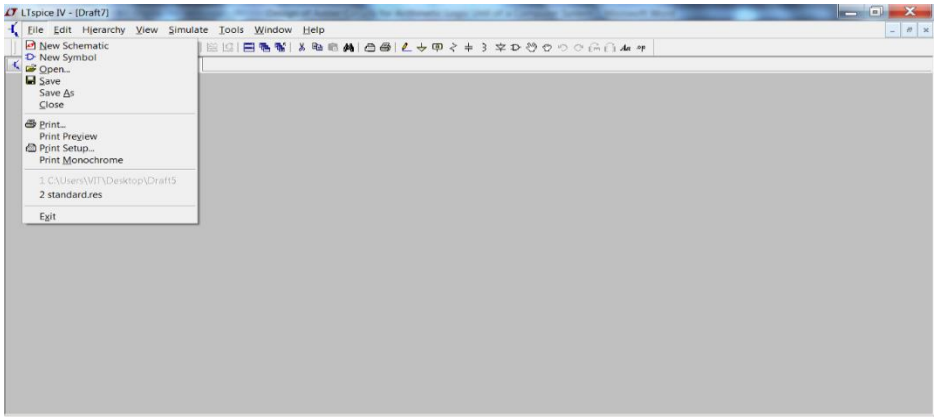
Note: Try alternative ways to implement a Half Adder

a) Using AND-NOR-NOR configuration

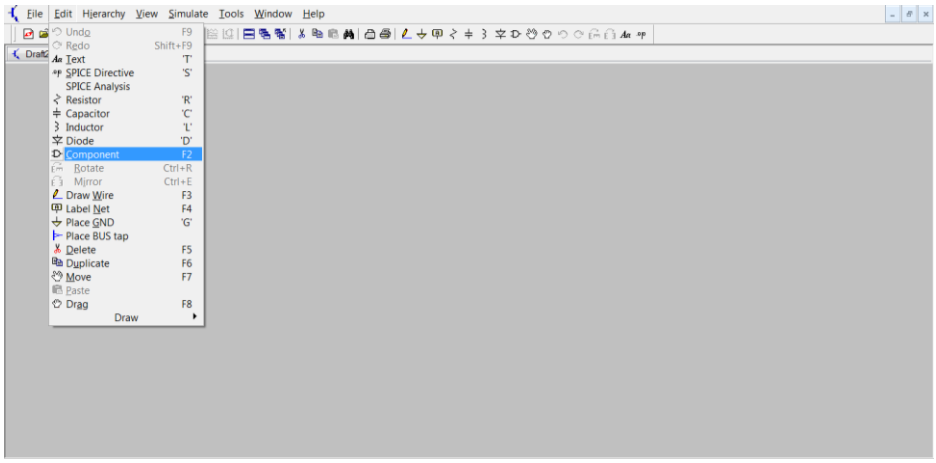
b) Using only AND, OR, and NOT logic

Procedure

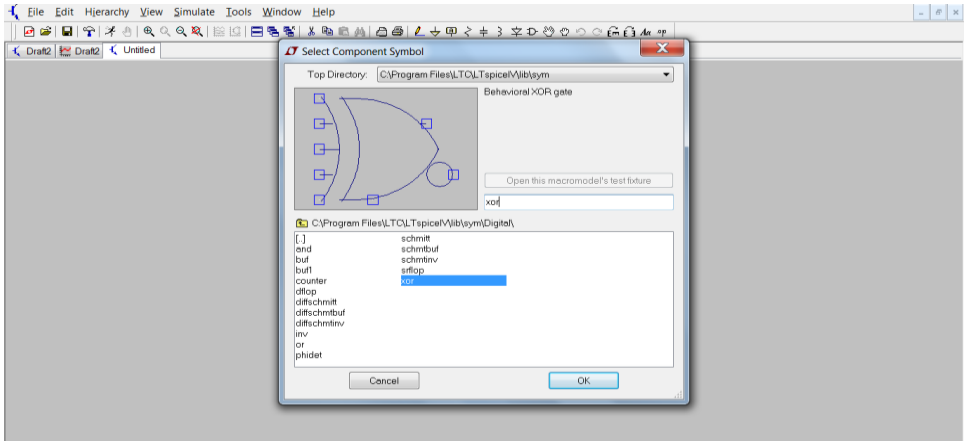
1) Open LTspice. Go to File – New Schematic.

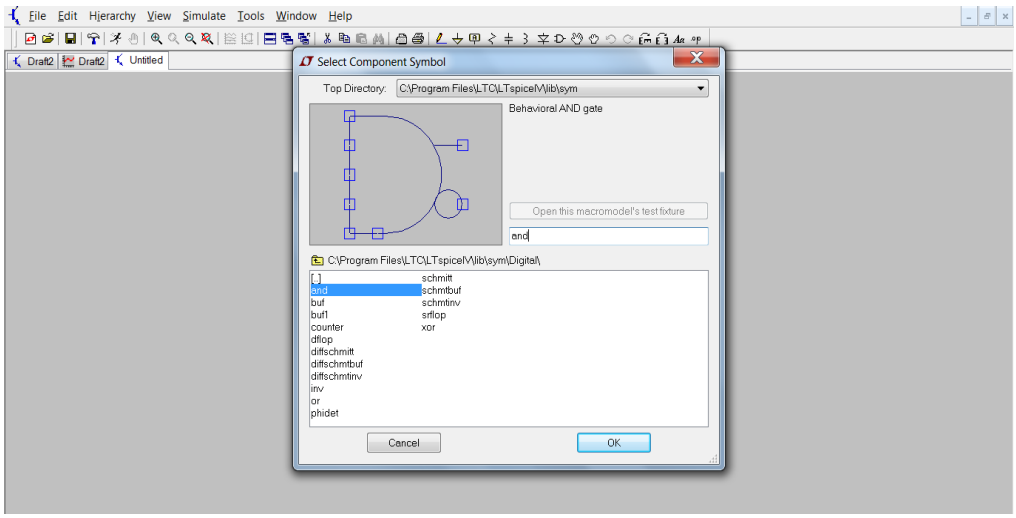


2) On the File Menu, click on Edit – Component.

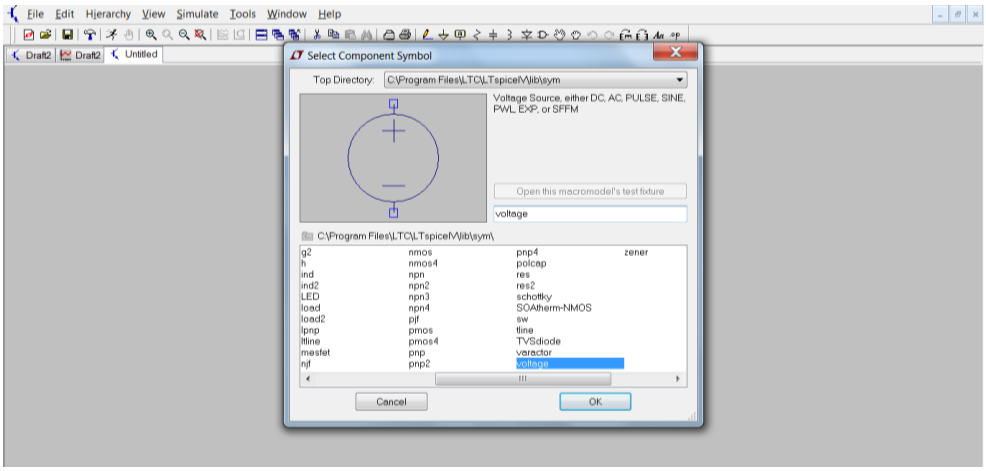


3) Place XOR gate, AND gate, two resistors, and ground on to schematic.

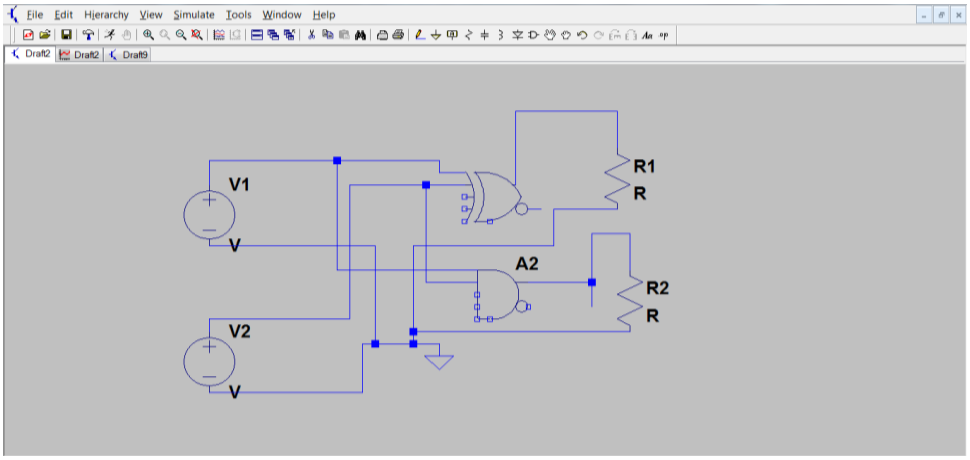




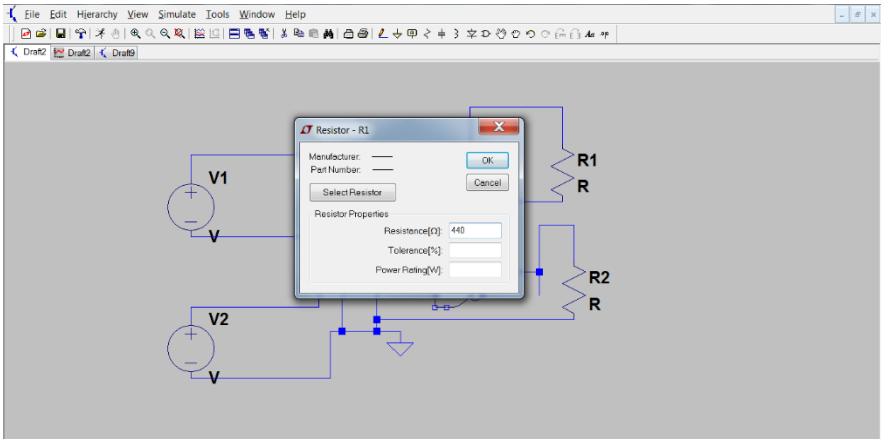
4) Place two voltage sources for the two inputs on the schematic.



5) Make necessary connections as per the circuit diagram. The first resistance is connected to the XOR output. The second resistance is connected to the AND gate output. Common terminal of both resistances are to be grounded. Voltage source 1 – positive terminal acts as 1st input, the other terminal is to be grounded; Voltage source 2 – positive terminal acts as 2nd input, the other terminal is to be grounded.



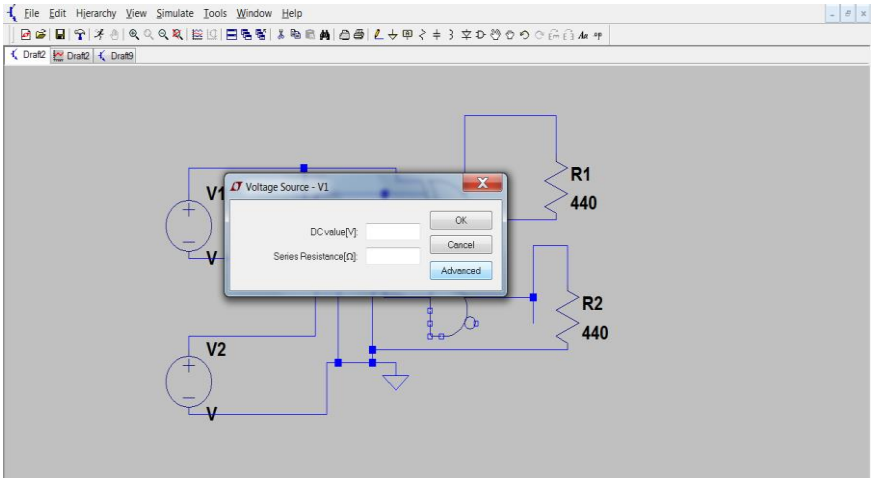
6) Right-click on the resistance and change its value to 440Ω. Repeat the step for the other resistance also.

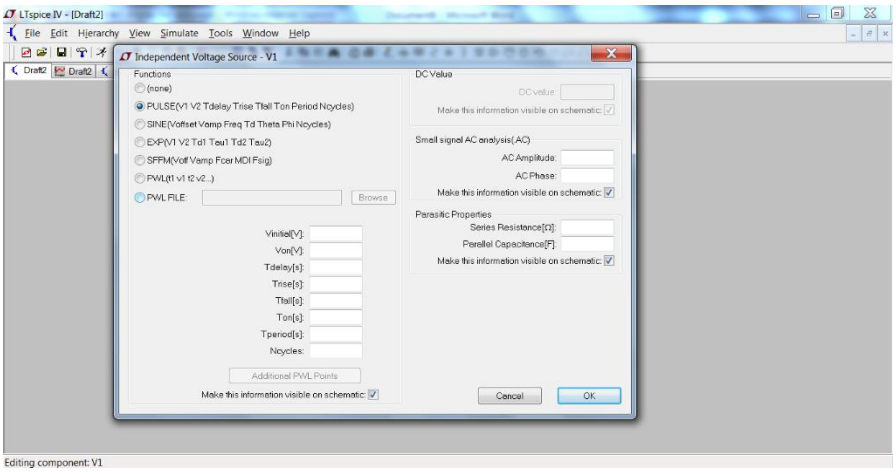


7) Provide input to the XOR gate. Right click on the first voltage source.

Select PULSE (V1 V2 Tdelay Trise Tfall Ton Period Ncycles).

Set the values as (0, 1, 0, 1ns, 1ns, 1ms, 2 ms).

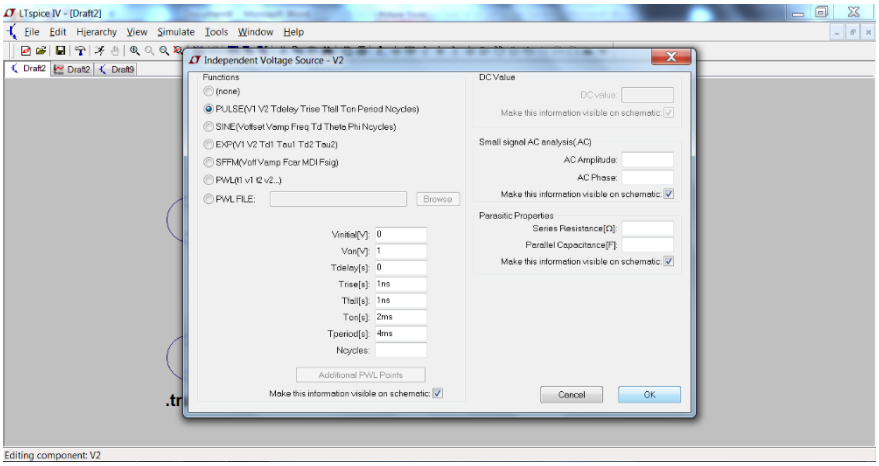


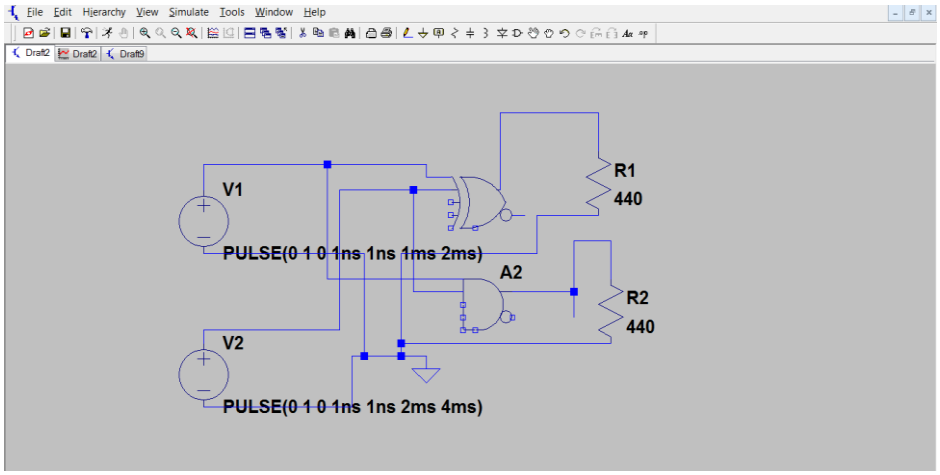


8) Provide input to the AND gate. Right-click on the first voltage source.

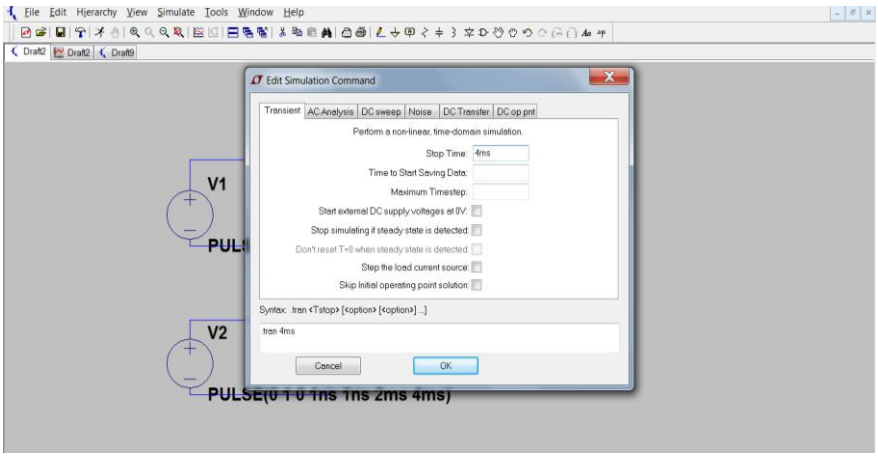
Select PULSE (V1 V2 Tdelay Trise Tfall Ton Period Ncycles).

Set the values as (0, 1, 0, 1ns, 1ns, 2ms, 4ms).





9) Go to Edit – SPICE analysis. Set the stop time to 4 ms

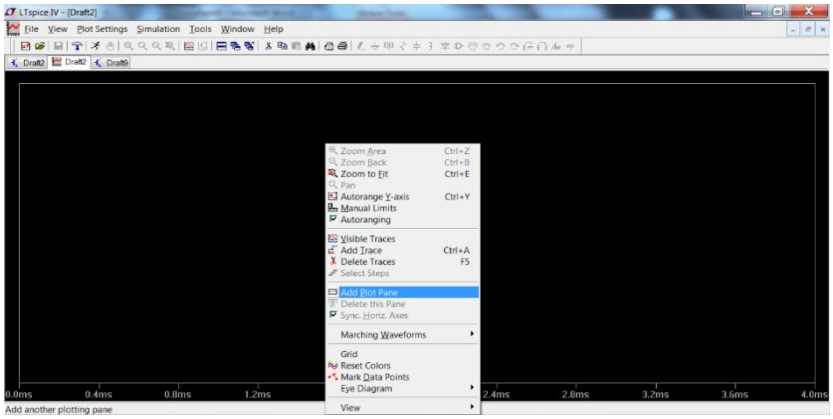


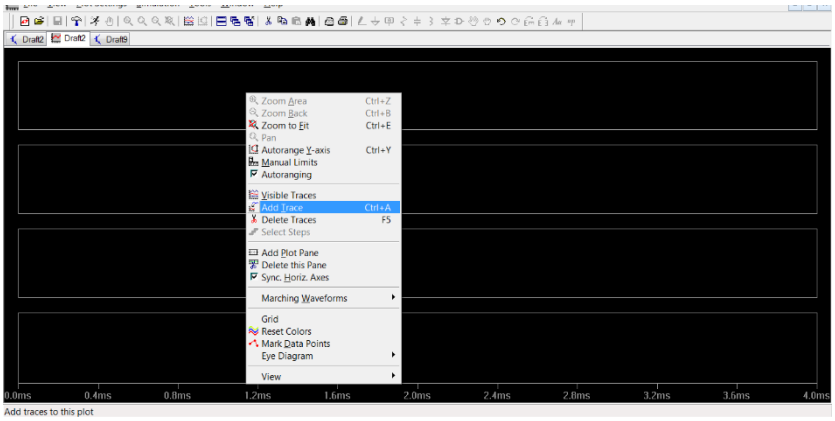
10) Run the simulation (run symbol is available on menu bar).

11) To view the results, right click – Add Plot Pane (add 4 plot panes to view the two inputs, sum and carry).

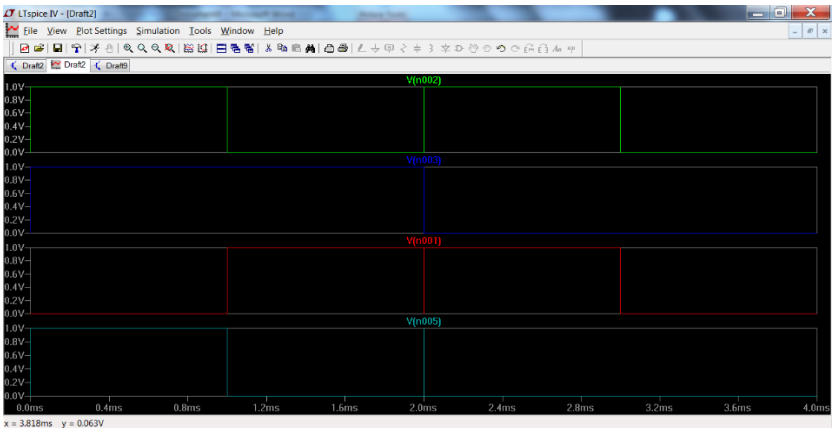
For each pane, right click – Add Trace – Select V (<<respective node>>). Change the background using Tools >> color preferences.

(nodes correspond to input 1, input 2, sum and carry)





12) Observe the waveforms and verify the truth table.



Results and Inferences:

Thus, a half adder circuit to implement addition operation in the ALU circuit using Exclusive-OR and AND gates is designed and its truth table is verified.

Practical Applications:

Data processing in micro-controller.

Course Outcome:

CO4. Design and implement various digital circuits

Student Learning Outcomes (SLO):

SLO2. Having a clear understanding of the subject related concepts and of contemporary issues

2. Full adder circuit:

Theory for Full adder:

Consider the problem of adding two single-bit numbers, A and B, resulting in a single two-bit answer. The truth table for this operation is shown above.

Carry (C)	**1 0 1 1 1 0 0 0**
Input-1 (A)	**1 0 1 1 1 0 0 1**
Input-2 (B)	**1 0 1 0 1 1 0 0**
Sum (S)	**0 1 1 0 0 1 0 1**

Note that, except for the right most columns, we are actually adding three bits: a bit from each of the 2 numbers and a carry bit from the bits immediately to the right. Note also that each addition produces 2 bits - the result bit (S), and the carry bit (C). Now, let's make a truth table for this addition process. The truth table will have three variables, one bit from each of the numbers A and B, and a carry in bit (C_{in}), which represents the carry from the previous position. The two outputs are the sum bit and the carry out bit (C_{out}), which will be used in the next position.

We'll use Karnaugh maps to simplify the two functions in the table above into MSOP form:

C_{in} \ AB	00	01	11	10
0	0	0	1	0
1	0	1	1	1

Carry (C_{out})= A.B+B.C_{in}+C_{in}.A

C_{in} \ AB	00	01	11	10
0	0	1	0	1
1	1	0	1	0

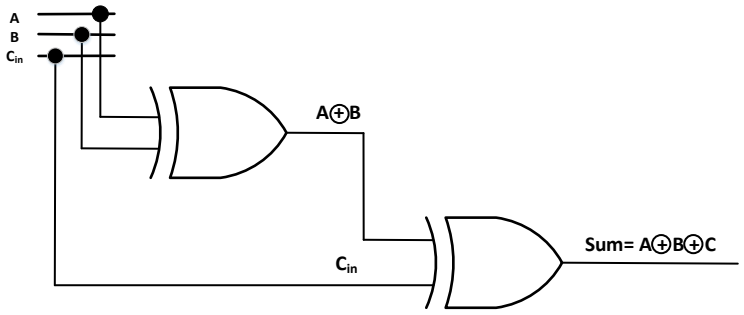
Sum (S) = A'B'C_{in} + AB' C_{in}'+ A'B C_{in}' + AB C_{in}

= A XOR B XOR C_{in}

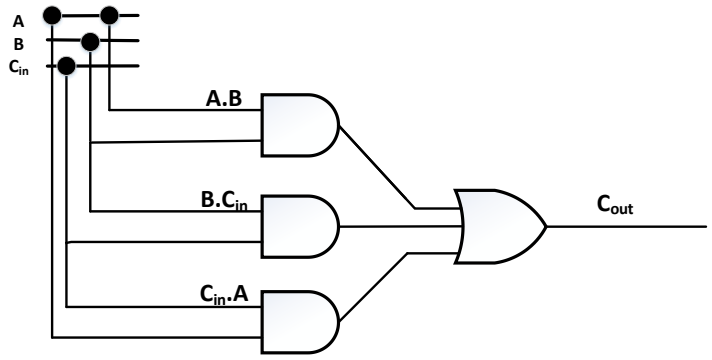
We can implement the function for Carry(C_{out}) and Sum (S) in a straightforward manner, as shown below in logical circuit diagram.

Logical Diagram and Truth Table for full adder:

1. **Logical Diagram for Realizing a Sum:**



2. ***Logical Diagram for Realizing a Carry:***

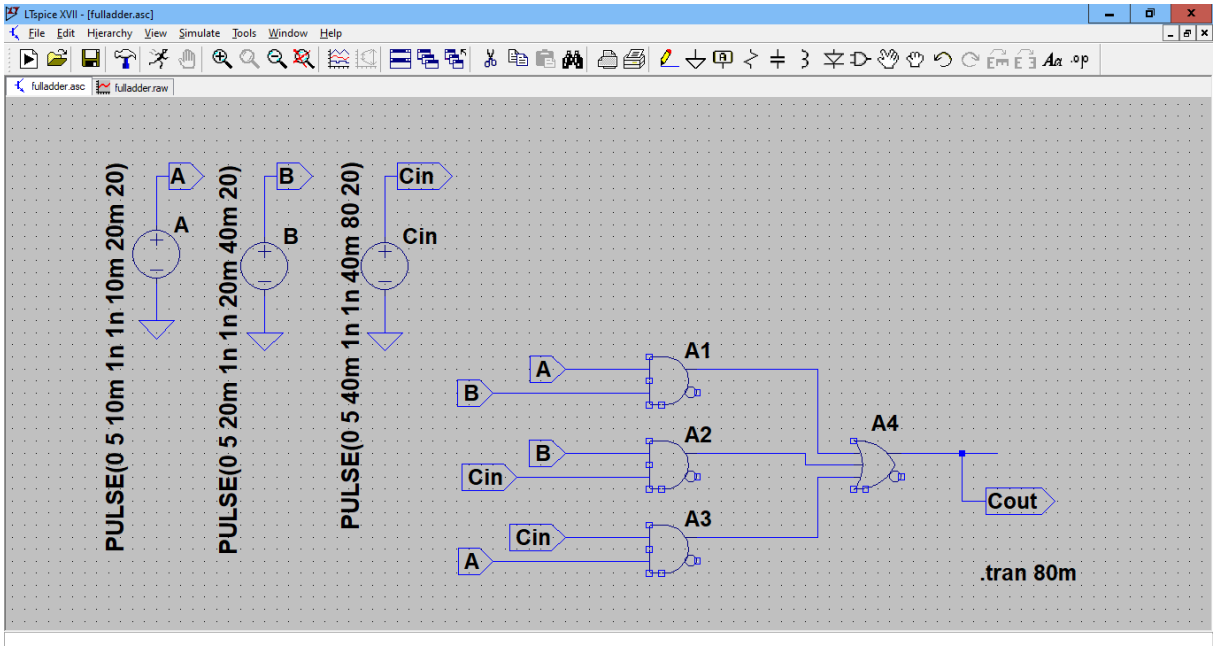


3. ***Observation Truth Table of Full adder:***

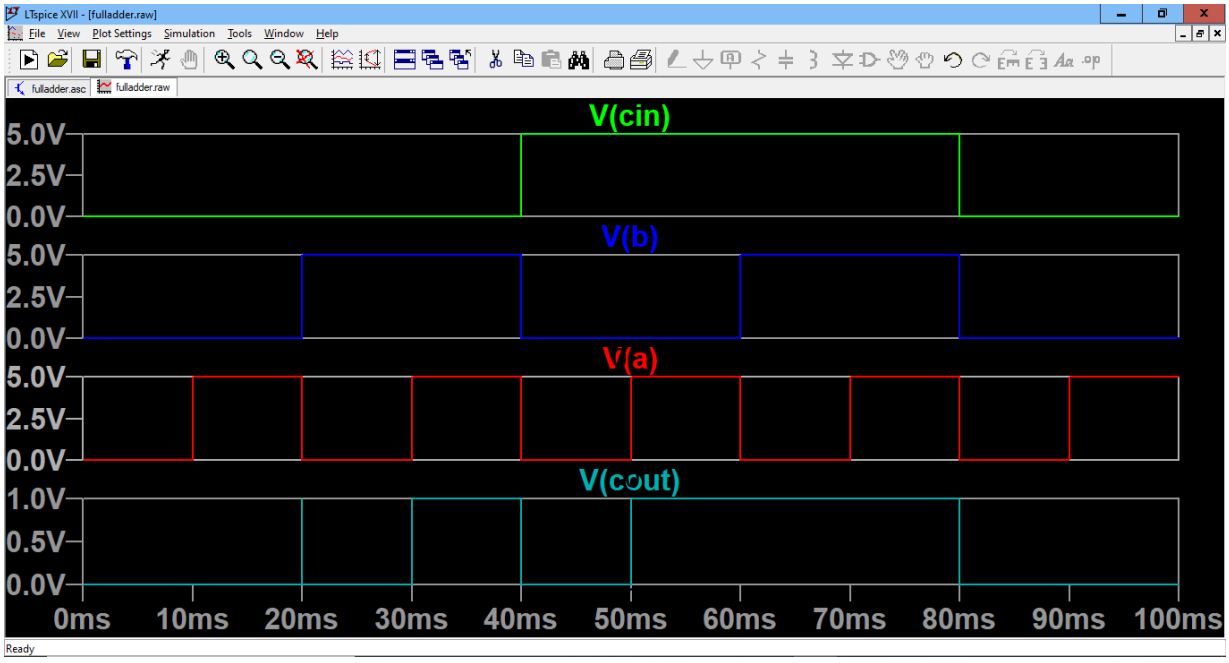
C_{in}	A	B	SUM (S)	CARRY (C_{out})
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

LTSPICE diagram and Waveforms

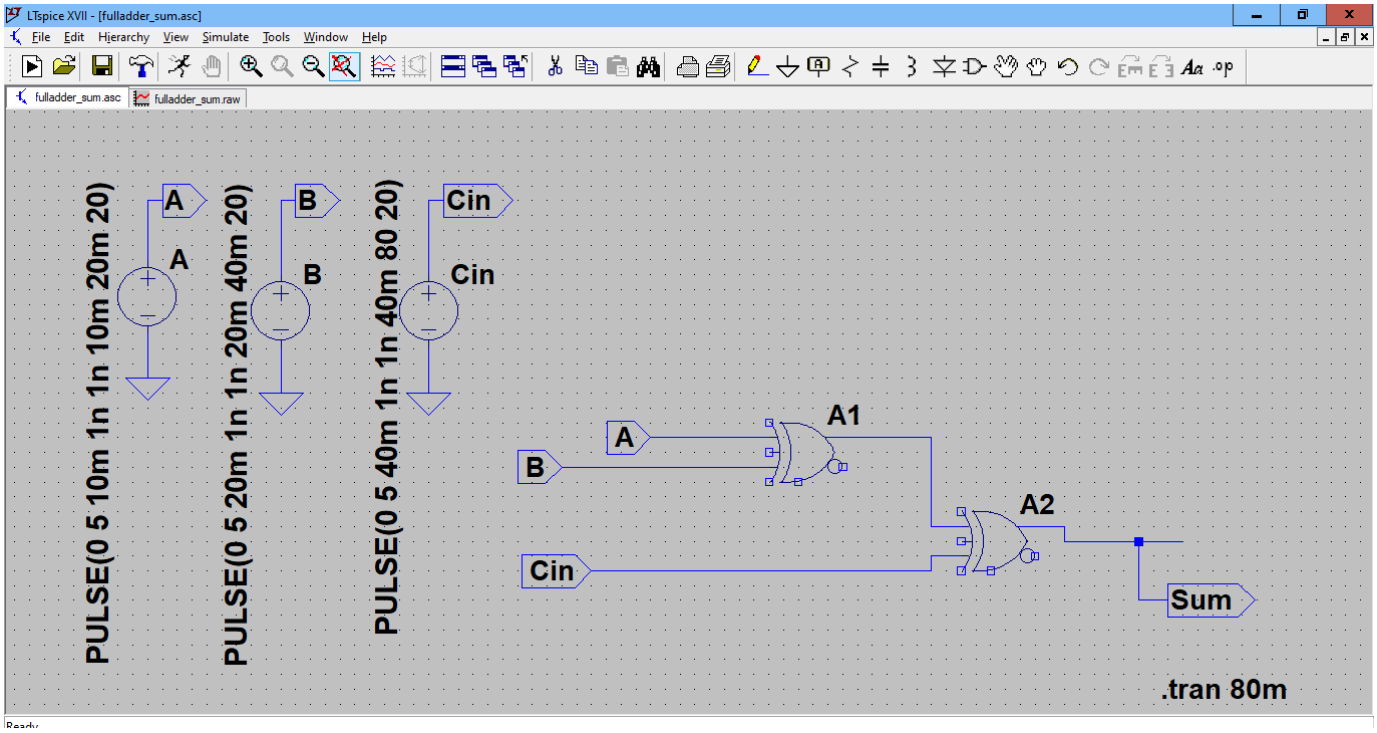
4. **LTSPICE Window to realize C_{out}**



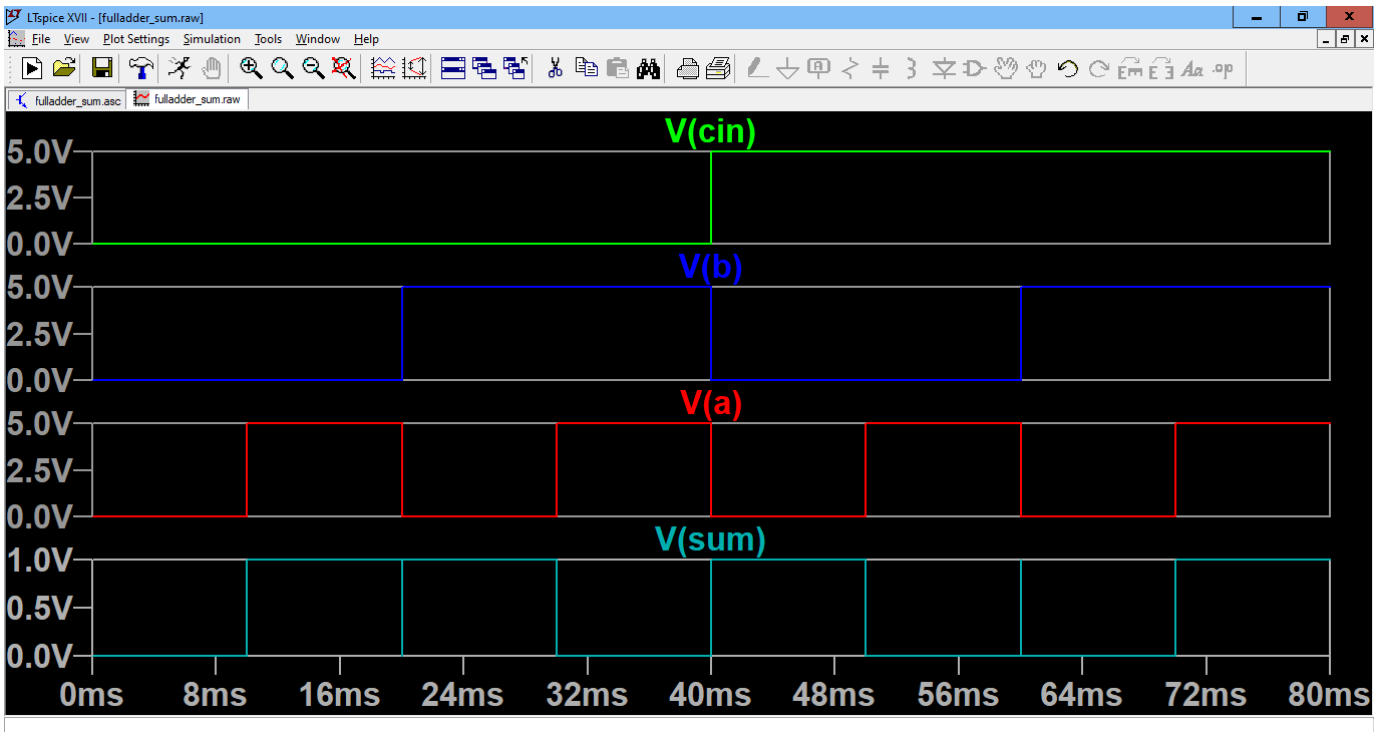
5. LTSPICE Window to realize C_{out} waveform.



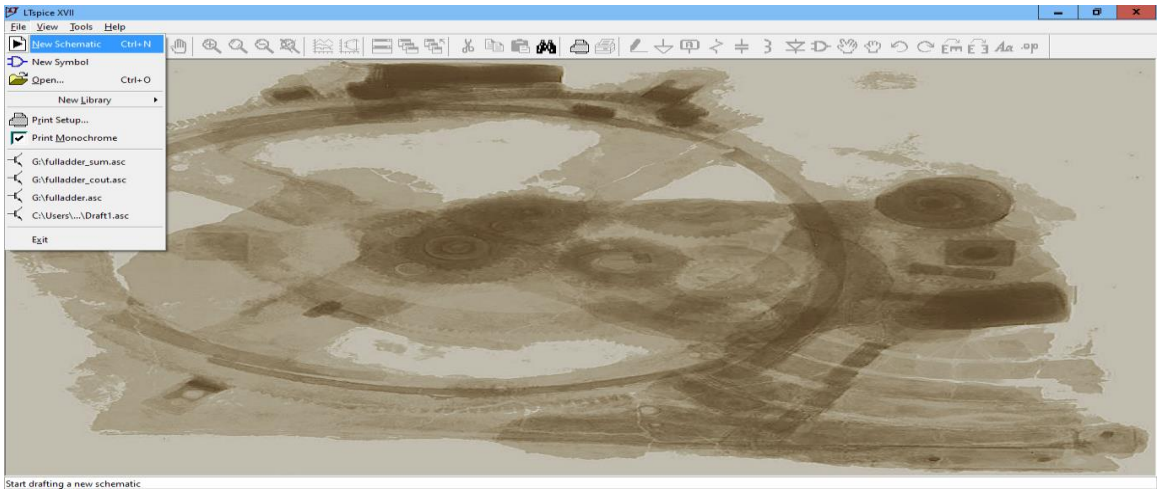
6. **LTSPICE Window to realize Sum(S)**



7. LTSPICE Window to realize Sum waveform.

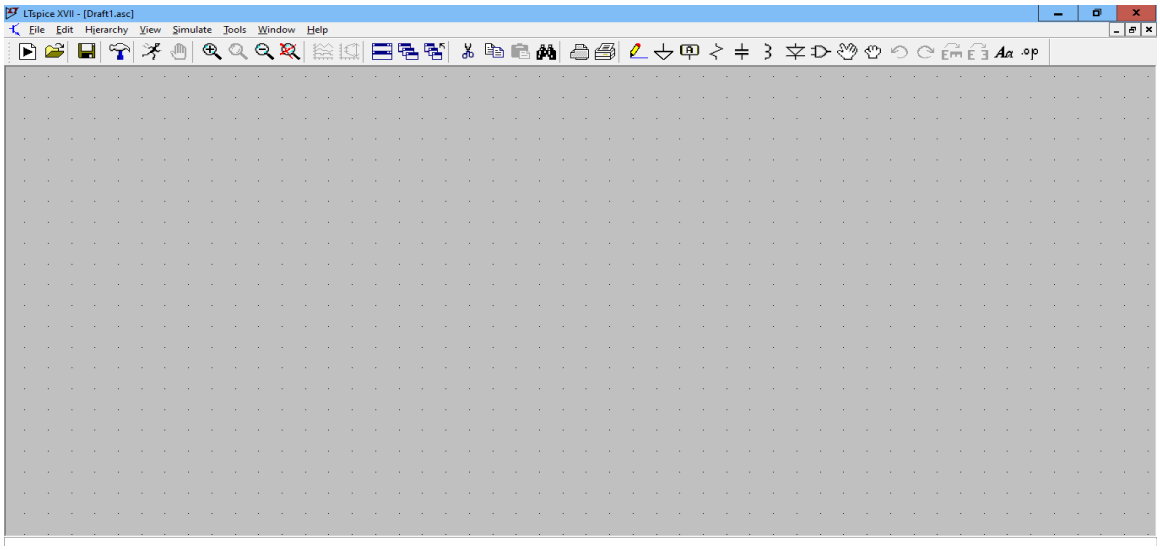


Procedure

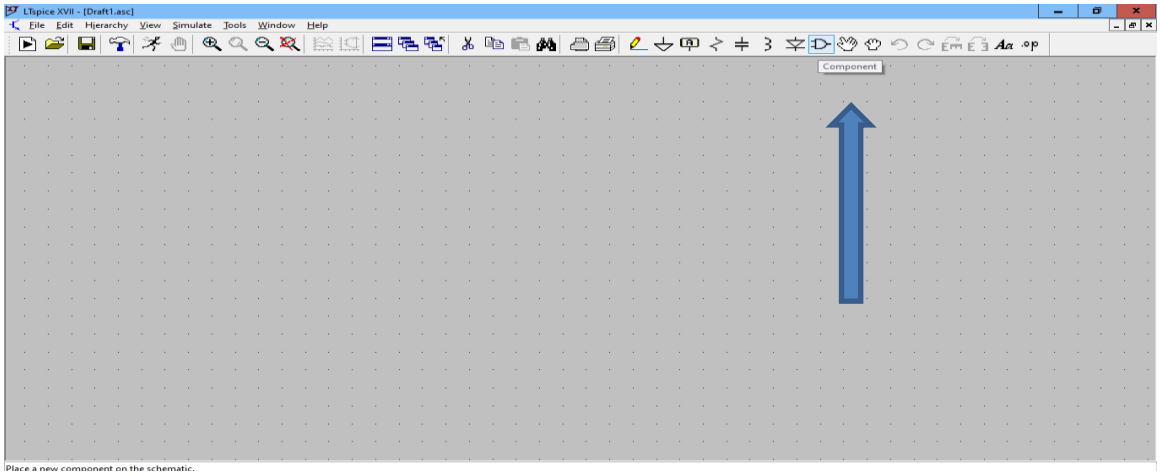


1. Open the LTSpice.exe to get the new schematic.

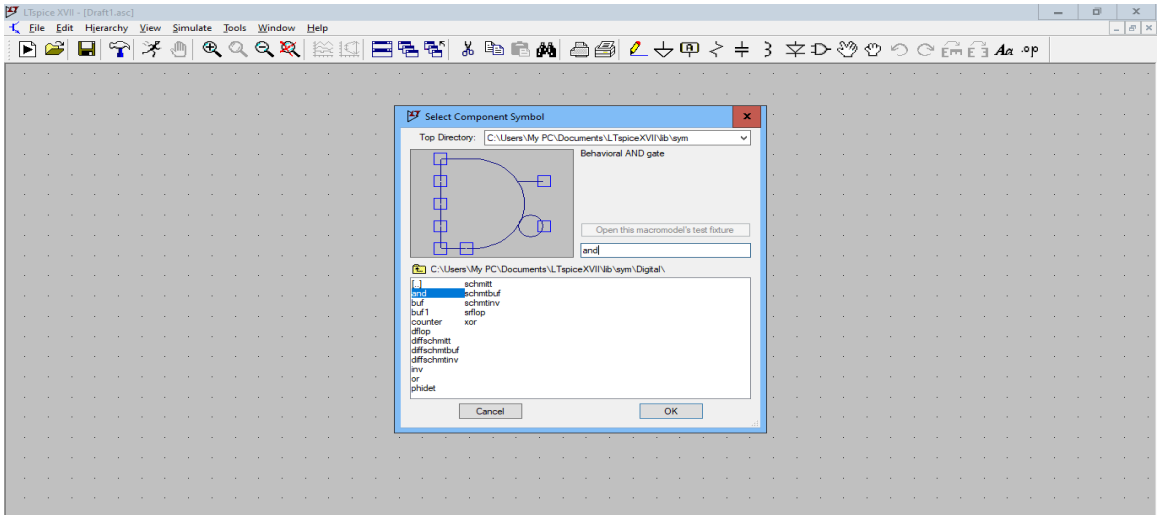
2. A New Draft1.asc schematic is opened



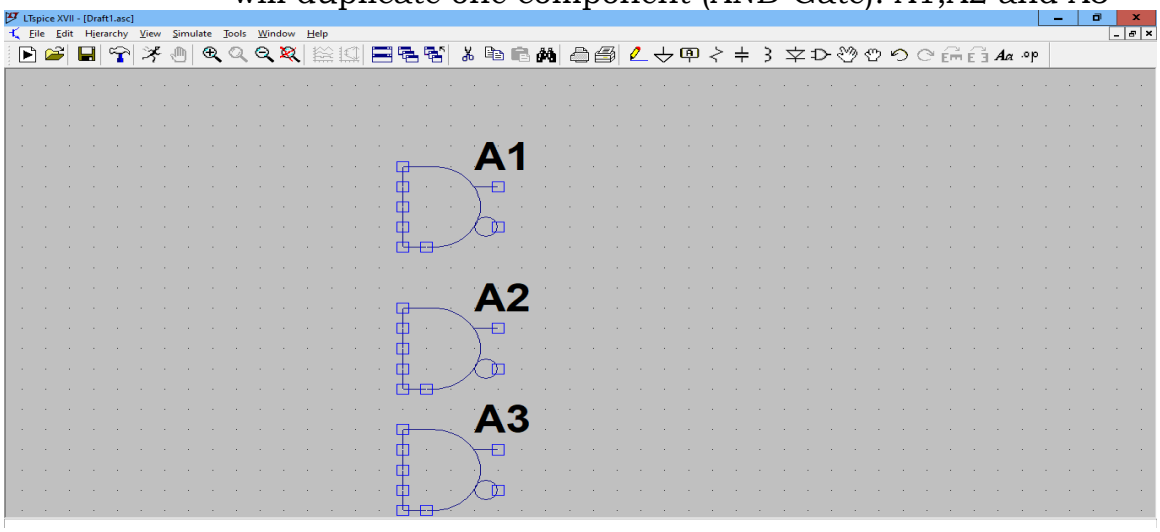
3. Click the component Menu



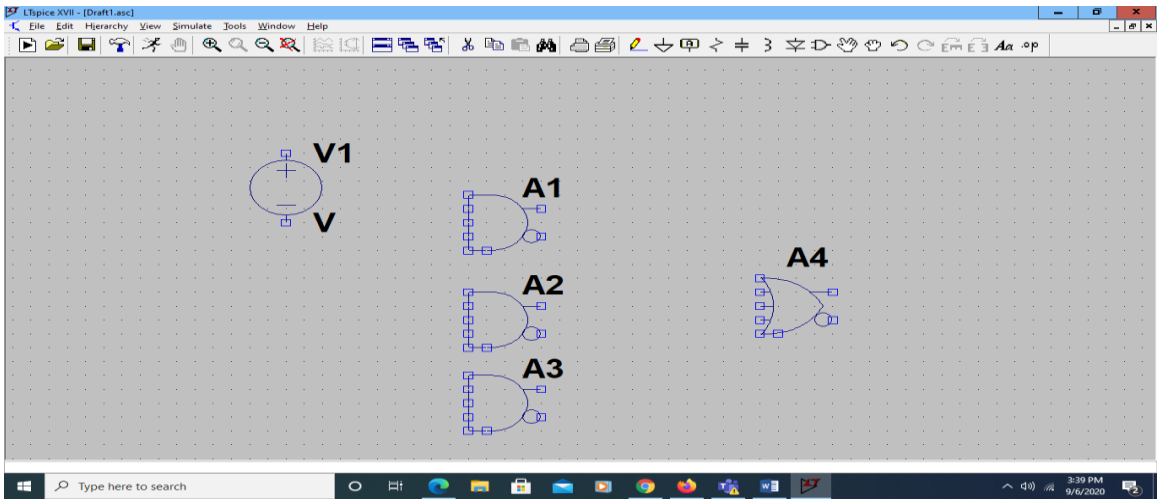
4. Type in the “Select Component Symbol” as AND to get the AND gate .Click Ok



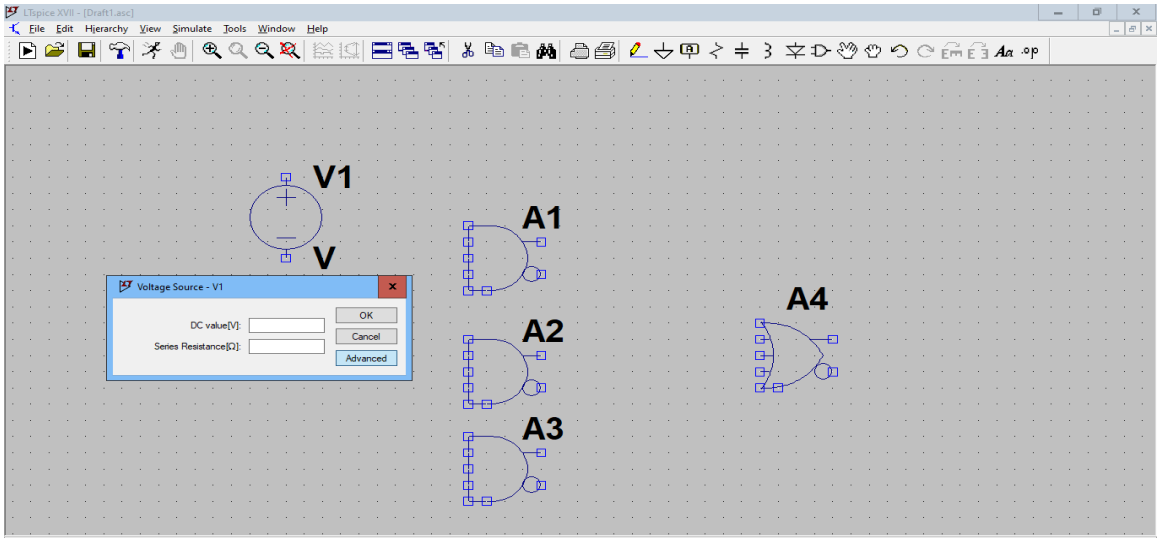
5. Drag it to the Schematic window. Each click in the Schematic will duplicate one component (AND Gate): A1,A2 and A3



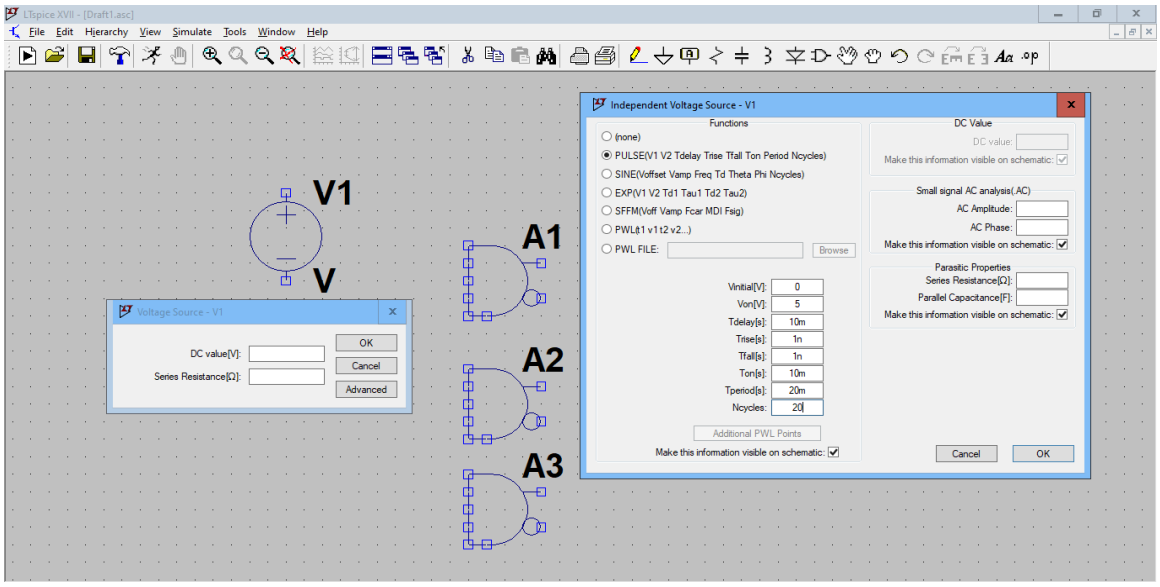
6. Similarly drag the OR gate (A4) and voltage source (V1)



7. Right-click the voltage source(V1) and click the Advanced icon to configure it.

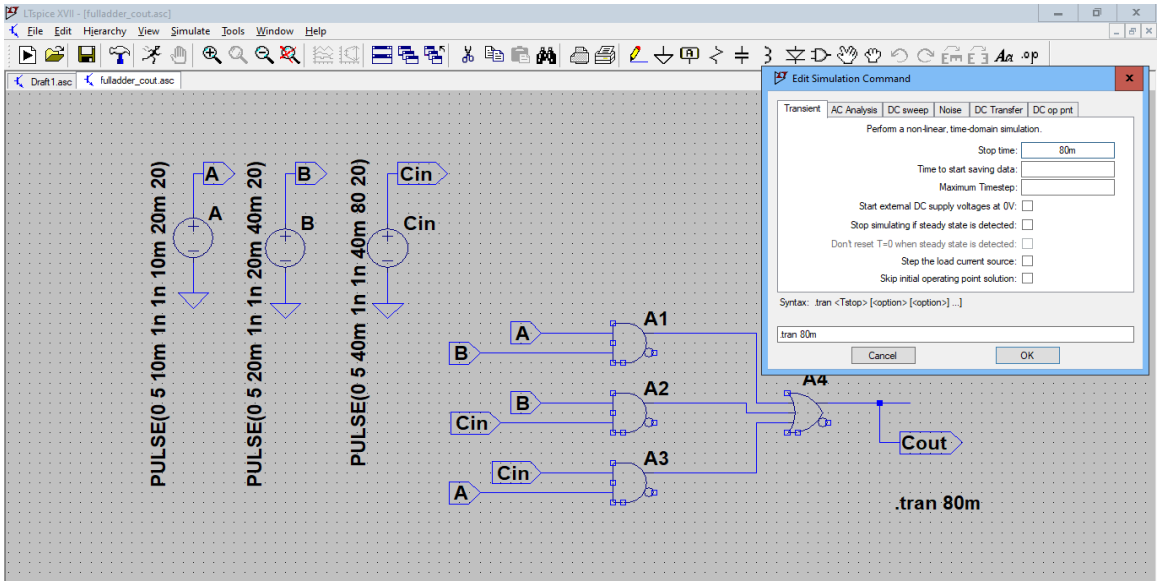


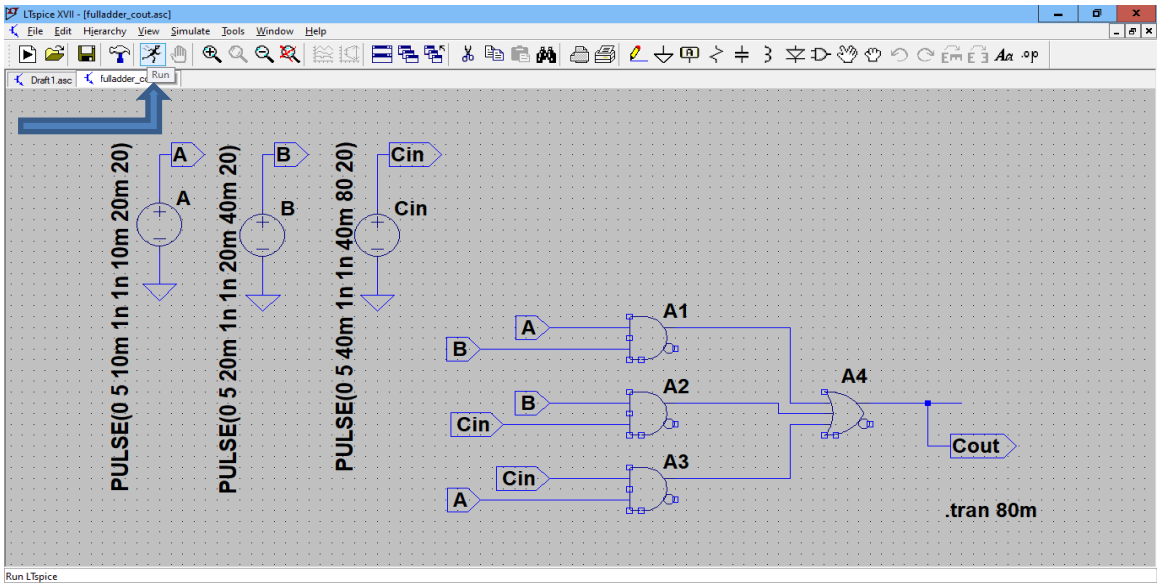
8. Select the Pulse Function and the initial values as shown below



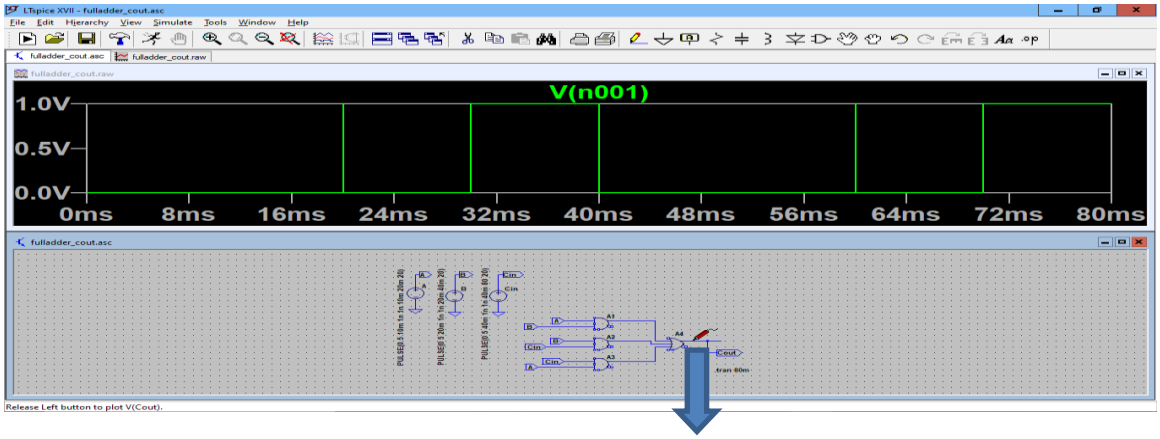
9. Connections are given as per the logic diagram Fig.4. LTSPICE Window to realize Cout**.** Click Simulate----------> Edit Simulation Cmd to set the simulation configuration as shown below. Set the transient menu Stop time as 80m in seconds

10. Click the Run icon to start the simulation.



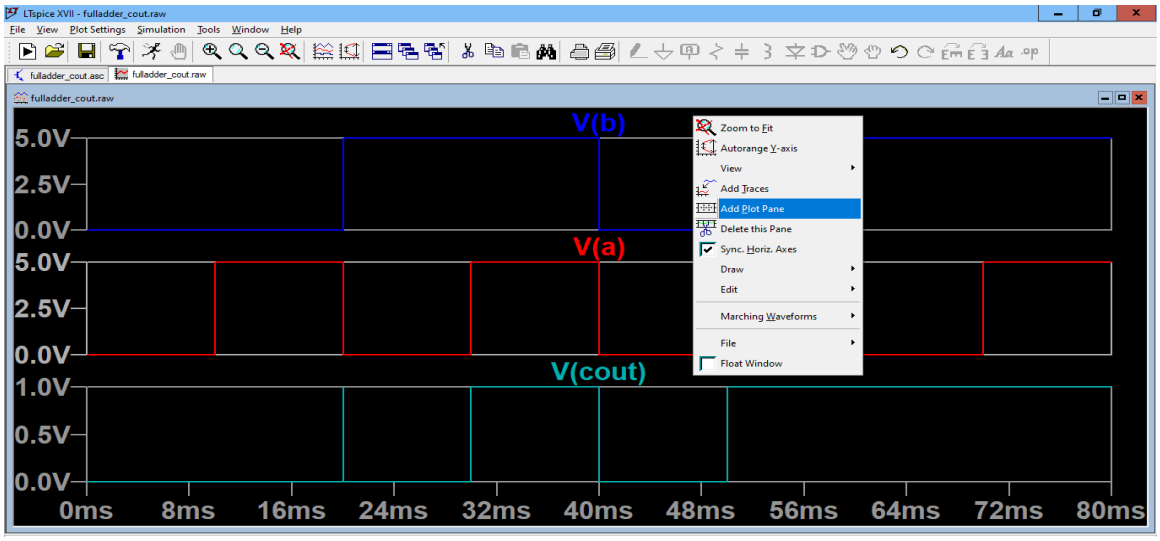


11.Click on the plot plane and simulate icon to get the voltage probe (red



colour)

12. Include more plot pane as follows.



13. Apply the inputs and verify the truth table for the full adder circuit as shown in figure 4, Figure 5, Figure 6 and Figure 7.

Results and Inferences:

Thus the design and verification of the truth table for the Full Adder circuit using Integrated circuits with open source software LTSPICE were done.

Practical Applications:

1. It is used in Digital Processors
2. ALU in computers and varieties of calculators
3. Different IC and microprocessor chips in PCs and laptops
4. In Ripple counters
5. An important tool in DSP (Digital Signal Processing)
6. The 74LS83 is a practical high-speed 4-bit fuller Adder IC with carry out feature.

Course Outcome:

CO4. Design and implement various digital circuits

CO6. Design and conduct experiments to analyze and interpret data

Student Learning Outcomes (SLO):

SLO2. Having a clear understanding of the subject related concepts and of contemporary issues