Asynchronous Counter:

If the flip-flops do not receive the same clock signal, then that counter is called as Asynchronous counter. The output of system clock is applied as clock signal only to first flip-flop. The remaining flip-flops receive the clock signal from output of its previous stage flip-flop. Hence, the outputs of all flip-flops do not change affect at the same time. Another name for Asynchronous counters is "Ripple counters". A digital counter is a set of flip flop. In ripple counter, the first flip-flop is clocked by the external clock pulse & then each successive flip-flop is clocked by the Q or Q' output of the previous flip-flop. Therefore, in an asynchronous counter the flip-flops are not clocked simultaneously.

For a 3-bit asynchronous DOWN counter, the clock inputs of all flip flops are cascaded and the D input (DATA input) of each flip flop is connected to logic 1. That means the flip flops will toggle at each active edge (positive edge) of the clock signal. This counter will count numbers from 7 to 0, downwards. The clock input is connected to first flip flop. The other flip flops in counter receive the clock signal input from Q output of previous flip flop, rather than Q' output. Here Q0, Q1, Q2 represents the count of the 3-bit down counter. The output of the first flip flop will change, when the positive edge of clock signal occurs.

Excitation Table: - The tabular representation of the operation of D flip flop:

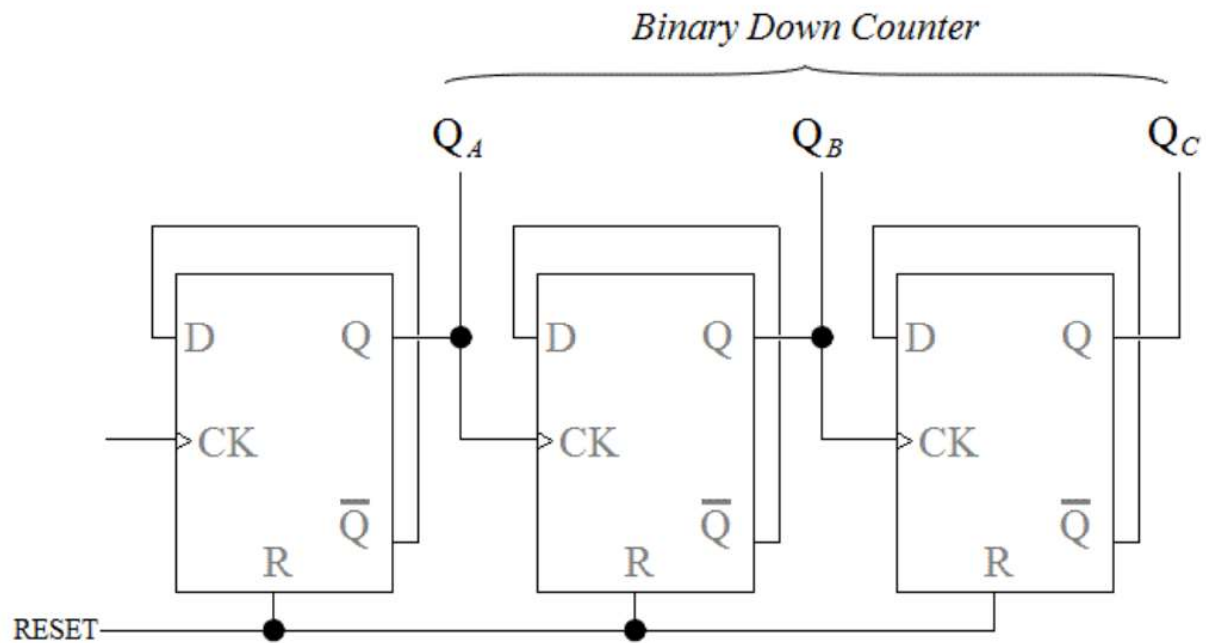| D	Present state Q_n	Next state Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Truth table of D flip flop

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Excitation table of D flip flop

Logic Diagram for Asynchronous Counter:

3 Bit Binary Down Counter using D Flip Flops

Binary Down Counter

Q_A Q_B Q_C

D	Q		D	Q		D	Q
CK			CK			CK	
	$\overline{Q}$			$\overline{Q}$			$\overline{Q}$
R			R			R	

RESET

State Table for 3-bit Asynchronous Counter (for down count):

Counter State	Q_2	Q_1	Q_0
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

Simulation Results:

3-bit Asynchronous Down Counter using D flip-flops
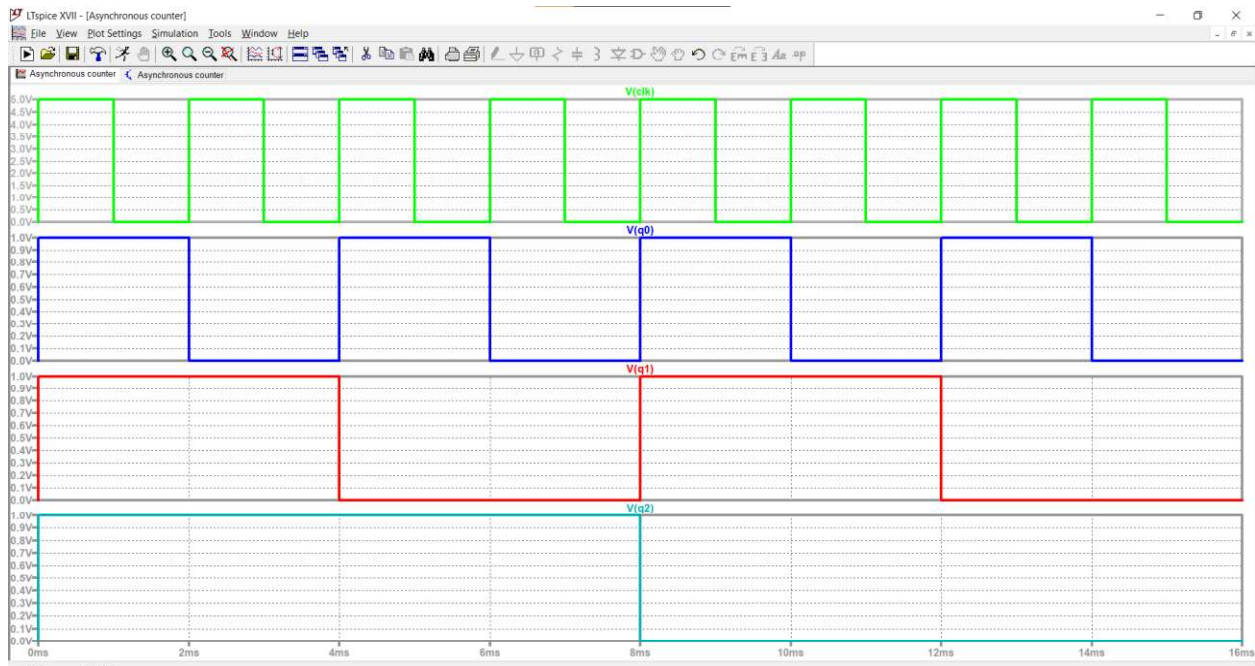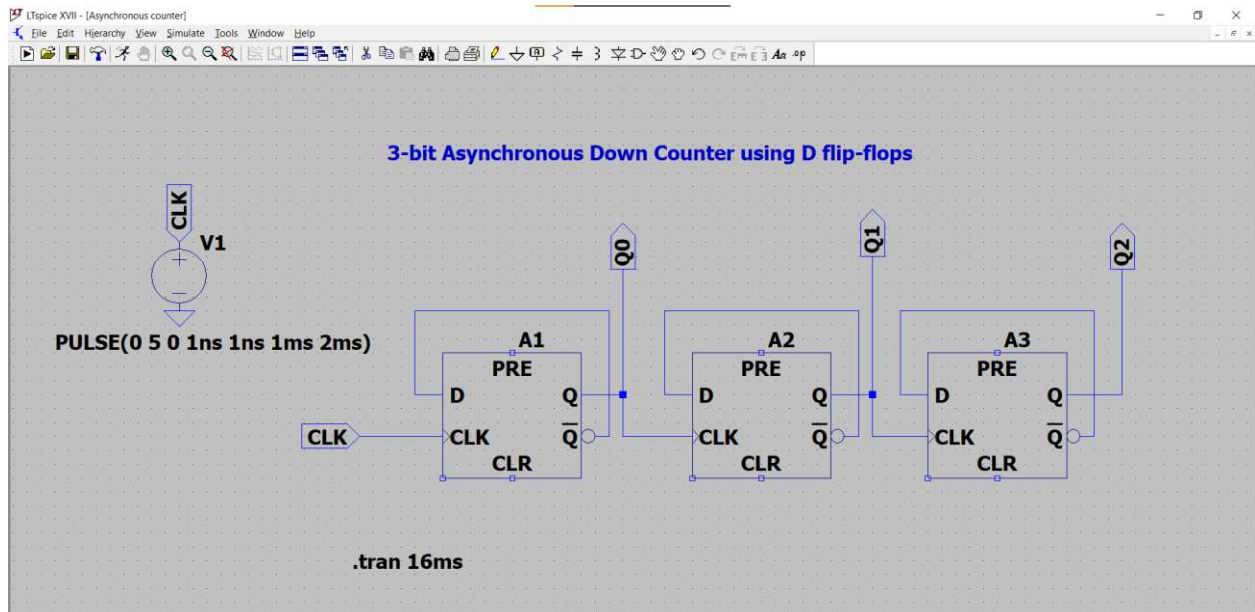
Results and Inferences:

Thus, asynchronous counter circuit is implemented for down count operation for low noise emission applications using D flip flops.