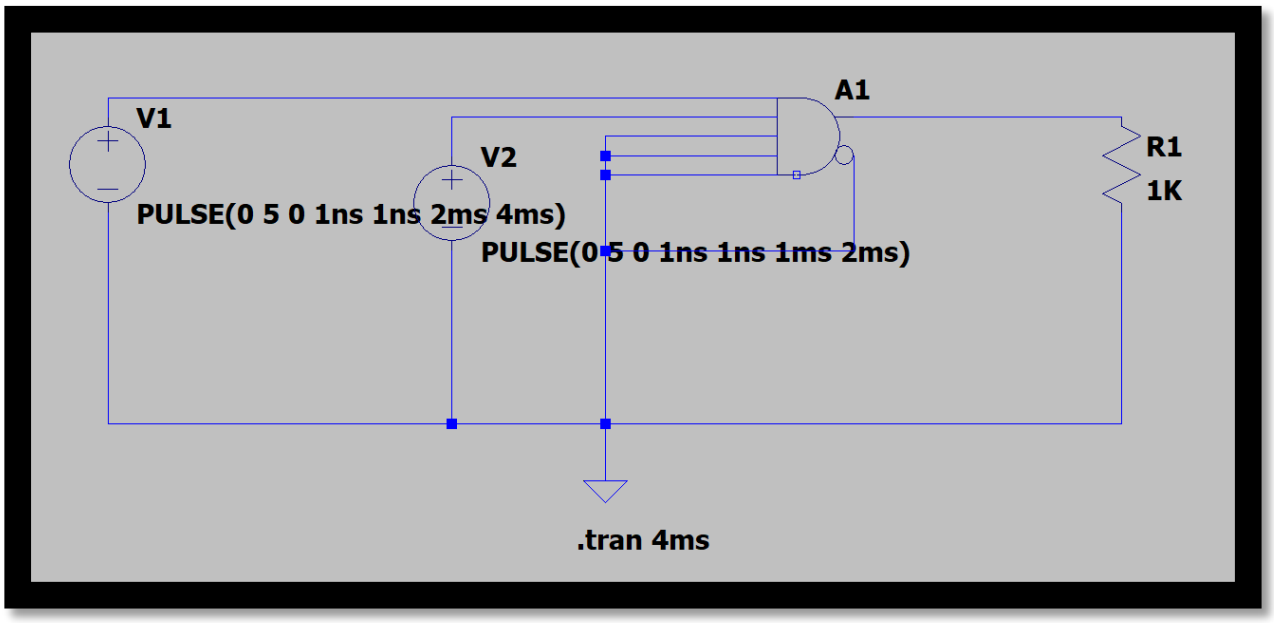
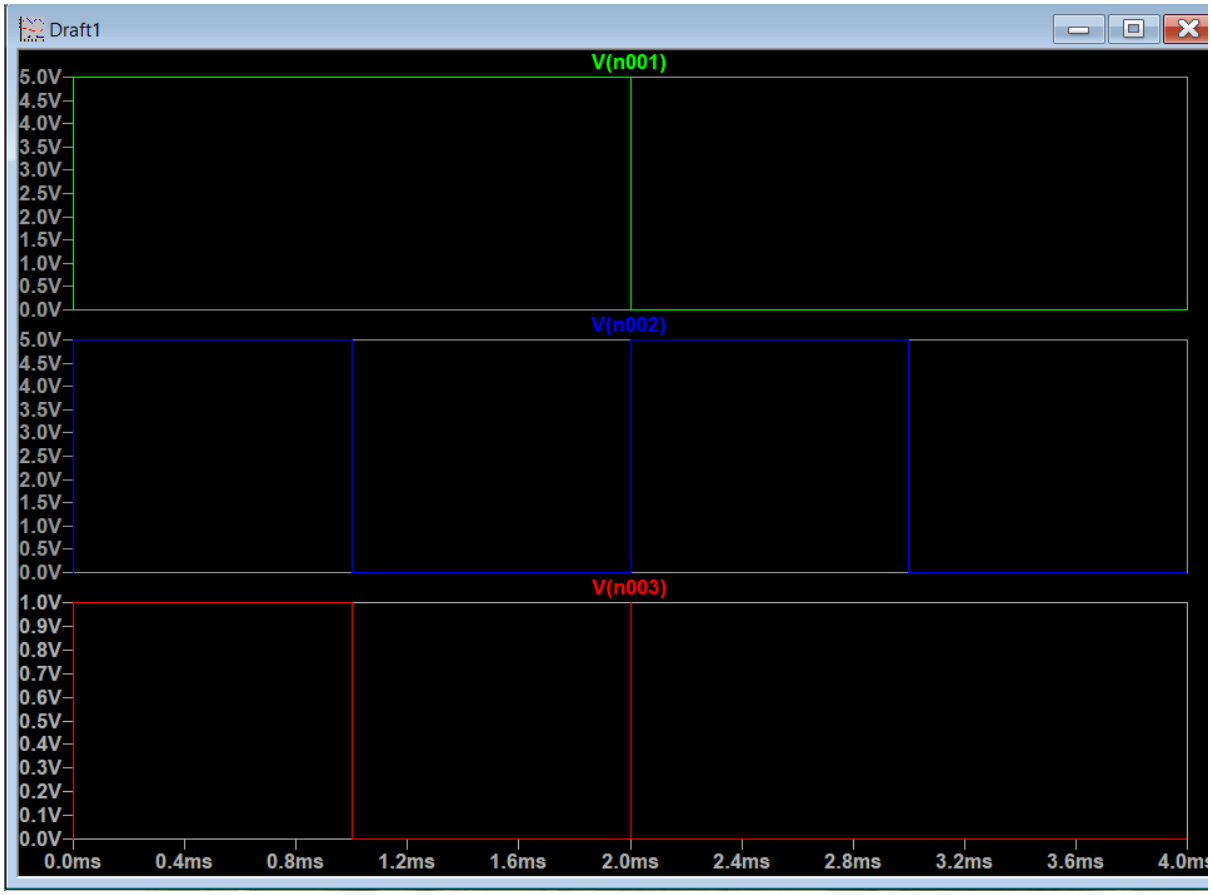
CSE1003-LAB

AND GATE

DIAGRAM

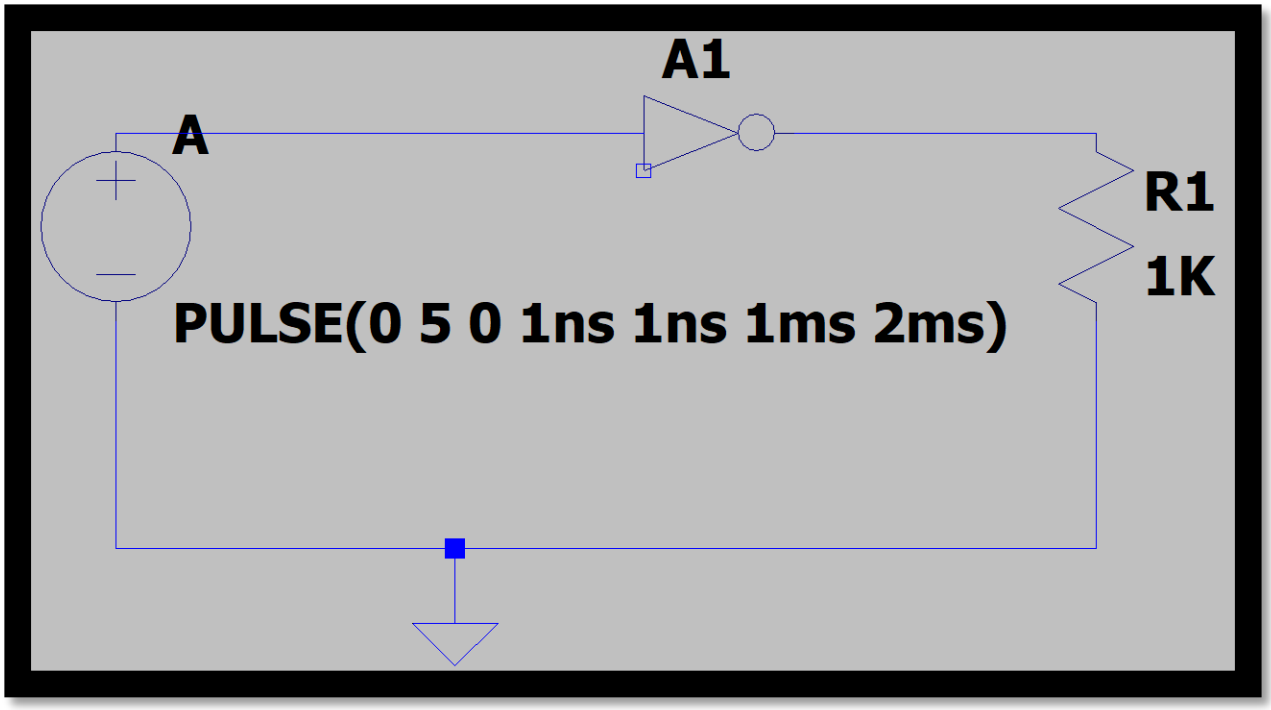


OUTPUT

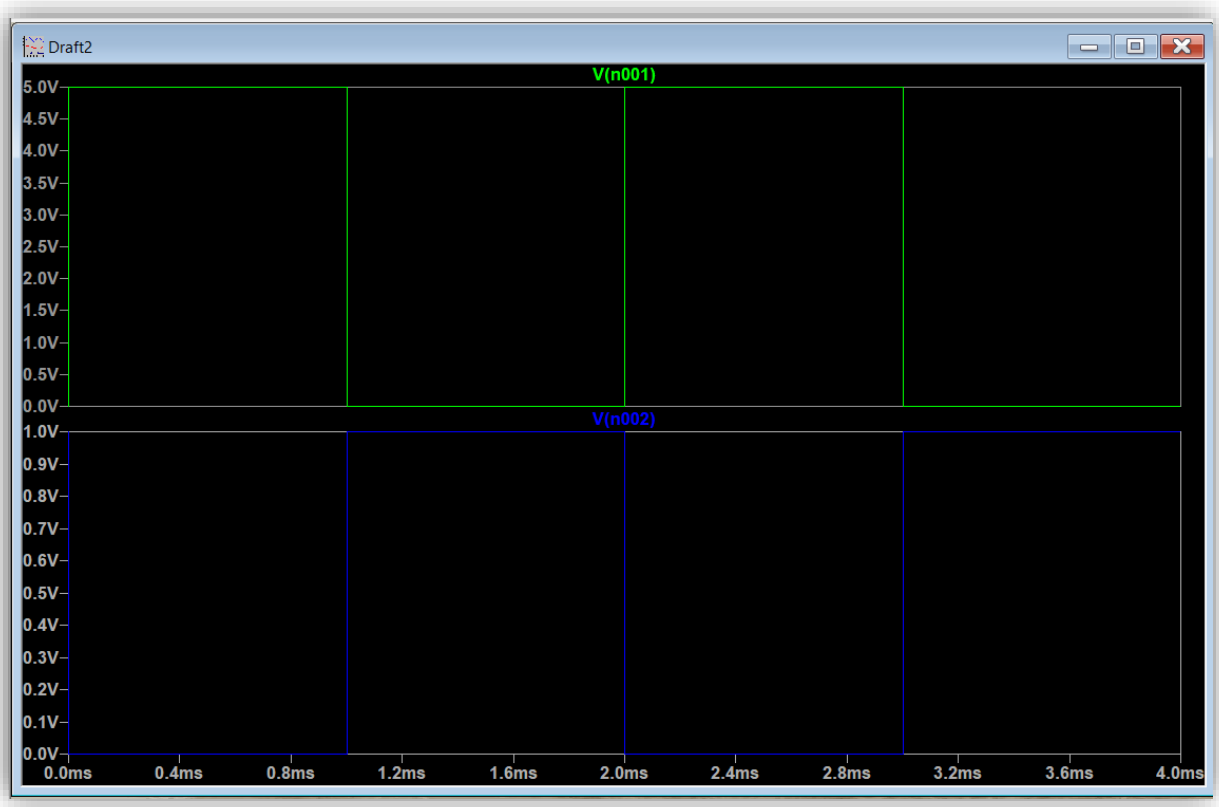


NOT GATE

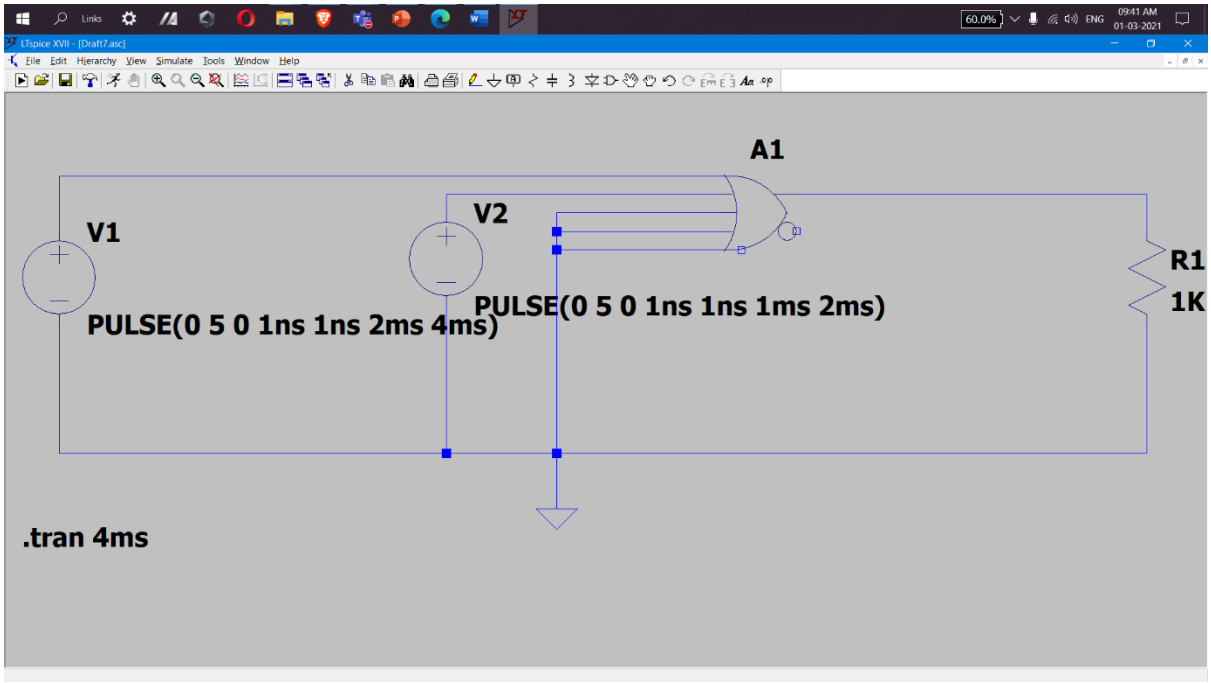
DIAGRAM


A1
A
R1
1K
PULSE(0 5 0 1ns 1ns 1ms 2ms)

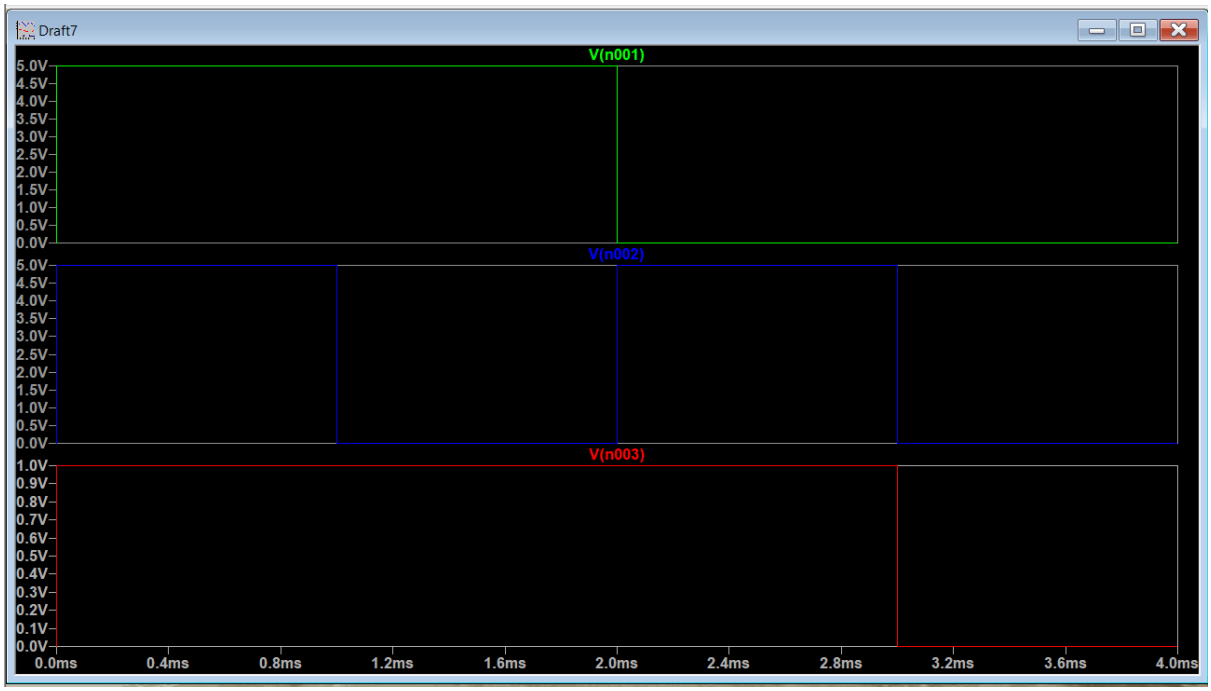
OUTPUT


Draft2
V(n001)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
V(n002)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
0.0ms
0.4ms
0.8ms
1.2ms
1.6ms
2.0ms
2.4ms
2.8ms
3.2ms
3.6ms
4.0ms

OR GATE

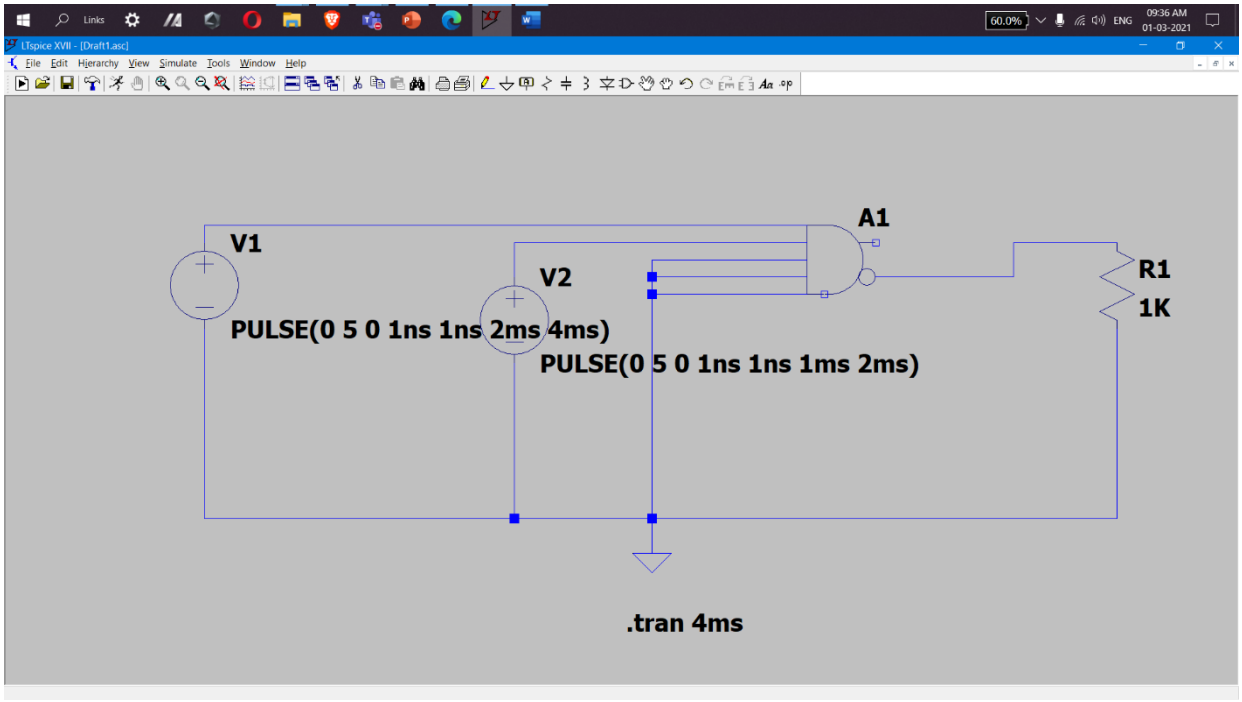


OUTPUT

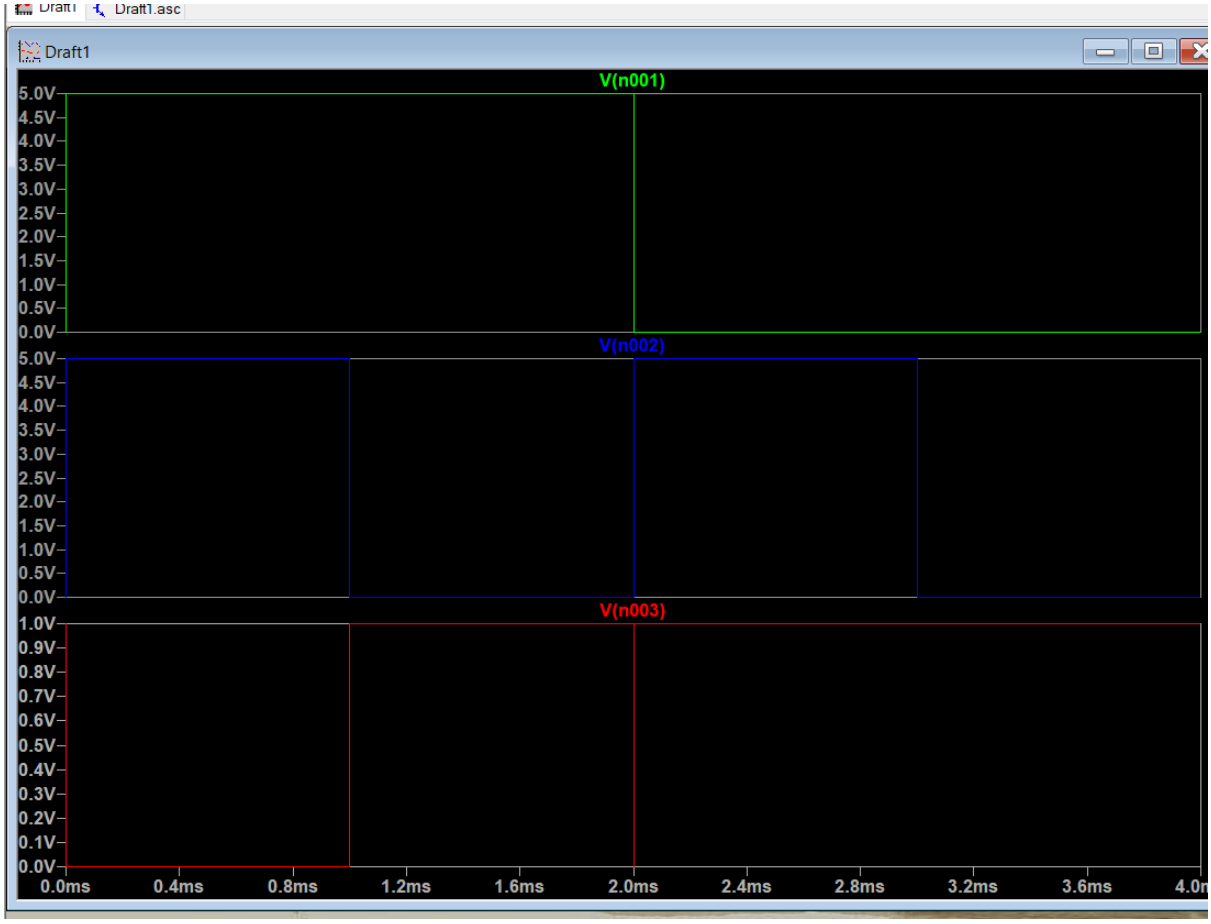


NAND GATE

DIAGRAM

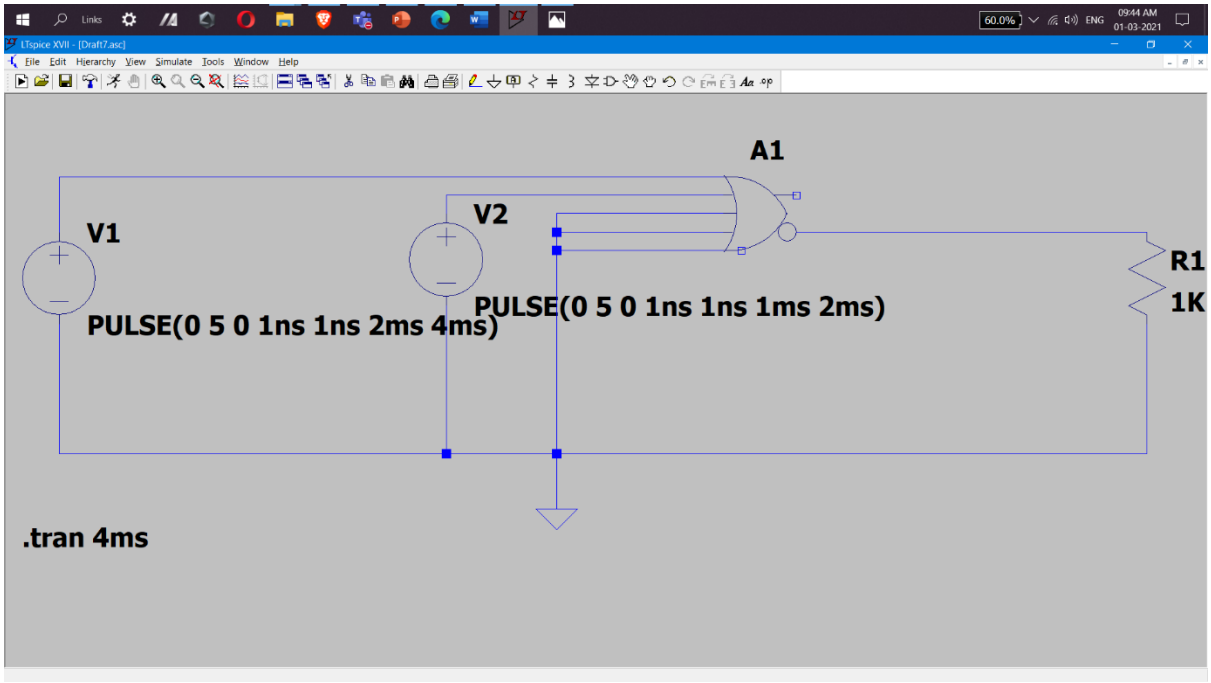


OUTPUT

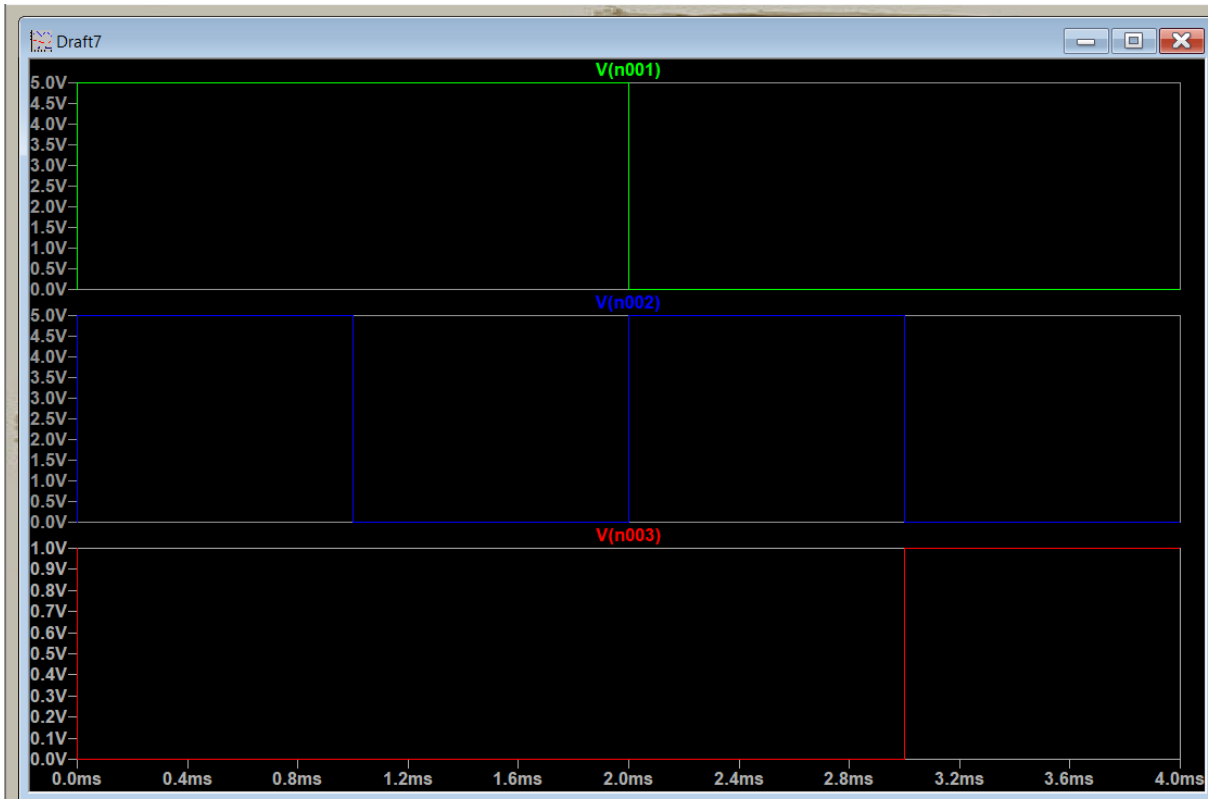


NOR GATE

DIAGRAM

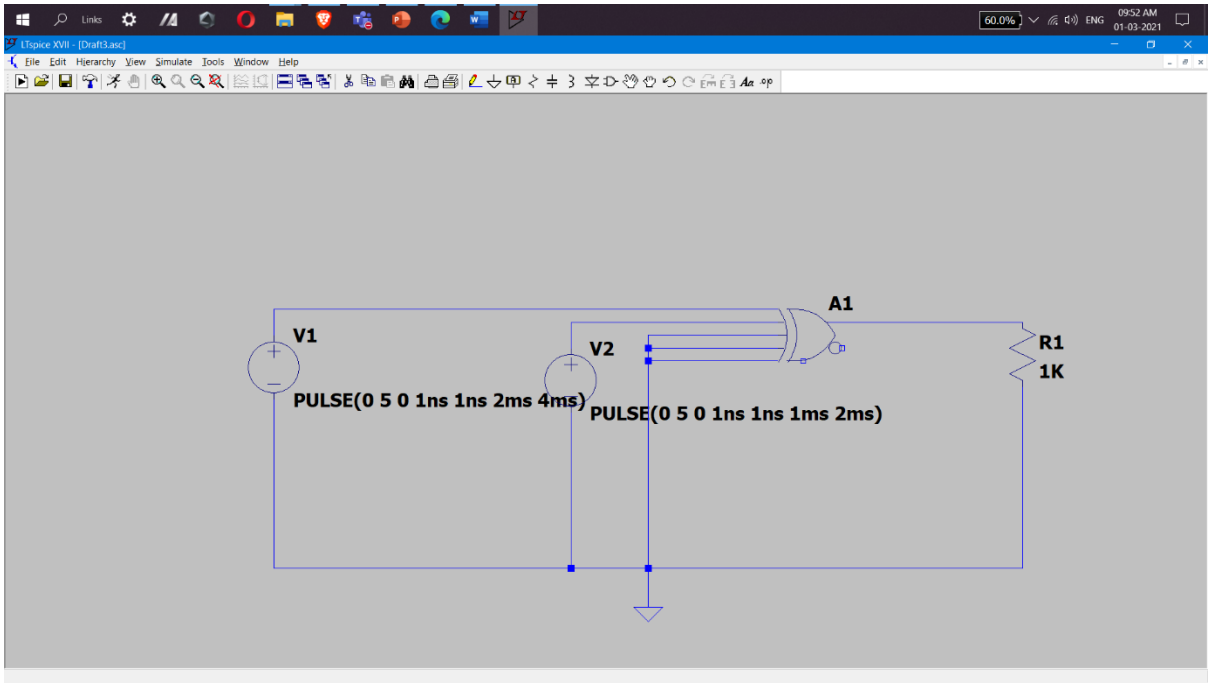

A1
V1
V2
R1
1K
PULSE(0 5 0 1ns 1ns 2ms 4ms)
PULSE(0 5 0 1ns 1ns 1ms 2ms)
.tran 4ms

OUTPUT

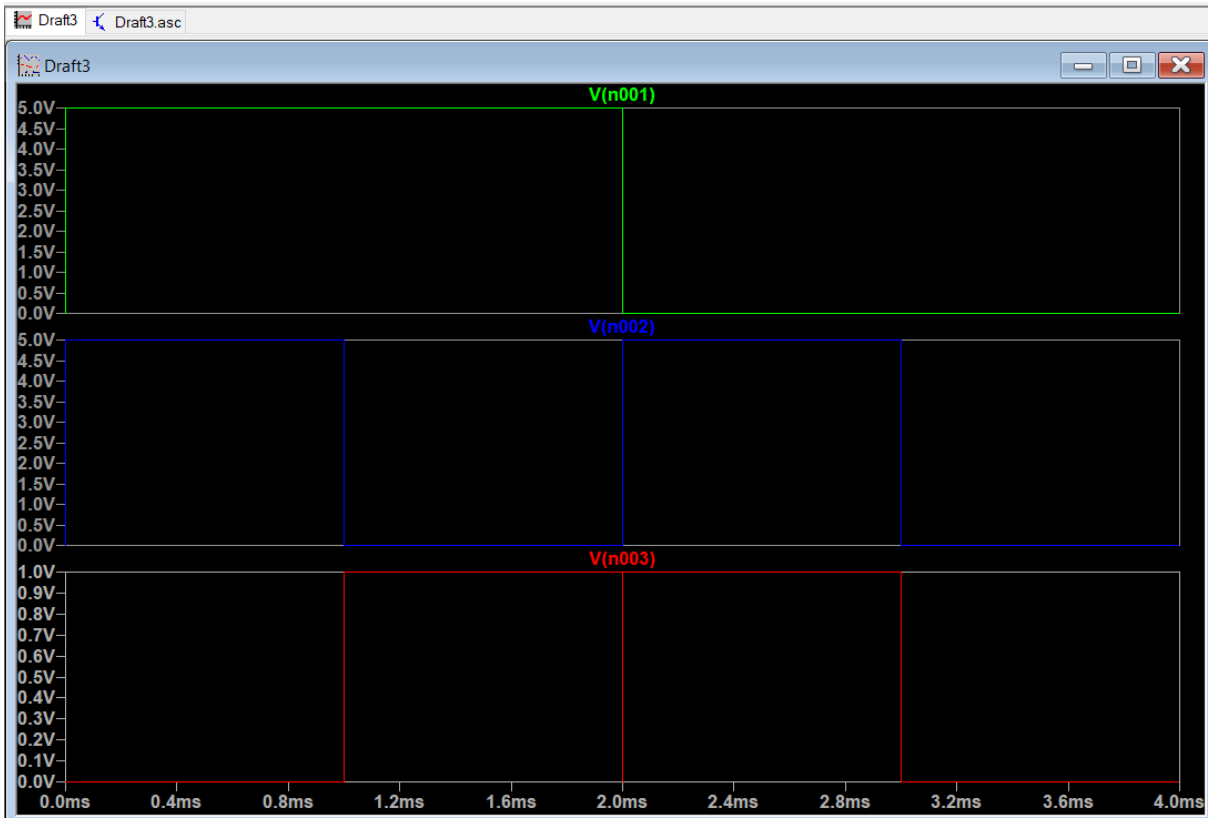

Draft7
V(n001)
V(n002)
V(n003)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0ms
0.4ms
0.8ms
1.2ms
1.6ms
2.0ms
2.4ms
2.8ms
3.2ms
3.6ms
4.0ms

XOR GATE

DIAGRAM



OUTPUT


Draft3
Draft3.asc
Draft3
V(n001)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
V(n002)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
V(n003)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
0.0ms
0.4ms
0.8ms
1.2ms
1.6ms
2.0ms
2.4ms
2.8ms
3.2ms
3.6ms
4.0ms