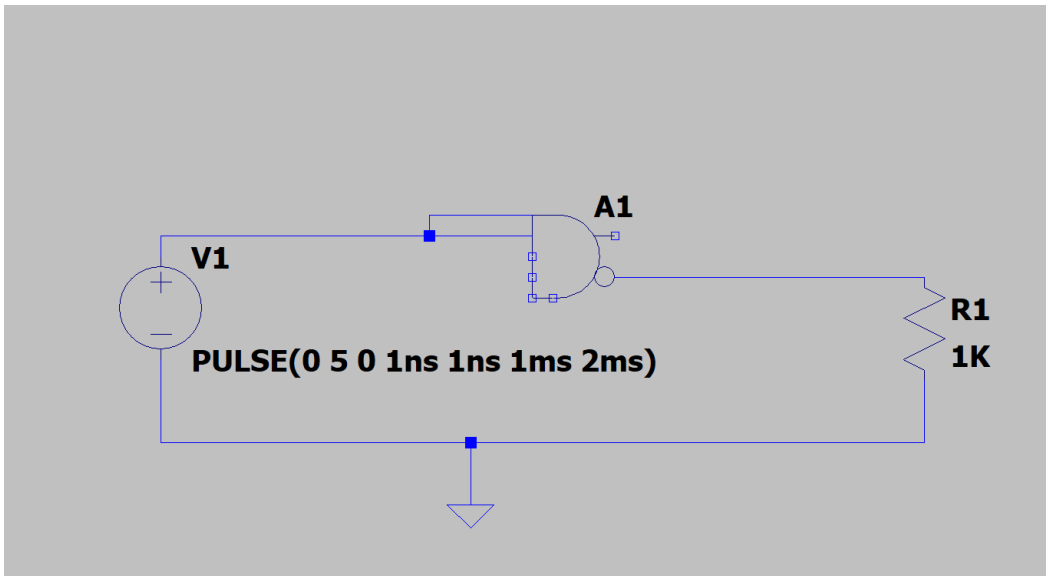
CSE1003 LAB-2

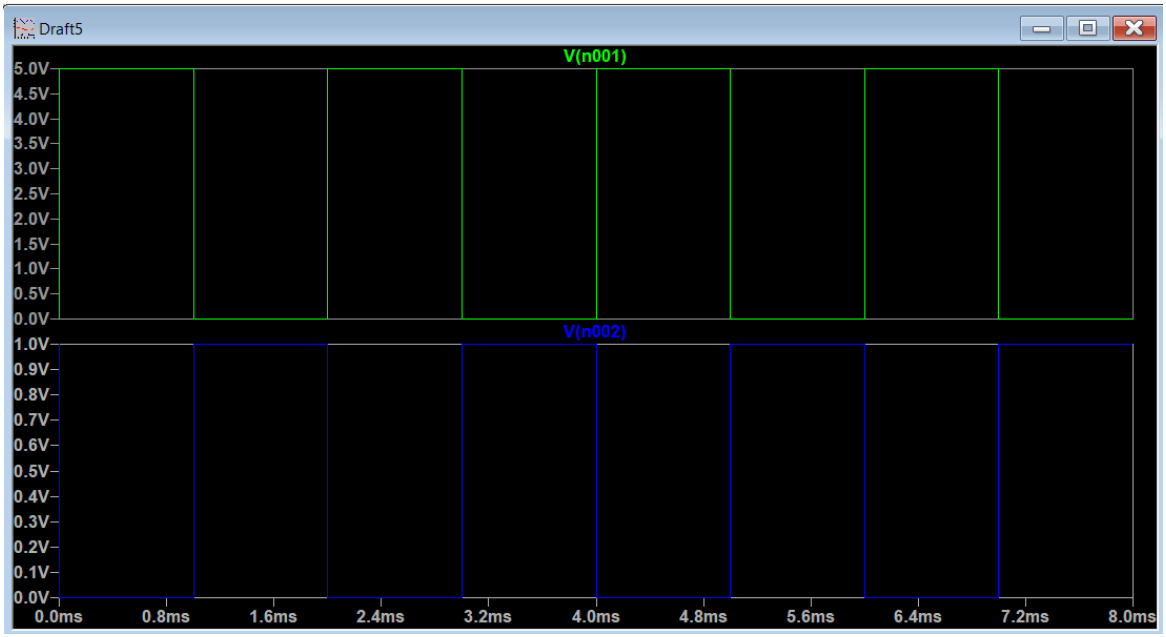
BY ASHUTOSH ARDU

REGISTRATION NO. 20BRS1262

NAND GATES AS NOT



OUTPUT



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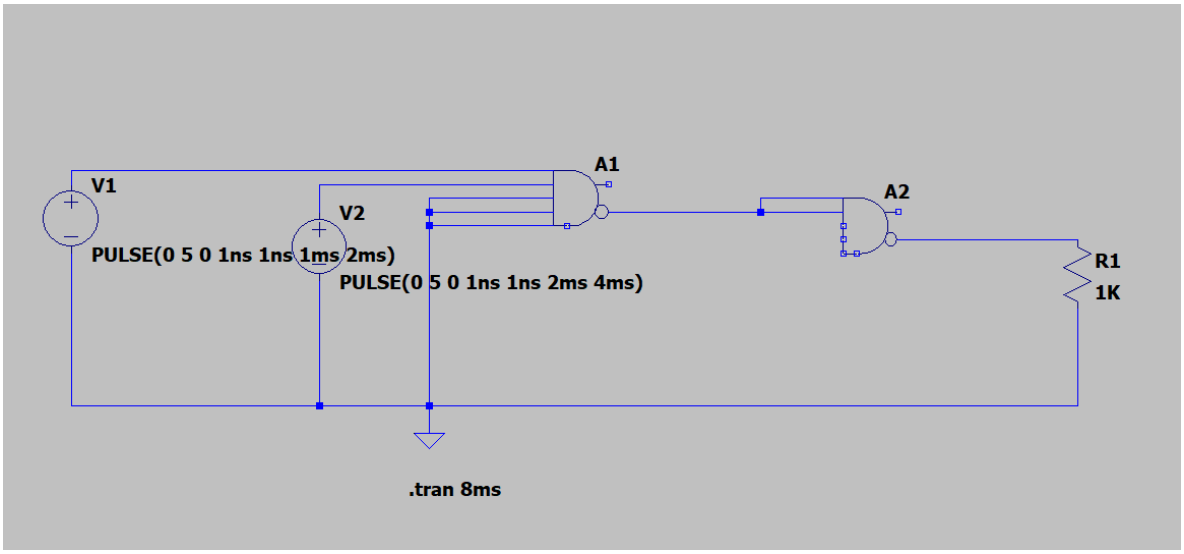

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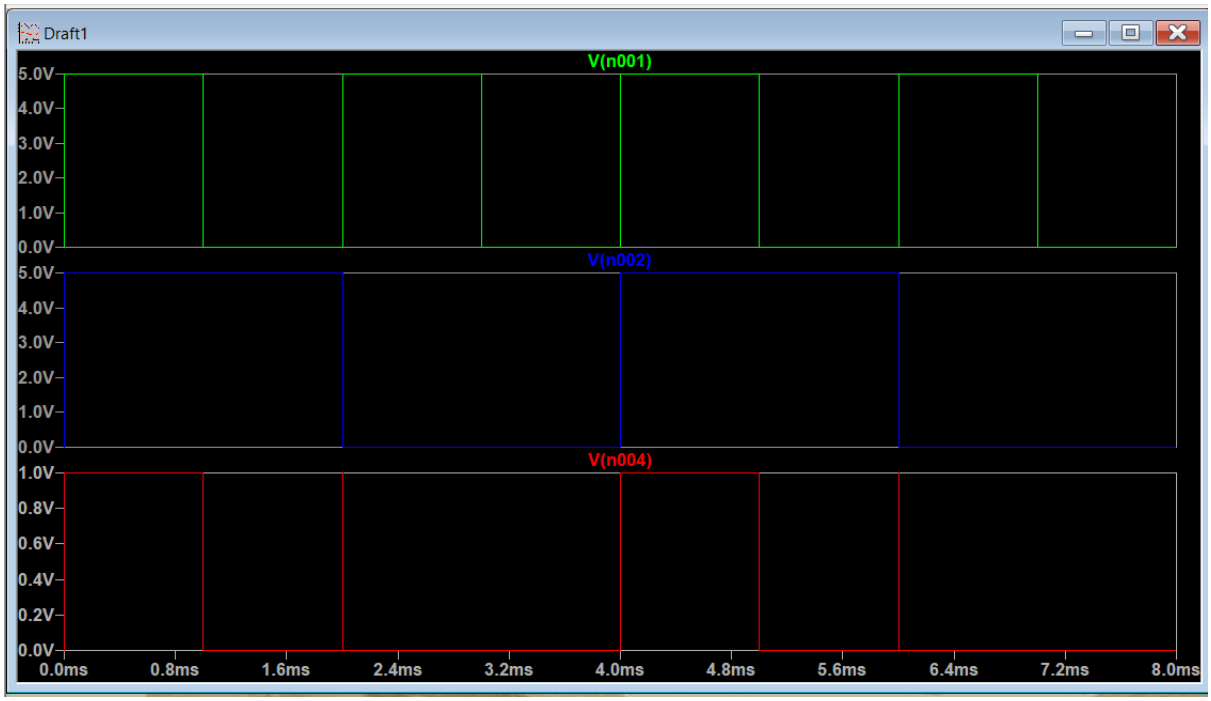
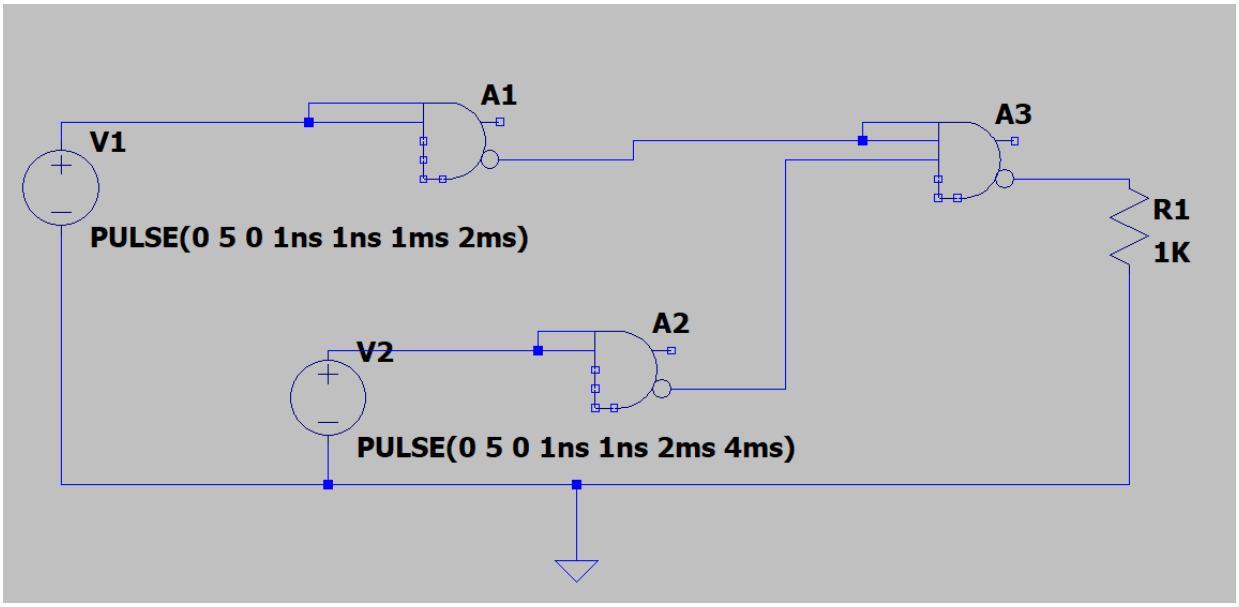
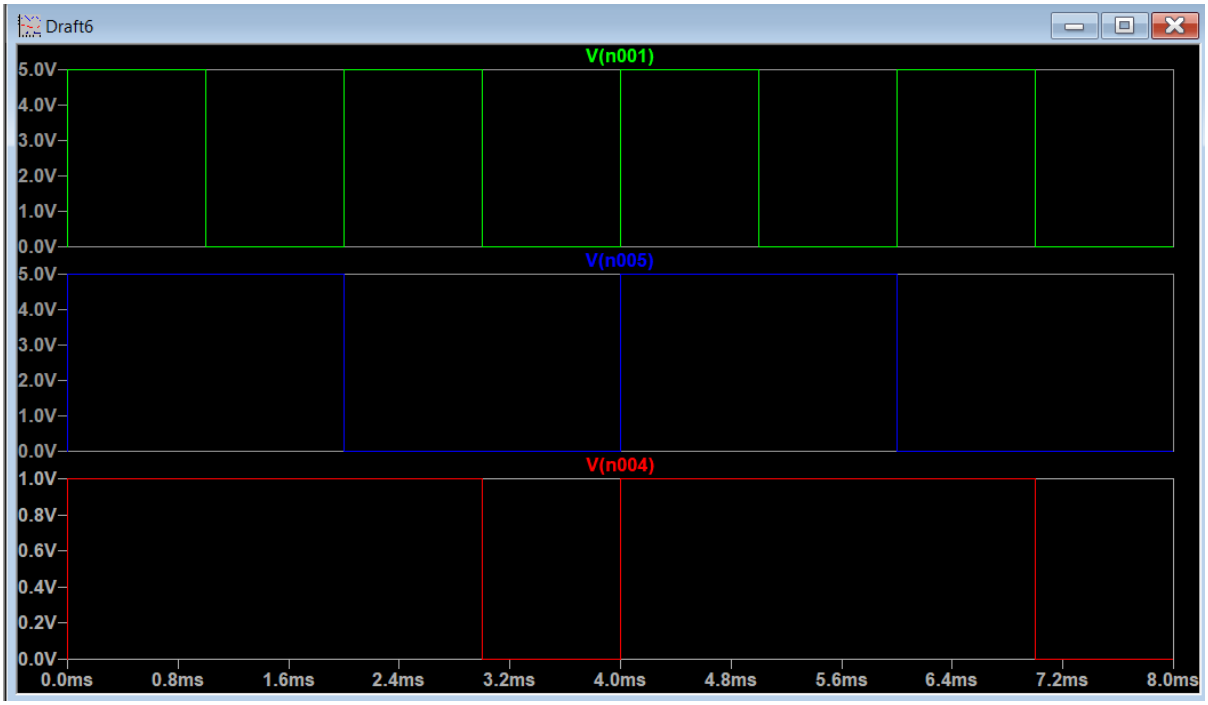


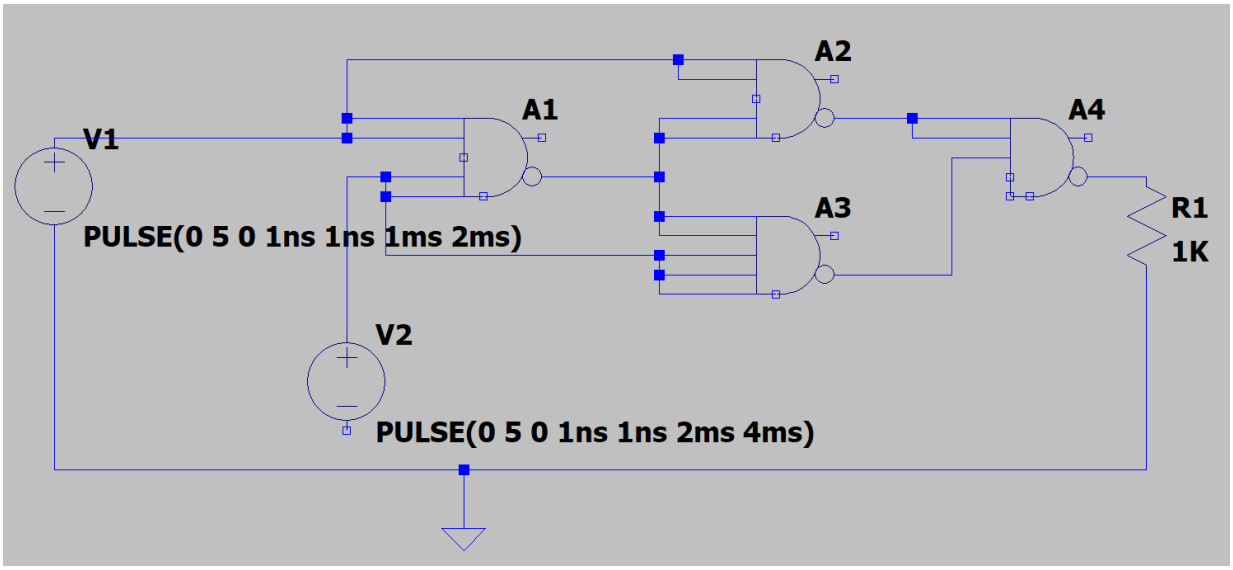
NAND GATES AS OR GATES



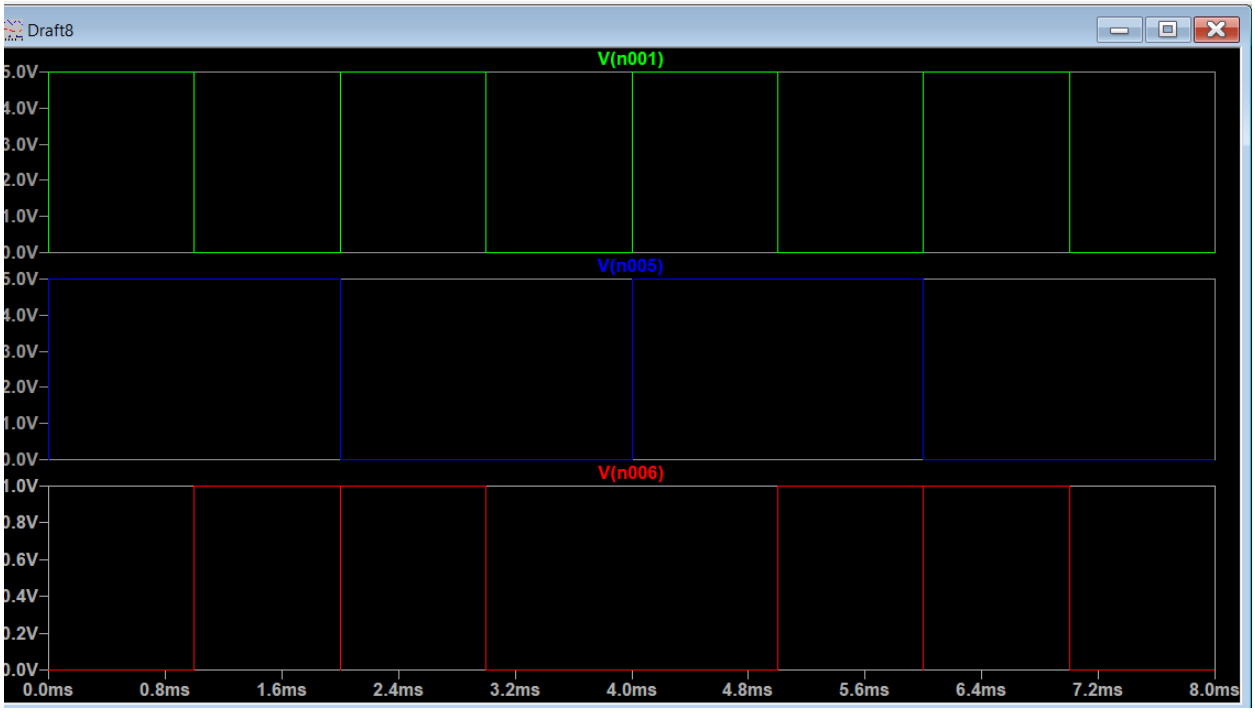
OUTPUT



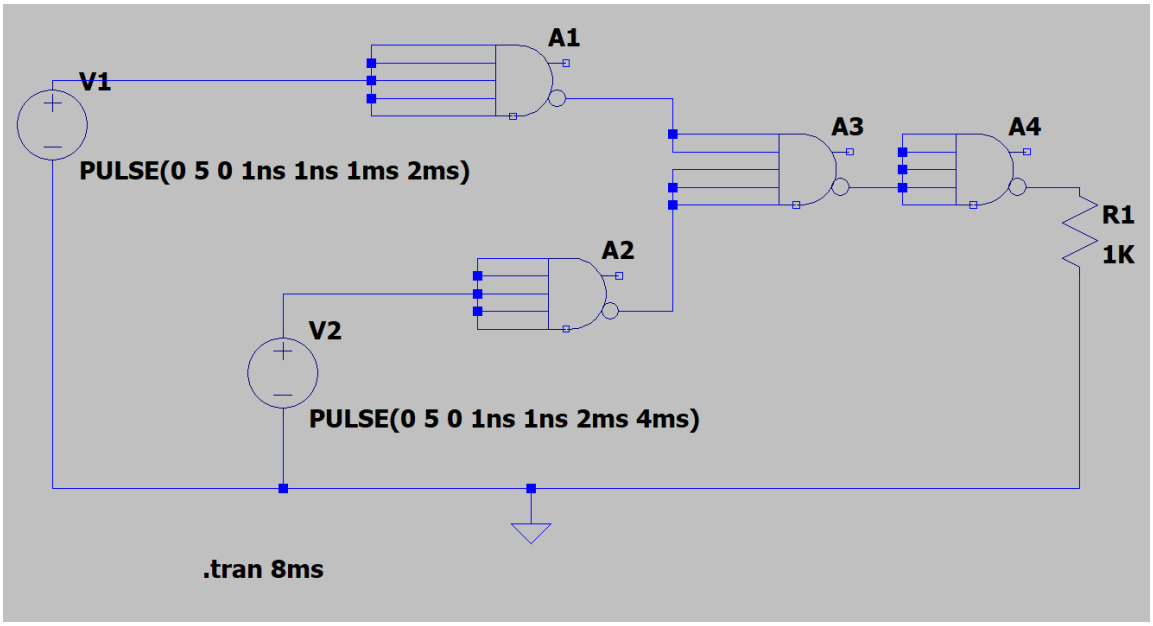
NAND GATES AS XOR GATES



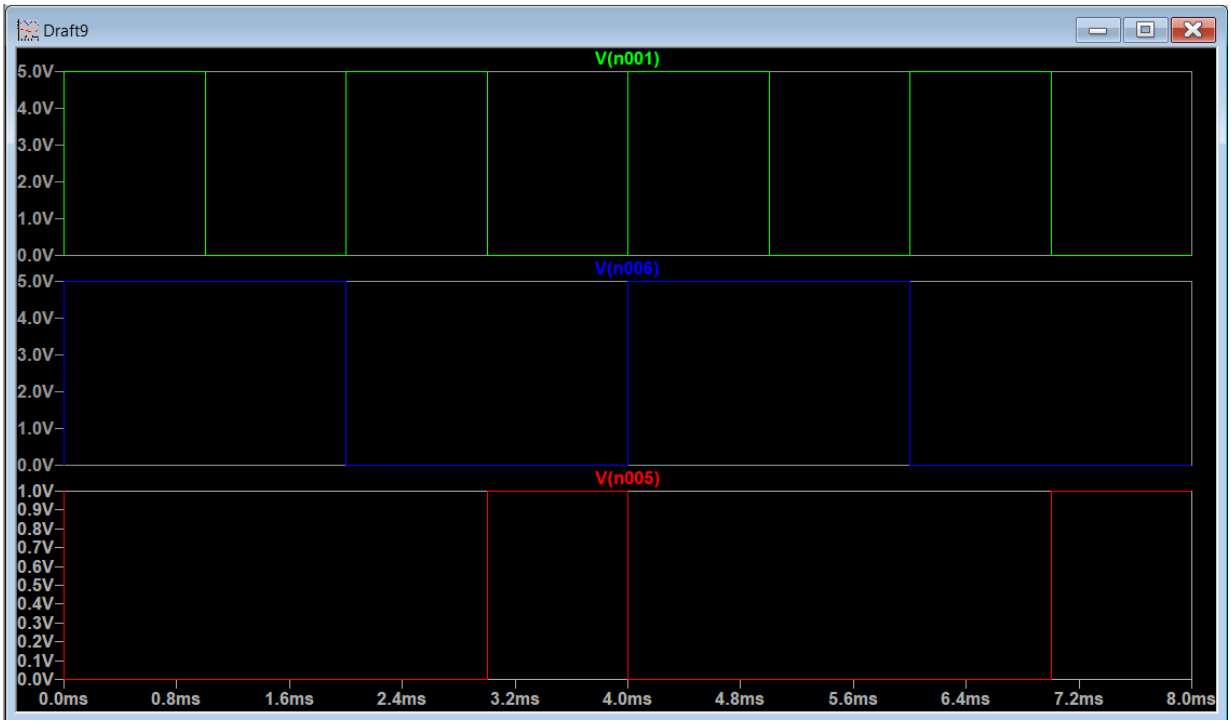
OUTPUT



NAND GATES AS NOR GATE


A1
V1
A3
A4
PULSE(0 5 0 1ns 1ns 1ms 2ms)
R1
1K
A2
V2
PULSE(0 5 0 1ns 1ns 2ms 4ms)
.tran 8ms

OUTPUT


Draft9
V(n001)
5.0V
4.0V
3.0V
2.0V
1.0V
0.0V
V(n006)
5.0V
4.0V
3.0V
2.0V
1.0V
0.0V
V(n005)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
0.0ms
0.8ms
1.6ms
2.4ms
3.2ms
4.0ms
4.8ms
5.6ms
6.4ms
7.2ms
8.0ms