Generation of a Triggering Pulse for the Power Conversion of a Half-Controlled Rectifier

Aim

With the help of necessary transistor circuits, simulate the Ramp Firing Circuit**,** which is used for controlling the firing angle of an SCR in a single-phase controlled converter.

Objective

The primary objective of this circuit is to generate gate pulses whose timing can be adjusted by varying a DC control voltage, and to synchronize these pulses with the AC supply.

Software:

PSIM Professional Version 9.1.1.400

Model Parameters:

Vin = 240Vac, Frequency= 50Hz

Basic Principle

The principle behind this circuit is phase control. The ramp waveform is generated and synchronized with each half-cycle of the AC input. This ramp is compared with a reference DC control voltage. When the ramp voltage equals the control voltage, the comparator output triggers the SCR gate.

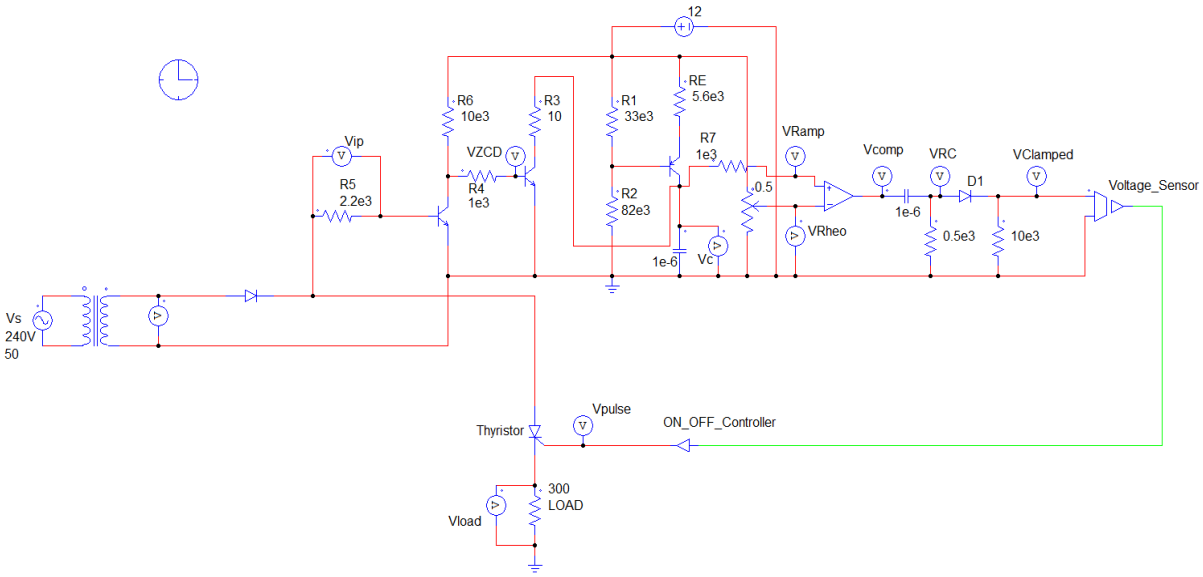
Thus, by varying the DC control voltage, we can delay or advance the firing angle, thereby controlling the output voltage across the load.

Circuit Blocks Overview

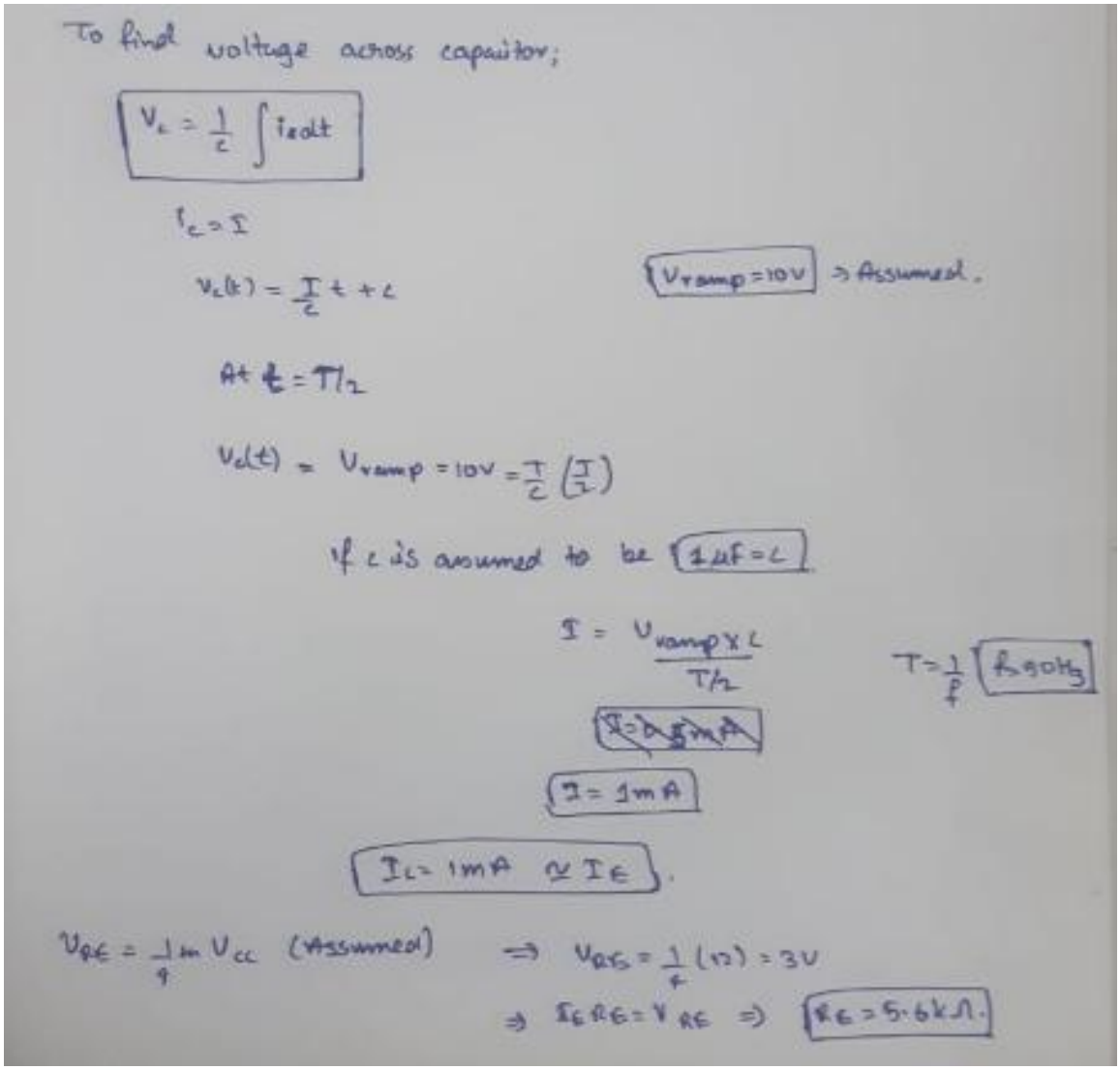
The entire circuit can be divided into four main sections:

1. Zero Crossing Detector (ZCD)
2. Ramp Generator
3. Comparator (Firing Pulse Generator)
4. Power Circuit with SCR and Load

Circuit:



Circuit Designing:

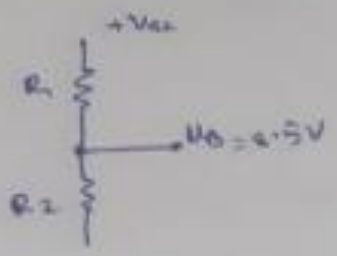


Considering transistor (PNP)

$V_B = V_{CC} - V_{RE} - V_{BE}$

$= 12 - 2.8 - 0.7$

$\boxed{V_B = 8.5V}$



$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$

$\Rightarrow R_2 = \frac{V_B \times (R_1 + R_2)}{V_{CC}}$

$R_2 = 5.5k\Omega \simeq \boxed{8.2k\Omega = R_2}$

$\therefore R_1 = 50k - 8.2k$

$\boxed{R_1 = 38k\Omega} \simeq \underline{33k\Omega}$

Assumptions; ⇒ Synchronization;

$\boxed{R_4 = 10k\Omega}$

Also, R_5 is considered to be $\frac{1}{10}$ of R_4

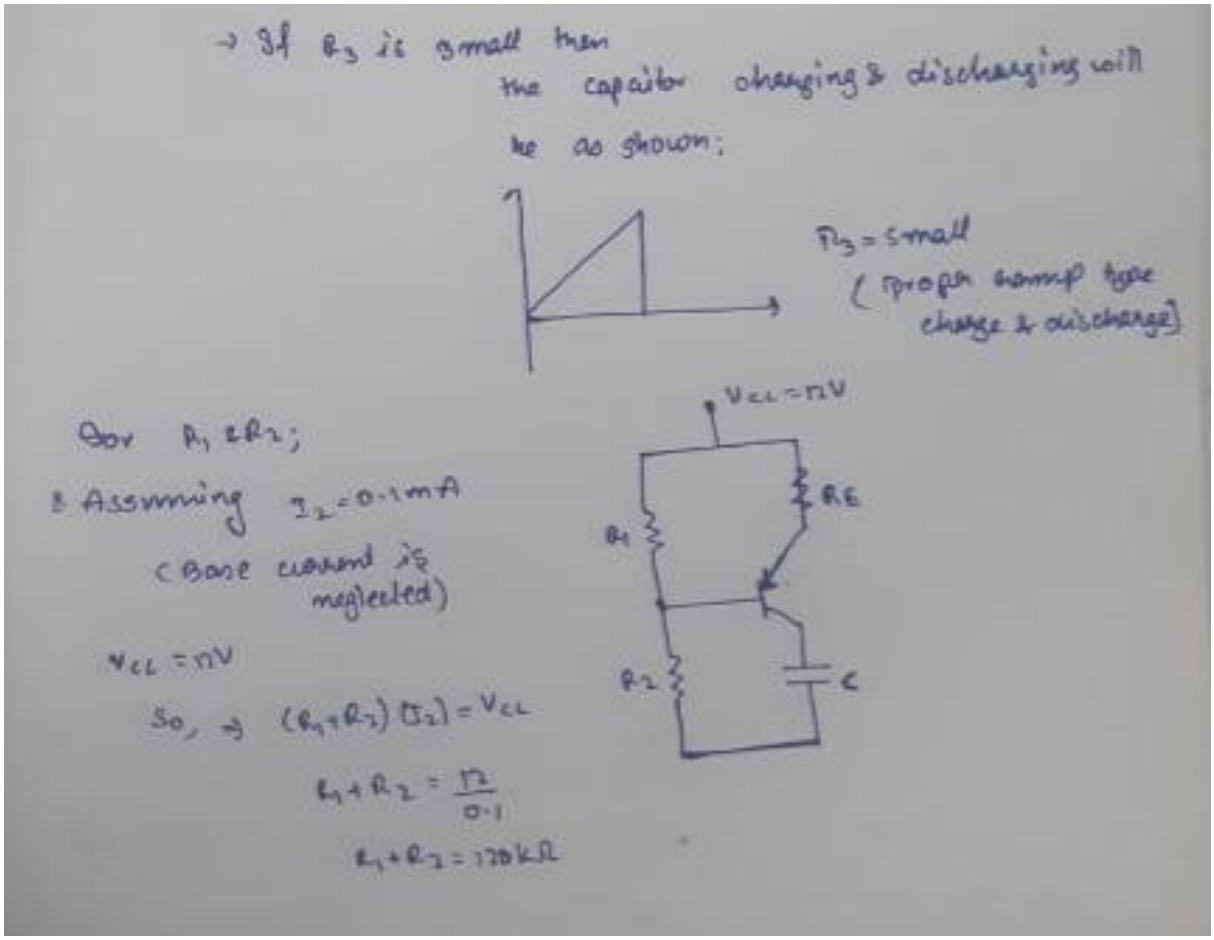
$\Rightarrow 1k\Omega \left(\frac{1}{10}(10k)\right)$

$\simeq 2.2k\Omega$ (availability)

$\therefore R_6 = 1k\Omega \rightarrow$ To obtain enough base current.

∴ Resistor R_3 is used to limit discharge current of the capacitor;

→ If R_3 is large then the capacitor charging and discharging will be as shown;

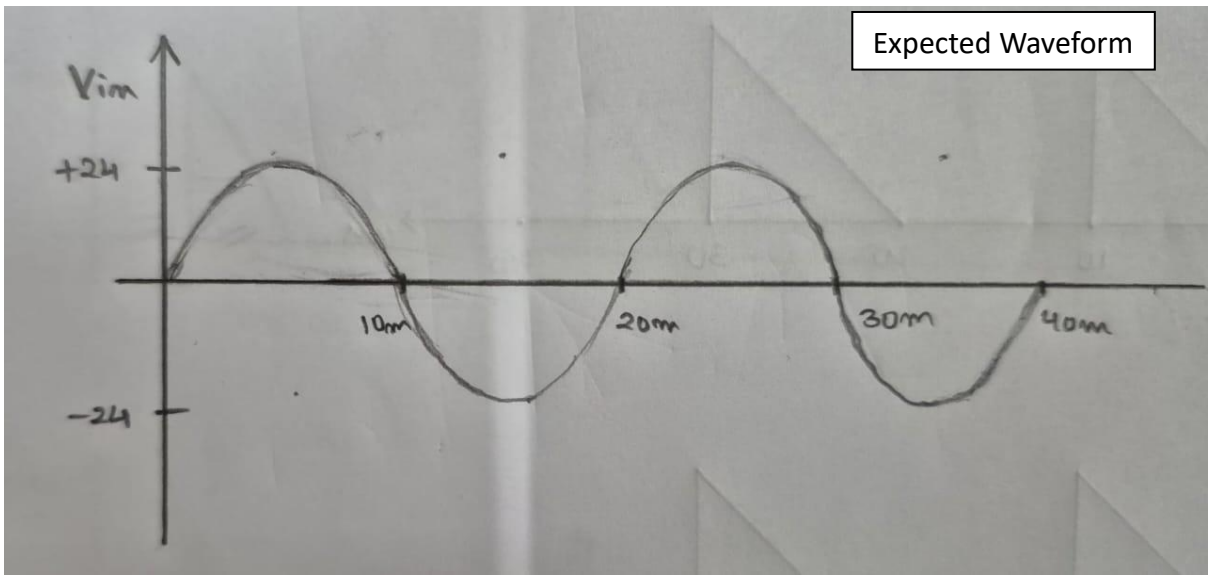


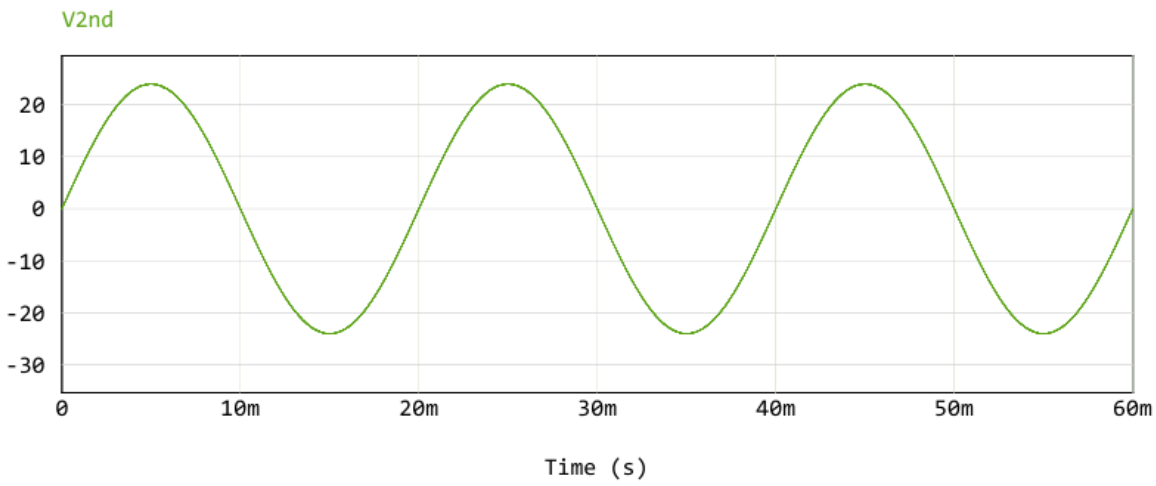
Pulse Generation Designing:

1. Step Down Transformer:

Here, a 10:1 turns ratio step-down transformer is used to get 8 volts as the secondary side output voltage. This sine waveform has an amplitude of +24 & -24 V magnitude.

Formula: $V_1/V_2 = N_1/N_2$ ➔ V_2 = 240/10= 24 volt





This secondary AC voltage is used as the input for the zero-crossing detector and the control circuit. It provides the base signal for synchronization.

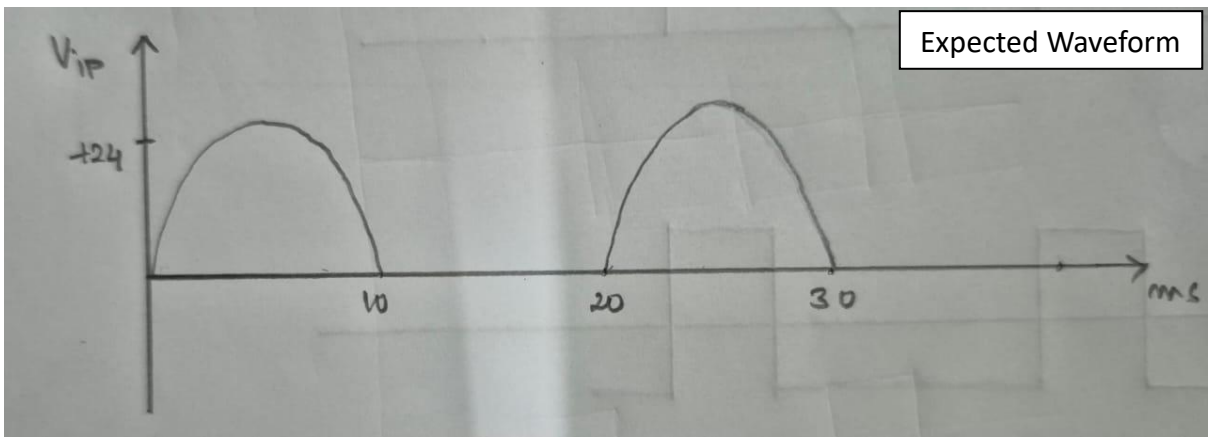
2. Rectified Graph (Input to the Control Circuit)

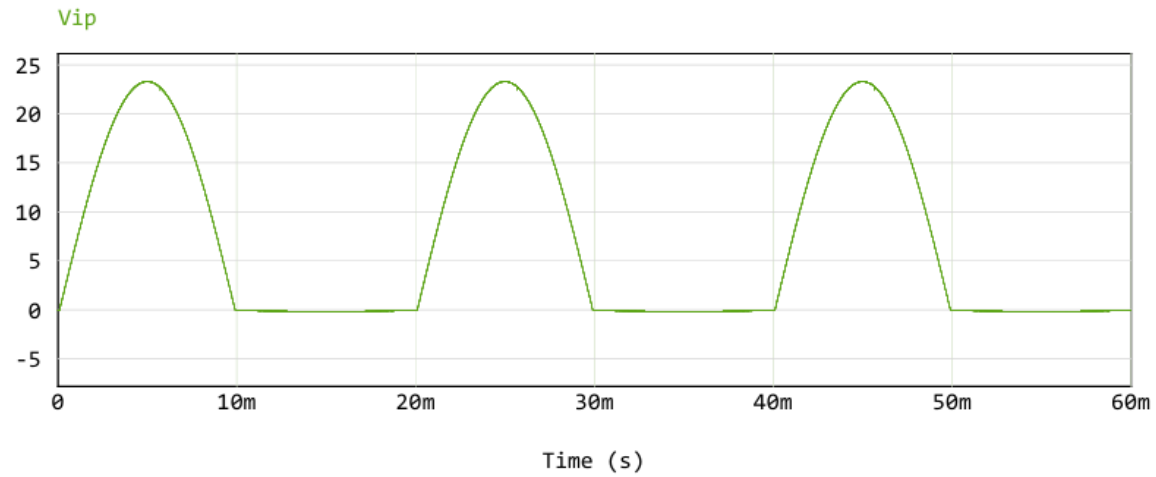
$$f = \frac{1}{T}$$

Example:
For a 50 Hz AC supply,

$$T = \frac{1}{50} = 0.02s = 20ms$$

Each half cycle, therefore, lasts 10ms, which defines how often the ramp waveform resets.



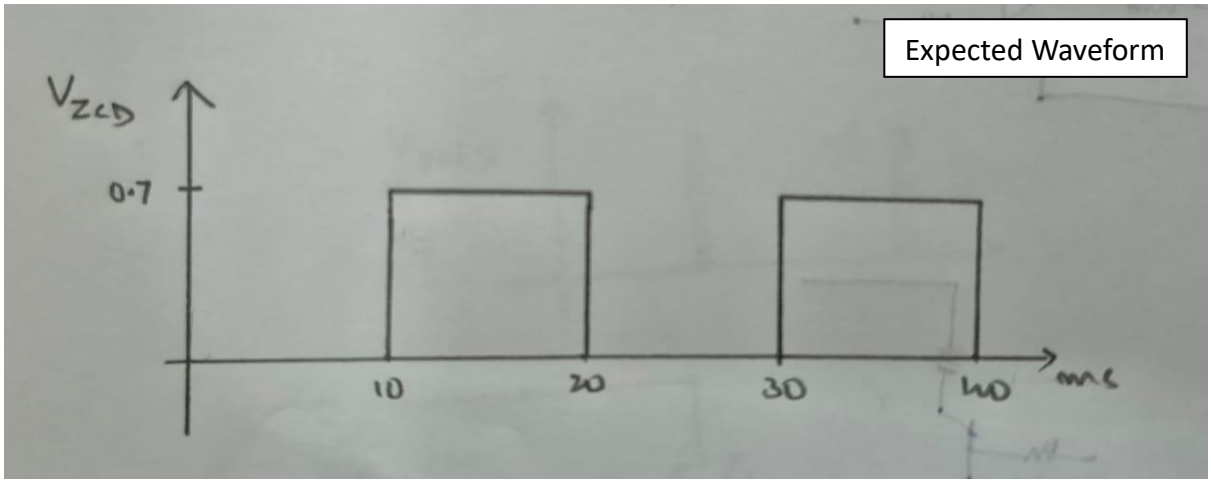


3. Zero Crossing Detector

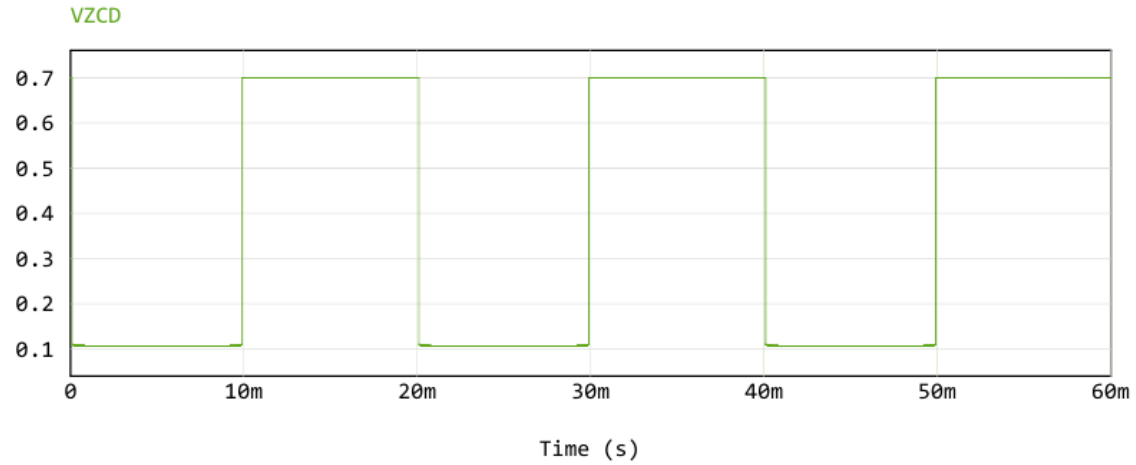
The Zero Crossing Detector senses when the input AC waveform crosses zero volts and generates synchronized square pulses. It uses a transistor switching circuit connected to the secondary of the step-down transformer. During the positive half-cycle, the transistor conducts, producing a low output; during the negative half-cycle, it cuts off, giving a high output.
Thus, the output waveform alternates between high and low levels at every zero crossing of the AC input. This ensures that the ramp generator starts precisely at each zero crossing, maintaining synchronization with the supply frequency (50 Hz).

$$f = \frac{1}{T}$$

where $f = 50Hz$and $T = 20ms$per cycle (10 ms per half-cycle).



In PSIM, we can observe this at the VZCD probe, where the output is a clean square wave corresponding to every zero crossing.



4. Ramp Generation

The ramp generator converts the ZCD pulses into a linearly increasing voltage waveform. It consists of a PNP transistor, resistors, and a timing capacitor **(C)**. When a zero-crossing pulse arrives, the transistor momentarily discharges the capacitor to zero. Afterward, the capacitor charges linearly through the resistors until the next pulse arrives. The ramp voltage is given by:

$$V_C(t) = \frac{V_{CC}}{RC}\, t$$

where V_{CC} is the supply voltage and RC is the time constant determining the ramp slope. This waveform repeats every half-cycle of the input signal.

Example:
If $V_{CC} = 12V$, $R = 1k\Omega$, and $C = 0.1\mu F$:

$$V_C(t) = \frac{12}{(10 \times 10^3)(0.1 \times 10^{-6})}\, t = 1200\, t$$

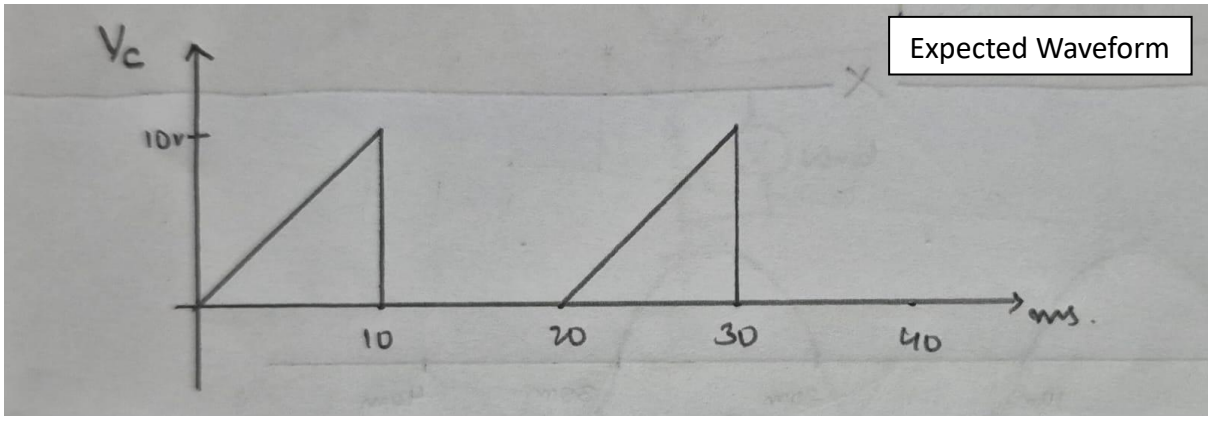
For $t = 10ms$:

$$V_C = 1200 \times 0.01 = 12V$$

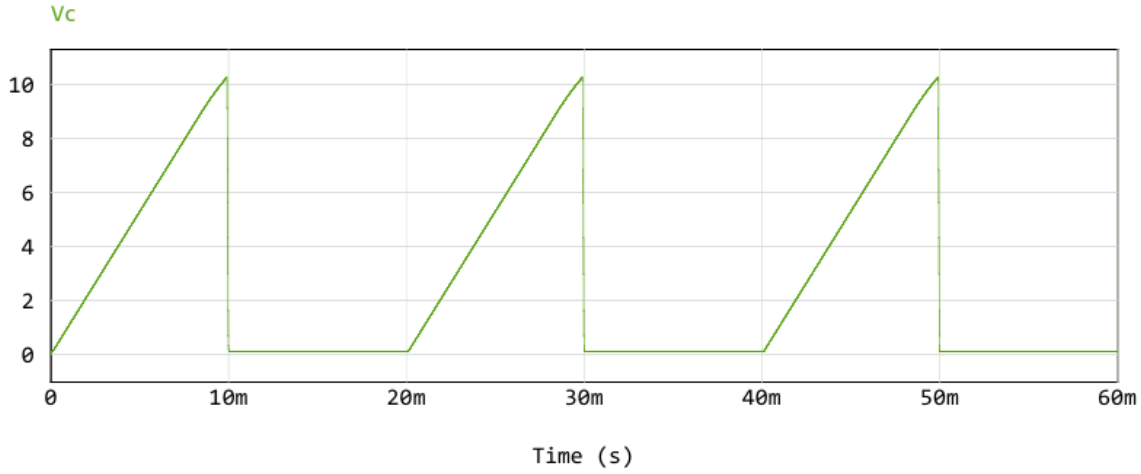
The ramp rises linearly from 0 V to ~12 V during each half-cycle and resets at every zero crossing.

In simulation, it is observed to be reaching a peak of 10.3V (as shown from the snippet taken from PSIM)

Vertical:	.	.	ΔY
	.	.	1.02987e+01



The generated ramp voltage can be observed at the probe VRamp in the simulation. This ramp repeats for each half-cycle of the AC waveform.



5. Comparator and Control Voltage

The comparator compares the instantaneous ramp voltage (V_{ramp}) with a reference control voltage (V_{ref}). When $V_{ramp} = V_{ref}$ The comparator switches and generates a firing pulse. By adjusting V_{ref} The intersection points change, which varies the firing angle (α) of the SCR. Hence, the conduction period of the SCR and the average output voltage are controlled as:

$$V_{avg} = \frac{V_m}{\pi}(1 + \cos\ \alpha)$$

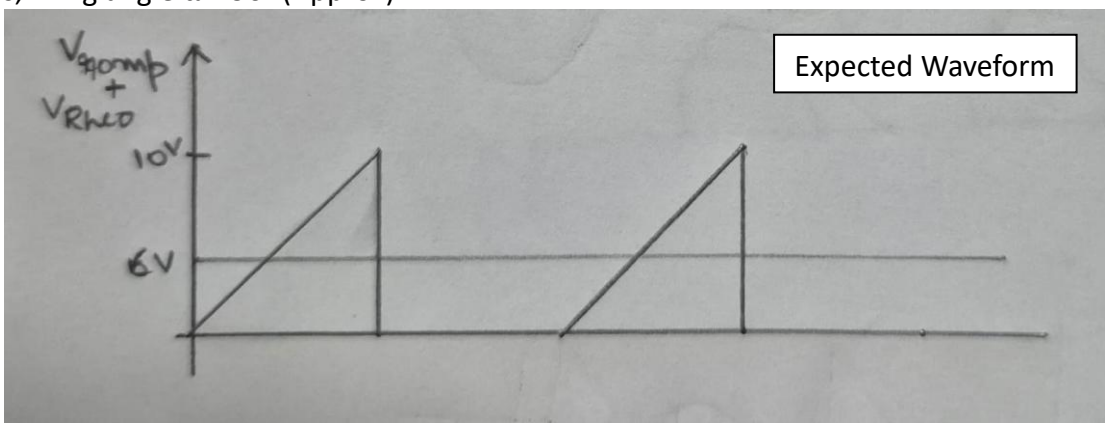
where $V_m$is the maximum input voltage.
Condition:

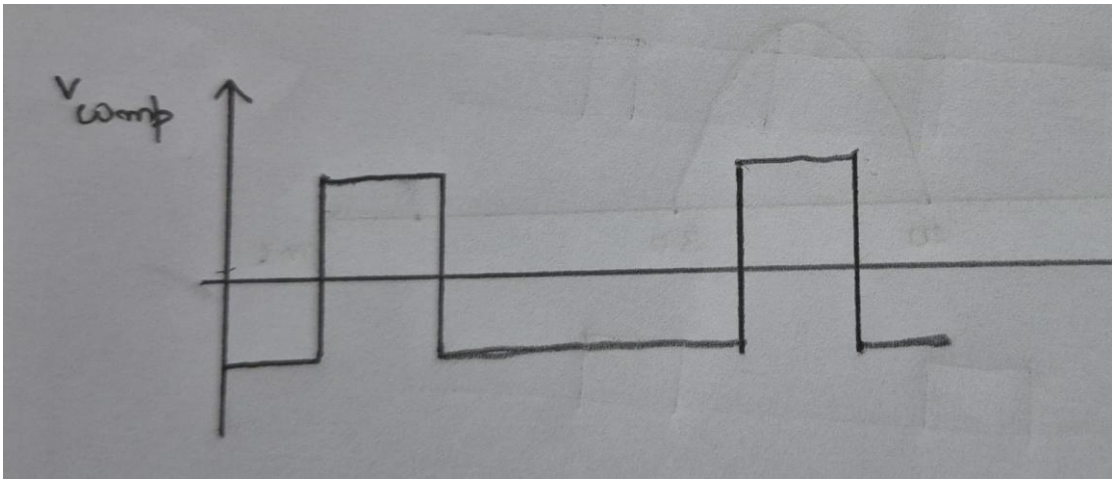
$$\mathrm{V_{ramp}} = \mathrm{V_{ref}}$$

When the instantaneous ramp voltage equals the reference control voltage, the comparator switches its output from LOW to HIGH, generating a **firing pulse**.
Example:
If $\mathrm{V_{ref}} = 6\mathrm{V}$and the ramp rises linearly from 0–12 V, the pulse occurs at

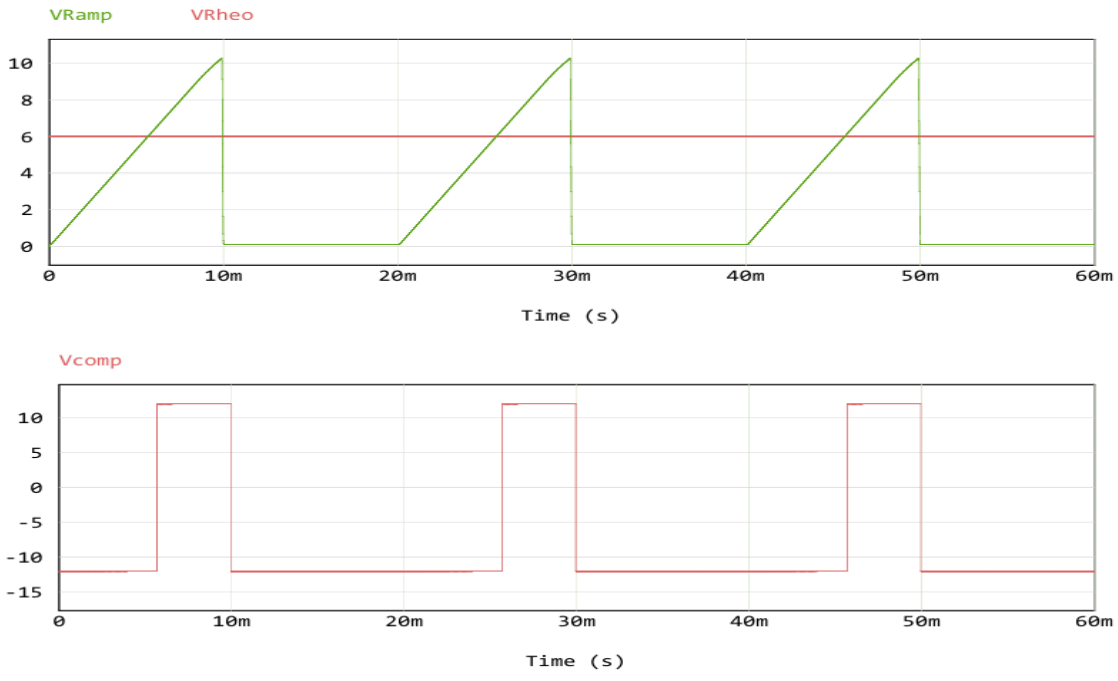
$$\frac{6}{12} \times 180° = 90°$$

Thus, firing angle α = 90° (Approx).



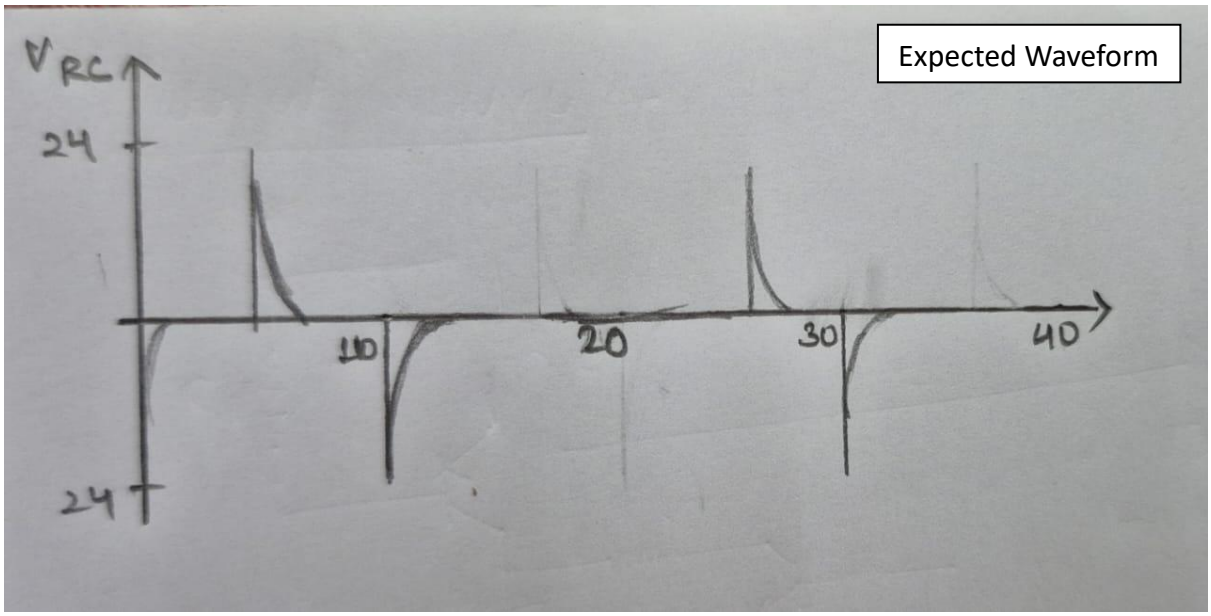


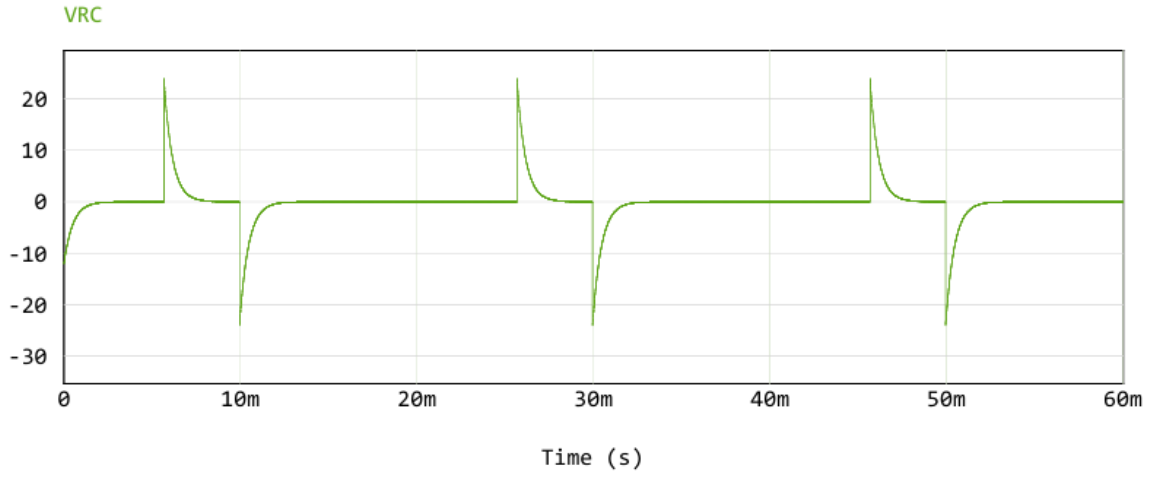
In the simulation, the comparator output can be observed at VComp**,** showing firing pulses synchronized with the AC waveform.



6. RC Differentiator

The RC differentiator narrows the width of the comparator output pulse. It consists of a small capacitor C and resistor R connected in series. This produces short, sharp pulses ideal for triggering the SCR gate without causing excessive heating or prolonged conduction.

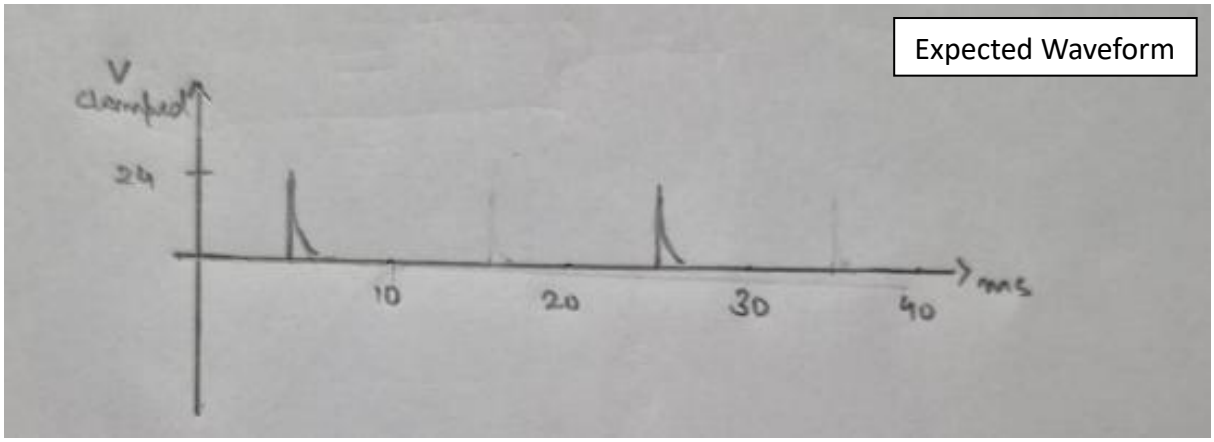


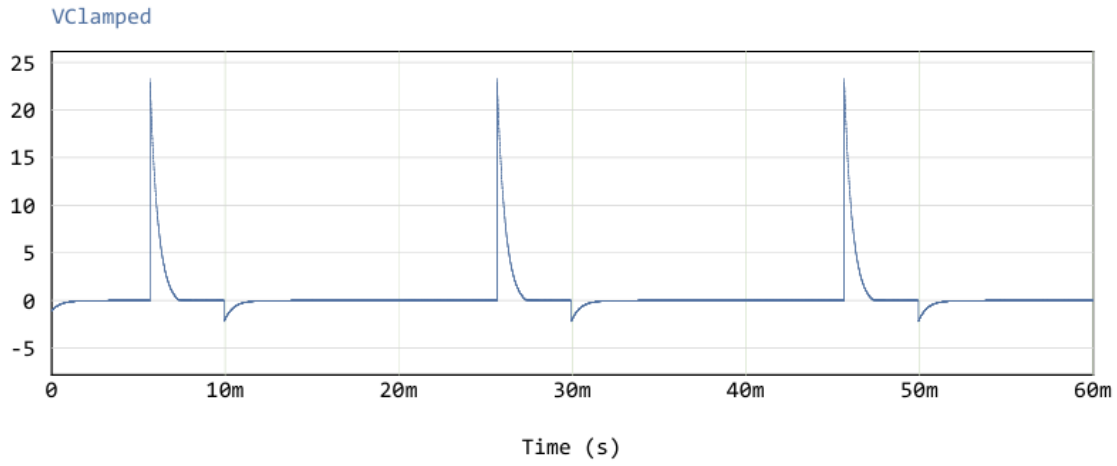


7. Clamping

The clamping circuit removes the negative portion of the differentiated waveform to ensure a purely positive gate pulse. A diode is used for positive clamping, which shifts the entire waveform above zero potential. This protects the SCR gate from reverse voltages and

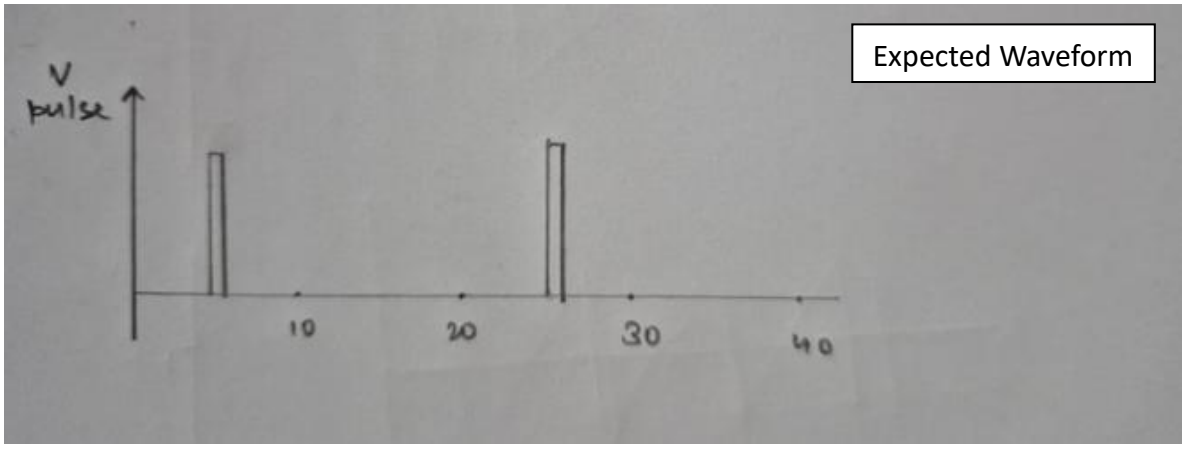
ensures reliable triggering.

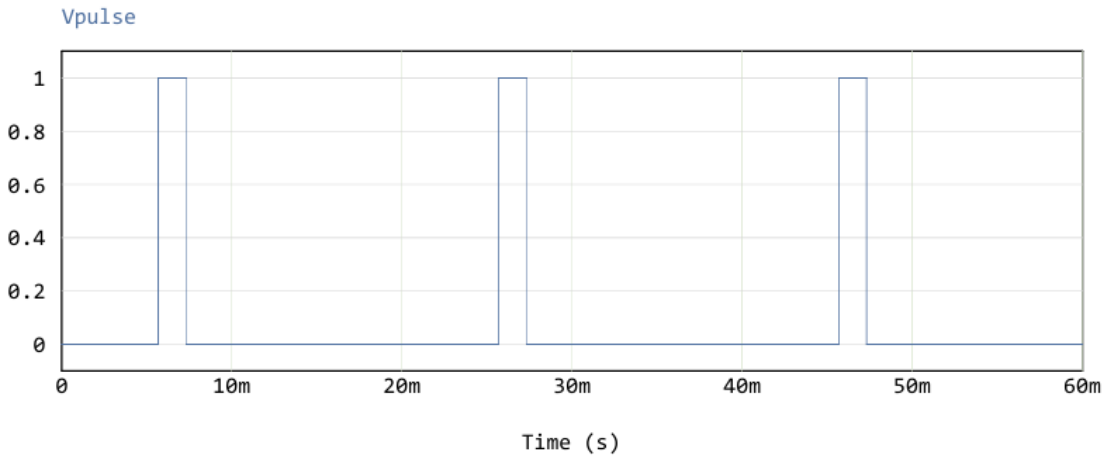




8. Pulse Generation and Load Voltage

After clamping, the clean, narrow firing pulse is applied to the **SCR gate terminal** through a current-limiting resistor. When triggered, the SCR conducts for the remaining half-cycle, allowing current through the load.





The average DC output voltage across the load is controlled by varying the firing angle (α). Thus, the circuit achieves smooth control of load voltage by adjusting the DC reference input.

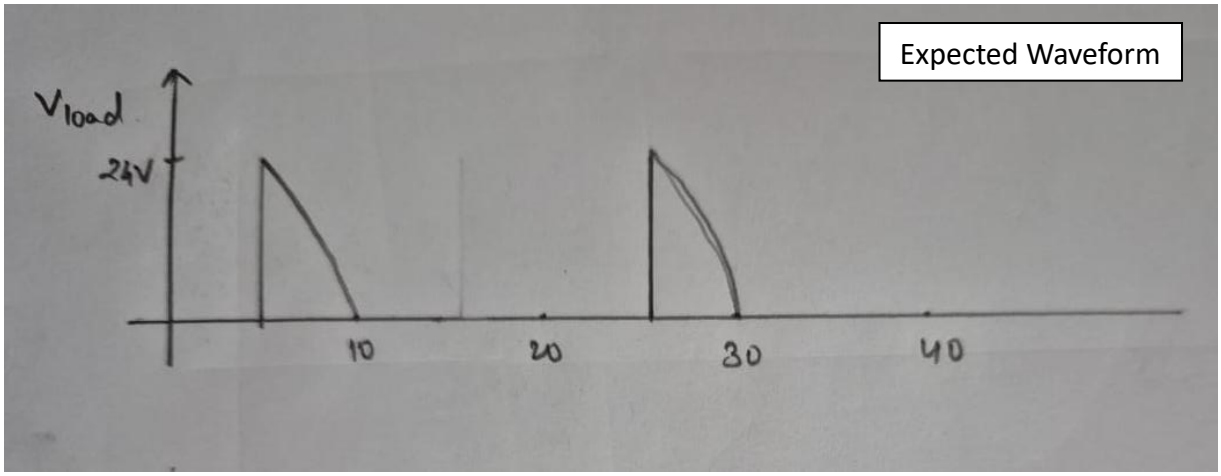
Example:
Let $V_m = 24V$ and $\alpha = 90°$:

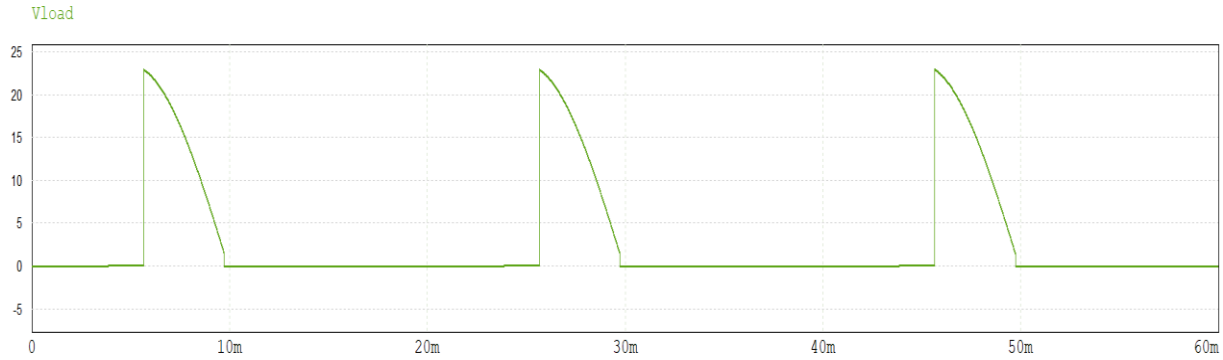
$$V_{avg} = \frac{24}{2\pi}(1 + \cos\ 90°) = \frac{24}{2\pi}(1 + 0) = 3.82V$$

In the simulation average value observed was **3.52V** (as shown in red)

Measure

	X1	X2	Δ	Average
Time	0.00000e+00	4.98039e-02	4.98039e-02	
Vload	6.89261e-04	4.41735e-03	3.72809e-03	3.52319e+00





Conclusion

The Ramp Firing Circuit successfully demonstrates a synchronized and controllable method of triggering an SCR in a single-phase half-controlled converter. The circuit uses a Zero Crossing Detector to align the control signals with the AC supply, a Ramp Generator to produce a linear voltage waveform for each half-cycle, and a Comparator to generate gate pulses based on the intersection of the ramp and a variable DC control voltage.

By varying the control voltage, the firing angle (α) of the SCR is linearly adjusted, resulting in a corresponding variation in the average output voltage, expressed as

$$V_{avg} = \frac{V_m}{2\pi}(1 + \cos\ \alpha)$$

This confirms that the ramp–comparator method provides smooth, accurate, and stable control of the SCR conduction period. The observed waveforms from the simulation validate the correct synchronization, pulse shaping, and gating behaviour. Hence, the designed circuit effectively achieves phase control and can be used in practical applications like DC motor control, voltage regulation, and power converters.