



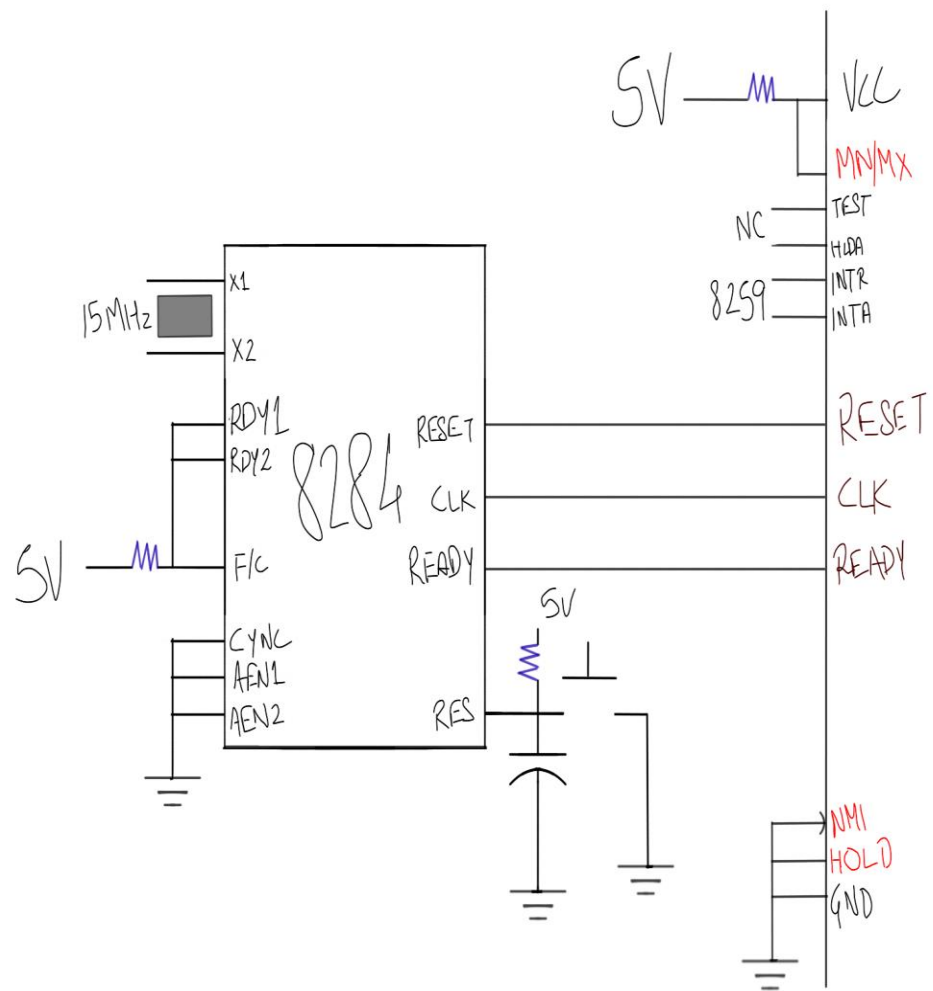
Design

Design Problem number-18

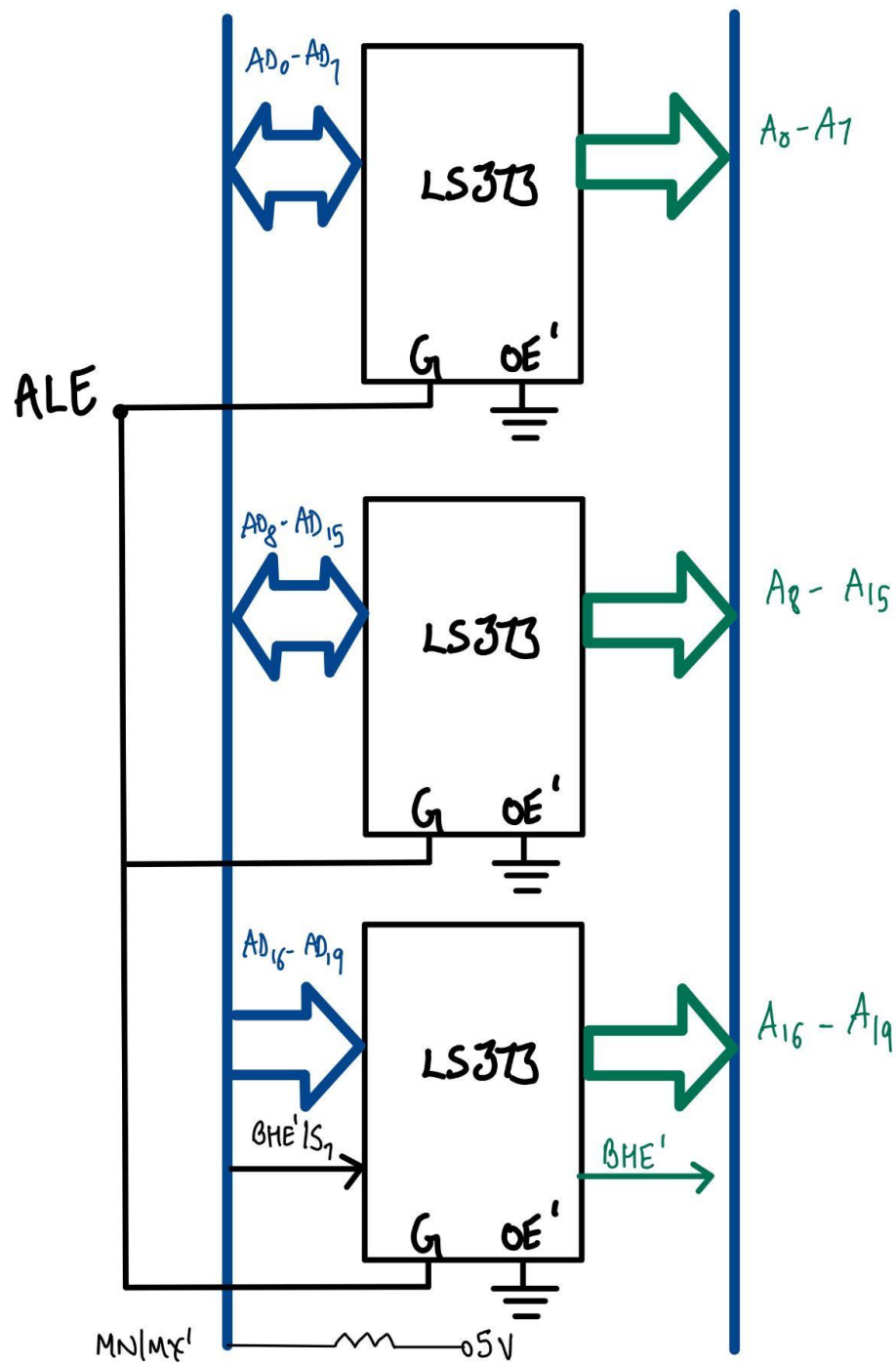
Submitted by Group-4

Group Members

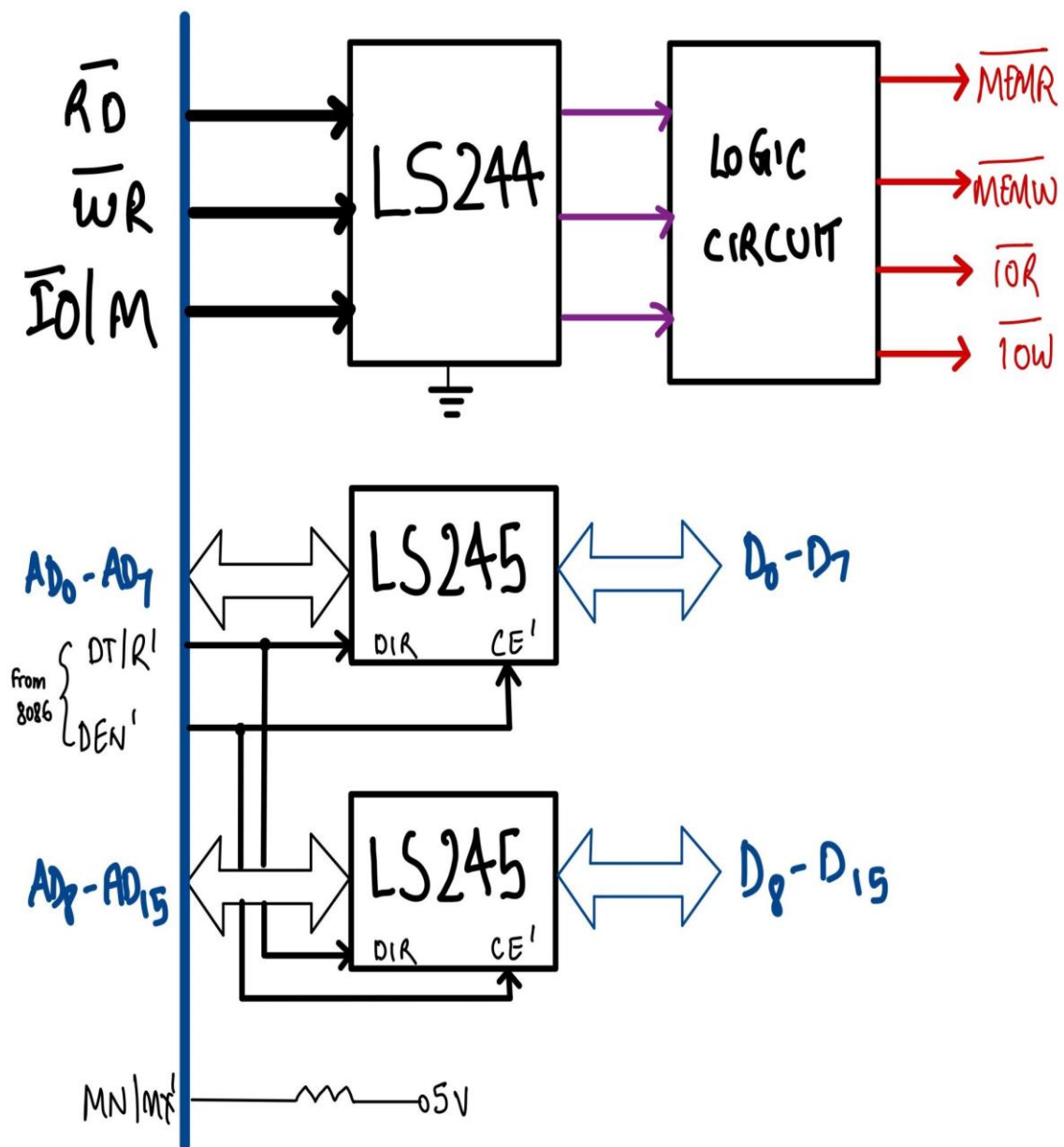
1. Ashutosh Gupta	2019AAPS0223G
2. Pranav Goyal	2019A8PS0548G
3. Sanskar Jain	2019AAPS0333G
4. Siddharth Barnwal	2019A7PS0114G
5. Sparsh Kachhadiya	2019A8PS0491G
6. Tanmay Bhonsale	2018B5A70903G



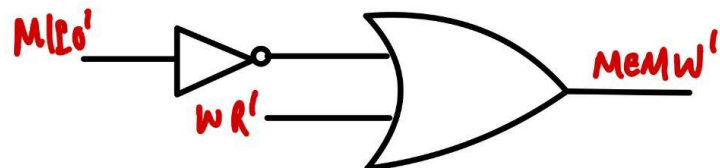
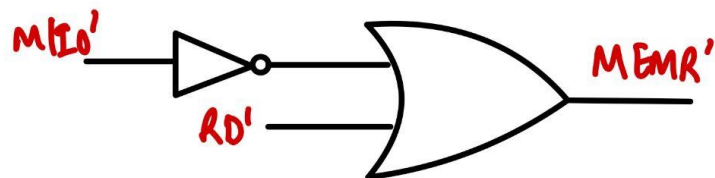
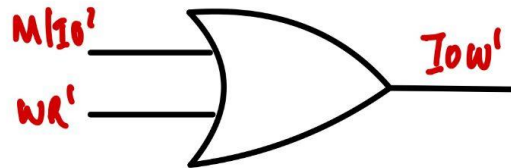
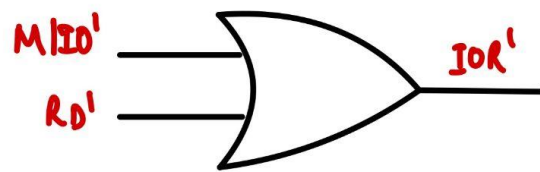
Inputs to 8086



System Bus OF 8086 (Address)

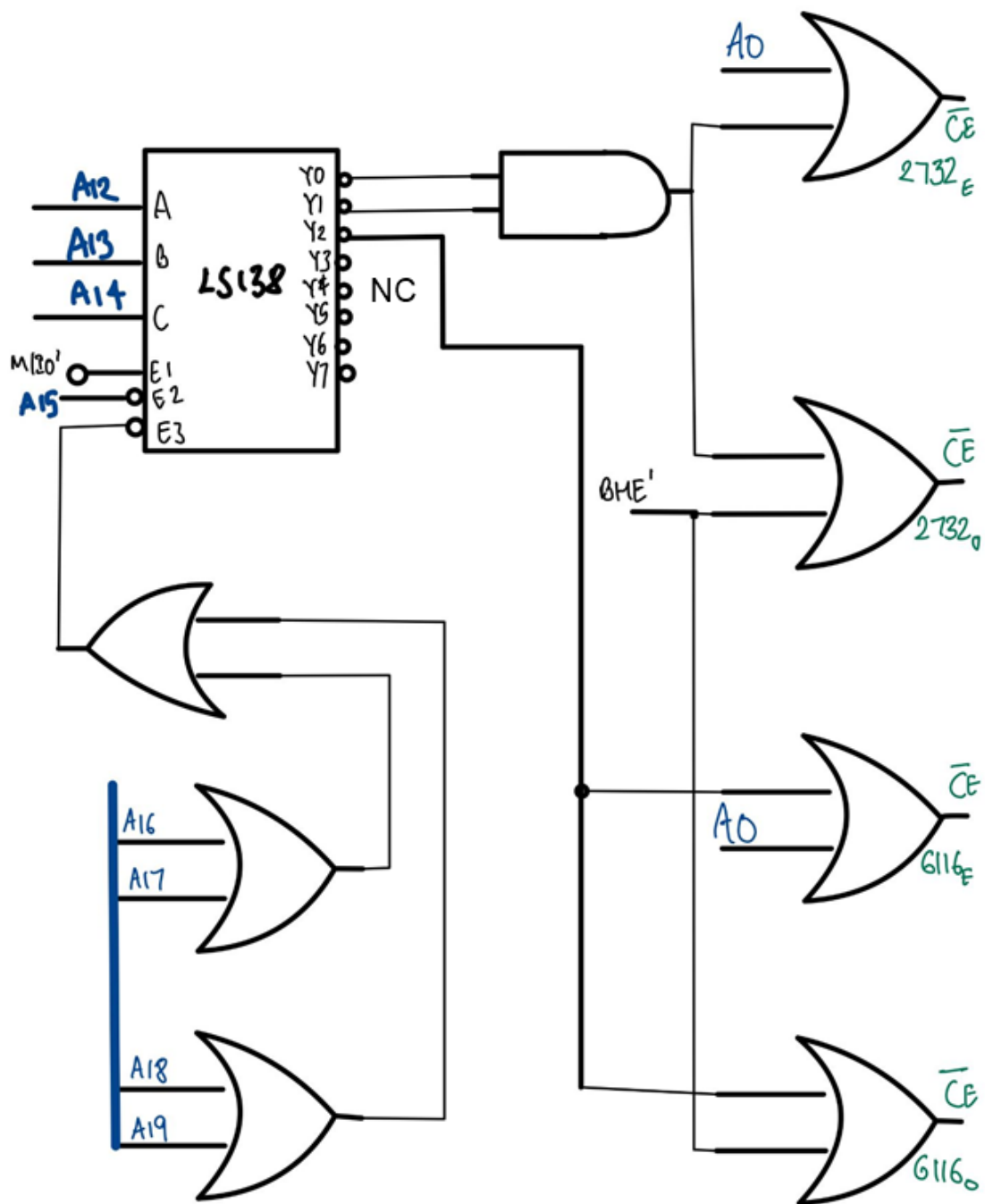


System Bus (Data + Control)

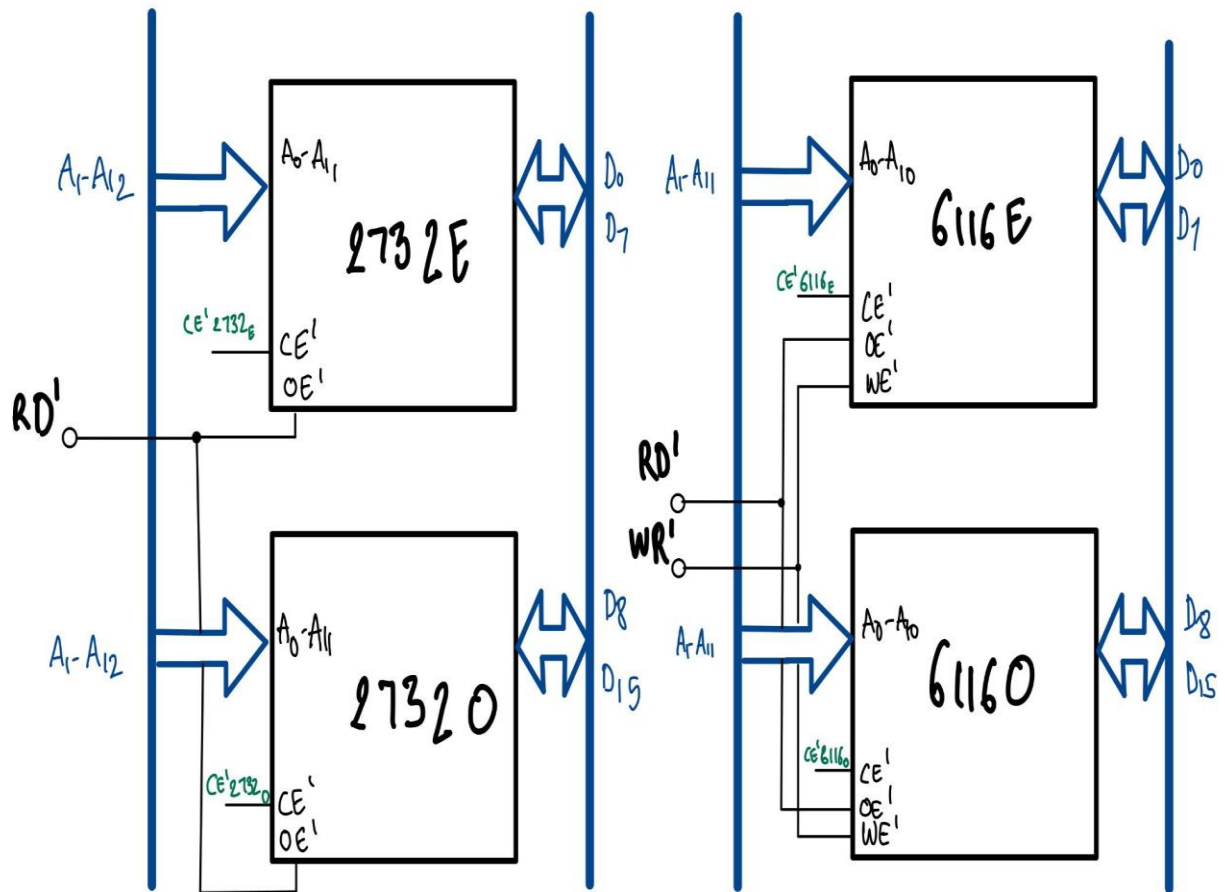


M / IO'	RD'	WR'	Bus Cycle
1	0	1	$MEMR'$
1	1	0	$MEMW'$
0	0	1	IOR'
0	1	0	IOW'

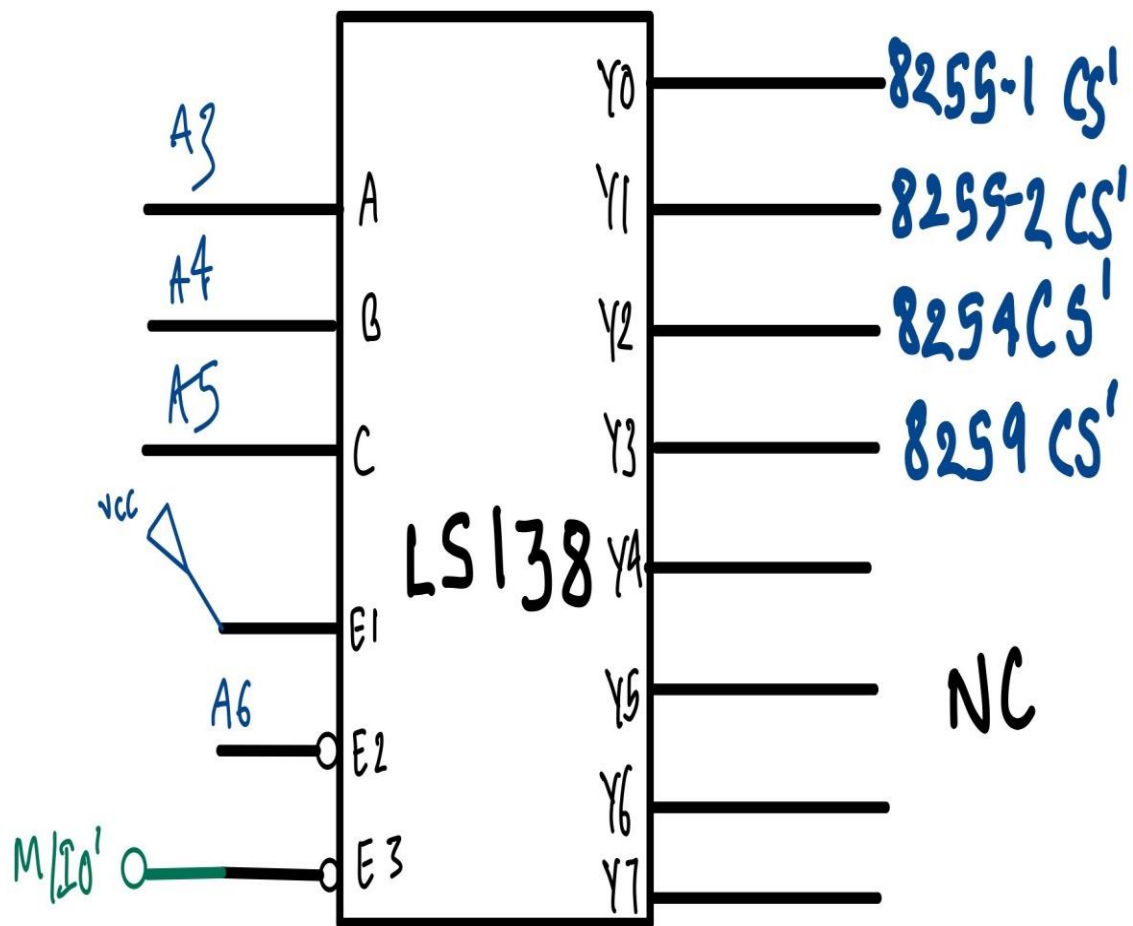
System Bus Logic



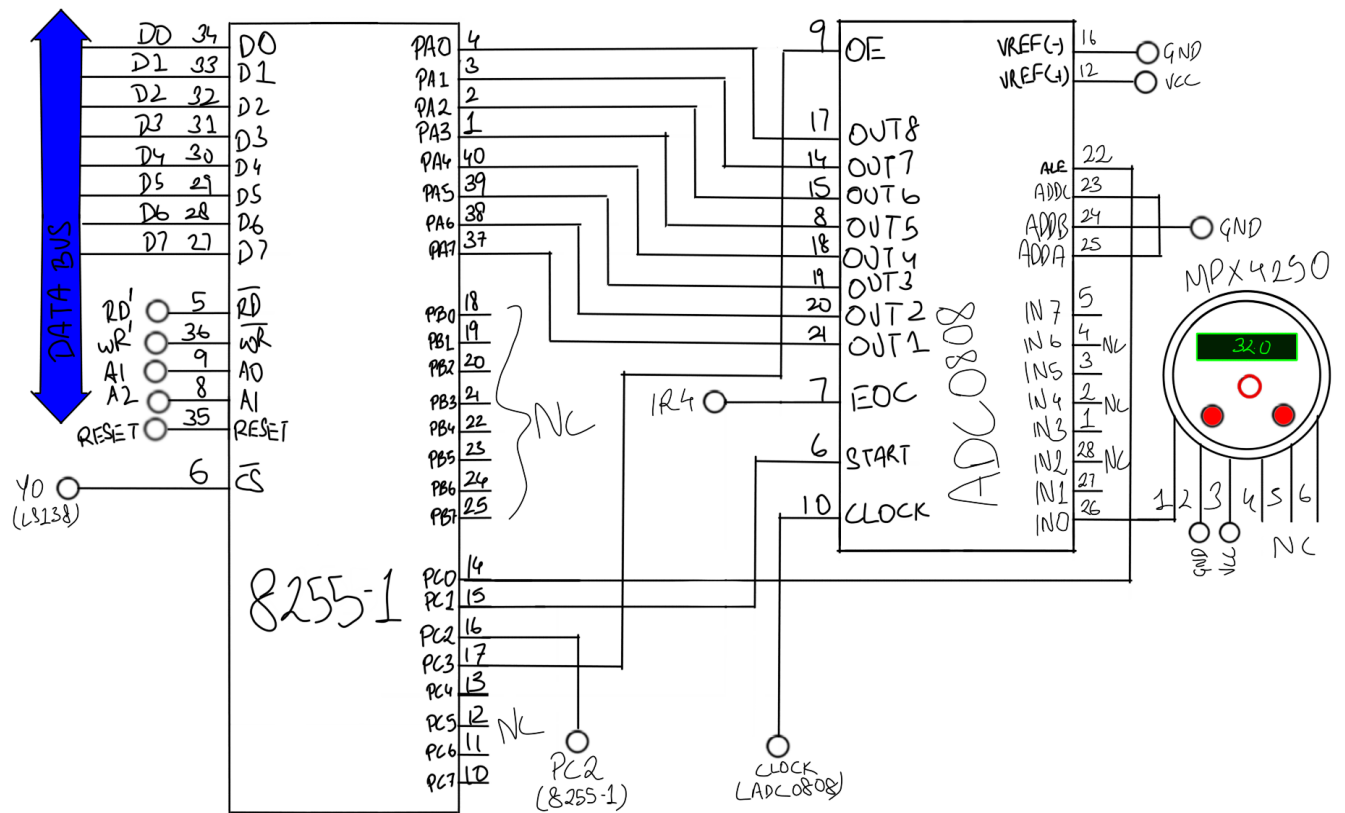
Memory Decoder



Memory Interfacing

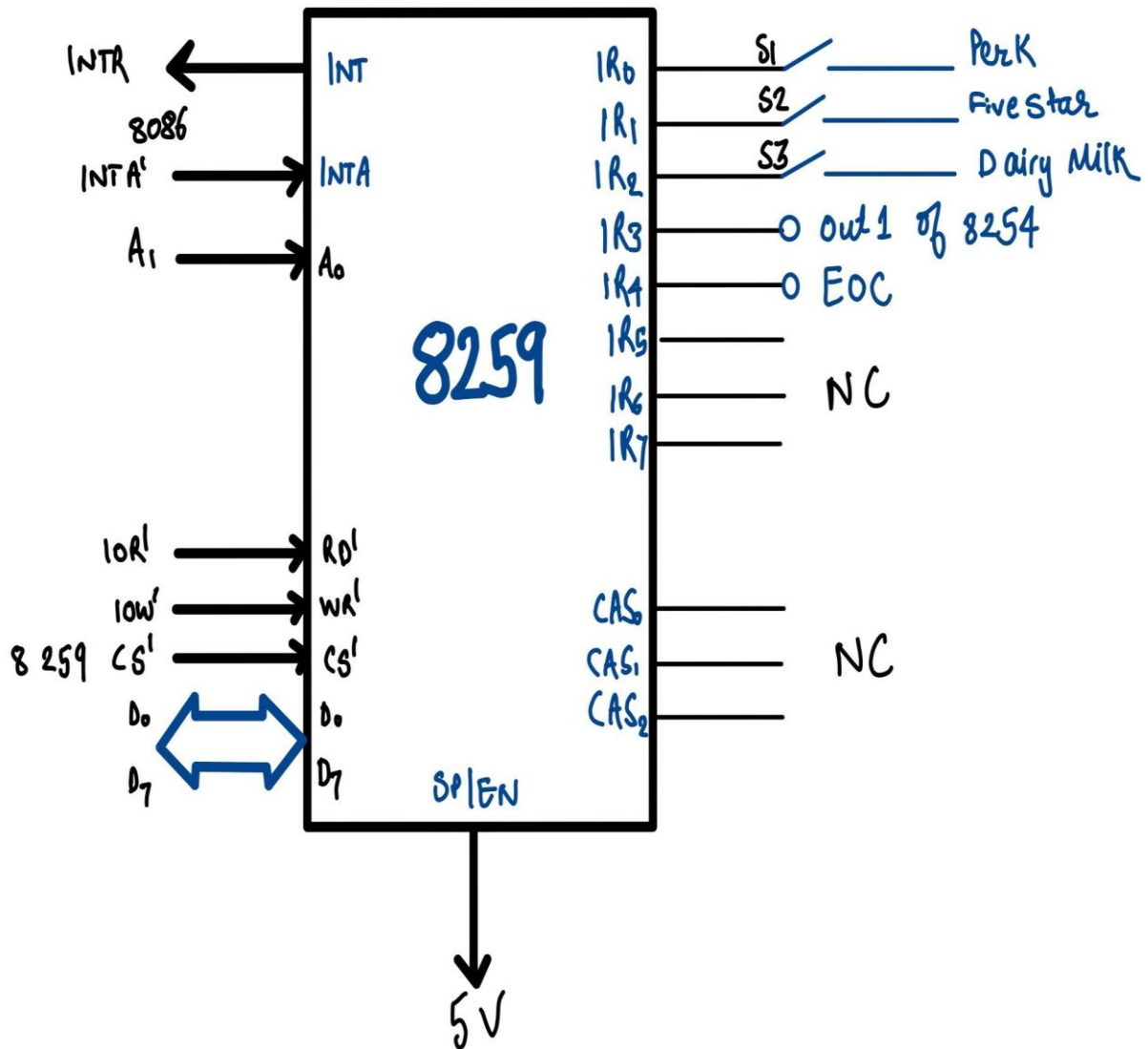


I/O Decoder

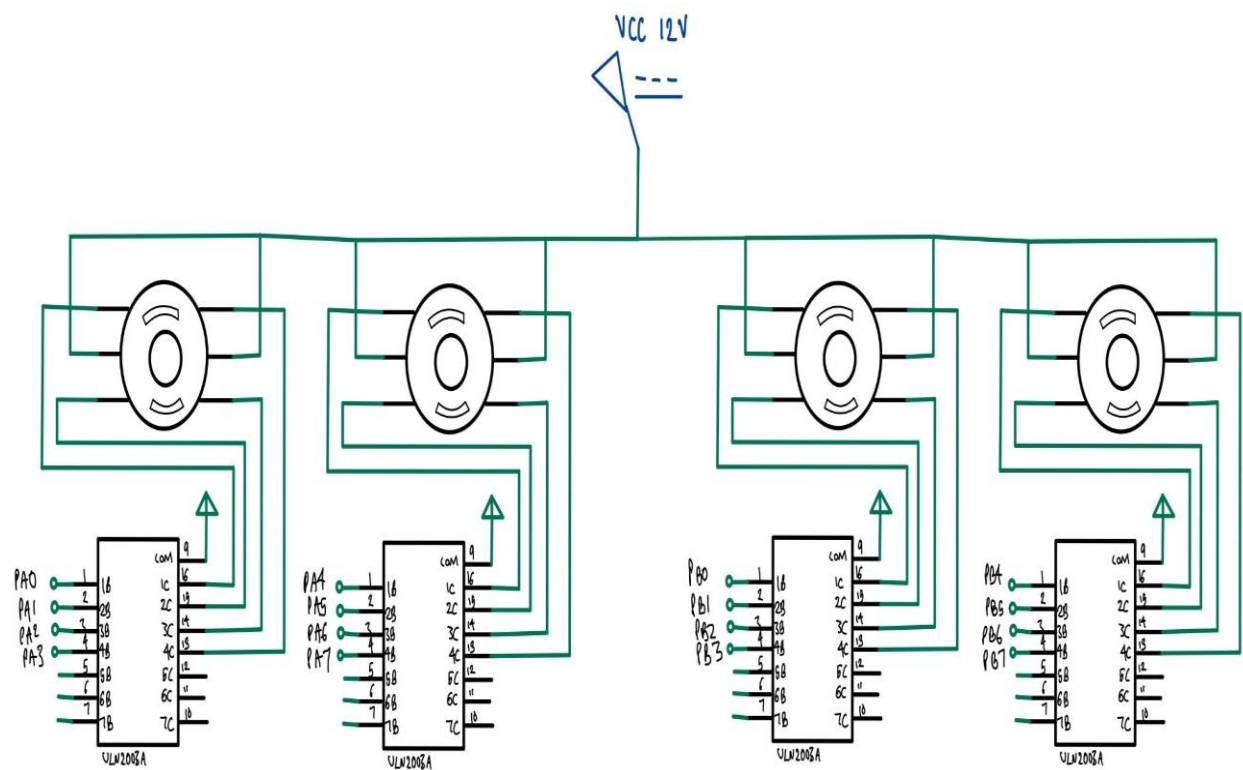


8255 -1

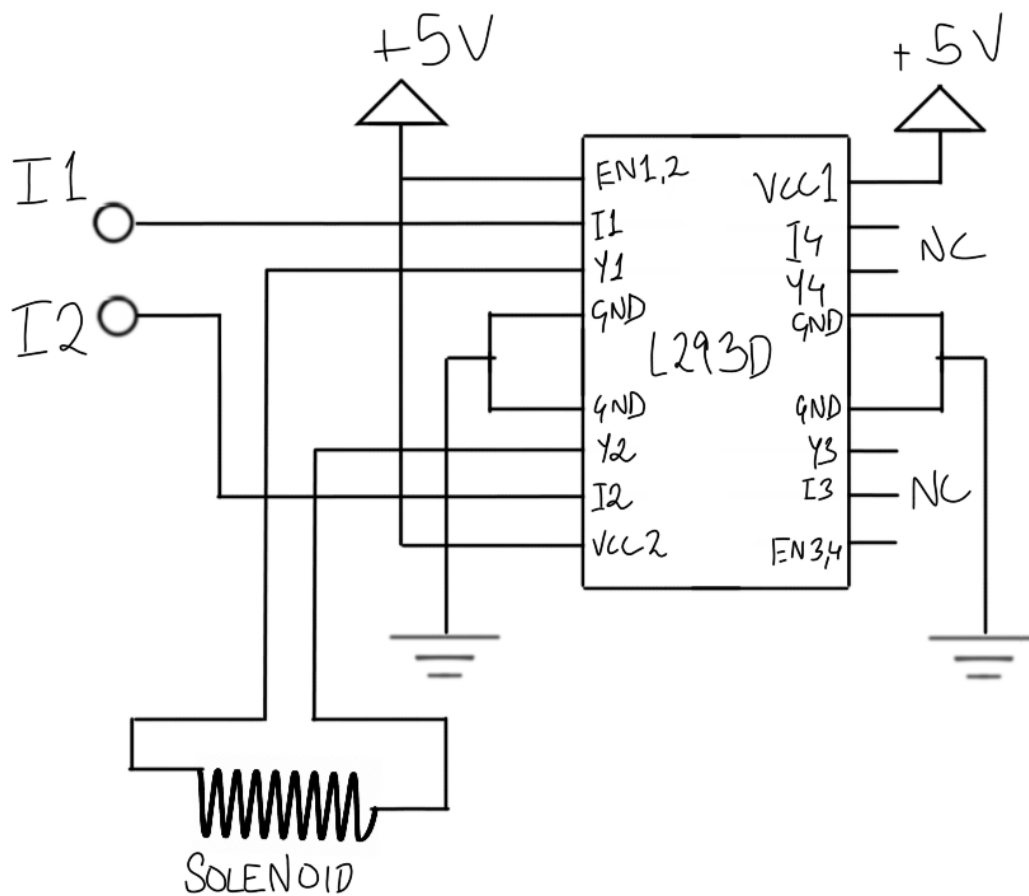




8259



Stepper Motors



Solenoid
(connected from Port B of 8255-1)