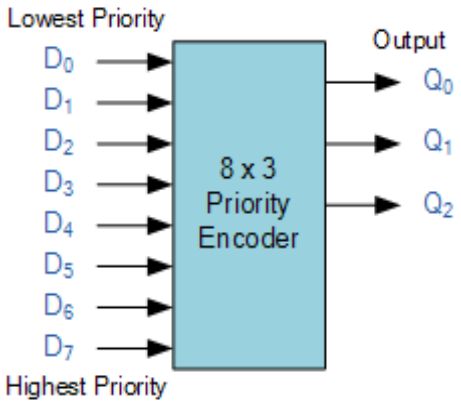
Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

Name of the participant : Ashutosh Gupta

Title of the circuit : 8X3 Priority Encoder

Theory/Description :



Priority encoders are available in standard IC form and the TTL 74LS148 is an 8-to-3 bit priority encoder which has eight active LOW (logic “0”) inputs and provides a 3-bit code of the highest ranked input at its output.

Priority encoders output the highest order input first for example, if input lines “D2“, “D3” and “D5” are applied simultaneously the output code would be for input “D5” (“101”) as this has the highest order out of the 3 inputs. Once input “D5” had been removed the next highest output code would be for input “D3” (“011”), and so on.

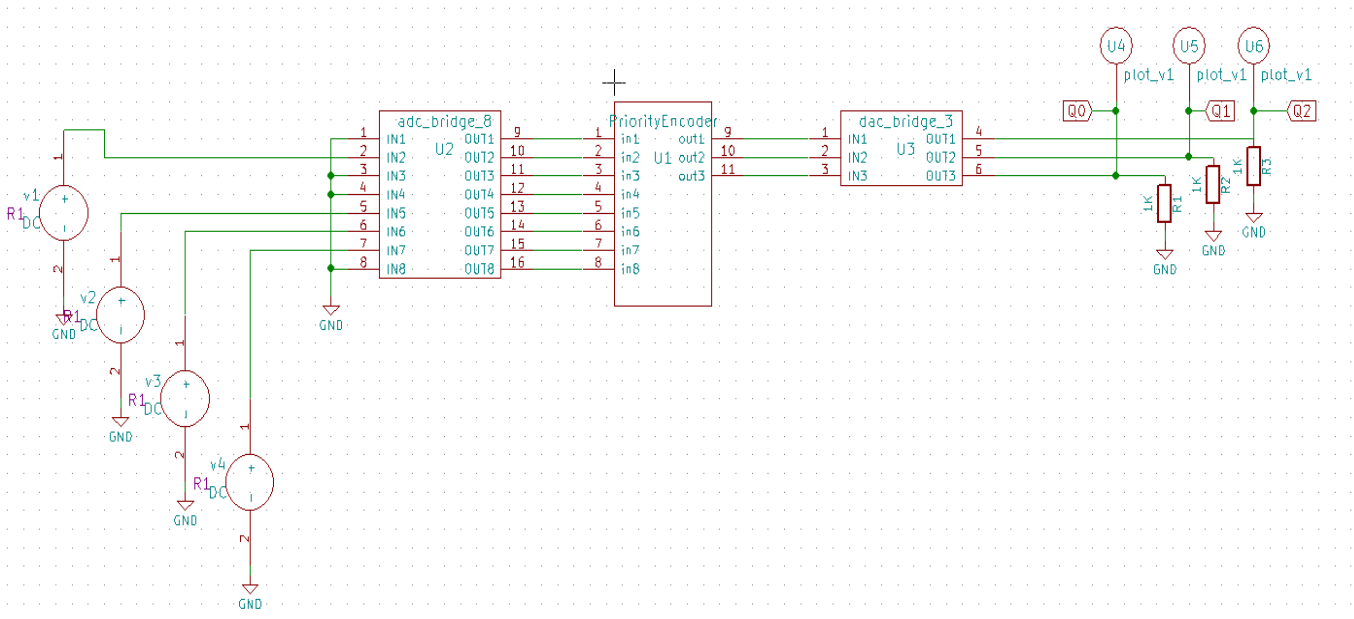
The truth table for a 8-to-3 bit priority encoder is given as:

Digital Inputs								Binary Output		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	**1**	0	0	0
0	0	0	0	0	0	**1**	X	0	0	1
0	0	0	0	0	**1**	X	X	0	1	0
0	0	0	0	**1**	X	X	X	0	1	1
0	0	0	**1**	X	X	X	X	1	0	0
0	0	**1**	X	X	X	X	X	1	0	1
0	**1**	X	X	X	X	X	X	1	1	0
1	X	X	X	X	X	X	X	1	1	1

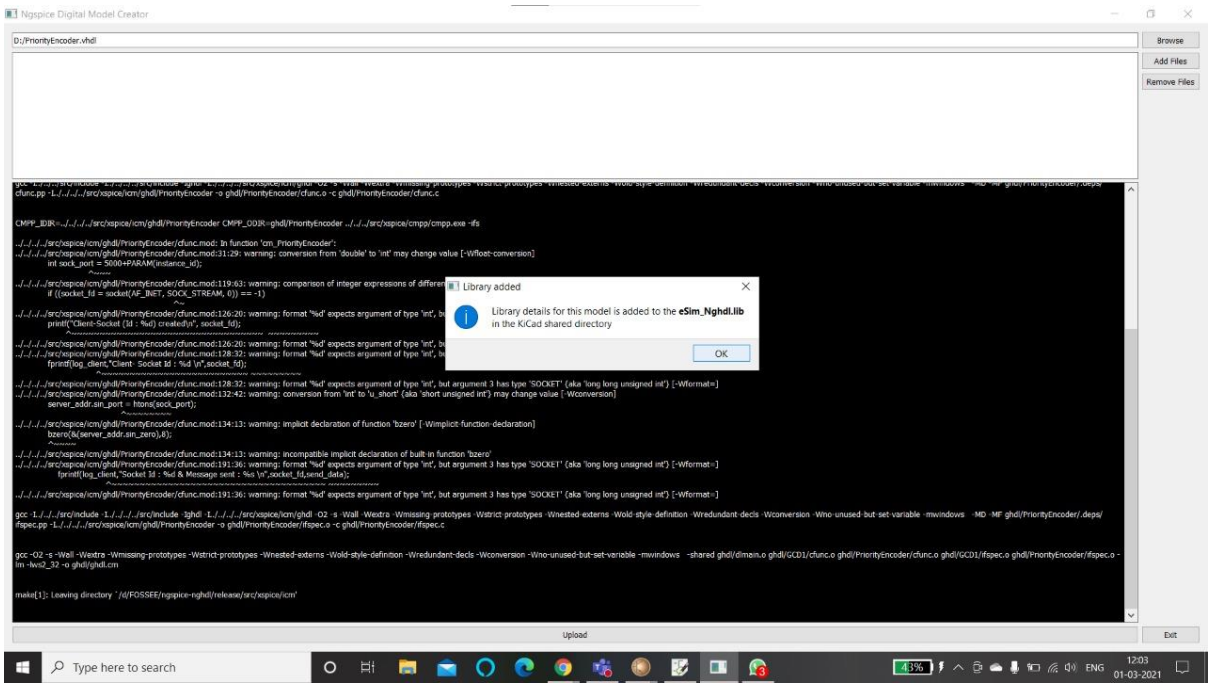
Where X equals “don’t care”, that is it can be at a logic “0” level or at a logic “1” level.

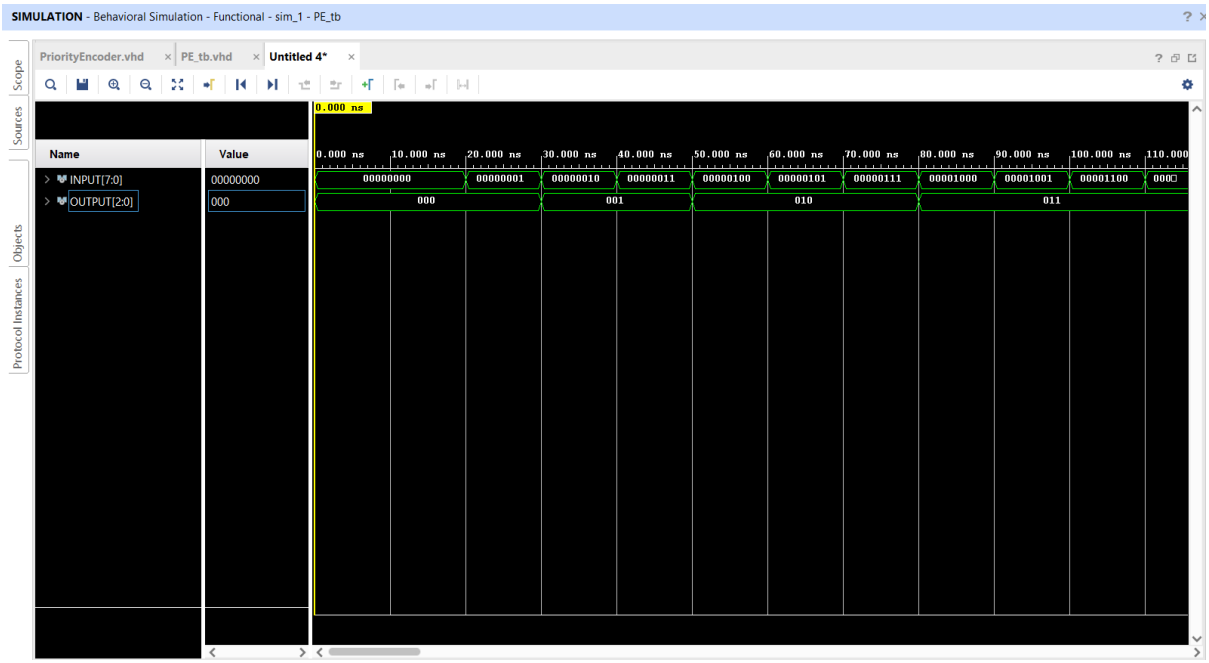
The VHDL implementation is done using the Behavioral Modeling.

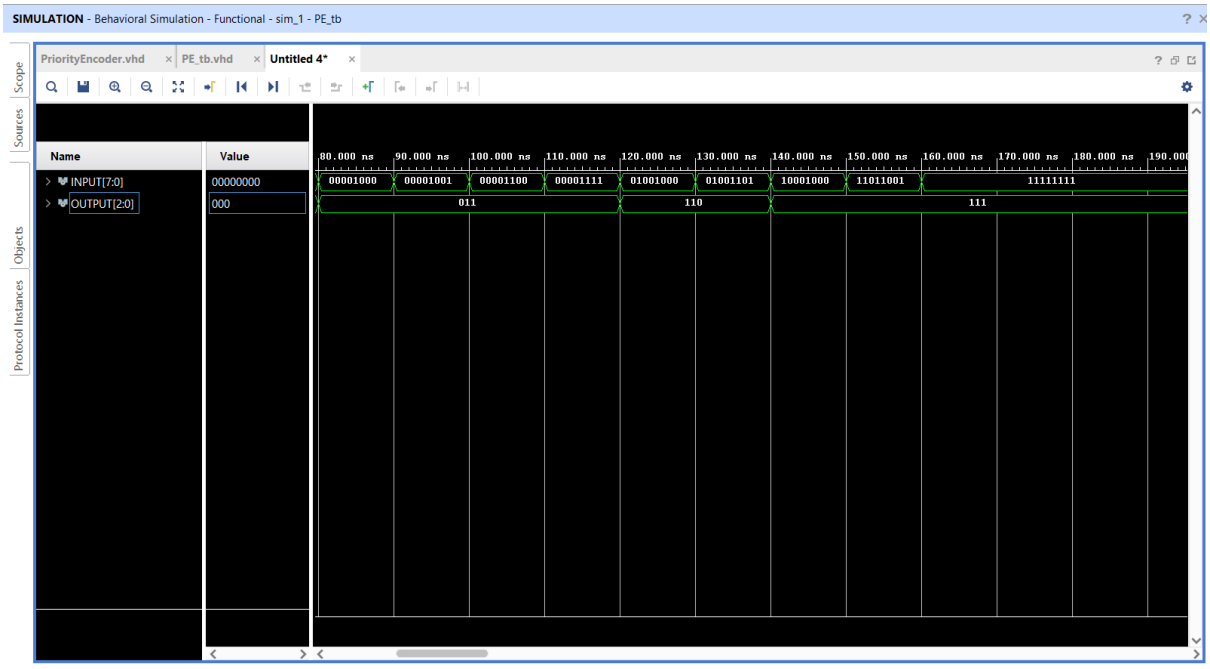
Circuit Diagram(s) :



Results (Input, Output waveforms and/or Multimeter readings) :







Source/Reference(s) :

https://www.electronics-tutorials.ws/combination/comb_4.html

https://www.geeksforgeeks.org/encoder-in-digital-logic/