HSCD LAB Assignment No. 1

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Date : 18/08/2024

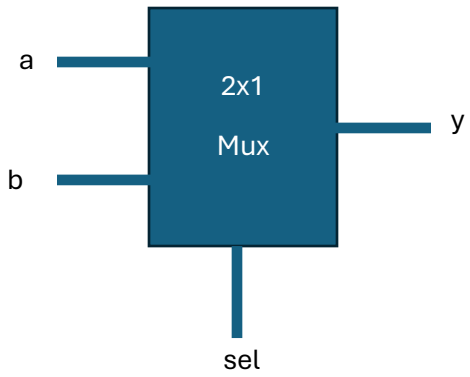
Place : Pune, Maharashtra

Multiplexer Design

What is multiplexer?

Multiplexer is a combinational logic circuit used to select only one input among several inputs based on selection lines.

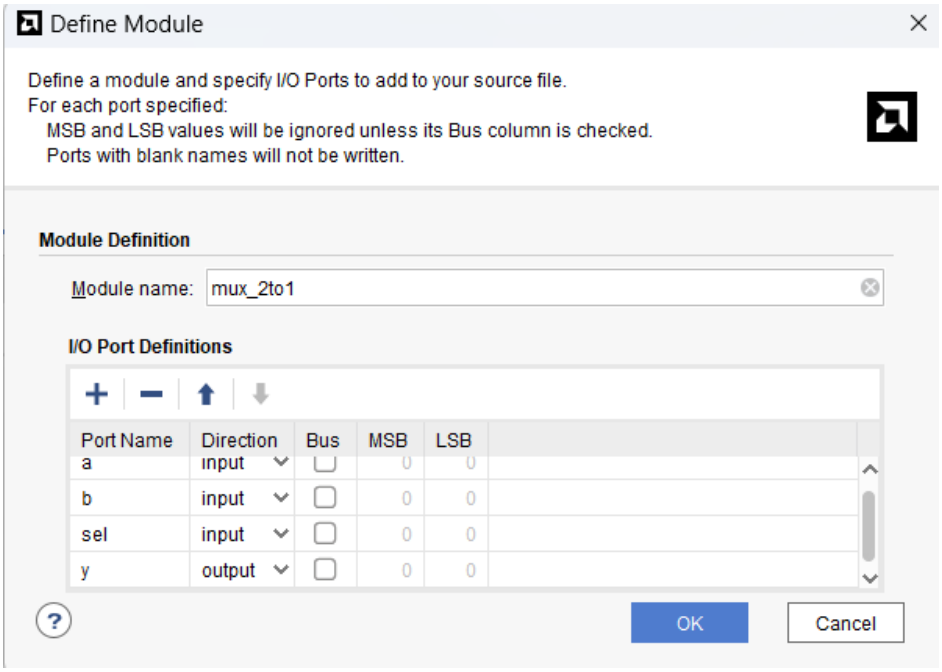
Task 1 : Design 2-to-1 Multiplexer



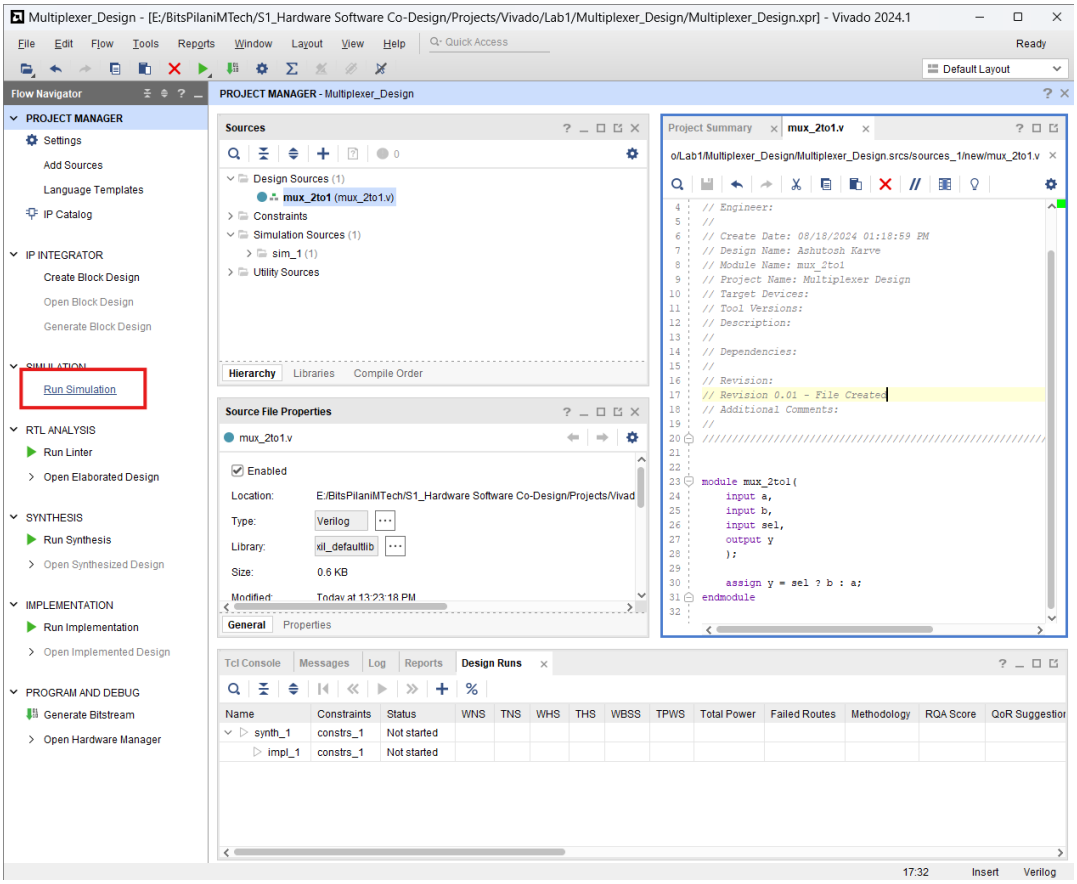
Sel	Y
0	a
1	b

sel	a	b	y
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

DEFINE MODULE >>

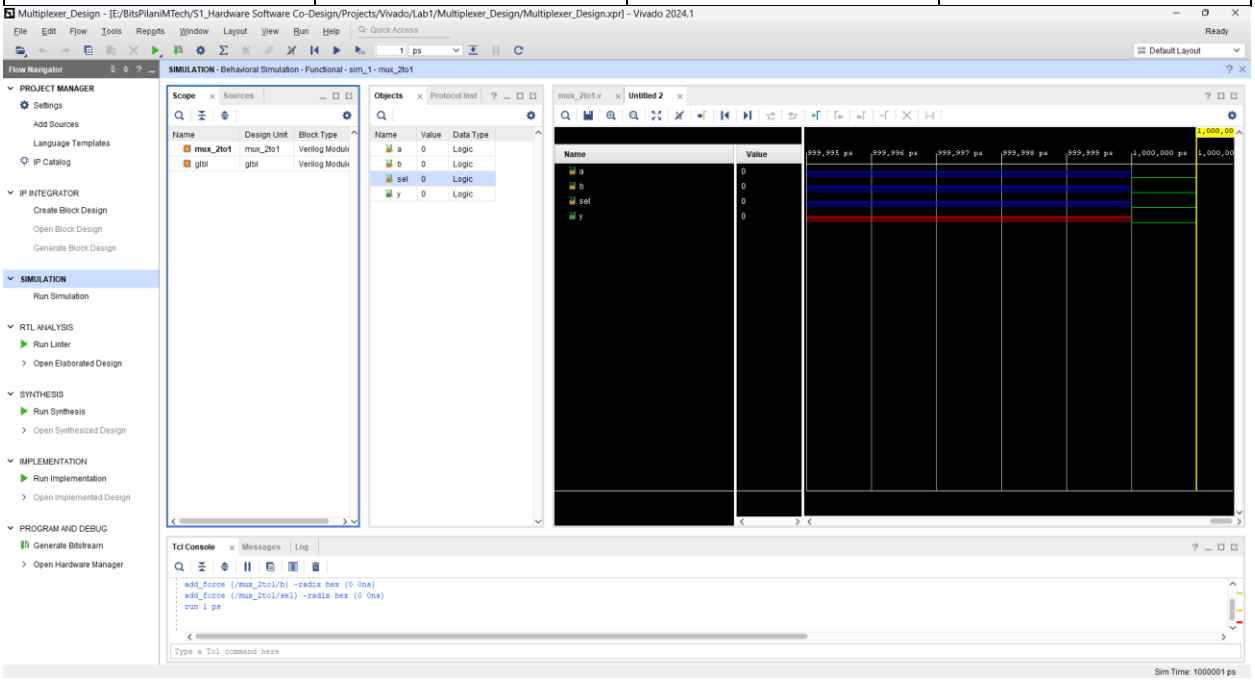


Design Source file >>



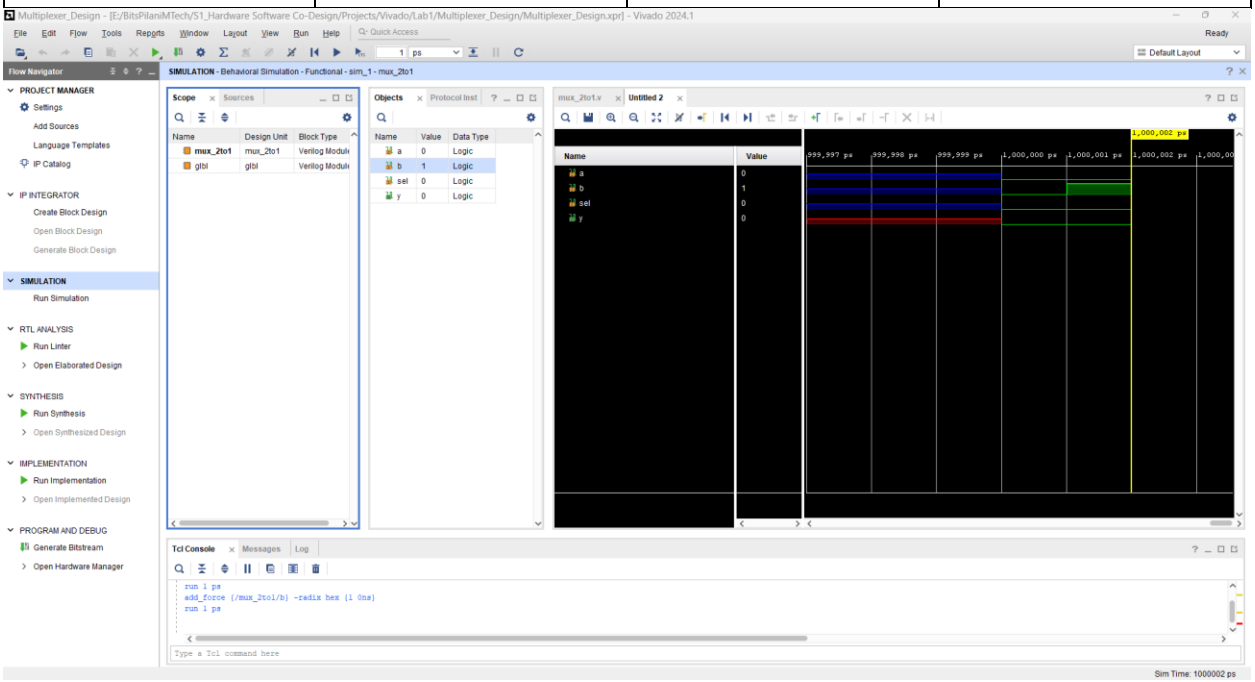
SIMULATION RESULTS 1 >>

Sel	a	b	Y
0	0	0	0



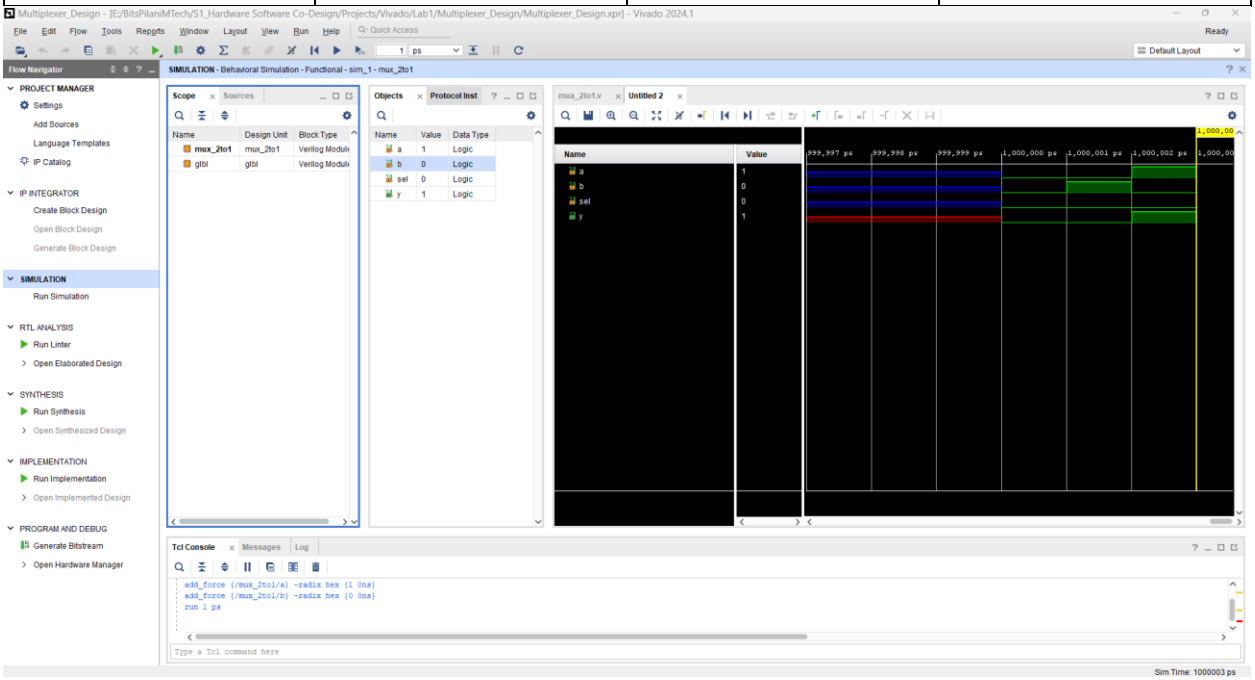
SIMULATION RESULTS 2 >>

Sel	a	b	Y
0	0	1	0



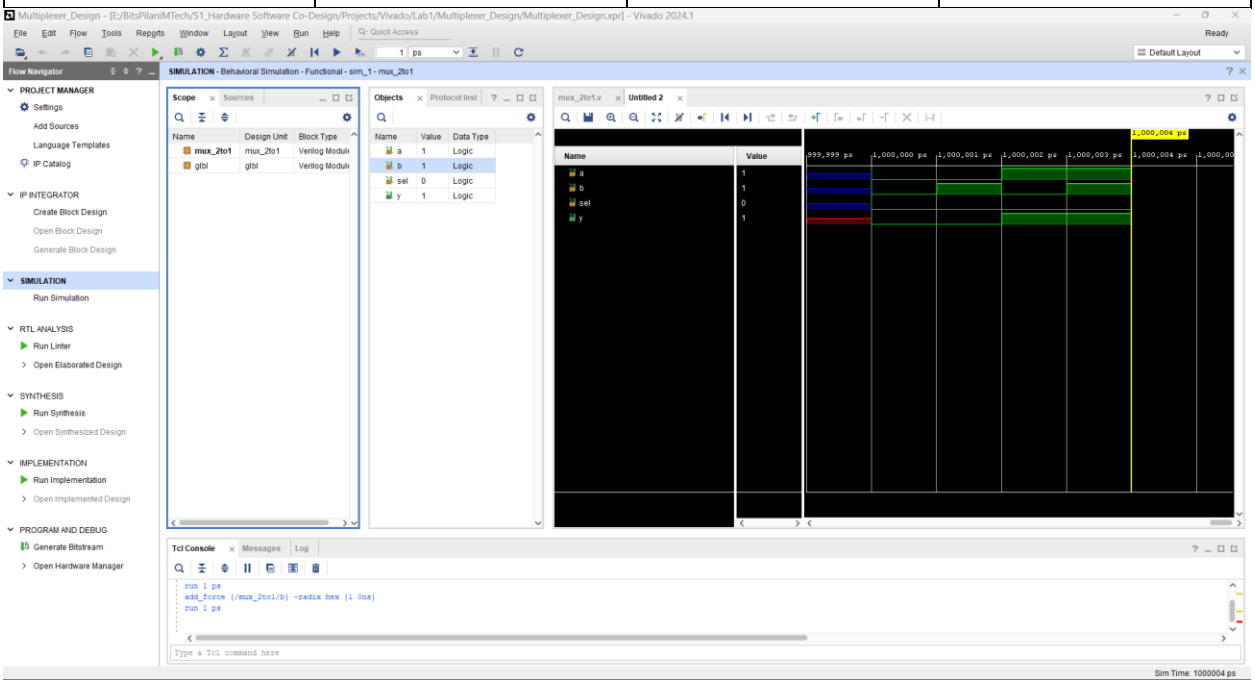
SIMULATION RESULTS 3 >>

Sel	a	b	Y
0	1	0	1



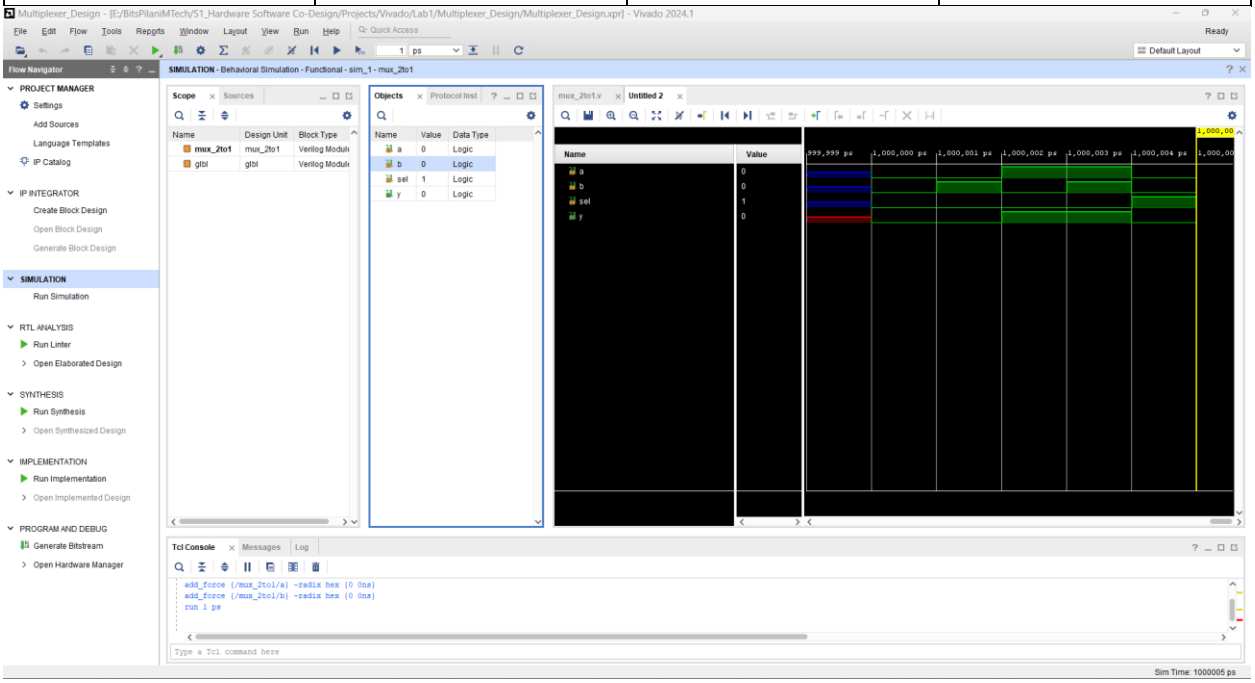
SIMULATION RESULTS 4 >>

Sel	a	b	Y
0	1	1	1



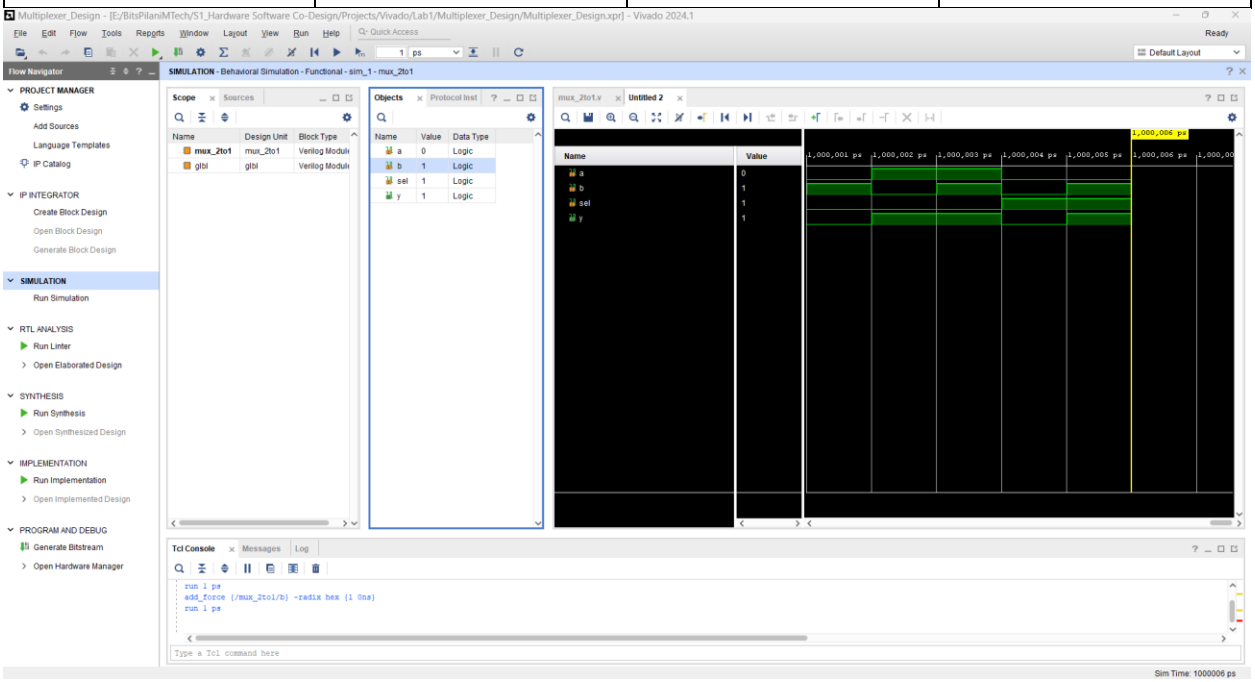
SIMULATION RESULTS 5 >>

Sel	a	b	Y
1	0	0	0



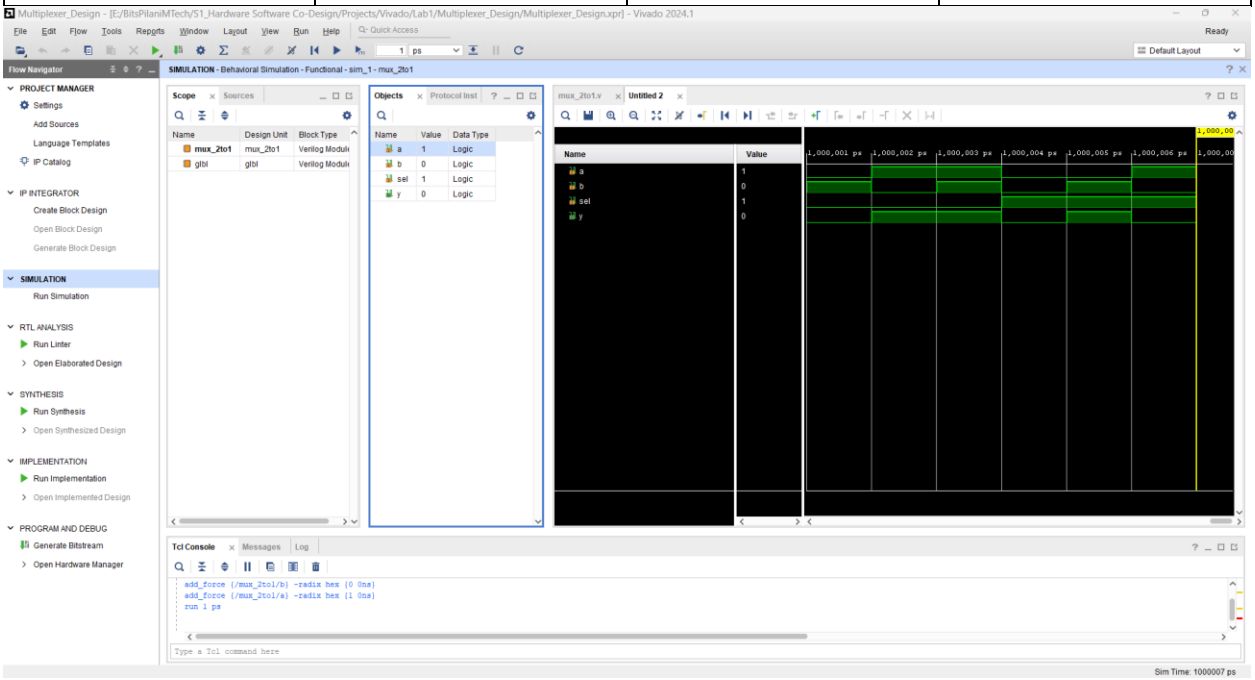
SIMULATION RESULTS 6 >>

Sel	a	b	Y
1	0	1	1



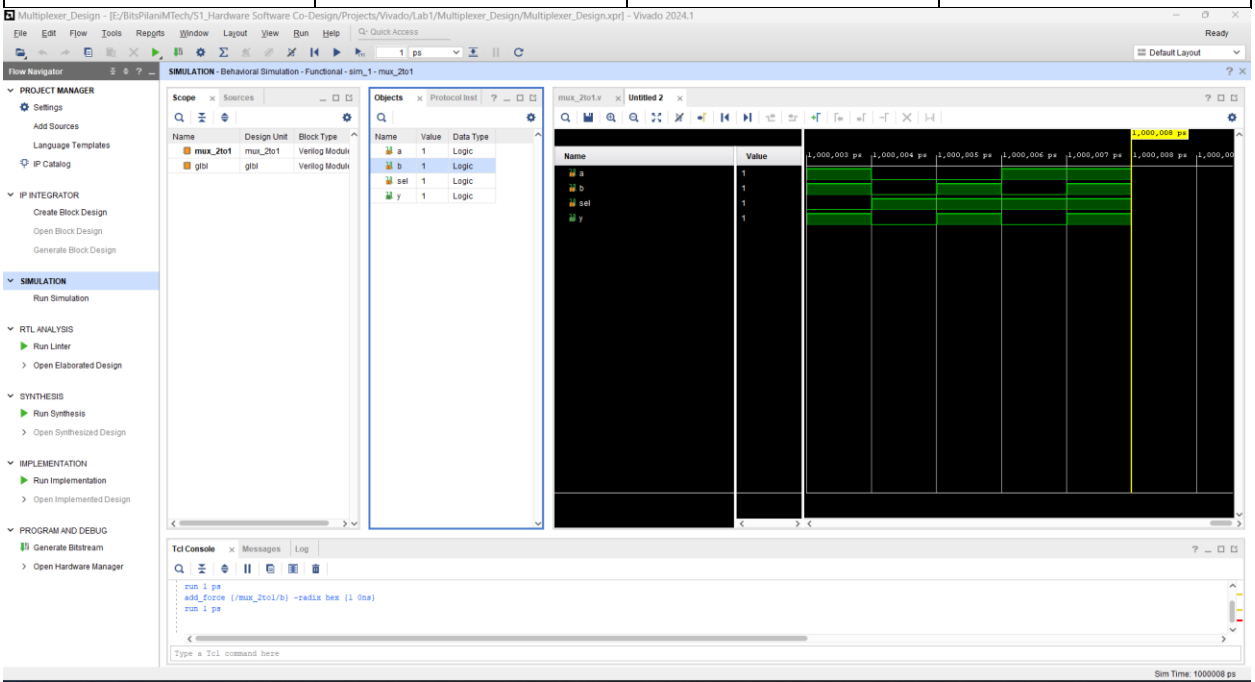
SIMULATION RESULTS 7 >>

Sel	a	b	Y
1	1	0	0

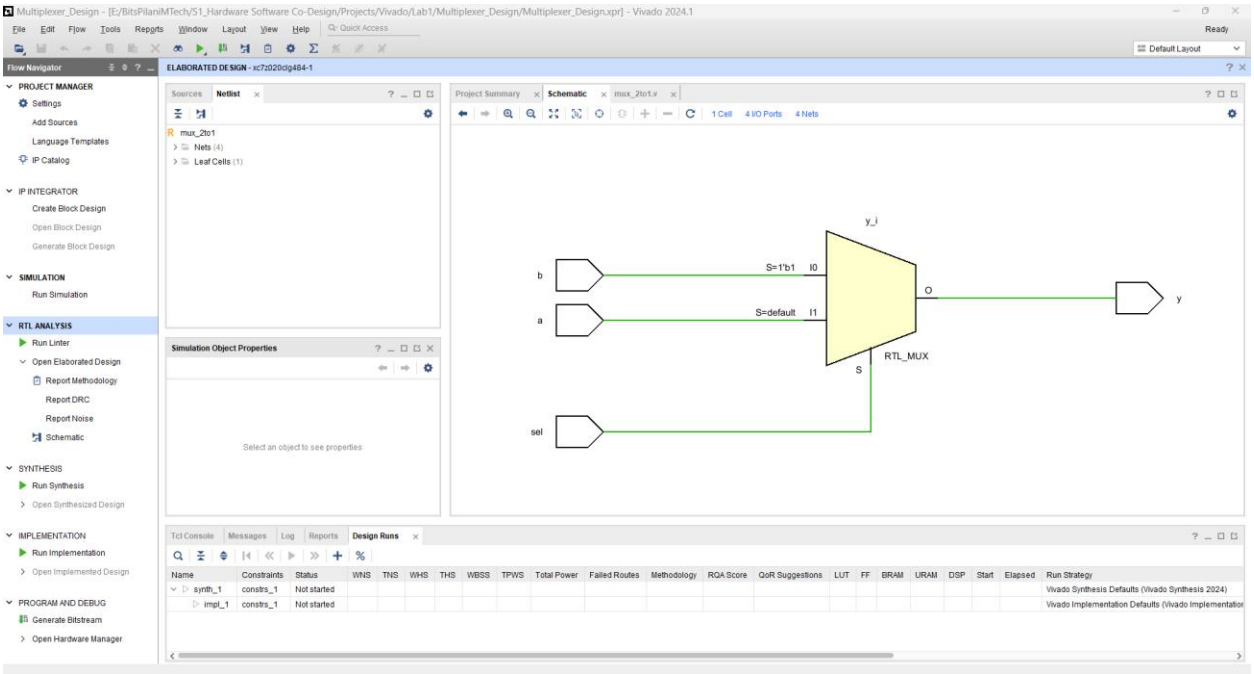


SIMULATION RESULTS 8 >>

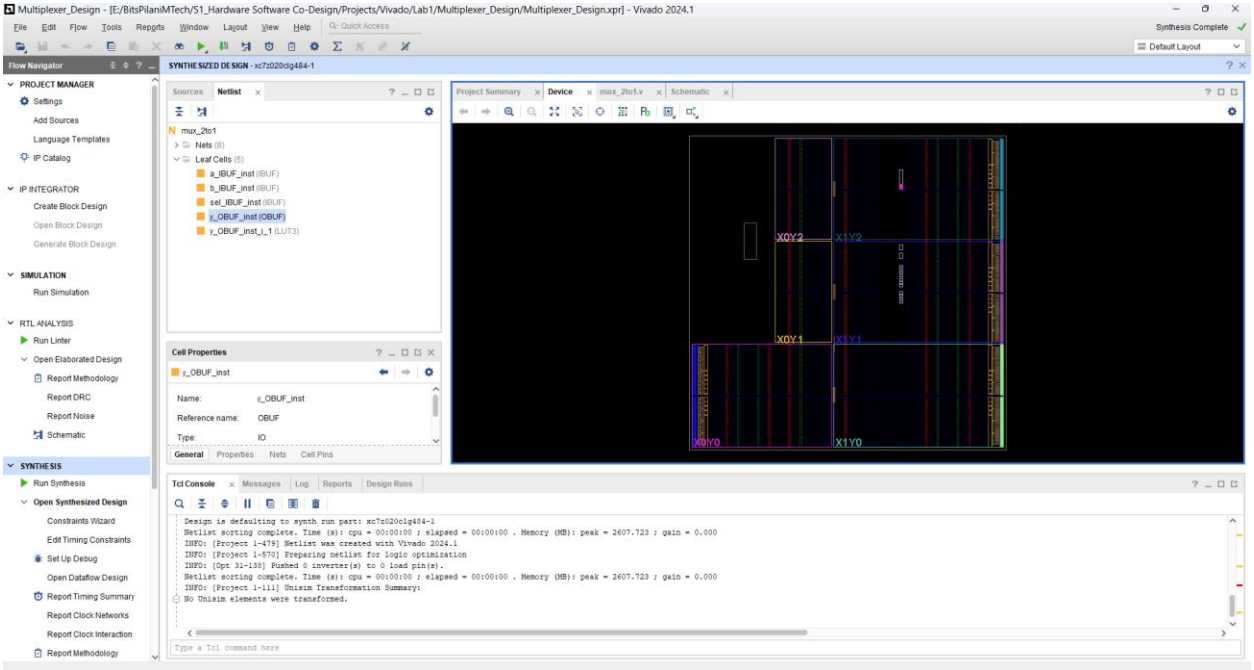
Sel	a	b	Y
1	1	1	1



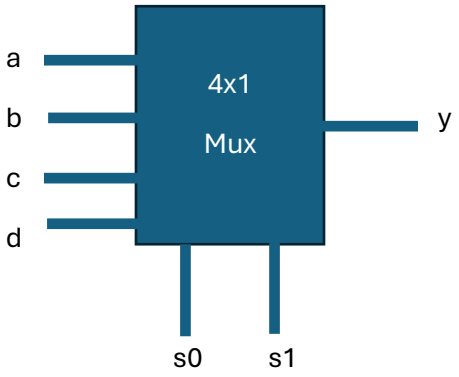
ELABORATED DESIGN >>



SYNTHESIZED DESIGN >>



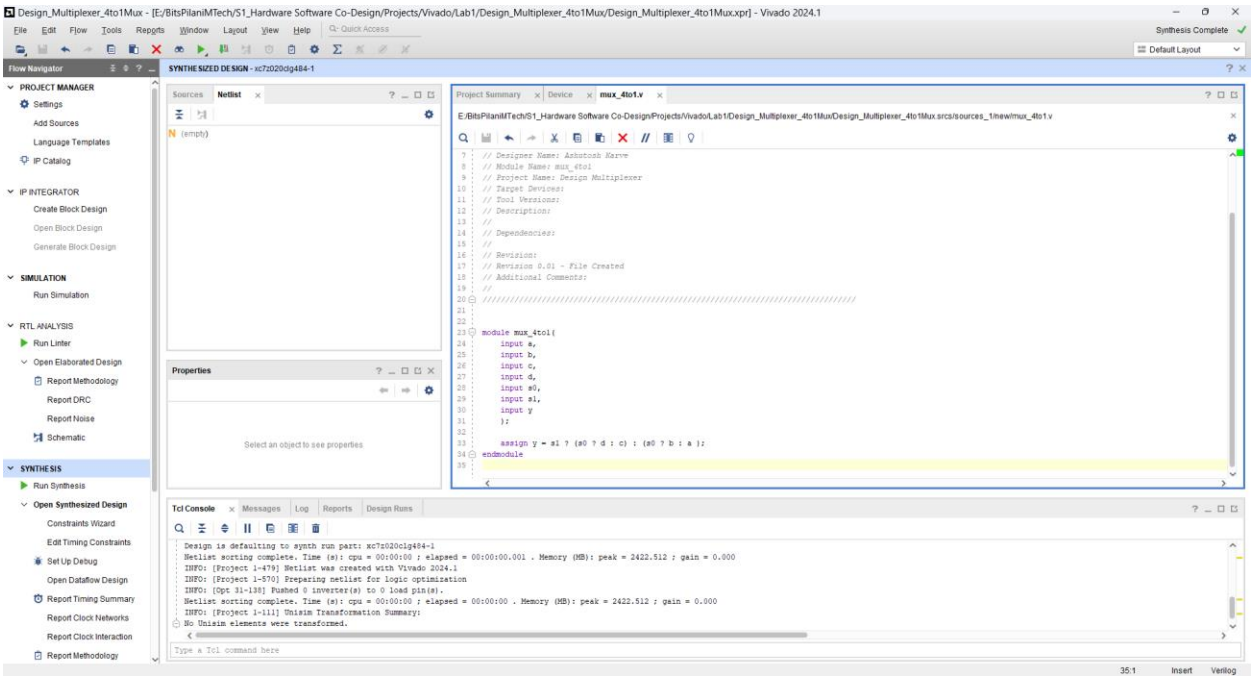
Task 2 : Design 4-to-1 Multiplexer



Truth Table

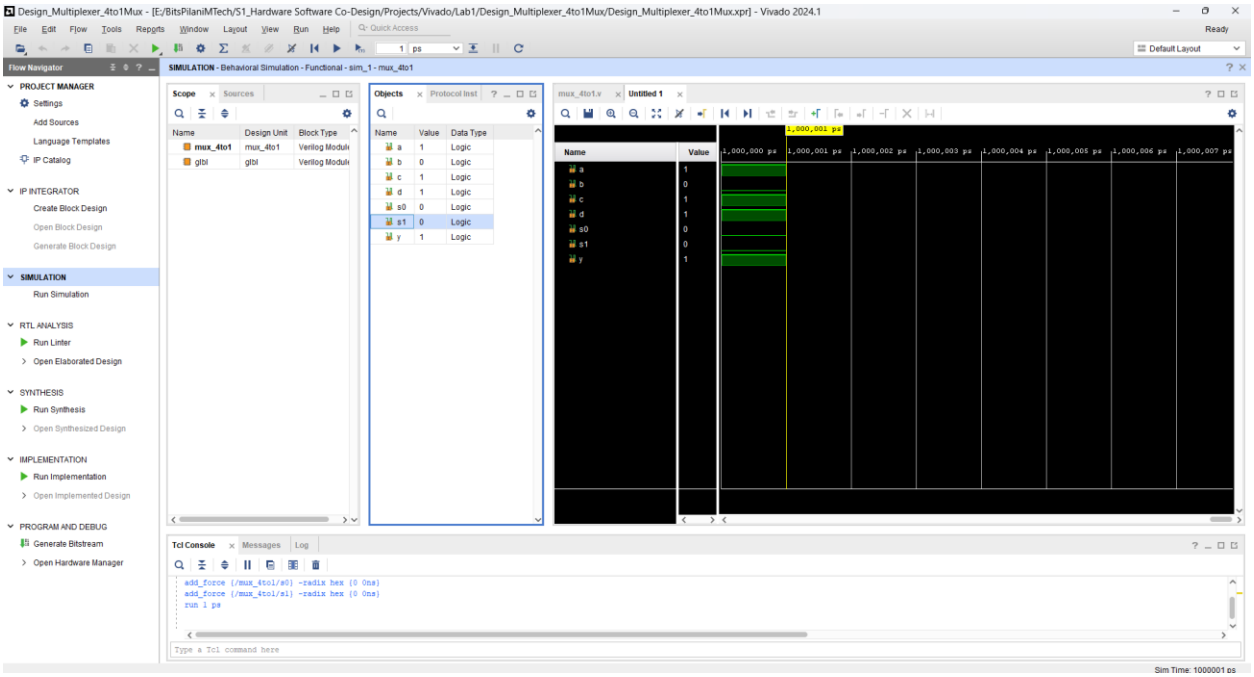
s1	s0	y
0	0	a
0	1	b
1	0	c
1	1	d

DESIGN SOURCE CODE >>



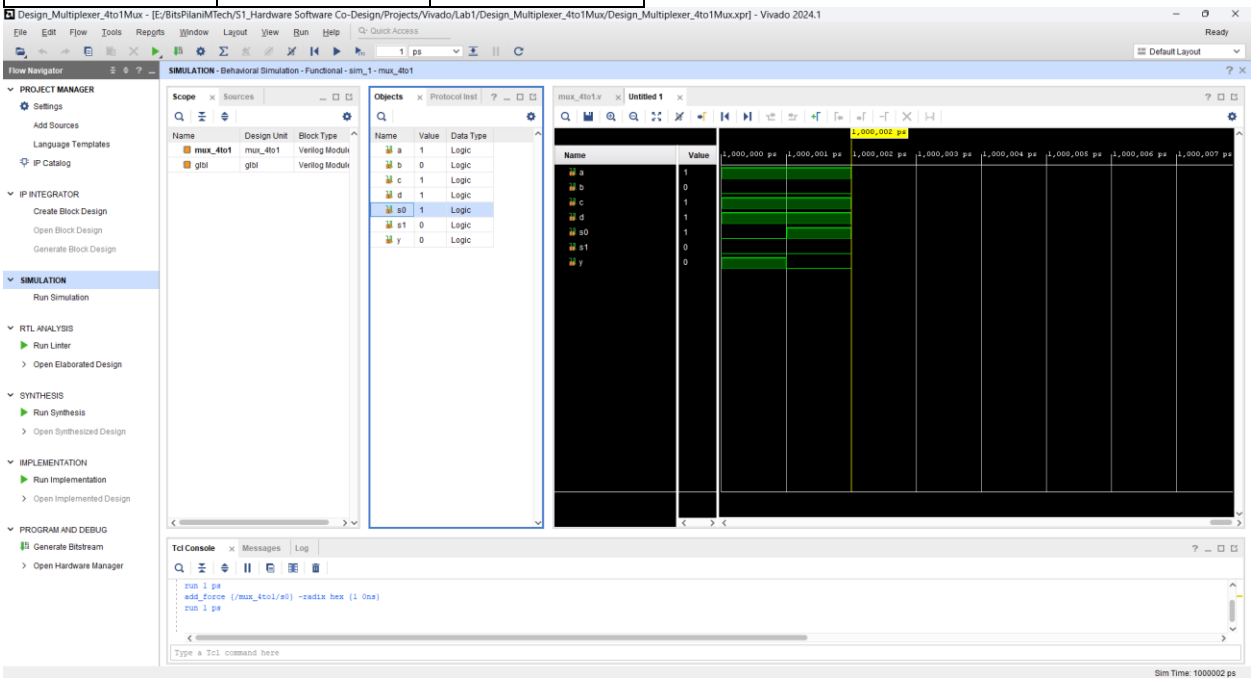
SIMULATION RESULTS 1 >>

s1	s0	y
0	0	a



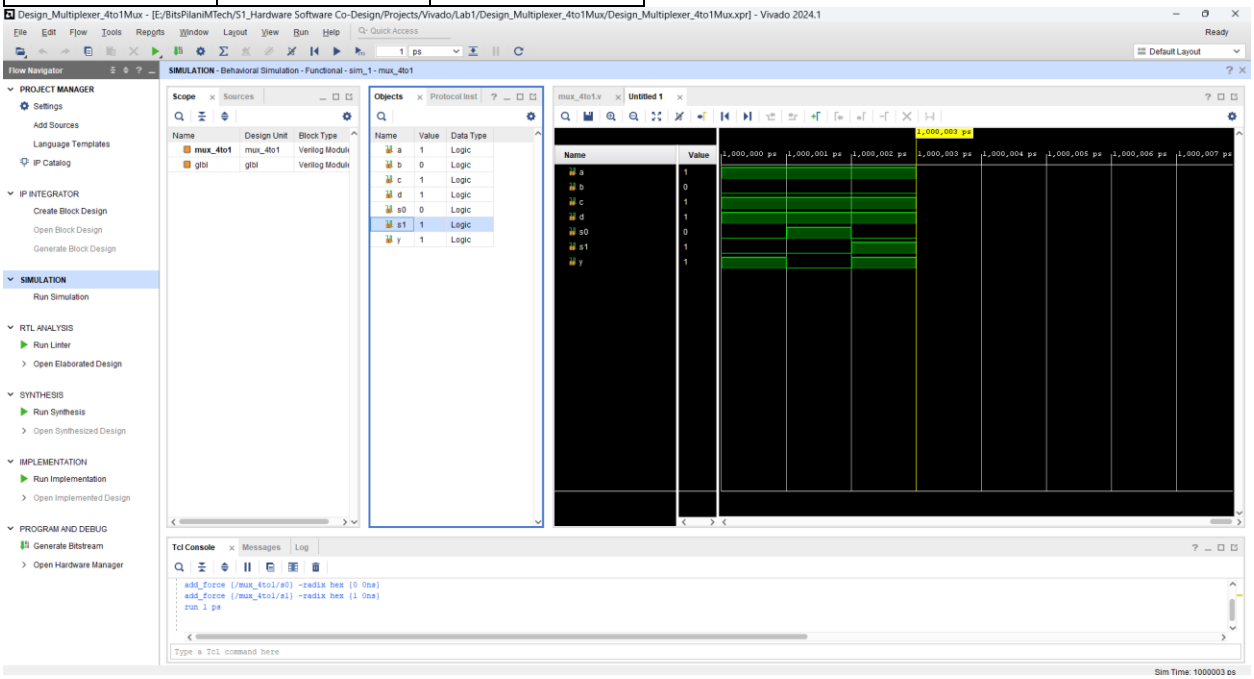
SIMULATION RESULTS 2 >>

s1	s0	y
0	1	b



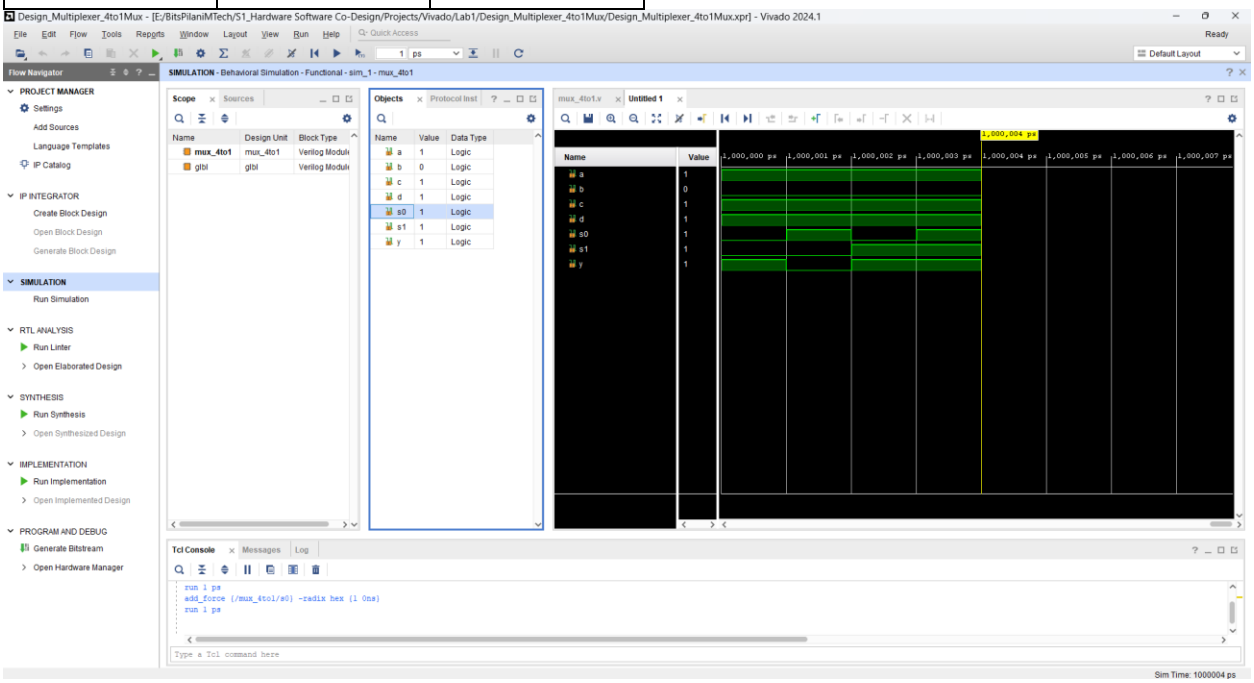
SIMULATION RESULTS 3 >>

s1	s0	y
1	0	c

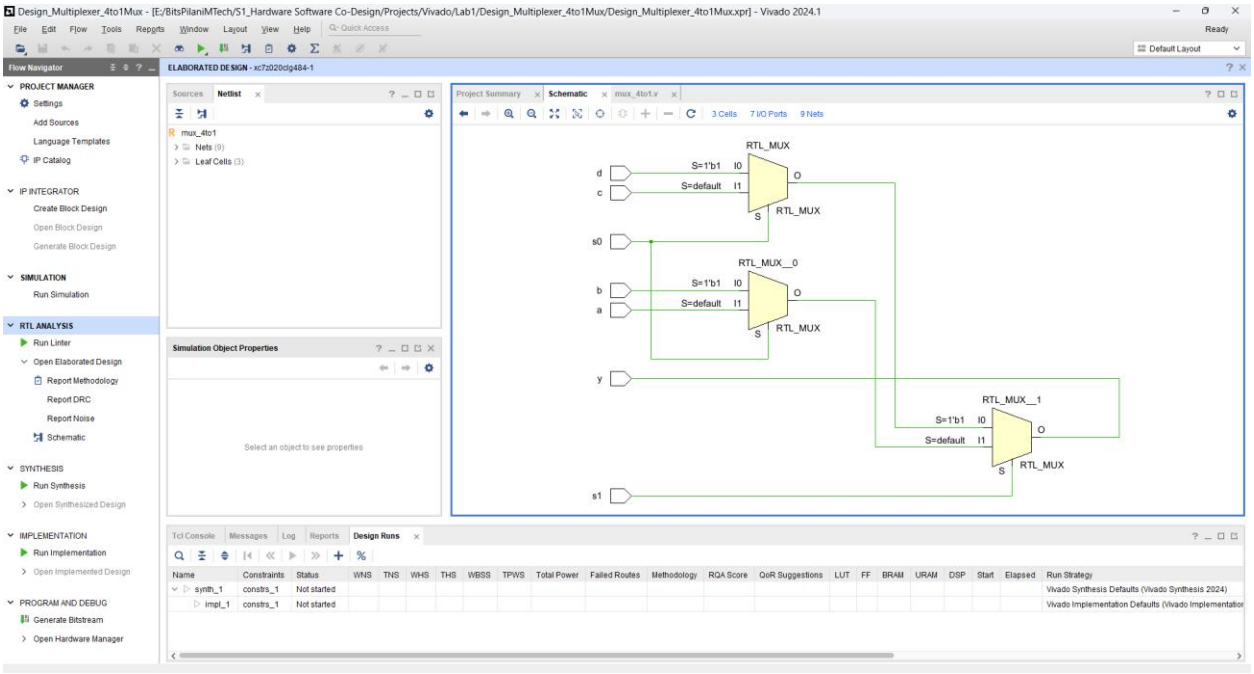


SIMULATION RESULTS 4 >>

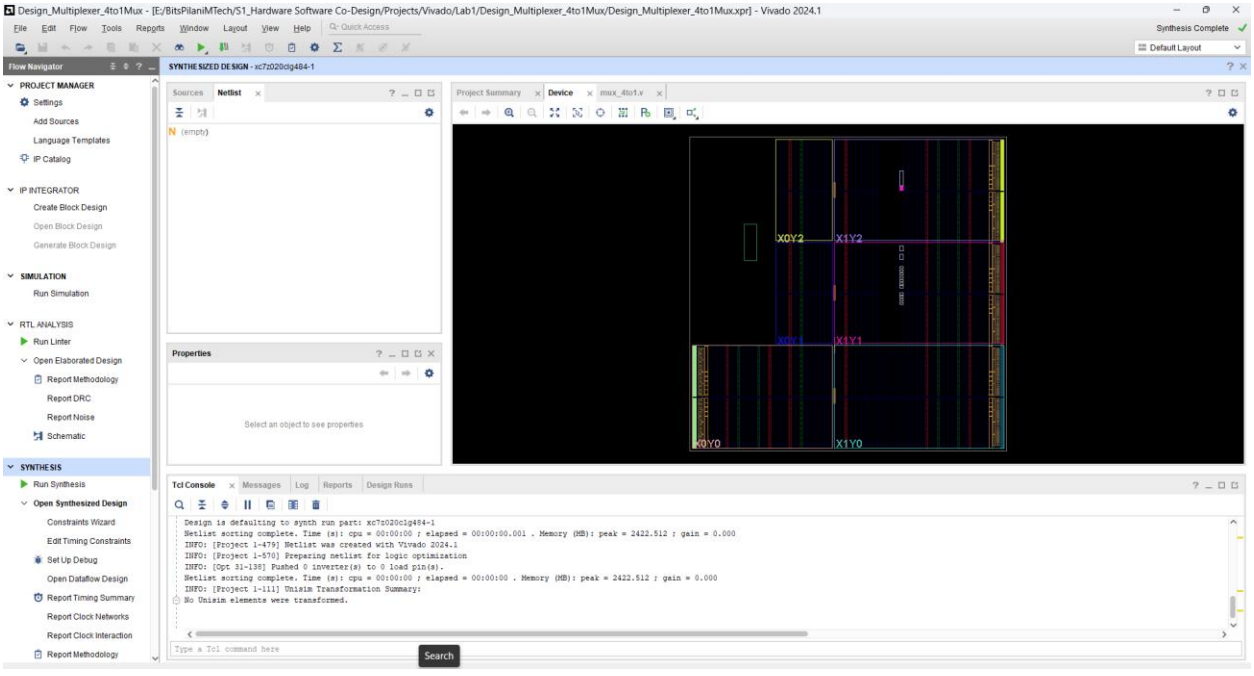
s1	s0	y
1	1	d



ELABORATION DESIGN >>



SYNTHESIZED DESIGN >>

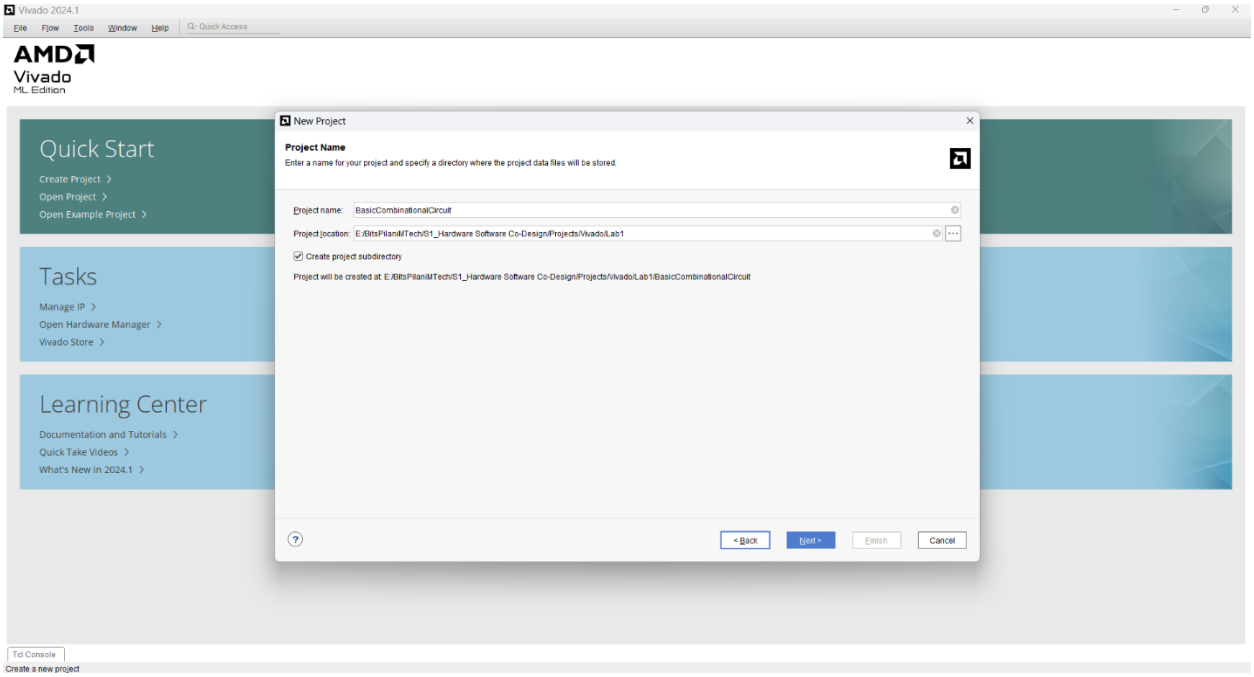


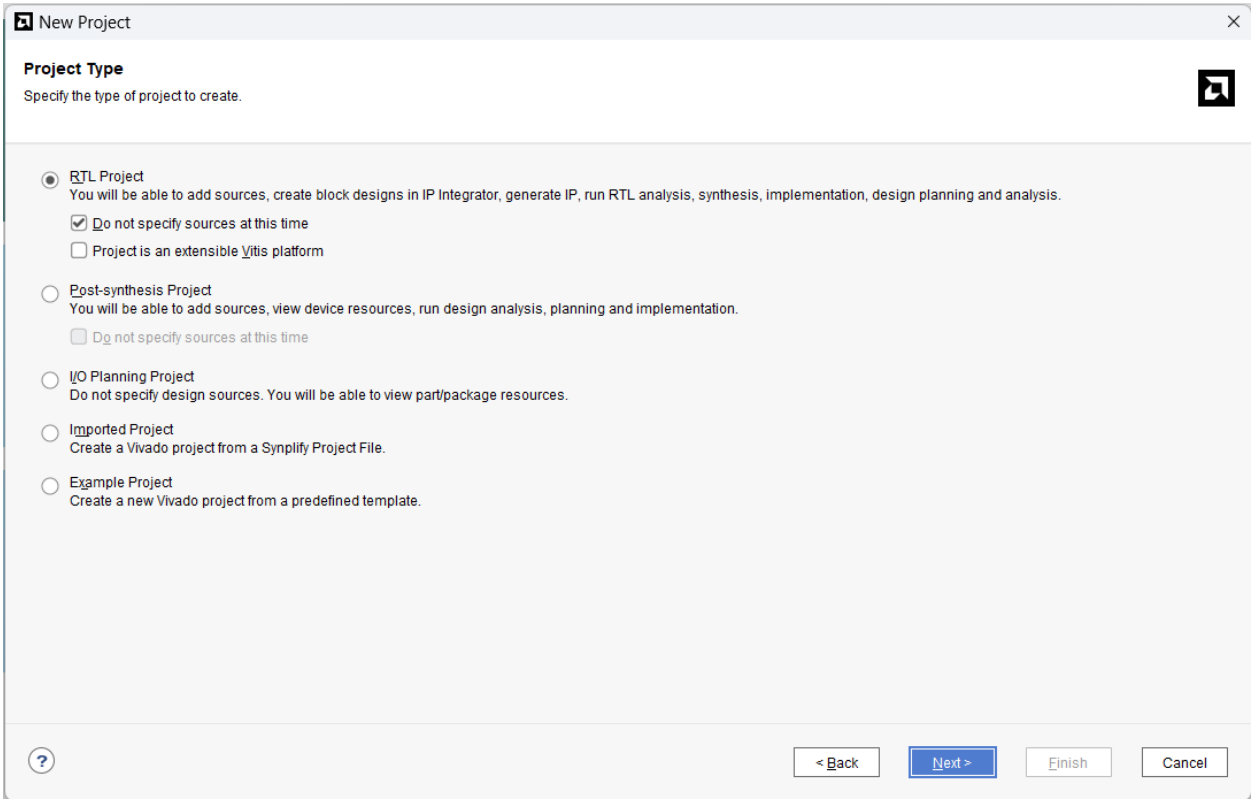
++++++++++++++++++++++++++++ASSIGNMENT END++++++++++++++++++++++++++++++++++

<< BASIC HOW TO CREATE PROJECT IN VIVADO >>

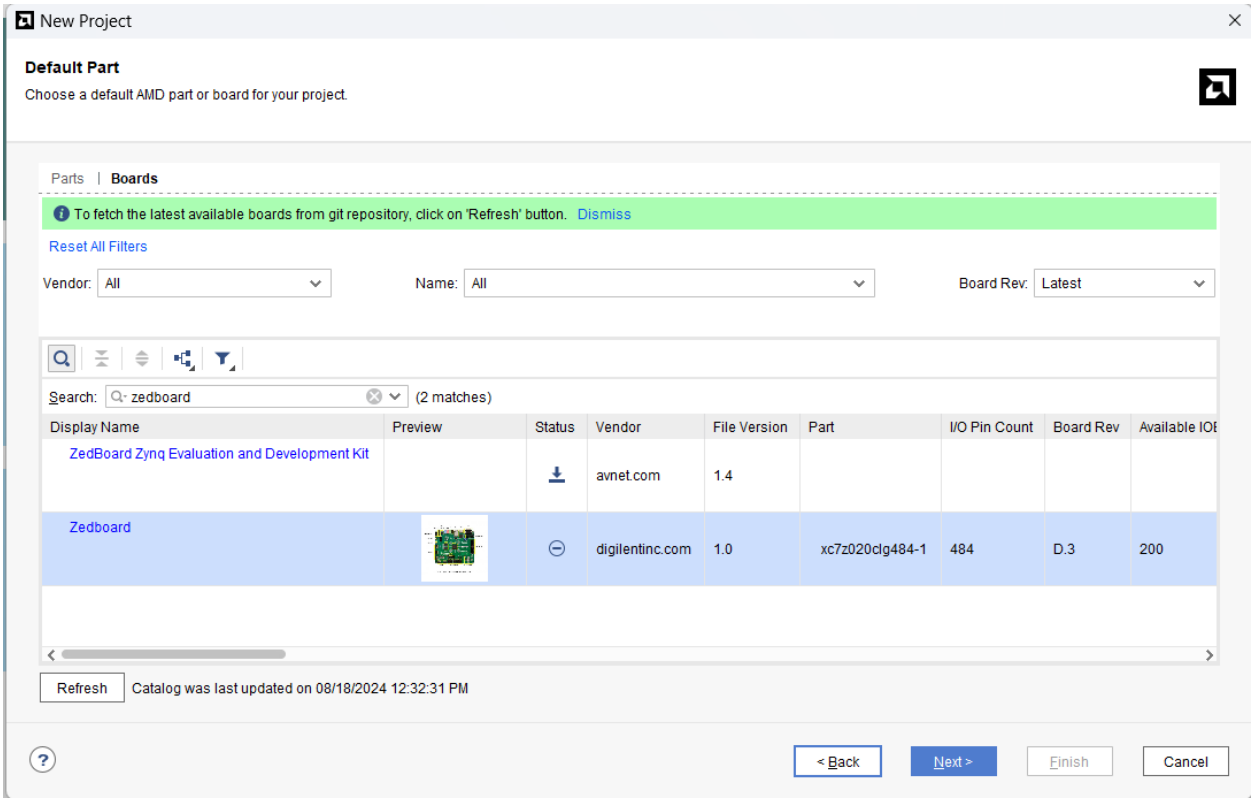
Creating New Project on vivado FPGA >>

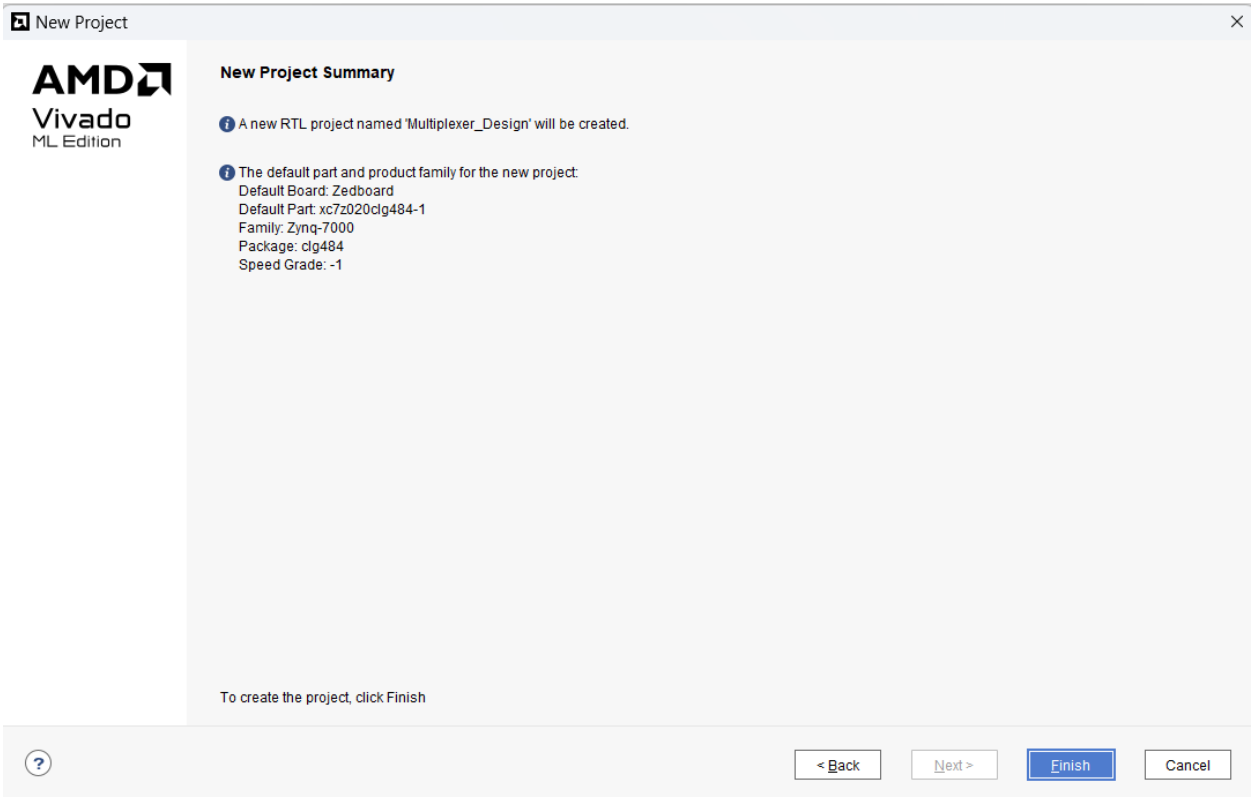
Files >> New Proejct



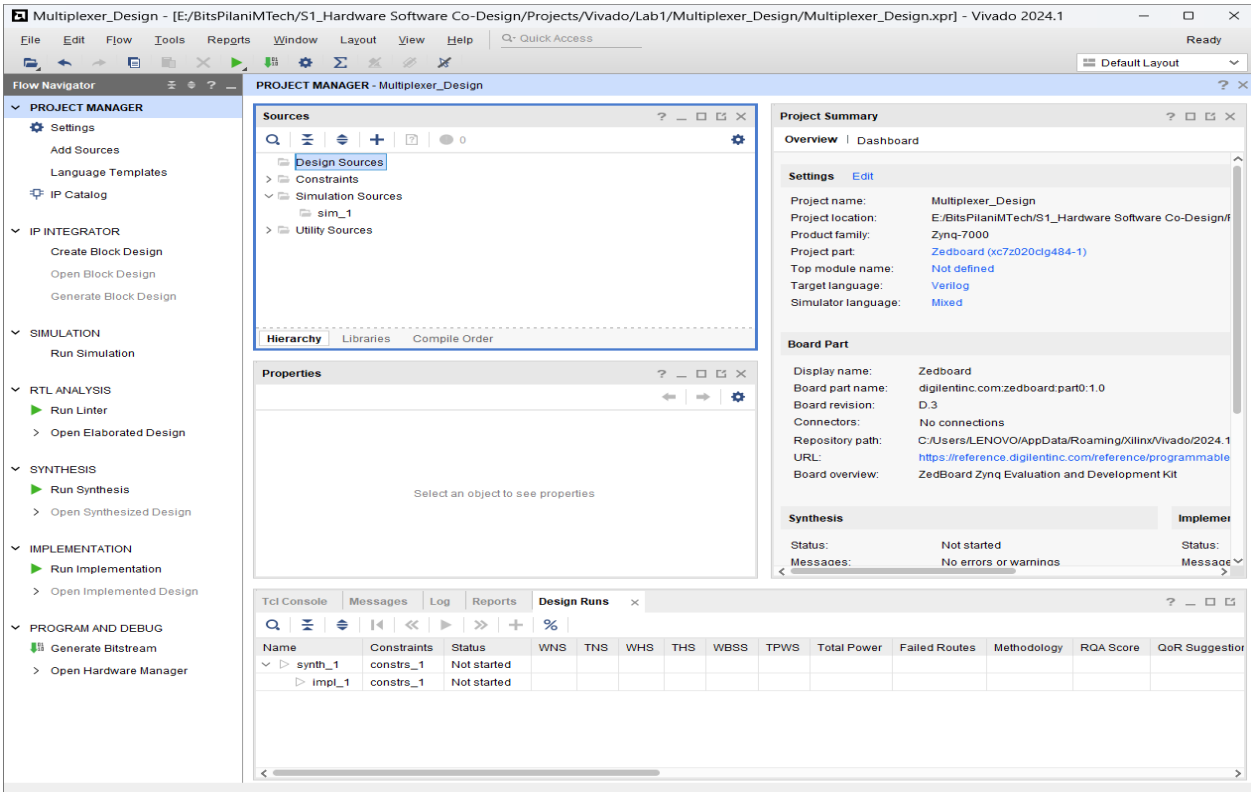


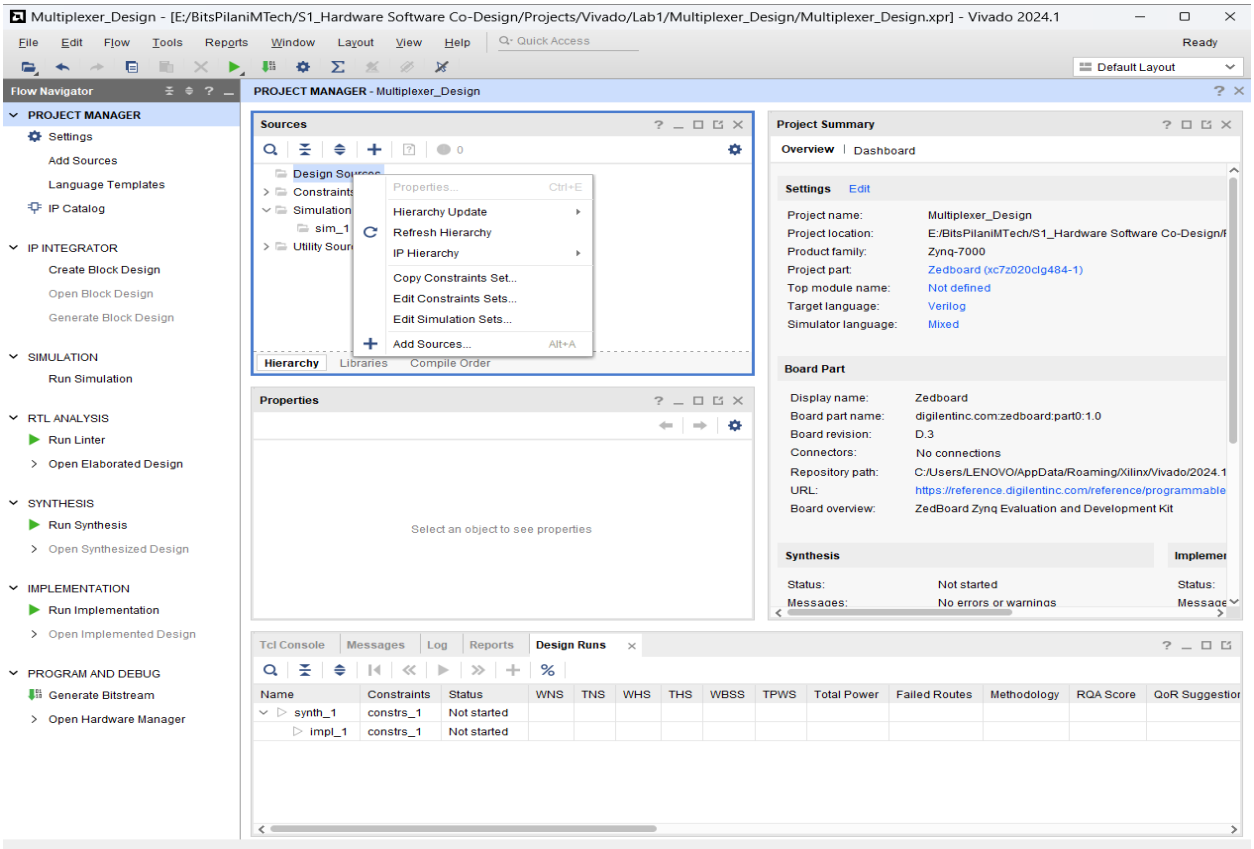
Search for ZedBoard >>



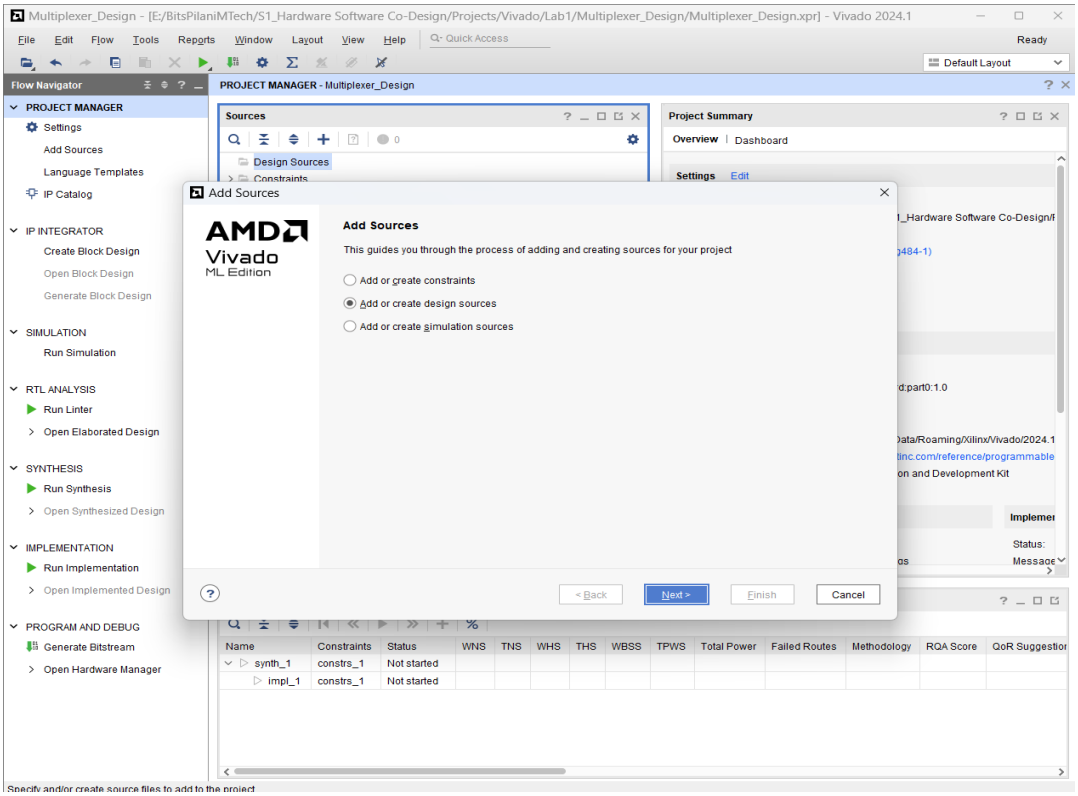


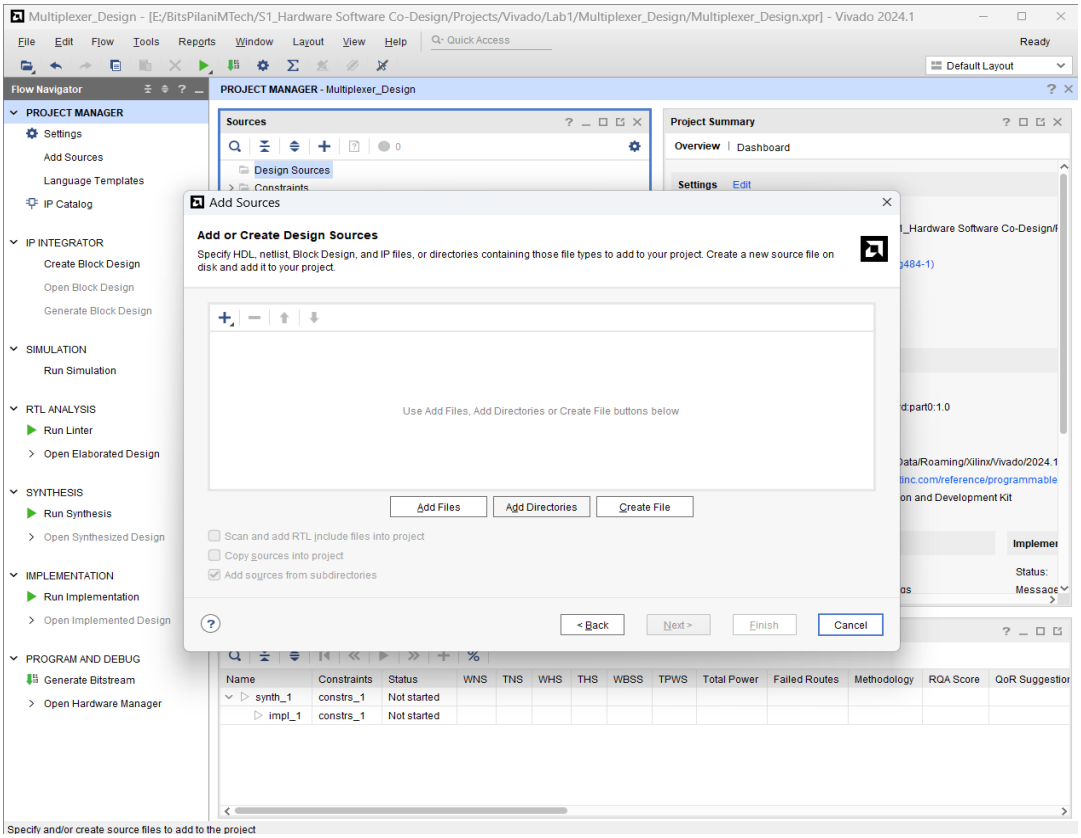
Right Click on >> Design Sources



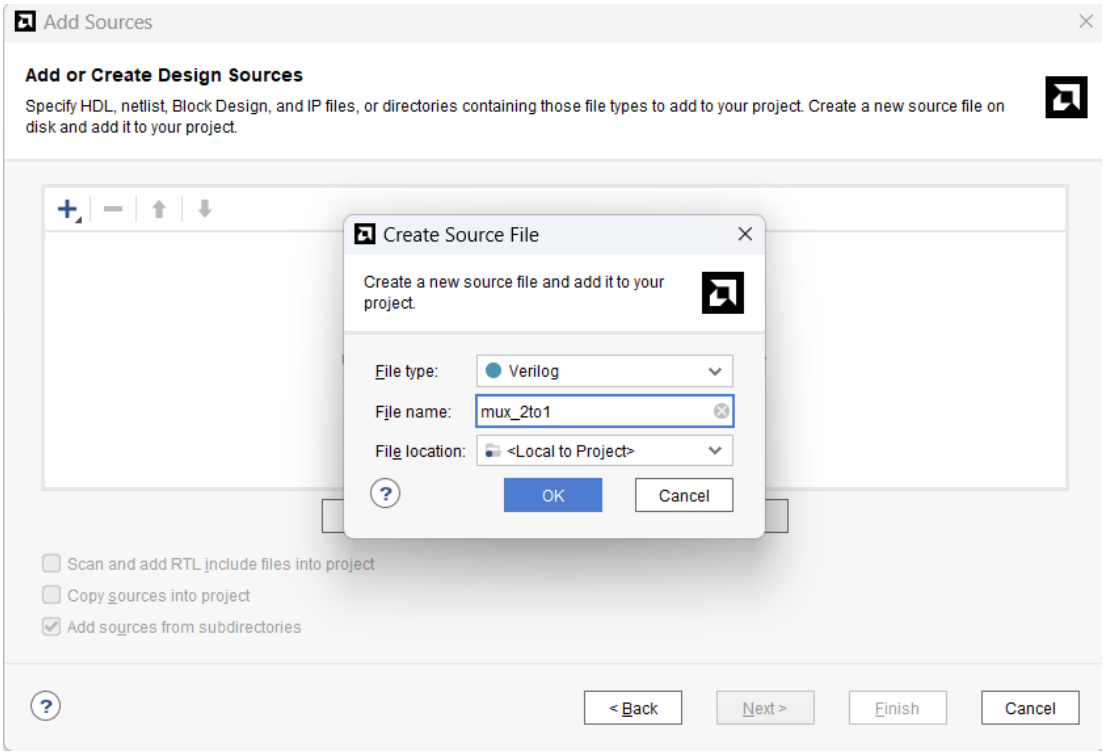


Select + Add Sources >> Add or create design sources >> Next

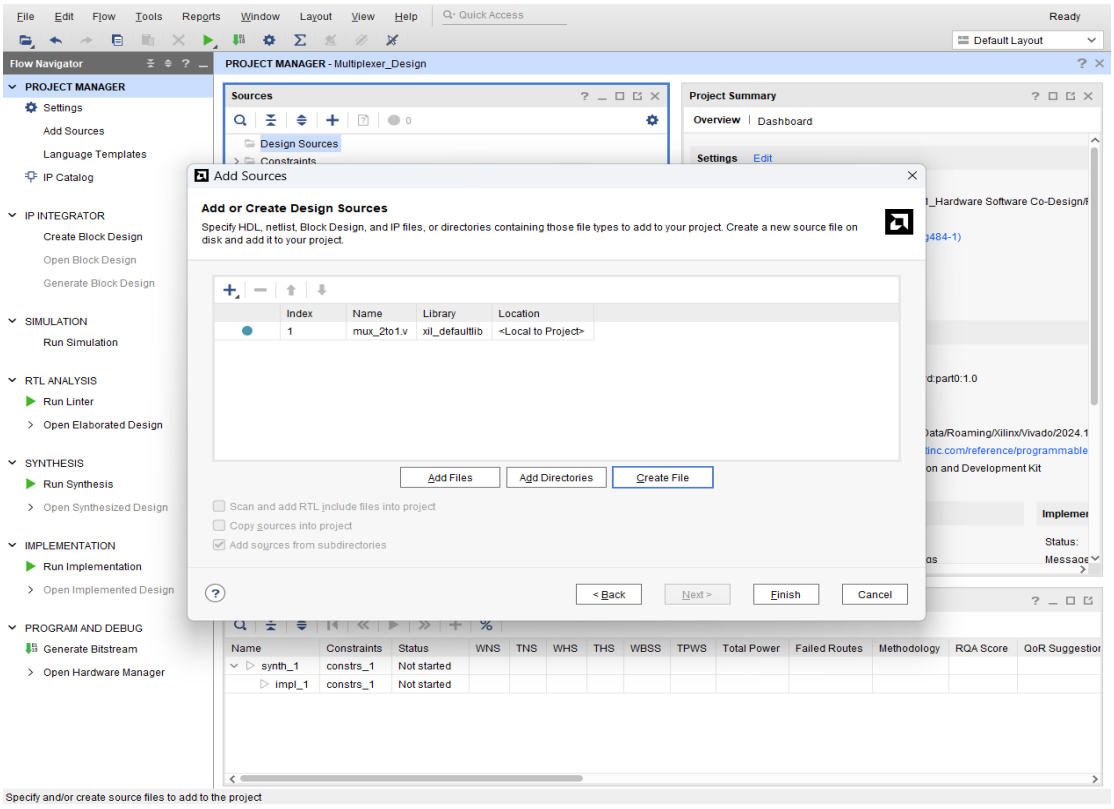


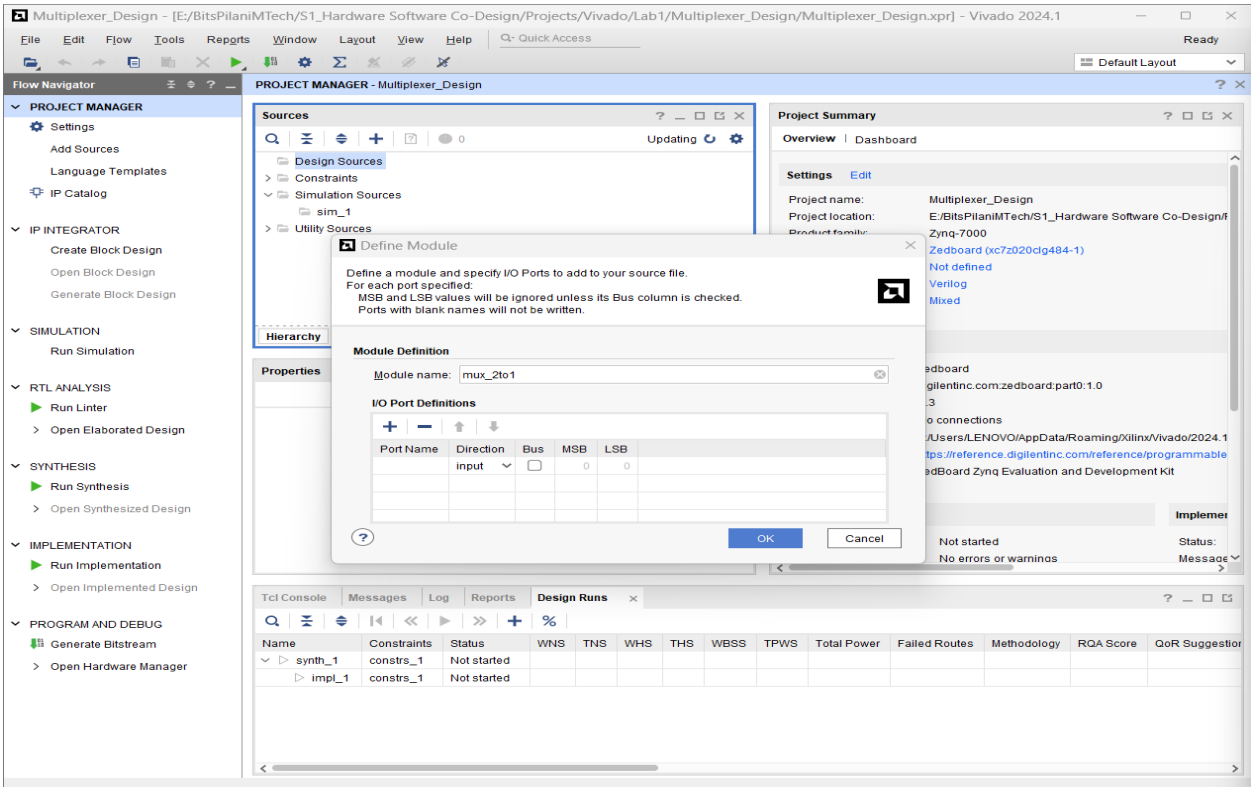


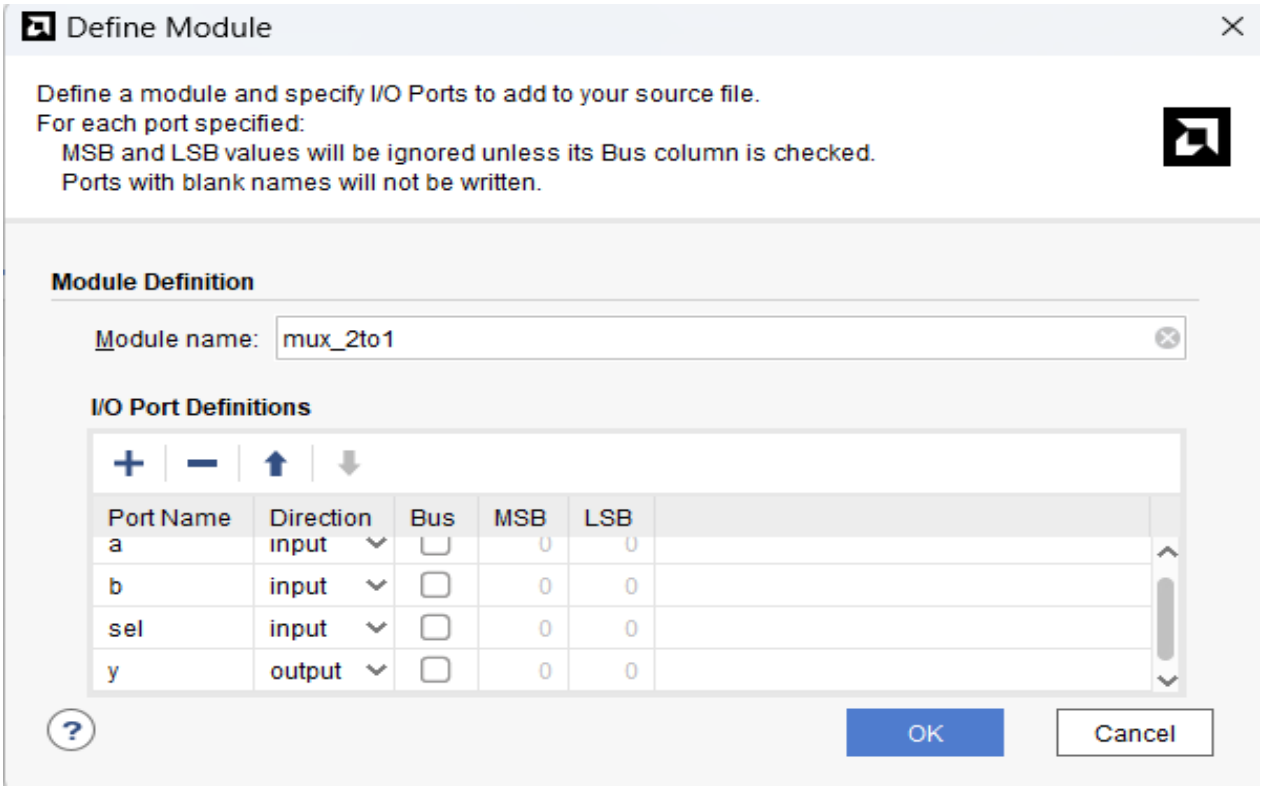
Click >> create File >> File name >> OK



Click >> Finish




Multiplexer_Design - [E:/BitsPilaniMTech/S1_Hardware Software Co-Design/Projects/Vivado/Lab1/Multiplexer_Design/Multiplexer_Design.xpr] - Vivado 2024.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - Multiplexer_Design
Sources
Updating
Design Sources
Constraints
Simulation Sources
sim_1
Utility Sources
Hierarchy
Properties
Project Summary
Overview | Dashboard
Settings Edit
Project name: Multiplexer_Design
Project location: E:/BitsPilaniMTech/S1_Hardware Software Co-Design/
Zynq-7000
Zedboard (xc7z020clg484-1)
Not defined
Verilog
Mixed
Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Module name: mux_2to1
I/O Port Definitions
Port Name Direction Bus MSB LSB
input
OK
Cancel
Not started
No errors or warnings
Status:
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS WBSS TPWS Total Power Failed Routes Methodology RQA Score
synth_1 constrs_1 Not started
impl_1 constrs_1 Not started


Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Module name: mux_2to1
I/O Port Definitions
Port Name Direction Bus MSB LSB
a input 0 0
b input 0 0
sel input 0 0
y output 0 0
OK
Cancel