**ESD Lab Assignment No.1**

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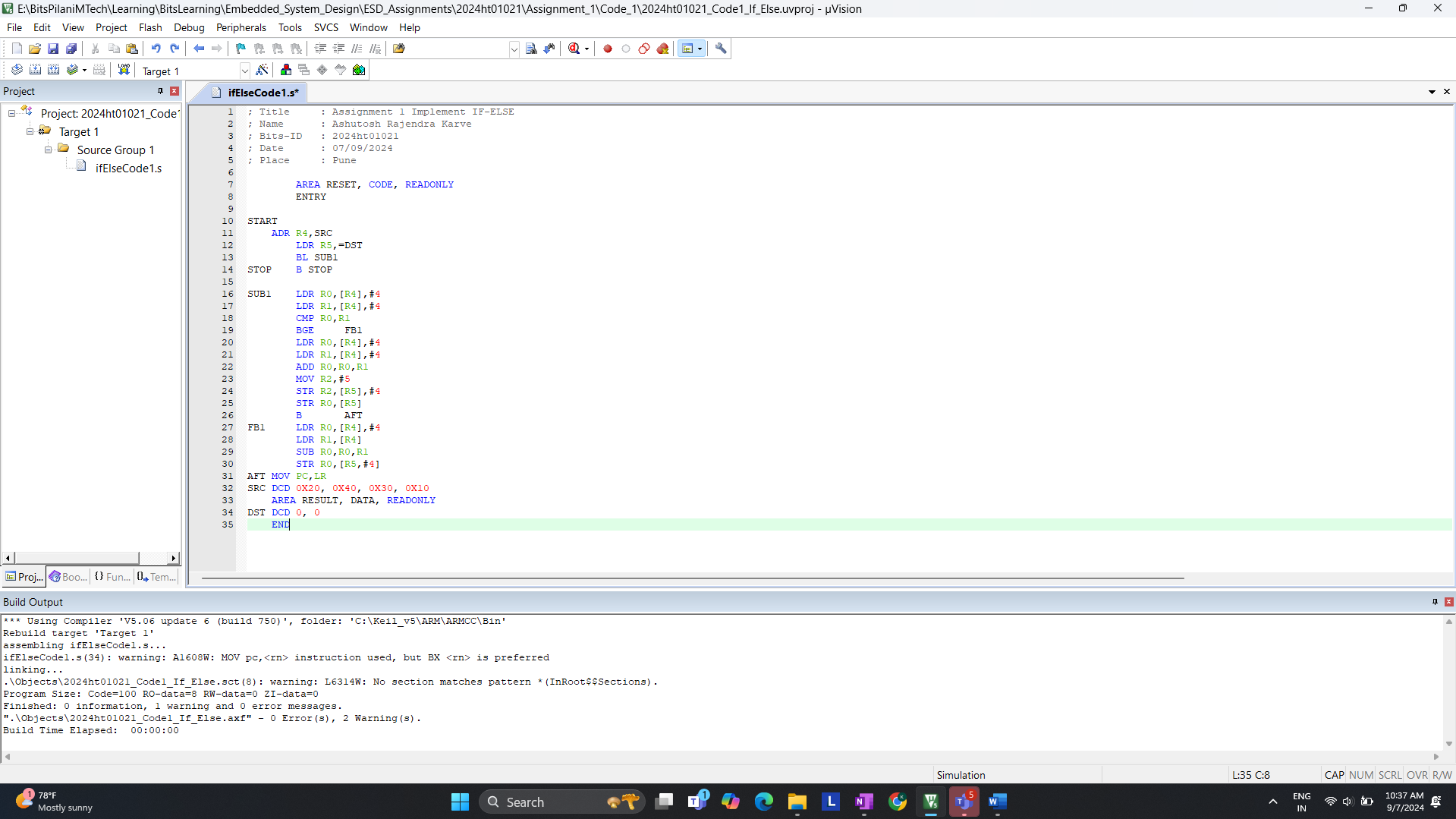
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Data : 05/09/2024

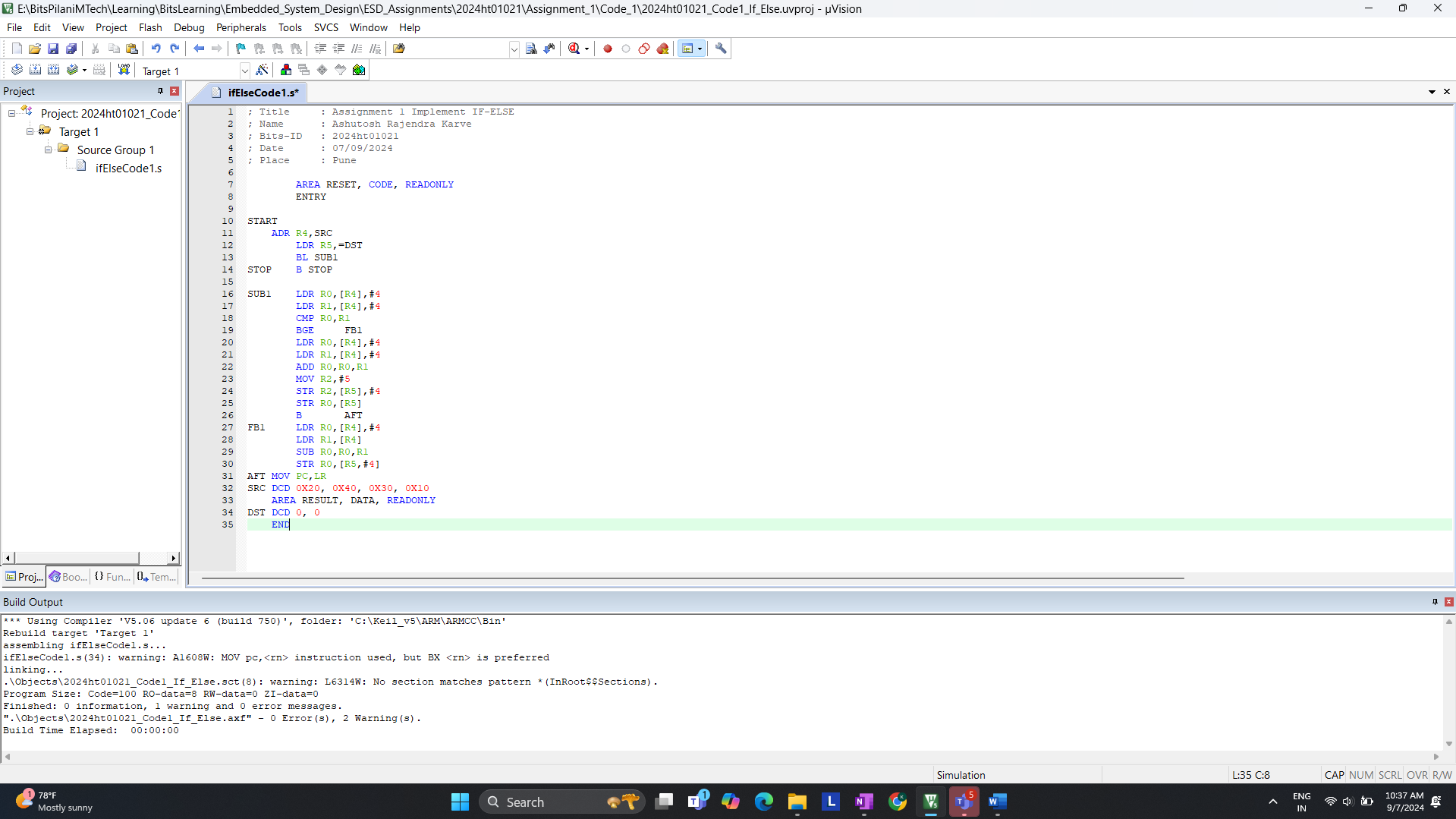
Place : Pune, Maharashtra

**Q.1. Assembly Language Program (ALP) for an LPC2378 processor to implement following IF-ELSE statement are given below:**If ( a<b )  
{  
 x=5;  
 y=c+d;  
}  
else  
 y=c-d

Code-1 >>

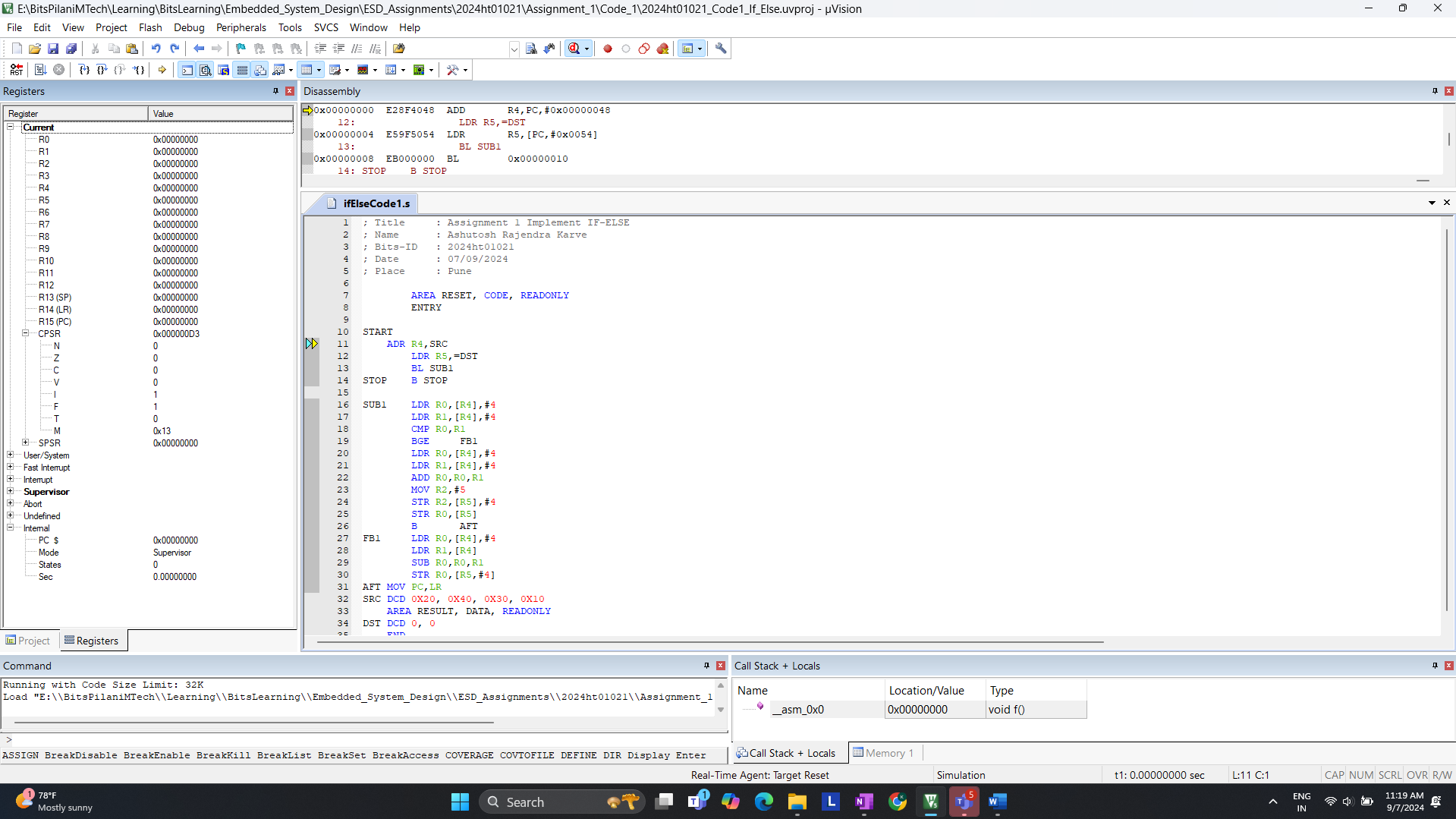


Code- 2 >> For now replace this below ss after taking ss



**a. On reset what is the LPC2378 processor’s state and mode of operation?**

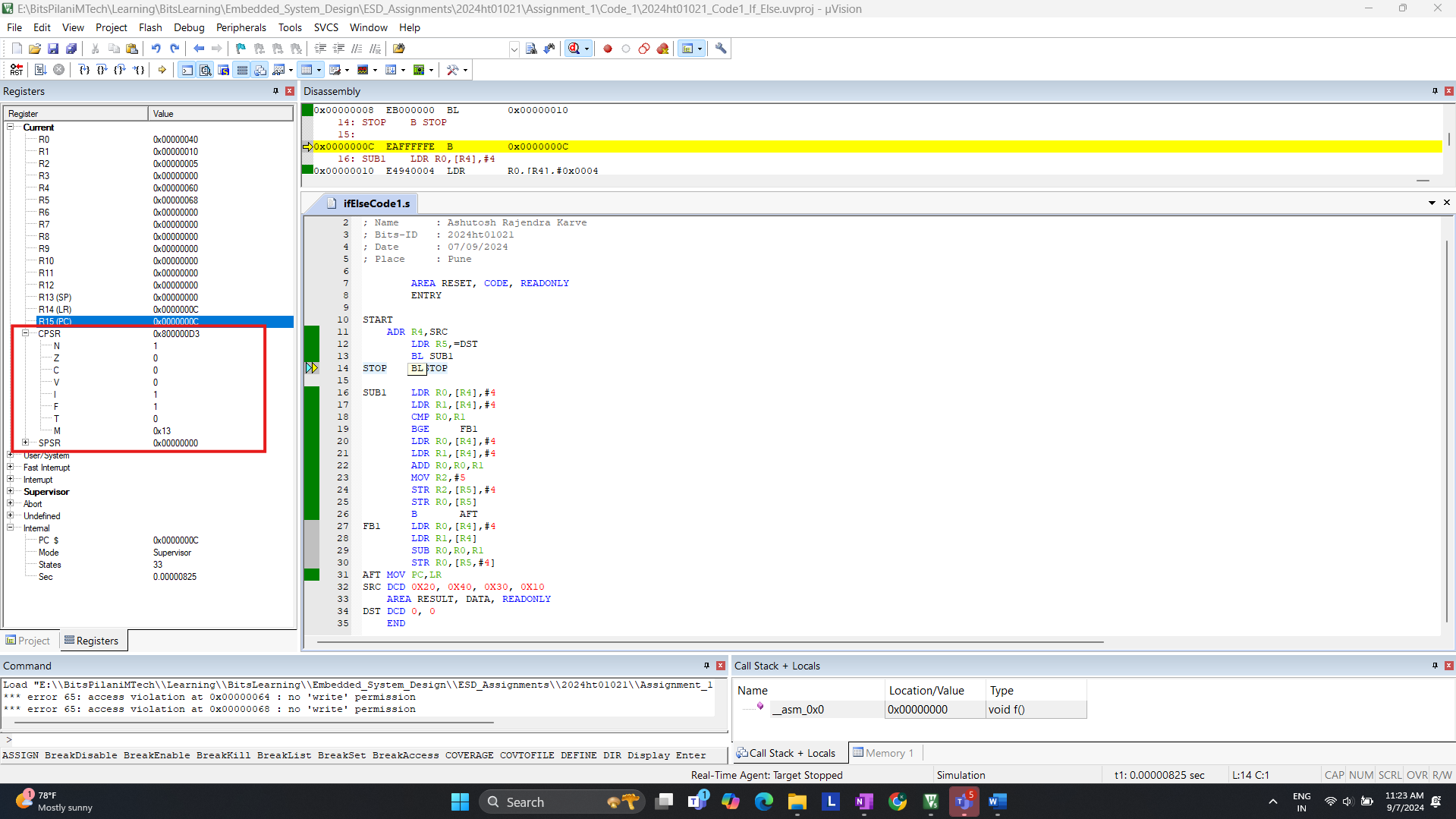
**CODE 1 >>**

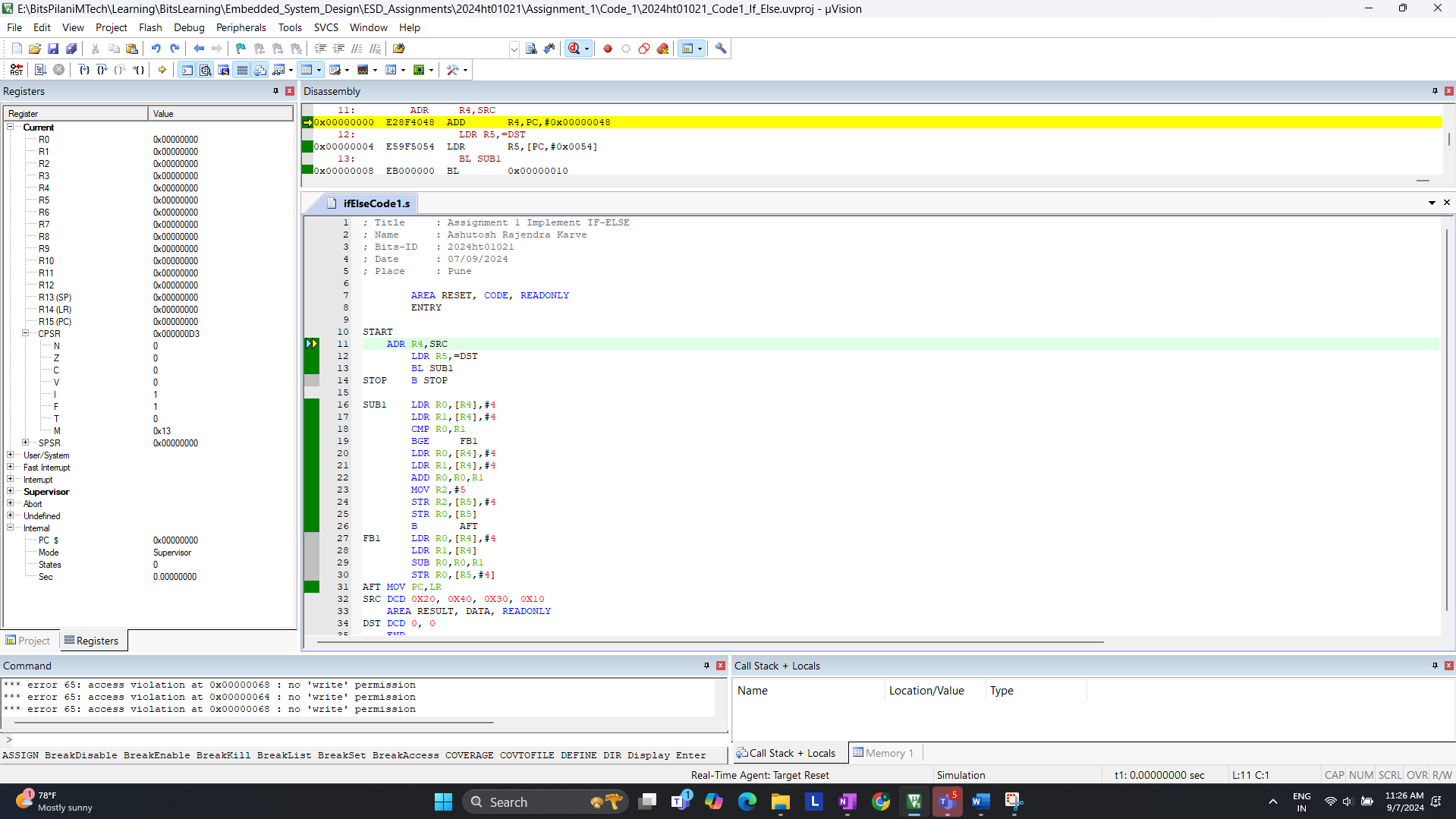
Start of debugging for code 1.  


After >> Step  
A computer screen shot of a computer

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Observation of Code 1.





**Answer:**

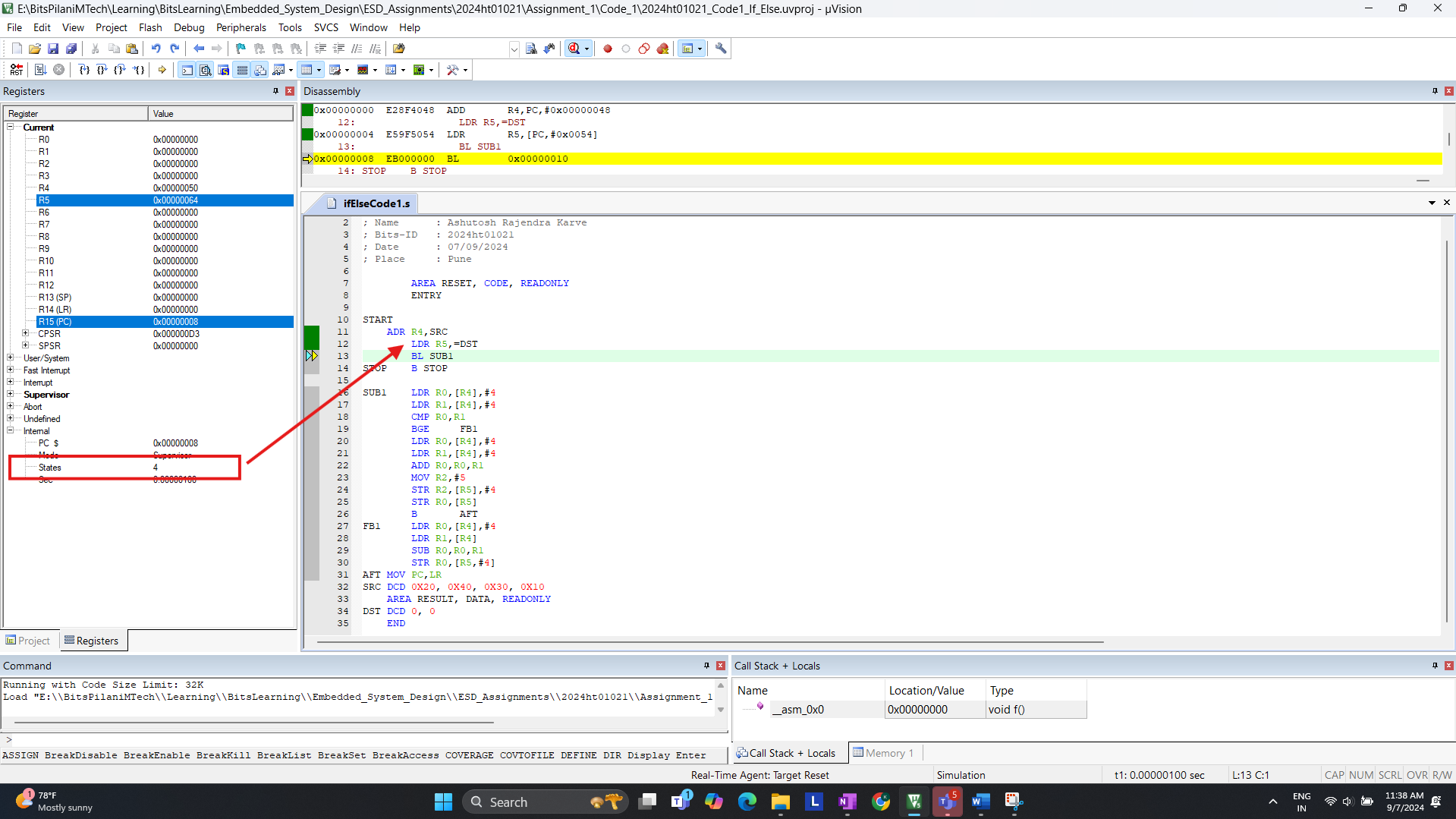
* Looking at CPSR. You will see that the processor is in **Supervisor Mode** after reset
* The Processor starts in **ARM State** (32-bit mode) on reset
* It takes total **33 states**

**b. How many states are taken for the execution of an Arithmetic instruction, Load and Store instruction respectively (For Code-1)?**

A screenshot of a computer

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Example for LDR >> Code 1.

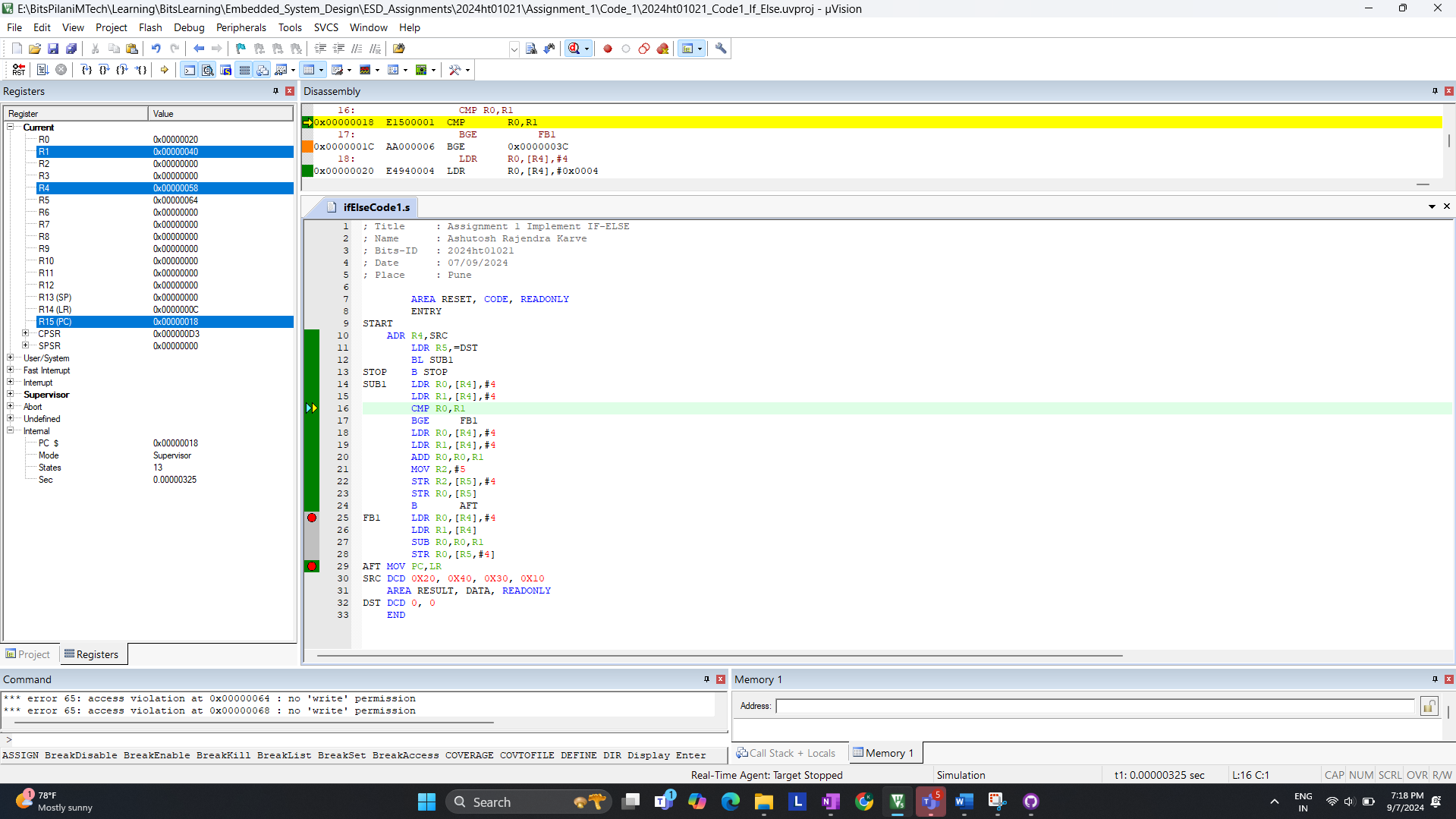


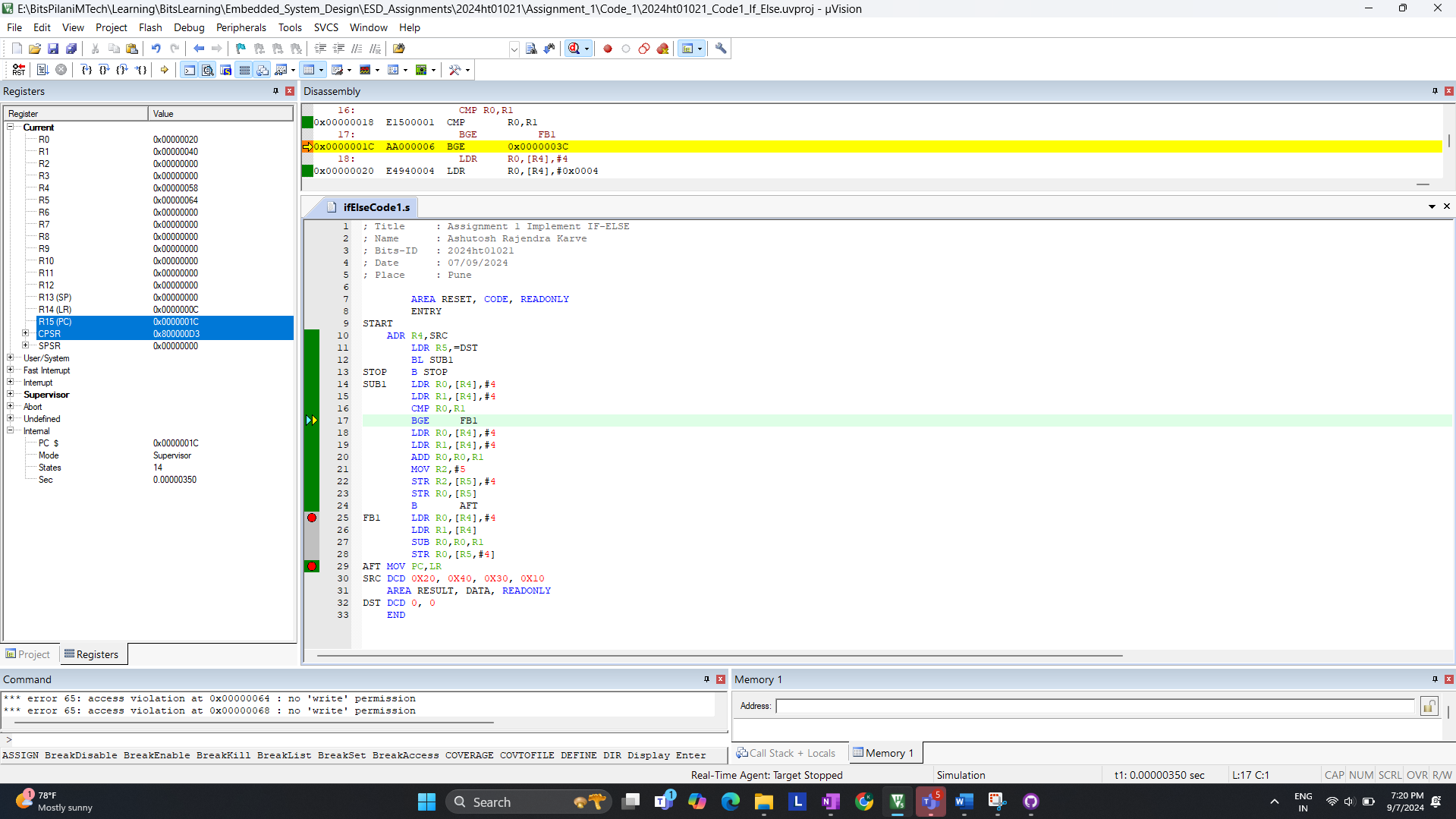
**Answer:**

* Observing: Load (LDR) , Store (STR) & Arithmetic (ADD)
  + **LDR** instruction takes **3 Cycles**.
  + **STR** instruction takes **2 Cycles**.
  + **ADD** instruction takes **1 Cycles**.
* Total Cycle takes place is **33 Cycles.** We can observein the above screen shot.

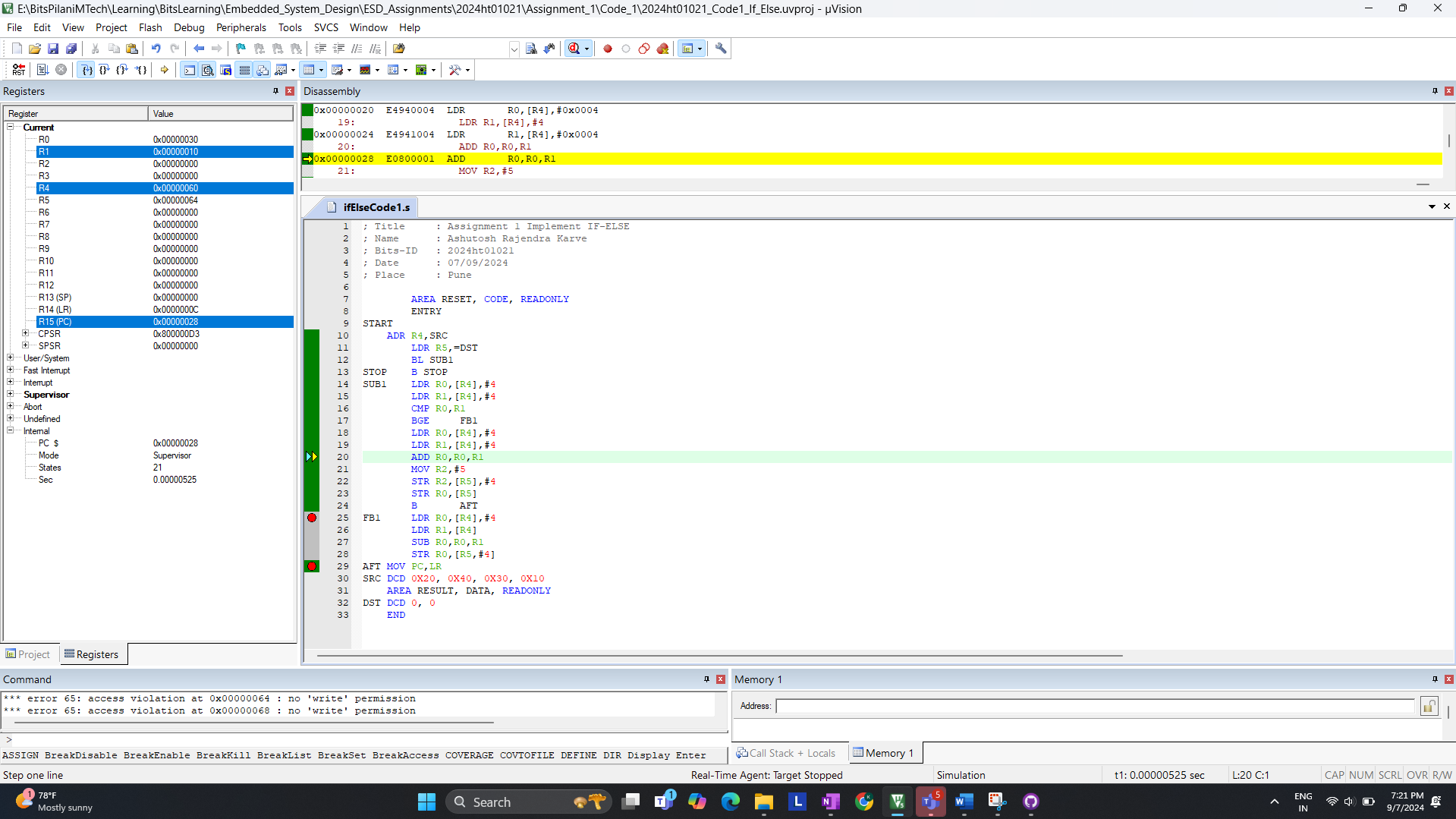
**c. Are the number of states taken for completion the same for BGE instruction if the branch (1) is taken (2) not taken? Please give the states are taken for each. (For Code – 1)**

We Need to determine the number of states for the BGE instruction when:  
1. Branch is taken  
2. Branch is not taken

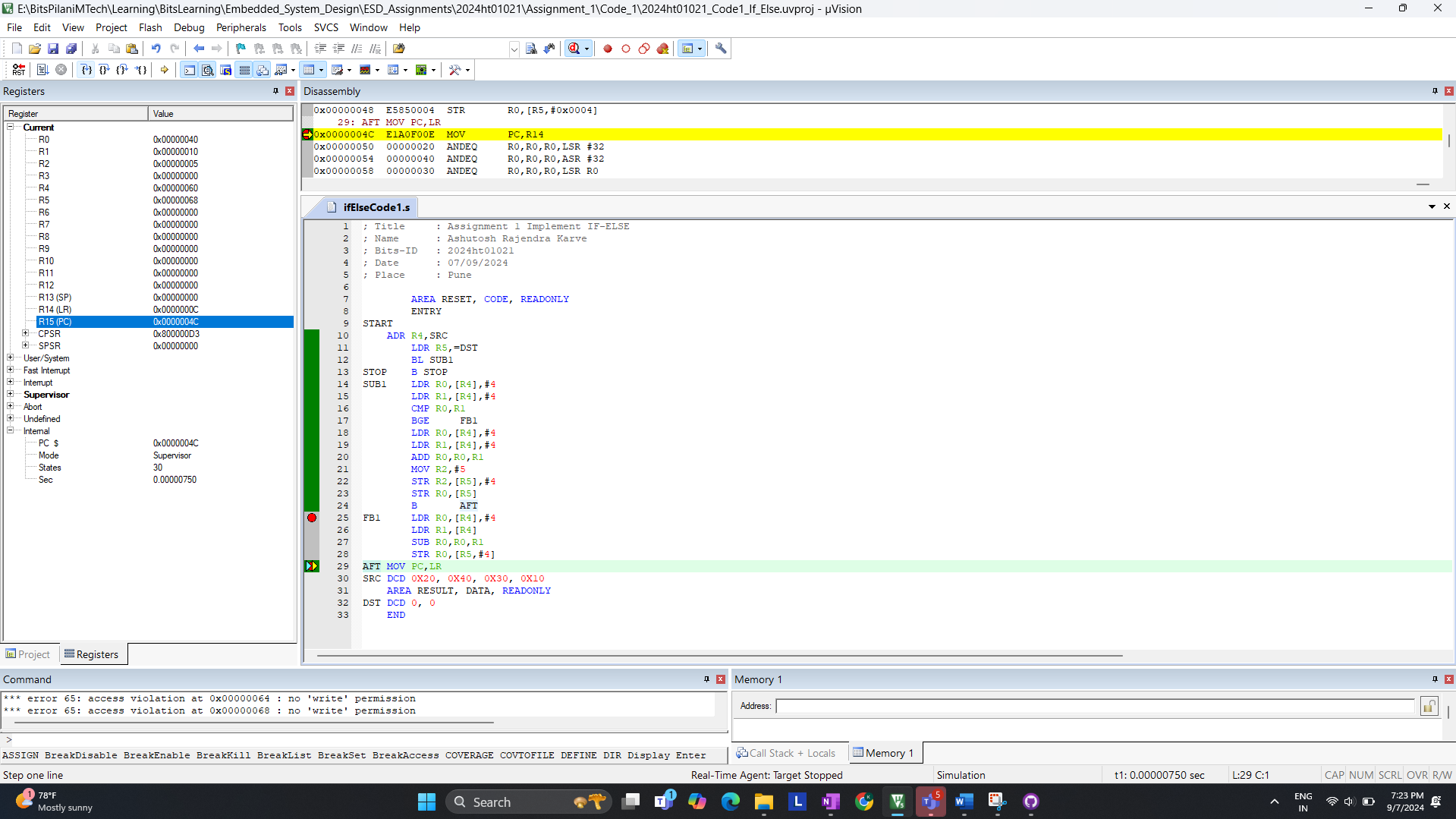
**1. Branch Is Taken >>**  
code: SRC DCD 0x20, 0x40, 0x30, 0x10 ( R0 < R1 )  


After comparison; for now R0 is loaded with 20 & R1 is Loaded with 40; States 13  


Now R0 and R1 is loaded with 30 & 10



We are in {if loop} since (R0 < R1 ) new values update for R0 is 40 and R2 is 5 which is our   
{If Block X , Y Value} State : 30

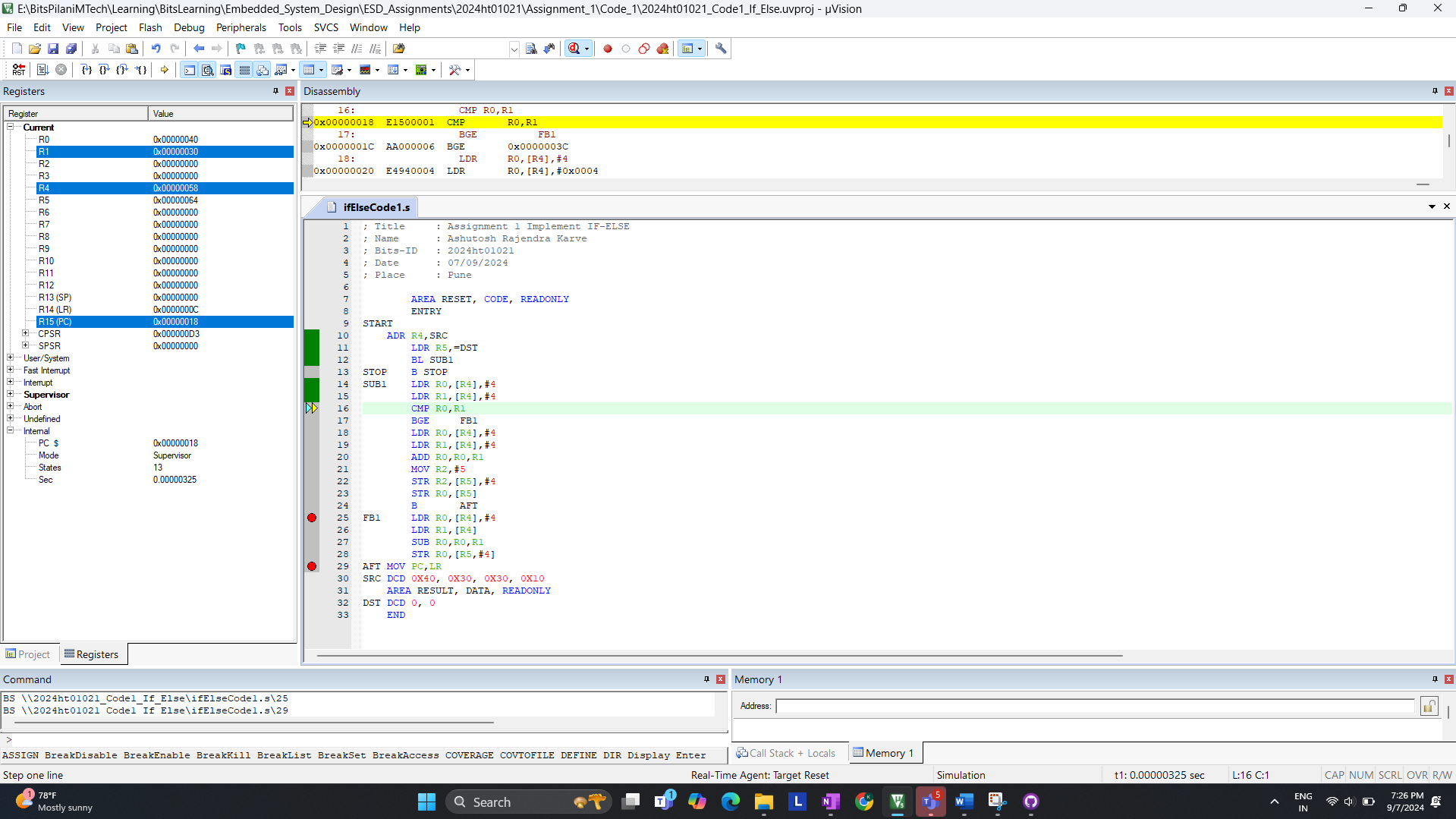


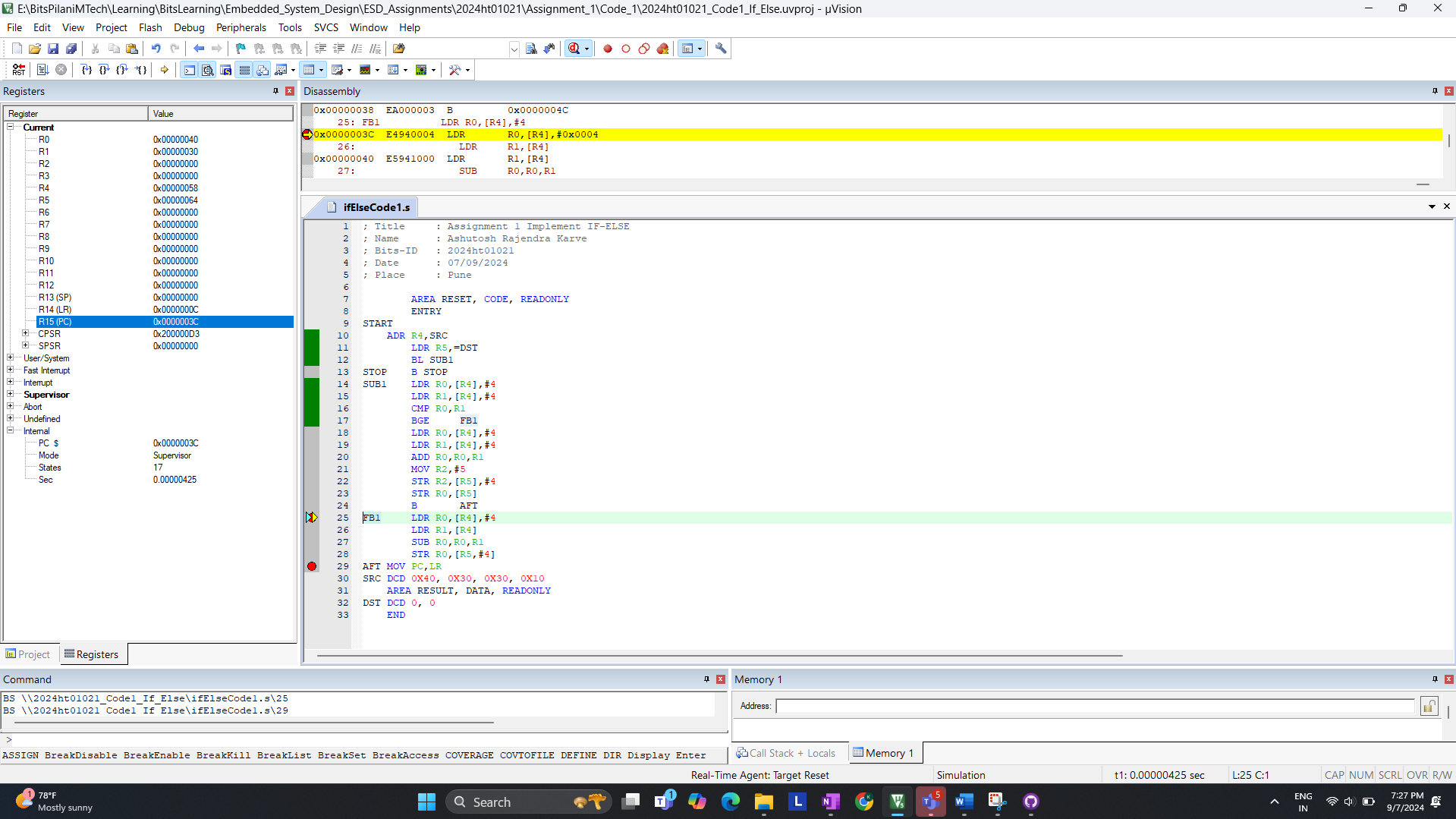
END OF CODE:

A computer screen shot of a program

Description automatically generated

>> Final State with Branch is Taken is 33

**2. Branch Is Not Taken:**  
I. code: SRC DCD 0x20, 0x40, 0x30, 0x10 ( R0 > R1)  
For now value of R0 & R1 is loaded with 40,30 ( 40 > 30 )  


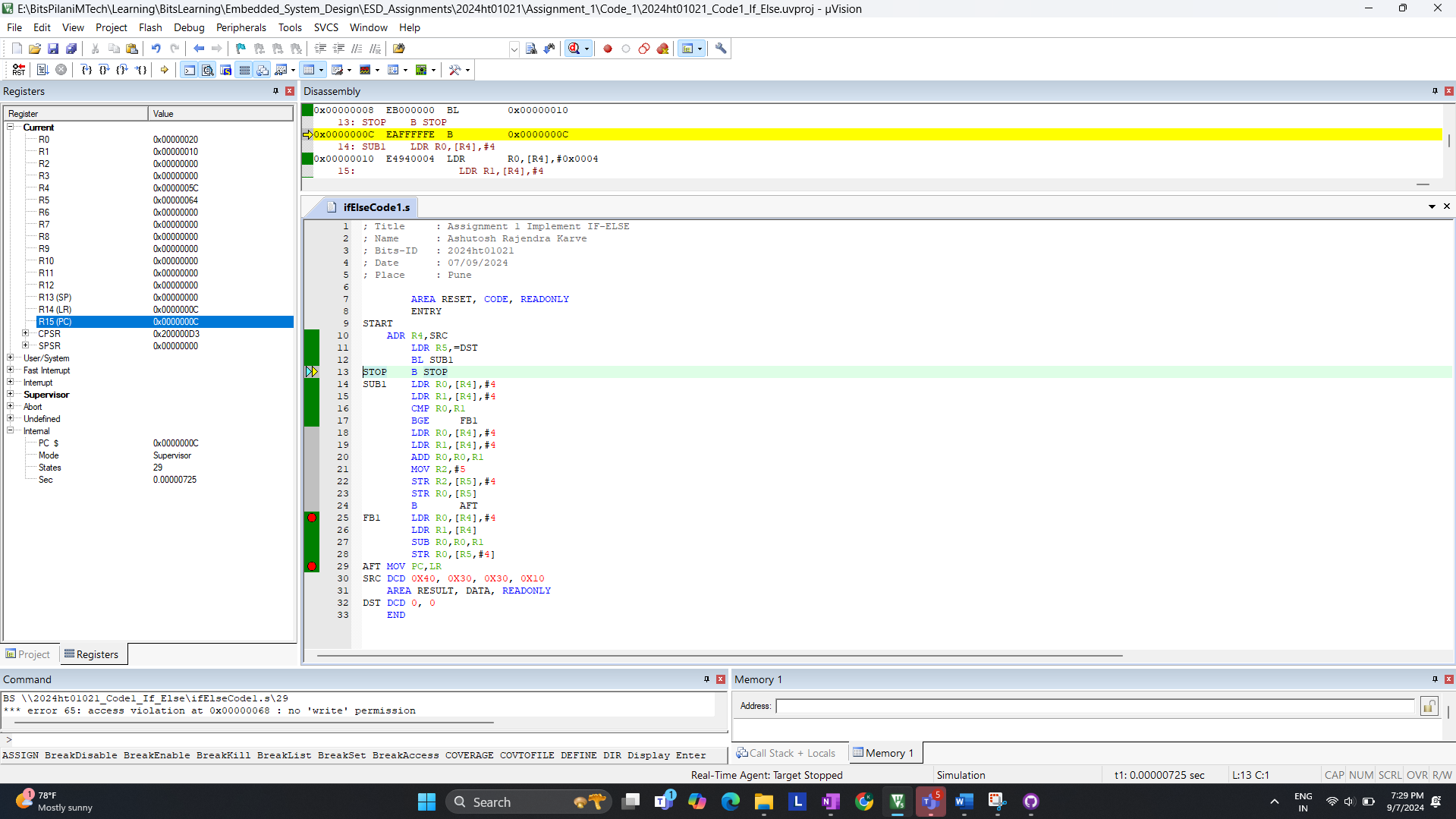
After comparison; it skip the IF-BLOCK enters ELSE-BLOCK; States 17  


After Subtraction operation; Value of R0 Changes to 20; State 24

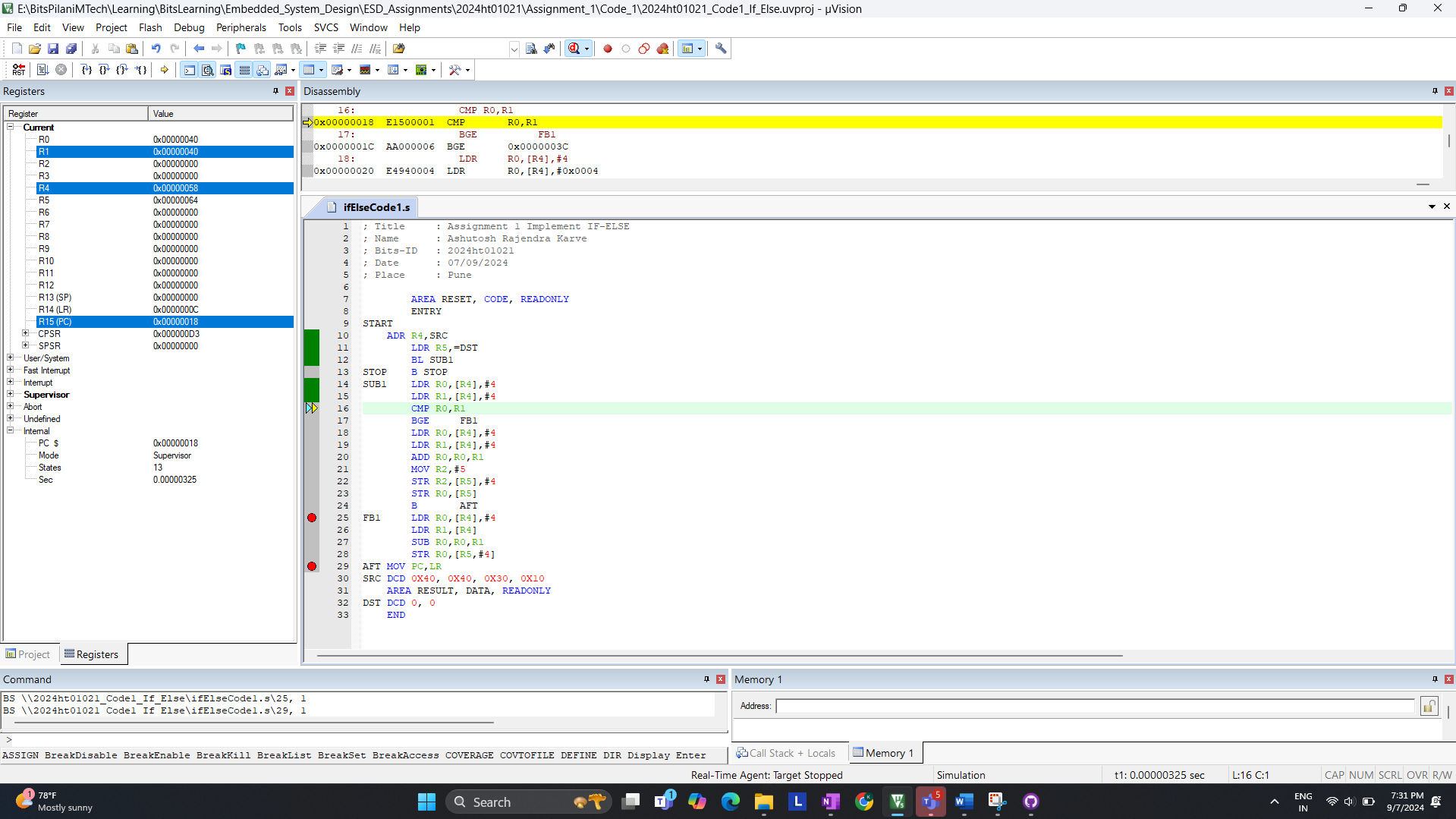
A computer screen shot of a program

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END OF CODE:



>> Final State with Branch is not Taken is 29

II. code: SRC DCD 0x40, 0x40, 0x30, 0x10 ( R0 == R1)  
For now R0 & R1 is loaded with 40 & 40 ( 40 == 40 )  


After comparison; it skip the IF-BLOCK enters ELSE-BLOCK; States 17

A computer screen shot of a program

Description automatically generated

A computer screen shot of a program

Description automatically generated

END OF CODE:

A computer screen shot of a program

Description automatically generated

>> Final State with Branch is not Taken is 29

**Answer:**

* Branch Taken: The instruction takes 33 cycles when the branch is taken.
* Branch not Taken: The instruction takes 29 cycles when the branch is not taken.

>> Number of states for completion is **not same** for BGE instruction