

HSCD LAB Assignment No. 1

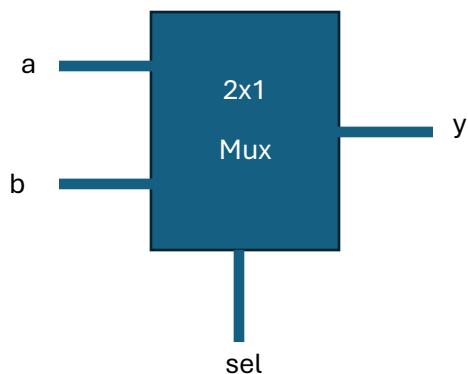
Name : Ashutosh Rajendra Karve
Mail : 2024ht01021@wilp.bits-pilani.ac.in
Contact : +91 9765541324
Date : 18/08/2024
Place : Pune, Maharashtra

Multiplexer Design

What is multiplexer?

Multiplexer is a combinational logic circuit used to select only one input among several inputs based on selection lines.

Task 1 : Design 2-to-1 Multiplexer



Sel	Y
0	a
1	b

sel	a	b	y
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

DEFINE MODULE >>

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name:

I/O Port Definitions

+ - ↑ ↓

Port Name	Direction	Bus	MSB	LSB
a	input	<input type="checkbox"/>	0	0
b	input	<input type="checkbox"/>	0	0
sel	input	<input type="checkbox"/>	0	0
y	output	<input type="checkbox"/>	0	0

?

OK

Cancel

Design Source file >>

Multiplexer_Design - [E:/BitsPilaniMTech/S1_Hardware Software Co-Design/Projects/Vivado/Lab1/Multiplexer_Design/Multiplexer_Design.xpr] - Vivado 2024.1

File Edit Flow Tools Reports Window Layout View Help

Q: Quick Access

Ready

Default Layout

Flow Navigator

PROJECT MANAGER - Multiplexer_Design

PROJECT MANAGER

Settings

Add Sources

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

Run Linter

Open Elaborated Design

SYNTHESIS

Run Synthesis

Open Synthesized Design

IMPLEMENTATION

Run Implementation

Open Implemented Design

PROGRAM AND DEBUG

Generate Bitstream

Open Hardware Manager

Sources

Design Sources (1)

mux_2to1 (mux_2to1.v)

Constraints

Simulation Sources (1)

sim_1 (1)

Utility Sources

Hierarchy Libraries Compile Order

Source File Properties

mux_2to1.v

Enabled

Location: E:/BitsPilaniMTech/S1_Hardware Software Co-Design/Projects/Vivad

Type: Verilog

Library: xil_defaultlib

Size: 0.6 KB

Modified: Today at 13:23:18 PM

General Properties

Project Summary

mux_2to1.v

o/Lab1/Multiplexer_Design/Multiplexer_Design.srcs/sources_1/new/mux_2to1.v

```
4 // Engineer:
5 //
6 // Create Date: 08/18/2024 01:18:59 PM
7 // Design Name: Ashutosh Karve
8 // Module Name: mux_2to1
9 // Project Name: Multiplexer Design
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 //
22 //
23 module mux_2to1(
24     input a,
25     input b,
26     input sel,
27     output y
28 );
29
30     assign y = sel ? b : a;
31 endmodule
32
```

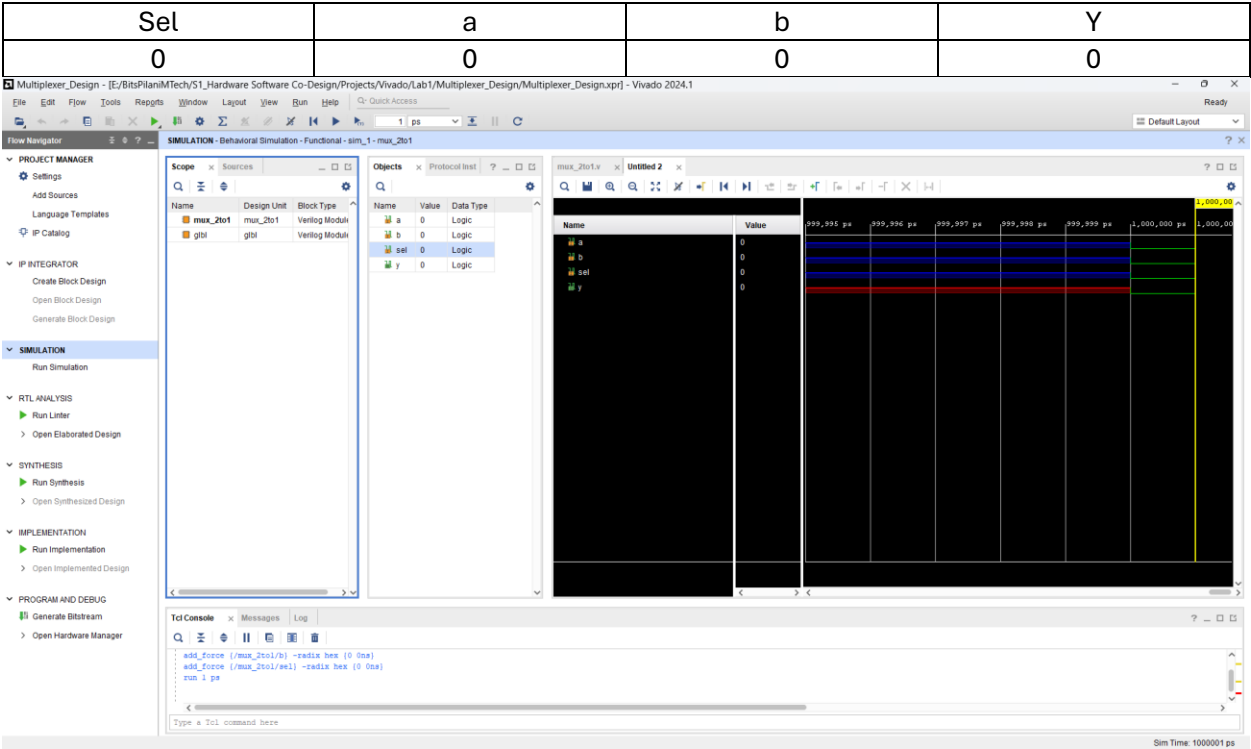
Tcl Console Messages Log Reports Design Runs

Design Runs

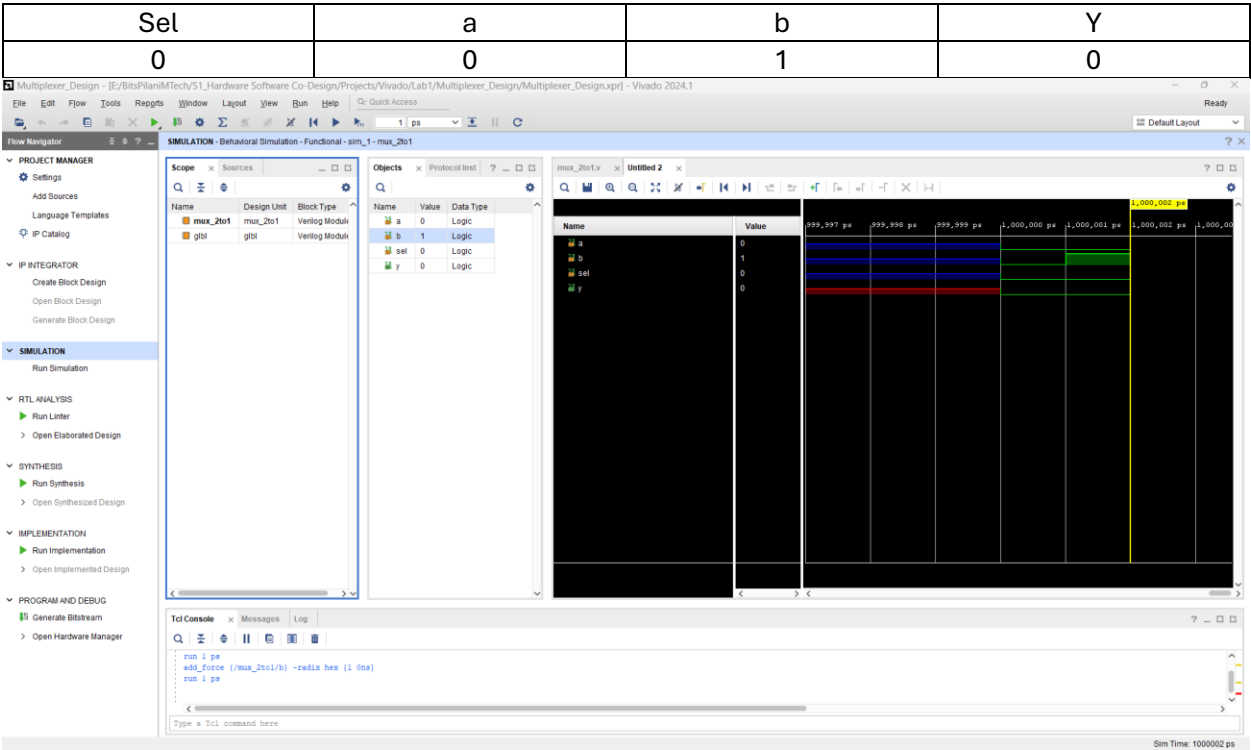
Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	ROA Score	QoR Suggestion
synth_1	constrs_1	Not started											
impl_1	constrs_1	Not started											

17:32 Insert Verilog

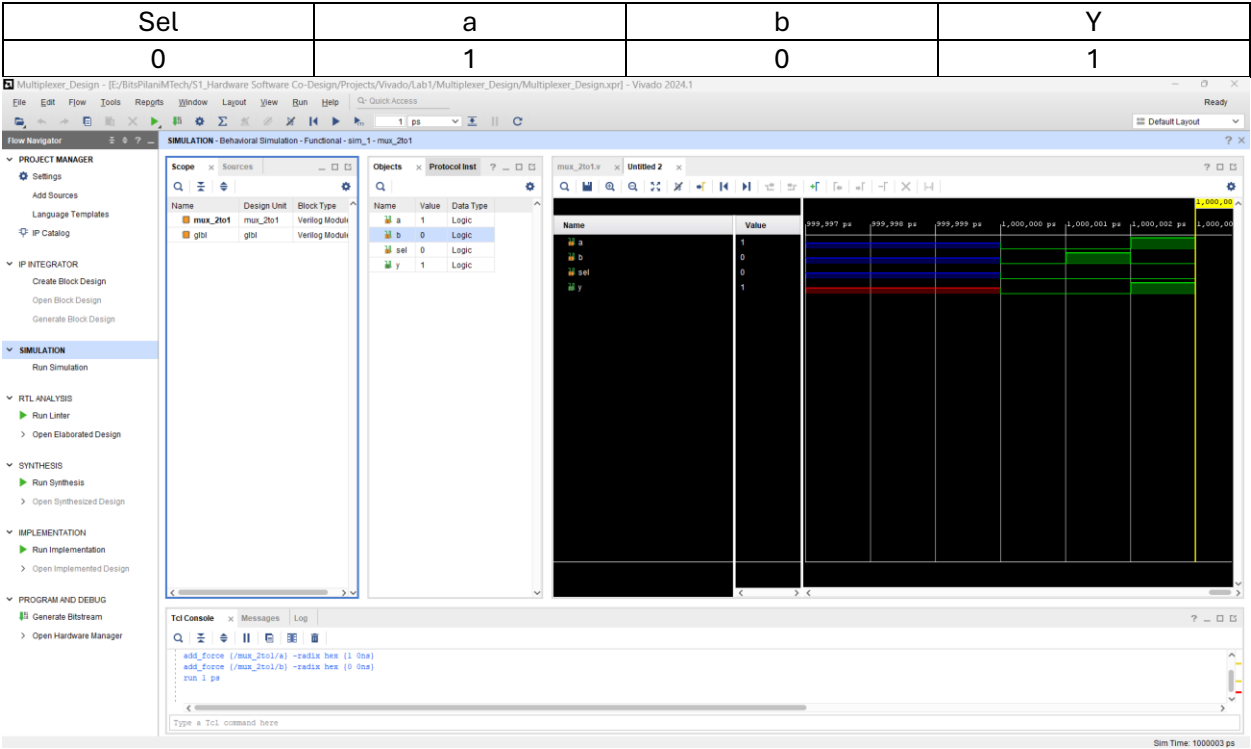
SIMULATION RESULTS 1 >>



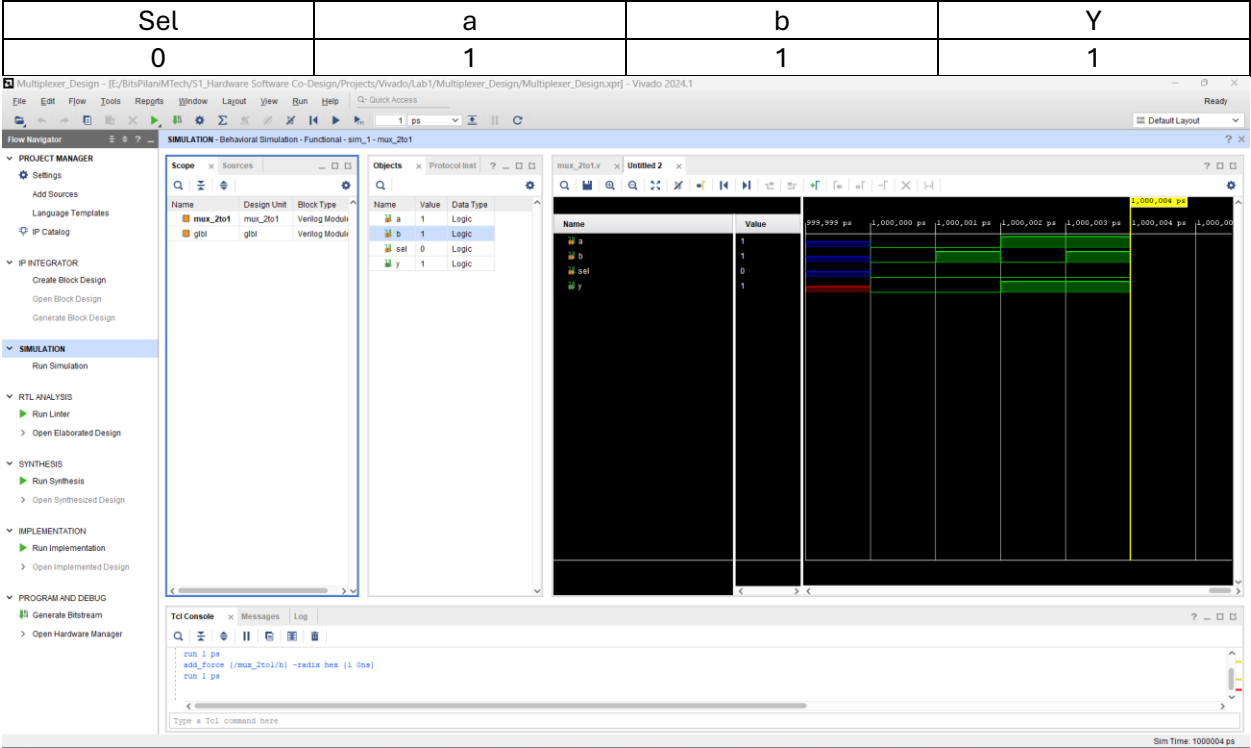
SIMULATION RESULTS 2 >>



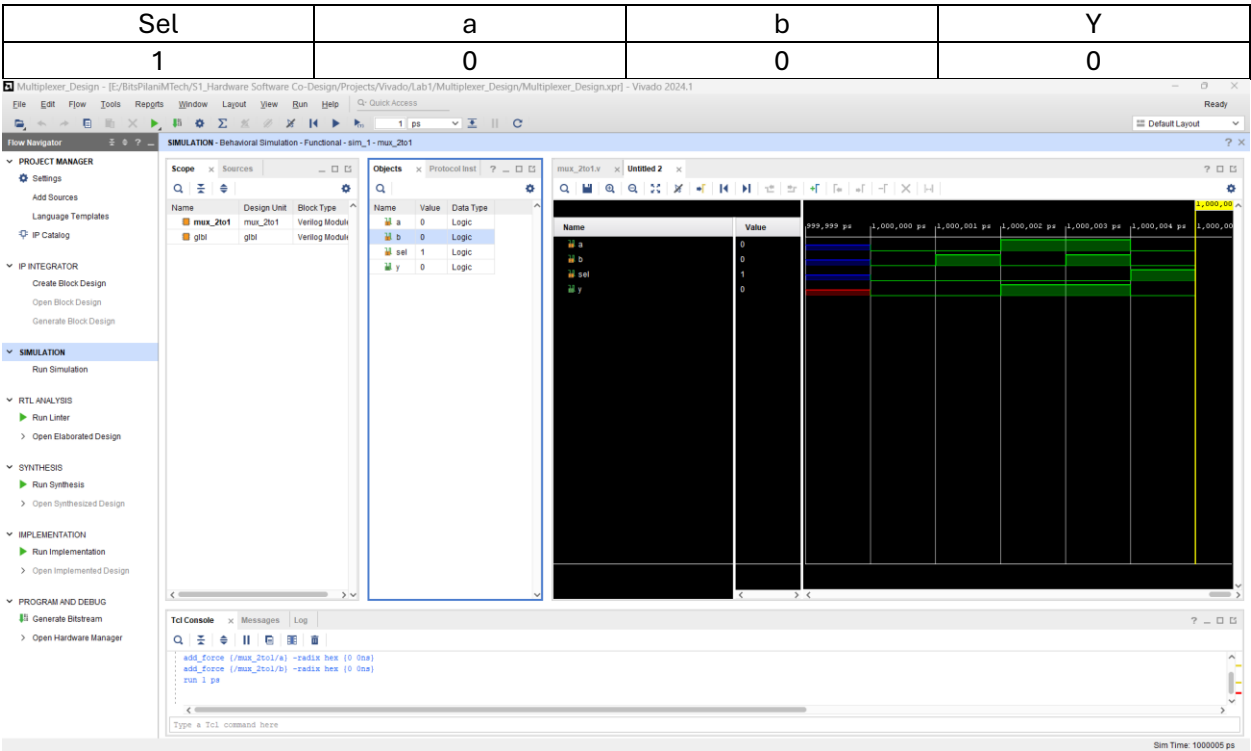
SIMULATION RESULTS 3 >>



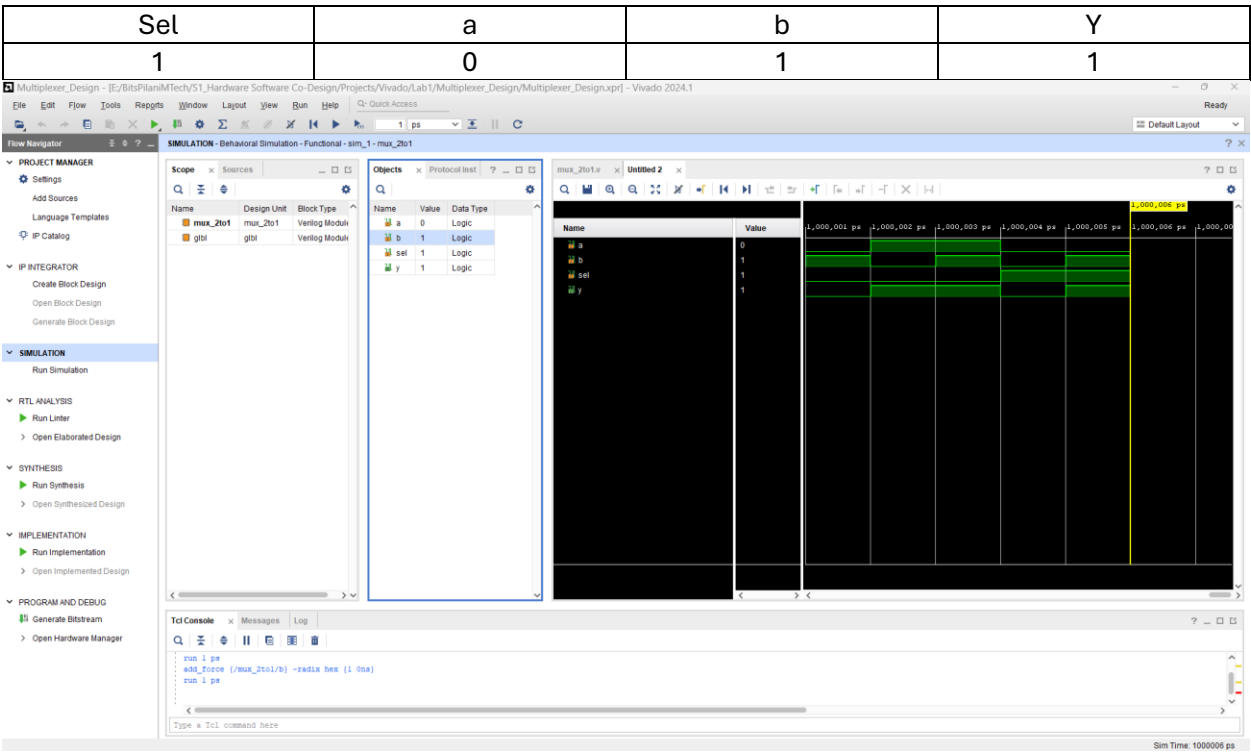
SIMULATION RESULTS 4 >>



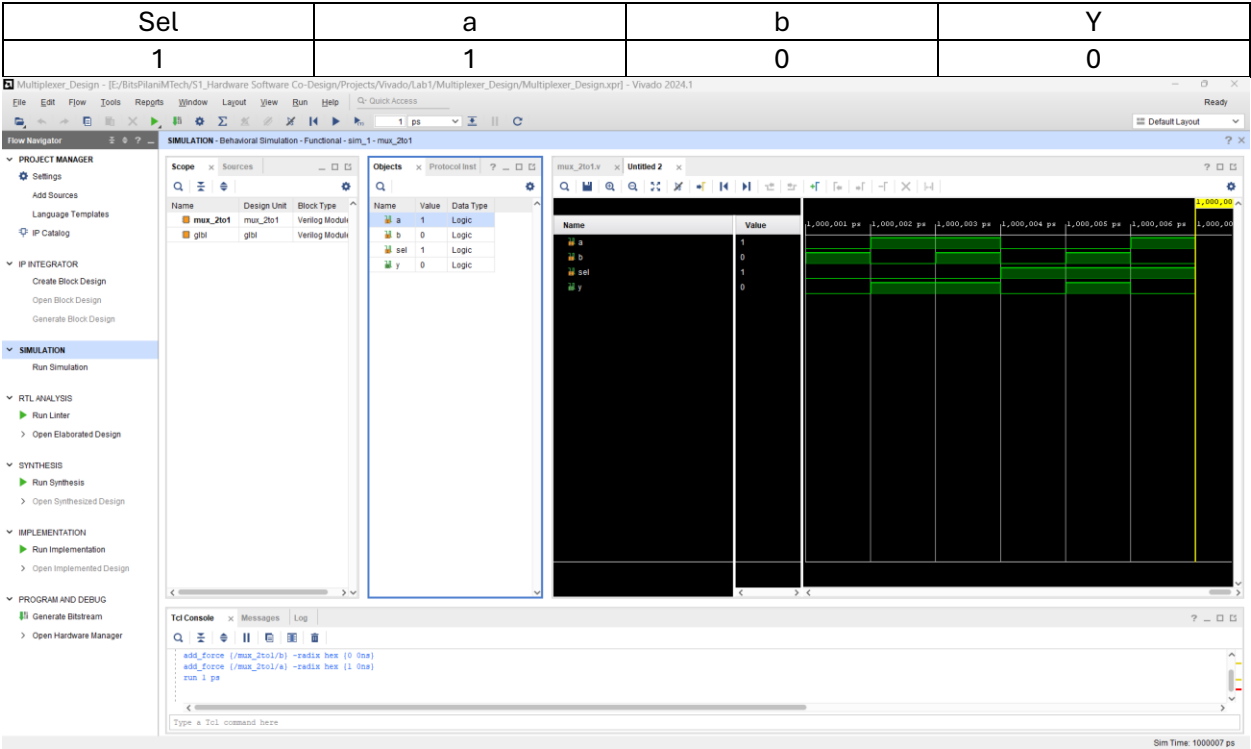
SIMULATION RESULTS 5 >>



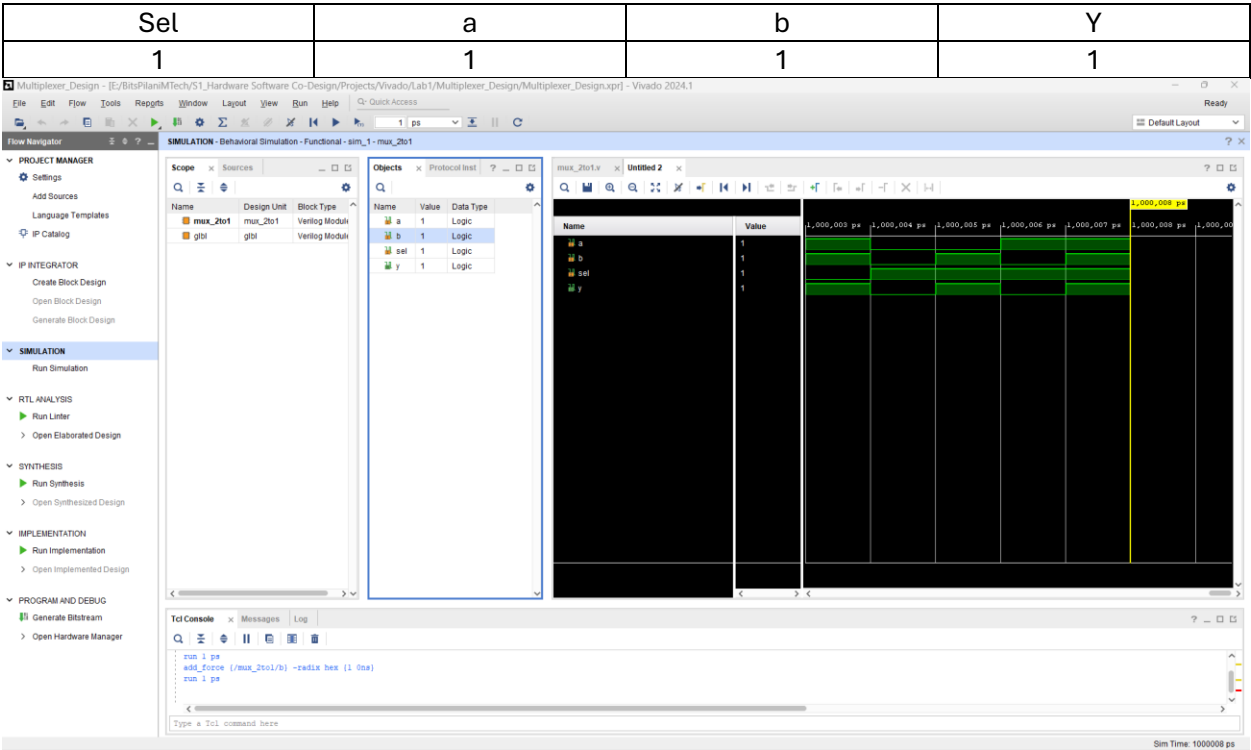
SIMULATION RESULTS 6 >>



SIMULATION RESULTS 7 >>



SIMULATION RESULTS 8 >>



ELABORATED DESIGN >>

ELABORATED DESIGN - xc7z020dpg484-1

Sources | **Netlist**

- mux_2to1
- Nets (4)
- Leaf Cells (1)

Simulation Object Properties

Select an object to see properties

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	
synth_1	constraints_1	Not started																				Vivado Synthesis Defaults (Vivado Synthesis 2024)
impl_1	constraints_1	Not started																				Vivado Implementation Defaults (Vivado Implementation 2024)

SYNTHESIZED DESIGN >>

SYNTHESIZED DESIGN - xc7z020dpg484-1

Sources | **Netlist**

- mux_2to1
- Nets (8)
- Leaf Cells (5)
- a_OBUF_inst (OBUF)
- b_OBUF_inst (OBUF)
- sel_OBUF_inst (OBUF)
- y_OBUF_inst (OBUF)
- y_OBUF_inst_L1 (LUT3)

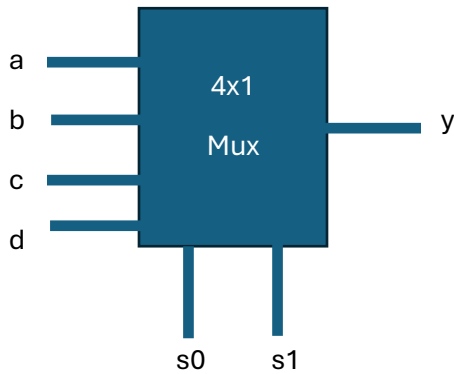
Cell Properties

Name: y_OBUF_inst
Reference name: OBUF
Type: IO

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	
synth_1	constraints_1	Completed																				Vivado Synthesis Defaults (Vivado Synthesis 2024)
impl_1	constraints_1	Completed																				Vivado Implementation Defaults (Vivado Implementation 2024)

Task 2 : Design 4-to-1 Multiplexer



Truth Table

s1	s0	y
0	0	a
0	1	b
1	0	c
1	1	d

DESIGN SOURCE CODE >>

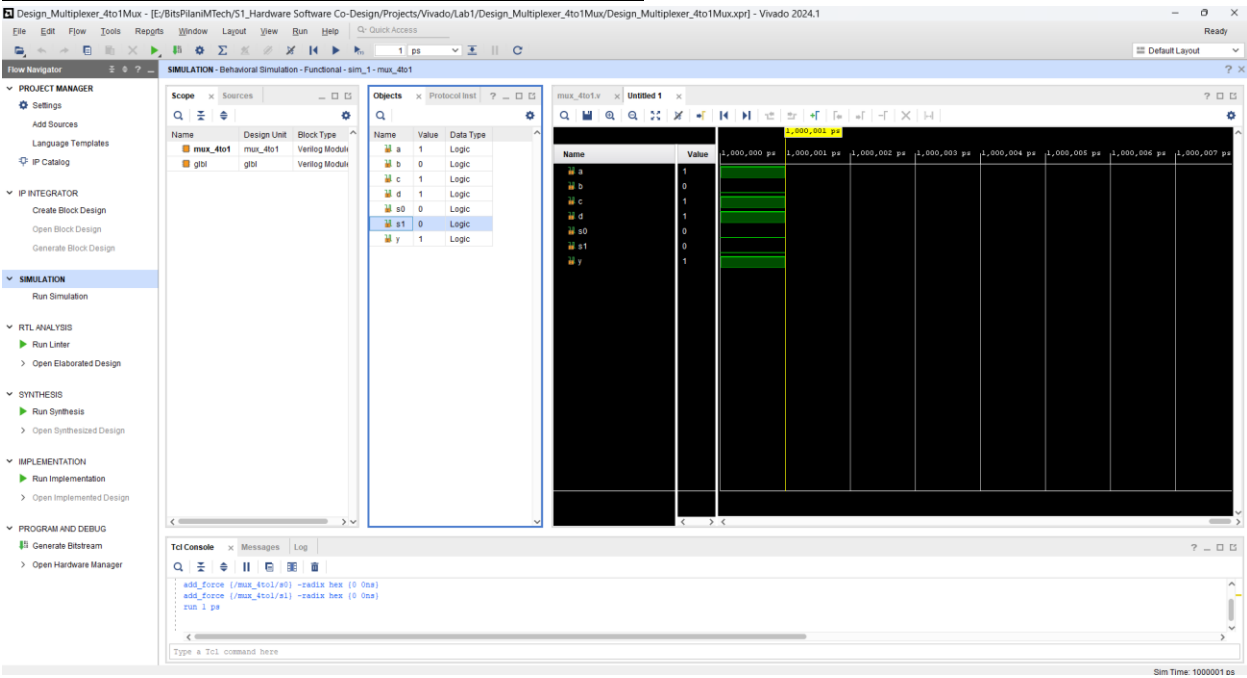
```
// Design_Multiplexer_4to1Mux - [E:/BitsPlanITech/S1_Hardware Software Co-Design/Projects/Vivado/Lab1/Design_Multiplexer_4to1Mux/Design_Multiplexer_4to1Mux.vpr] - Vivado 2024.1
// Designer Name: Ashutosh Narve
// Module Name: mux_4to1
// Project Name: Design Multiplexer
// Target Devices:
// Tool Versions:
// Description:
// Dependencies:
//
// Revision:
// Version 0.01 - File Created
// Additional Comments:
//
//
// =====
21
22
23 module mux_4to1
24     input a,
25     input b,
26     input c,
27     input d,
28     input s0,
29     input s1,
30     input y
31     //
32
33     assign y = s1 ? (s0 ? d : c) : (s0 ? b : a);
34 endmodule
35
```

Tcl Console

```
Design is defaulting to synth run path: xc7z020clg484-1
Netlist sorting complete. Time (h): ops = 00:00:00 ; elapsed = 00:00:00.001 ; Memory (MB): peak = 2422.512 ; gain = 0.000
INFO: (Project 1-475) Netlist was created with Vivado 2024.1
INFO: (Project 1-570) Preparing netlist for logic optimization
INFO: (Opt 31-188) Running 0 inverters to 0 load pin(s).
Netlist sorting complete. Time (h): ops = 00:00:00 ; elapsed = 00:00:00 ; Memory (MB): peak = 2422.512 ; gain = 0.000
INFO: (Project 1-111) Unisim Transformation Summary:
0 No Unisim elements were transformed.
```

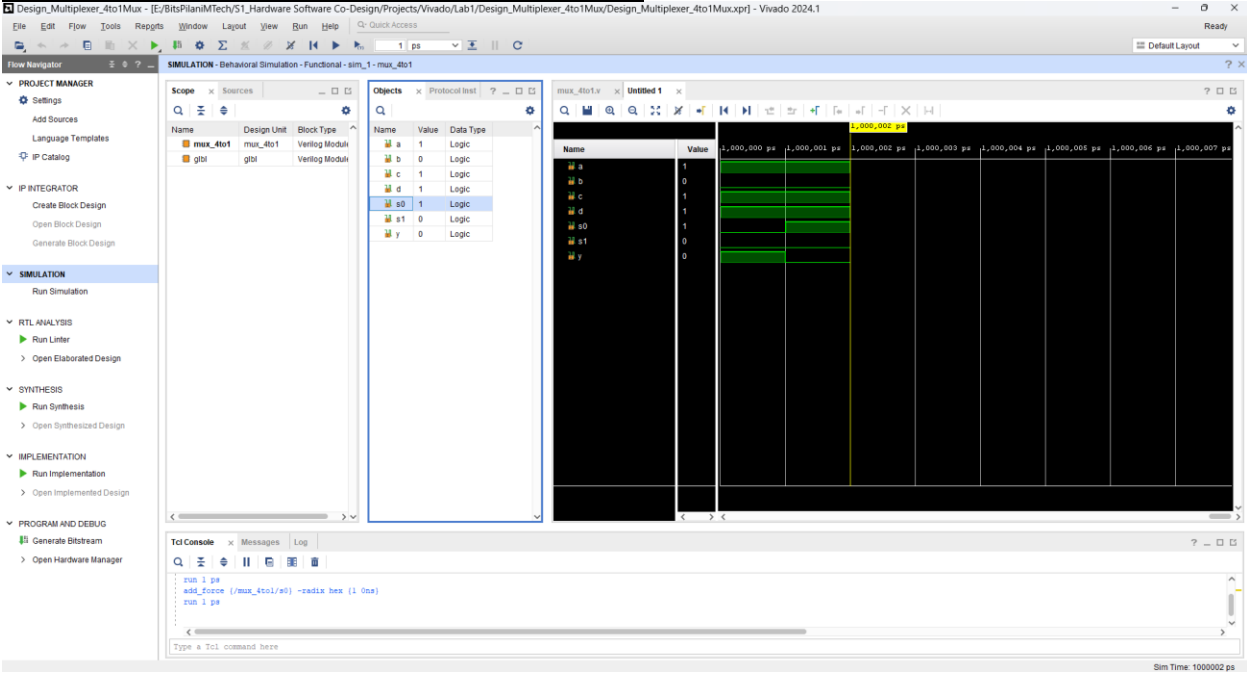

SIMULATION RESULTS 1 >>

s1	s0	y
0	0	a



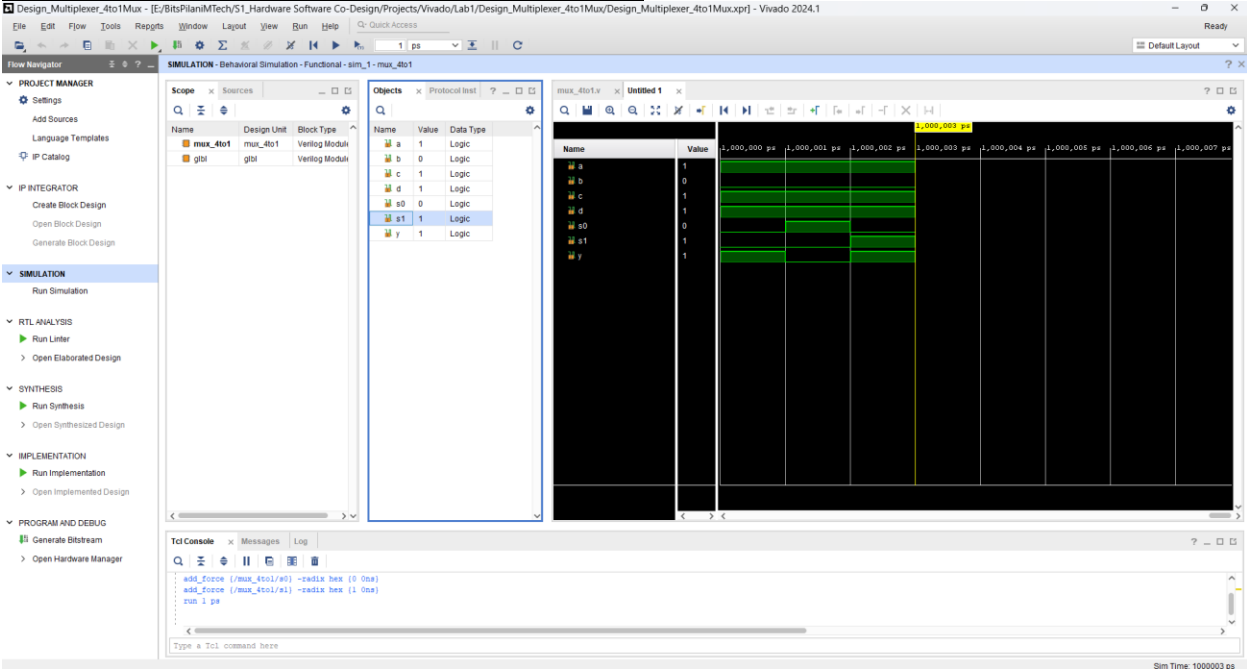
SIMULATION RESULTS 2 >>

s1	s0	y
0	1	b



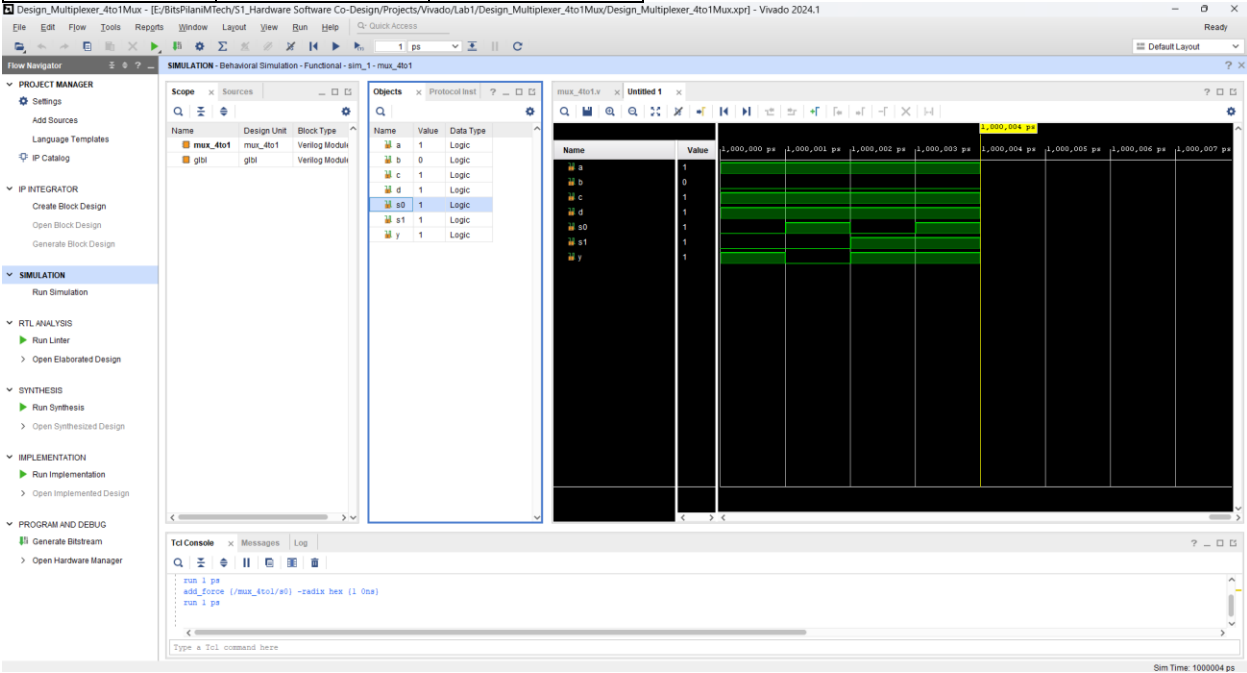
SIMULATION RESULTS 3 >>

s1	s0	y
1	0	c



SIMULATION RESULTS 4 >>

s1	s0	y
1	1	d



ELABORATION DESIGN >>

Design_Multiplexer_4to1Mux - [E:/BitsPianiM/Tech/S1_Hardware Software Co-Design/Projects/Vivado/Lab1/Design_Multiplexer_4to1Mux/Design_Multiplexer_4to1Mux.xpr] - Vivado 2024.1

ELABORATED DESIGN - xc7z020cpg484-1

Project Summary x Schematic x mux_4to1.x x

3 Cells 7 I/O Ports 9 Nets

RTL_MUX

RTL_MUX_0

RTL_MUX_1

RTL_MUX

Simulation Object Properties

Select an object to see properties

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	CoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	
synth_1	constraints_1	Not started																				Vivado Synthesis Defaults (Vivado Synthesis 2024)
impl_1	constraints_1	Not started																				Vivado Implementation Defaults (Vivado Implementation 2024)

SYNTHESIZED DESIGN >>

Design_Multiplexer_4to1Mux - [E:/BitsPianiM/Tech/S1_Hardware Software Co-Design/Projects/Vivado/Lab1/Design_Multiplexer_4to1Mux/Design_Multiplexer_4to1Mux.xpr] - Vivado 2024.1

SYNTHESIZED DESIGN - xc7z020cpg484-1

Project Summary x Device x mux_4to1.x x

Properties

Select an object to see properties

Tcl Console Messages Log Reports Design Runs

Design is defaulting to synth run part: xc7z020cpg484-1

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 ; Memory (MB): peak = 2422.512 ; gain = 0.000

INFO: (Project 1-479) Netlist was created with Vivado 2024.1

INFO: (Project 1-570) Preparing netlist for logic optimization

INFO: (Opt 31-138) Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 ; Memory (MB): peak = 2422.512 ; gain = 0.000

INFO: (Project 1-111) This is Transformation Summary:

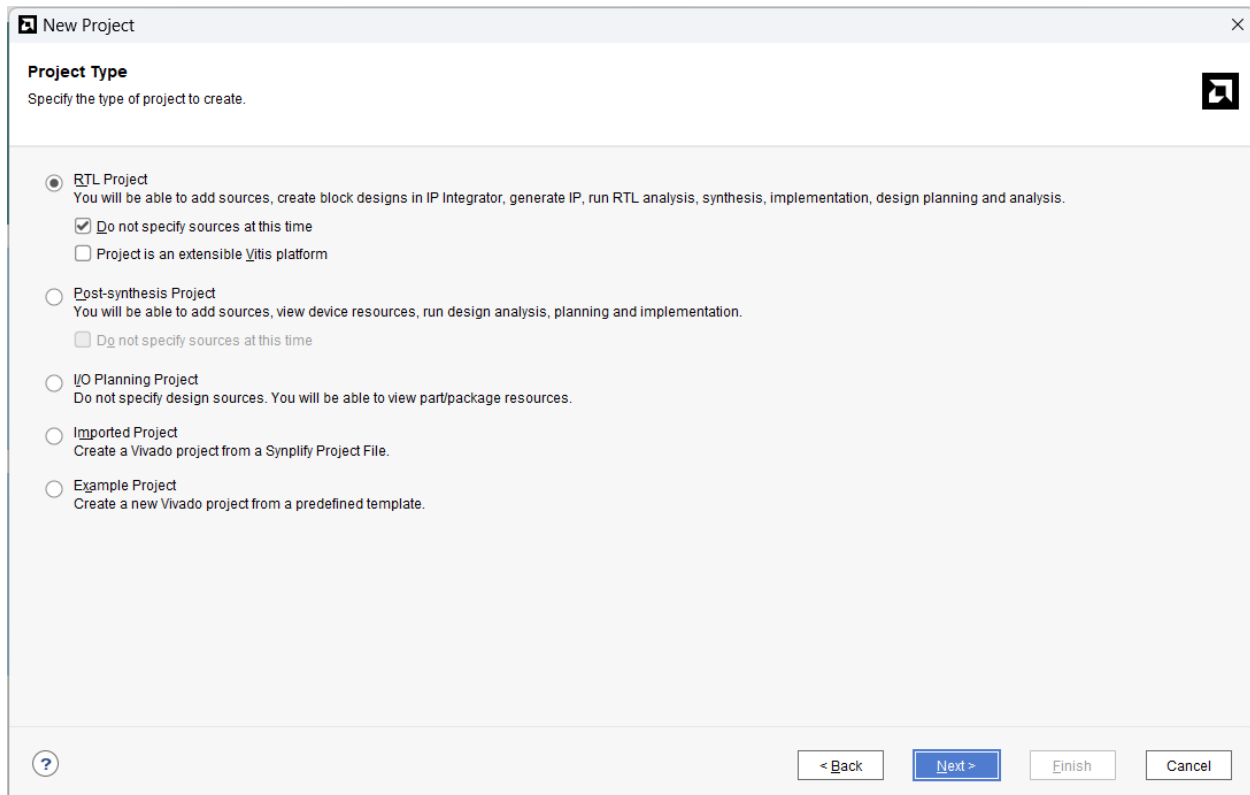
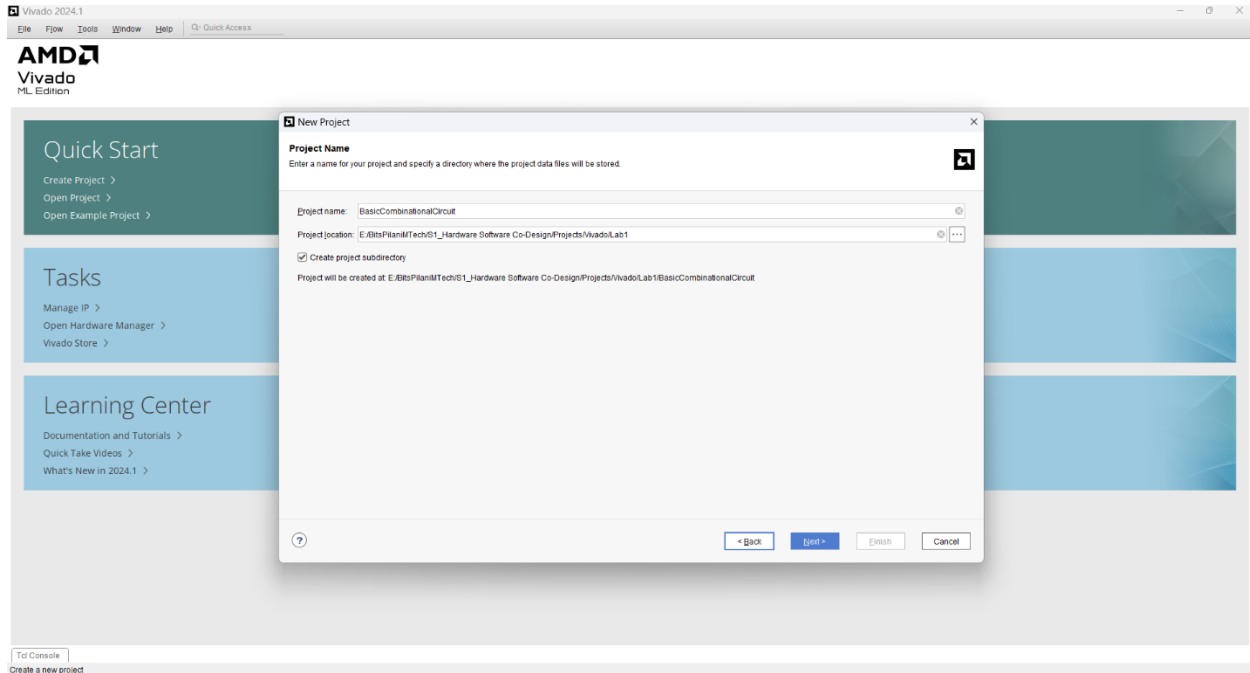
No Unisim elements were transformed.

+++++ASSIGNMENT END+++++

<< BASIC HOW TO CREATE PROJECT IN VIVADO >>

Creating New Project on vivado FPGA >>

Files >> New Proeject



Search for ZedBoard >>

New Project

Default Part

Choose a default AMD part or board for your project.

Parts | Boards

To fetch the latest available boards from git repository, click on 'Refresh' button. [Dismiss](#)

[Reset All Filters](#)

Vendor: All

Name: All

Board Rev: Latest

Search: Q zedboard

(2 matches)

Display Name	Preview	Status	Vendor	File Version	Part	I/O Pin Count	Board Rev	Available I/Os
ZedBoard Zynq Evaluation and Development Kit			avnet.com	1.4				
Zedboard			digilentinc.com	1.0	xc7z020clg484-1	484	D.3	200

Refresh

Catalog was last updated on 08/18/2024 12:32:31 PM

< Back

Next >

Finish

Cancel

New Project

AMD

Vivado

ML Edition

New Project Summary

A new RTL project named 'Multiplexer_Design' will be created.

The default part and product family for the new project:
Default Board: Zedboard
Default Part: xc7z020clg484-1
Family: Zynq-7000
Package: clg484
Speed Grade: -1

To create the project, click Finish

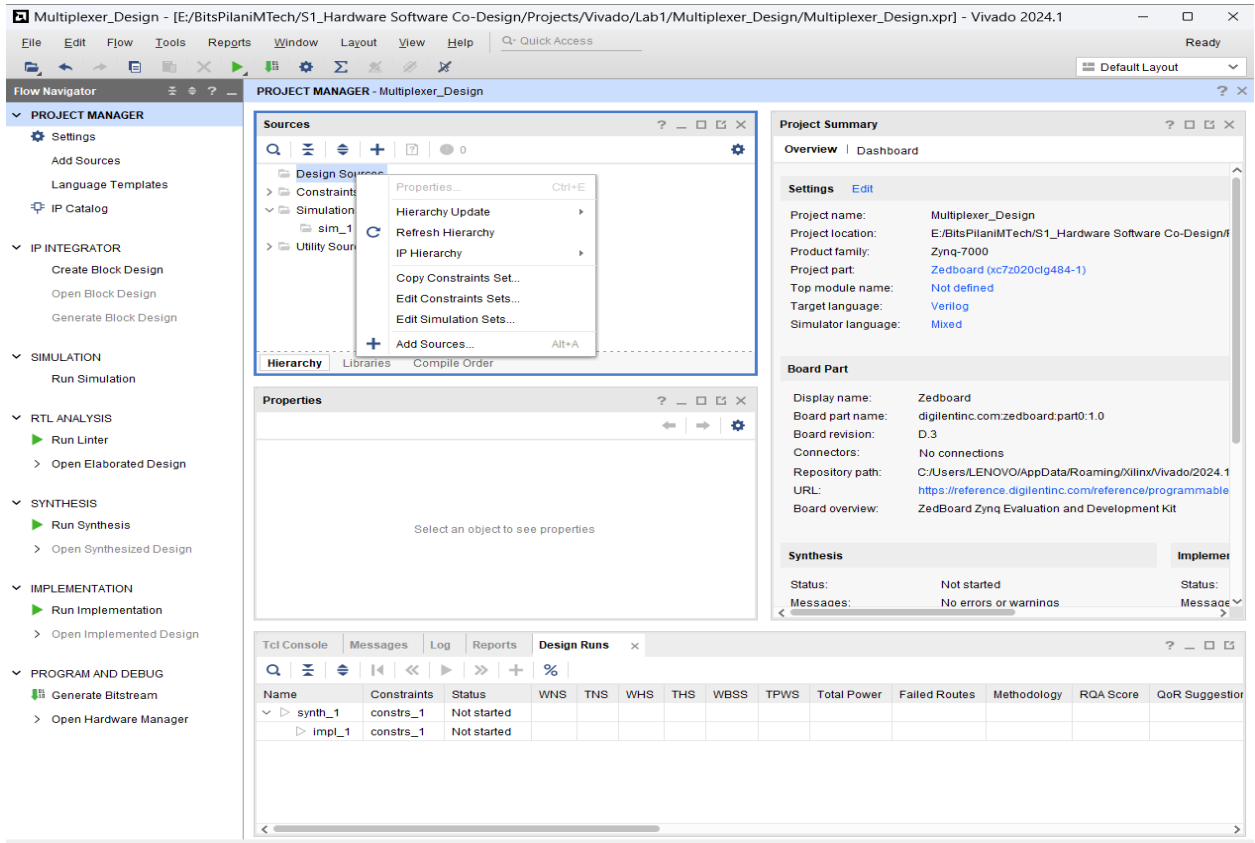
< Back

Next >

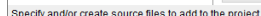
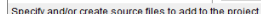
Finish

Cancel

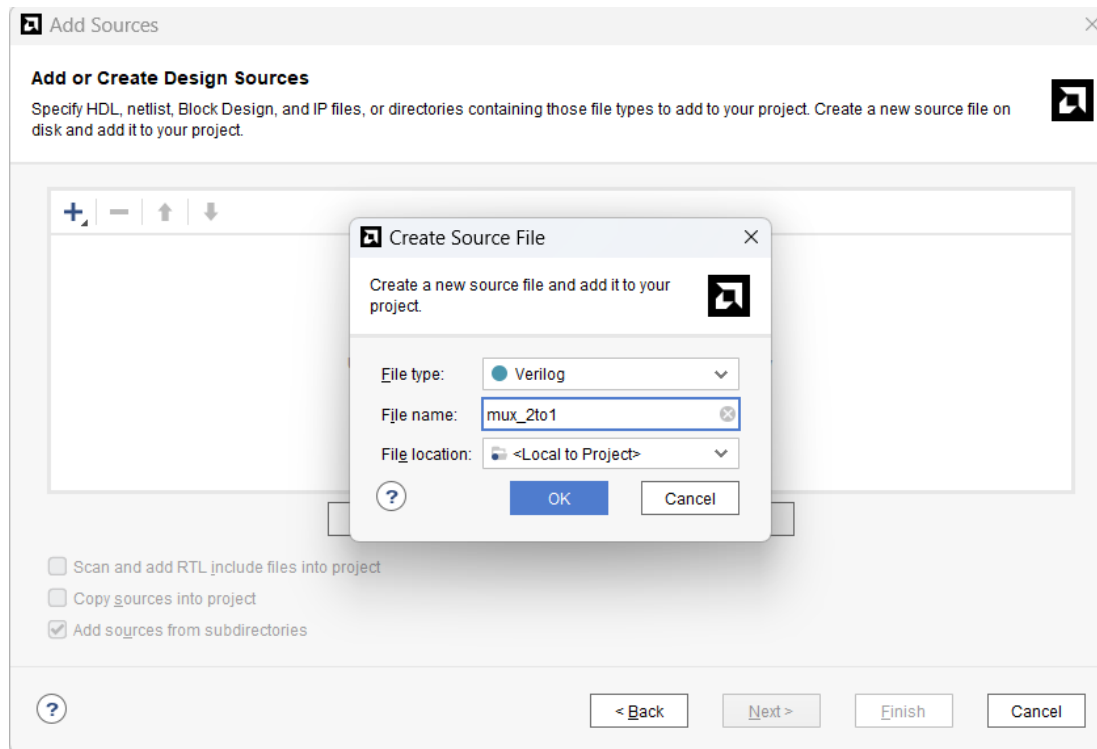
The screenshot displays the Vivado 2024.1 Project Manager interface for a project named 'Multiplexer_Design'. The interface is divided into several panes. On the left is the 'Flow Navigator' showing project stages: PROJECT MANAGER, IP INTEGRATOR, SIMULATION, RTL ANALYSIS, SYNTHESIS, IMPLEMENTATION, and PROGRAM AND DEBUG. The main area is titled 'PROJECT MANAGER - Multiplexer_Design' and contains three sub-panes: 'Sources', 'Properties', and 'Design Runs'. The 'Sources' pane shows a hierarchy of 'Design Sources' including 'Constraints', 'Simulation Sources' (with 'sim_1'), and 'Utility Sources'. The 'Properties' pane is currently empty, displaying the message 'Select an object to see properties'. The 'Design Runs' pane at the bottom shows a table of simulation runs. On the right side of the interface is the 'Project Summary' pane, which includes an 'Overview' tab and a 'Dashboard' section. The 'Settings' tab is active, showing project details like 'Project name: Multiplexer_Design', 'Project location: E:/BitsPilaniMITech/S1_Hardware Software Co-Design/Projects/Vivado/Lab1/Multiplexer_Design/Multiplexer.xpr', 'Product family: Zynq-7000', 'Project part: Zedboard (xc7z020cpg484-1)', 'Top module name: Not defined', 'Target language: Verilog', and 'Simulator language: Mixed'. Below this is the 'Board Part' section, showing details for the 'Zedboard' board, including its display name, board part name, revision, connectors, repository path, URL, and board overview. At the bottom right, the 'Synthesis' and 'Implementation' sections show the status of these tasks, both indicating 'Not started'.



Select + Add Sources >> Add or create design sources >> Next



Click >> create File >> File name >> OK



Click >> Finish

