**HSCD LAB Assignment No. 1**

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Place : Pune, Maharashtra

**Multiplexer Design**

**What is multiplexer?**  
Multiplexer is a combinational logic circuit used to select only one input among several inputs based on selection lines.

**Task 1 : Design 2-to-1 Multiplexer**

2x1

Mux

|  |  |
| --- | --- |
| Sel | Y |
| 0 | a |
| 1 | b |

a

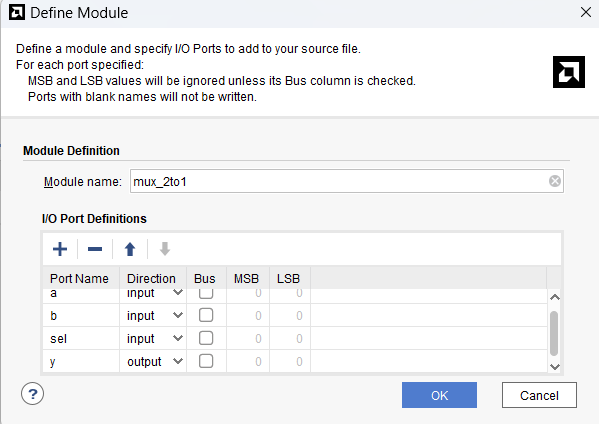
y

b

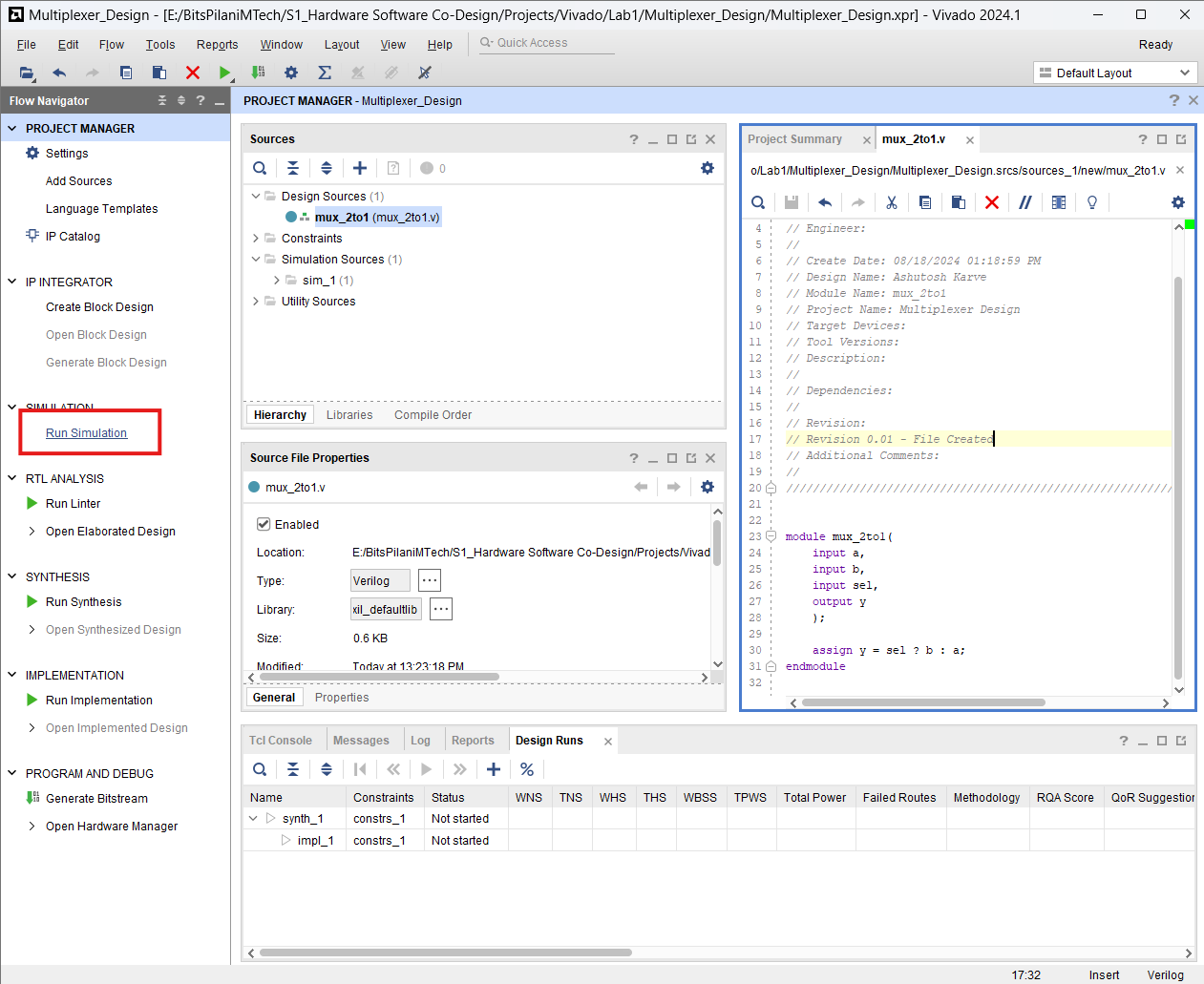
sel

|  |  |  |  |
| --- | --- | --- | --- |
| sel | a | b | y |
| 0 | 0 | X | 0 |
| 0 | 1 | X | 1 |
| 1 | X | 0 | 0 |
| 1 | X | 1 | 1 |

DEFINE MODULE >>

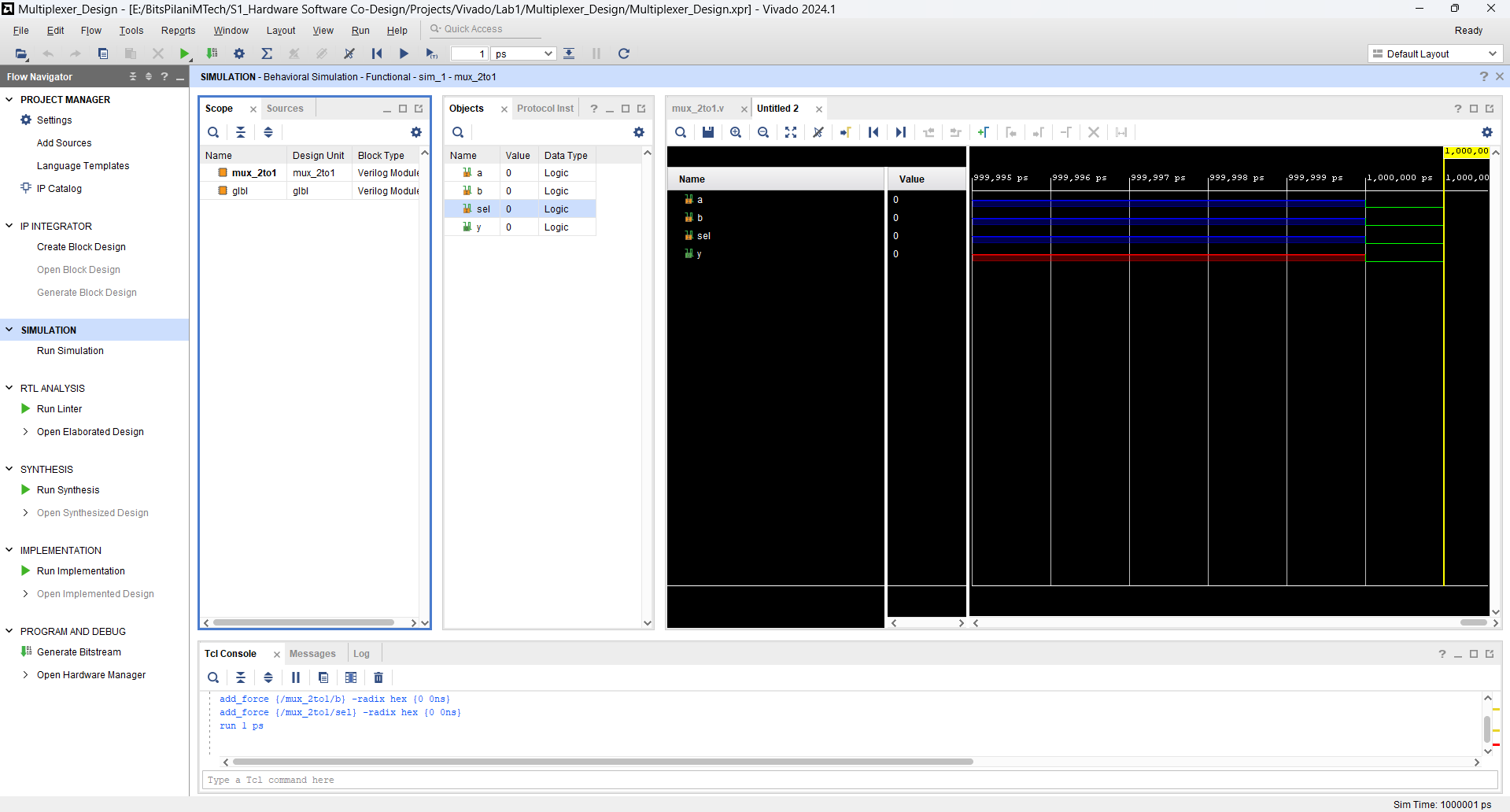


Design Source file >>



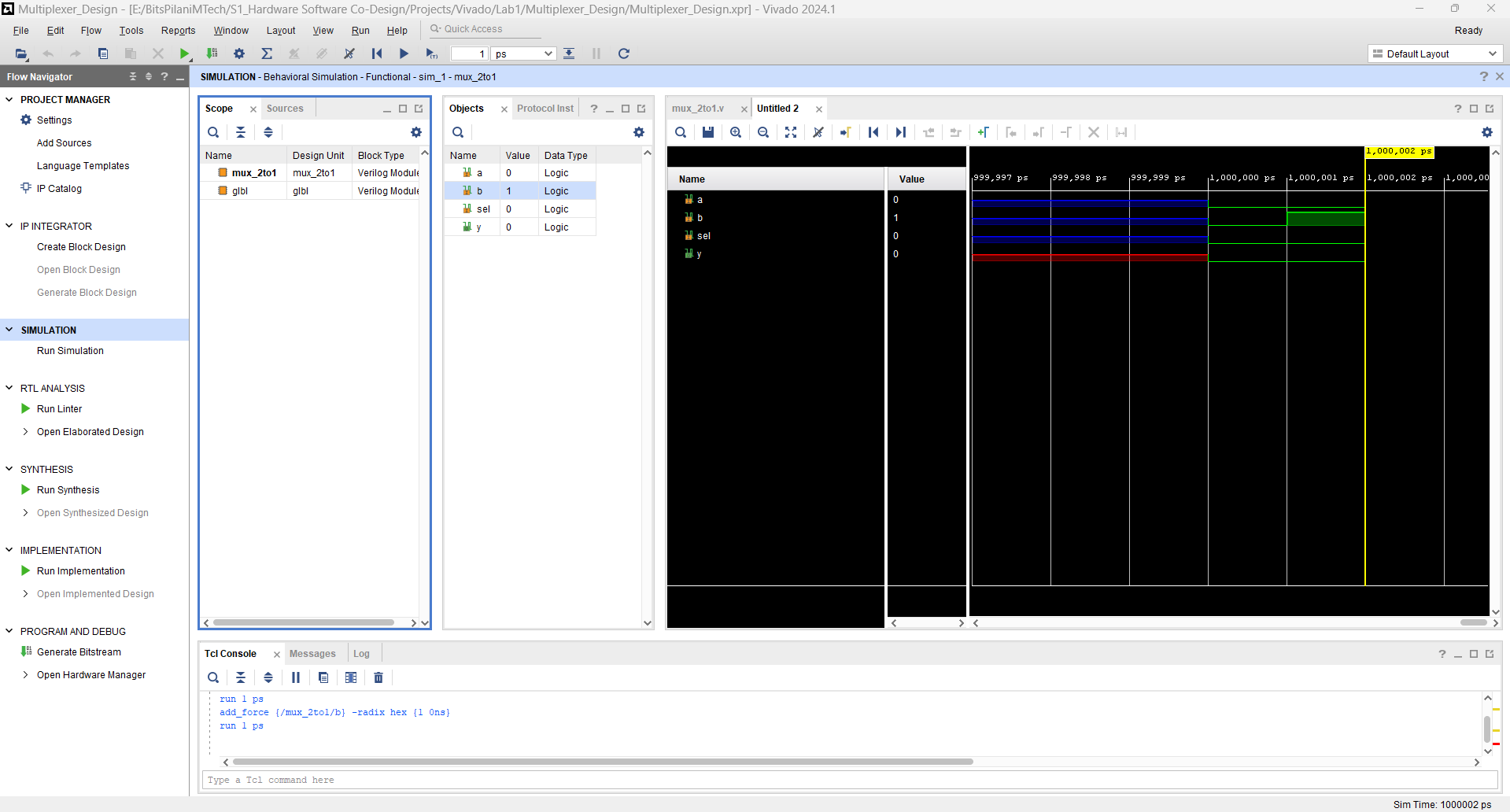
SIMULATION RESULTS 1 >>

|  |  |  |  |
| --- | --- | --- | --- |
| Sel | a | b | Y |
| 0 | 0 | 0 | 0 |



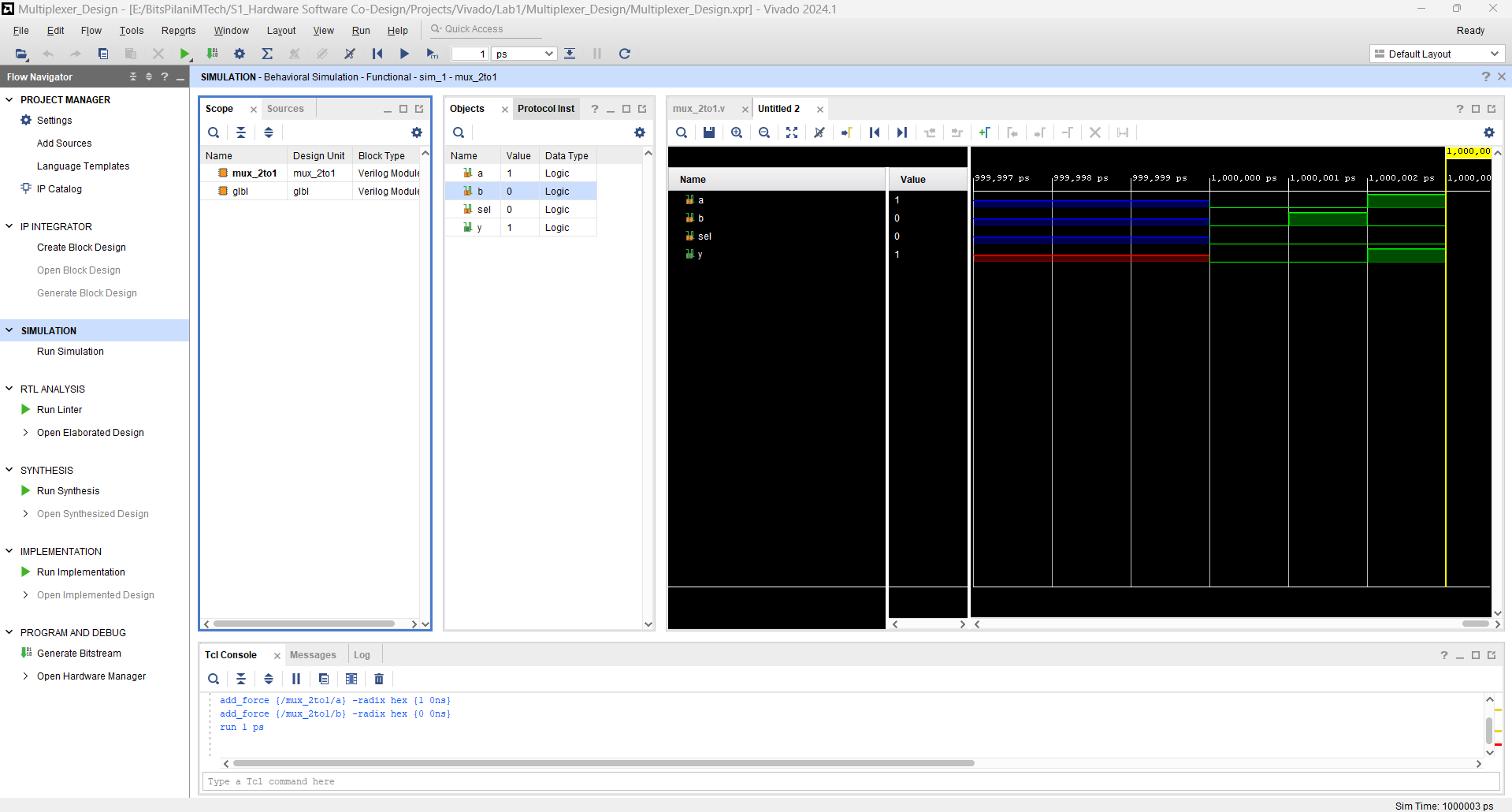
SIMULATION RESULTS 2 >>

|  |  |  |  |
| --- | --- | --- | --- |
| Sel | a | b | Y |
| 0 | 0 | 1 | 0 |



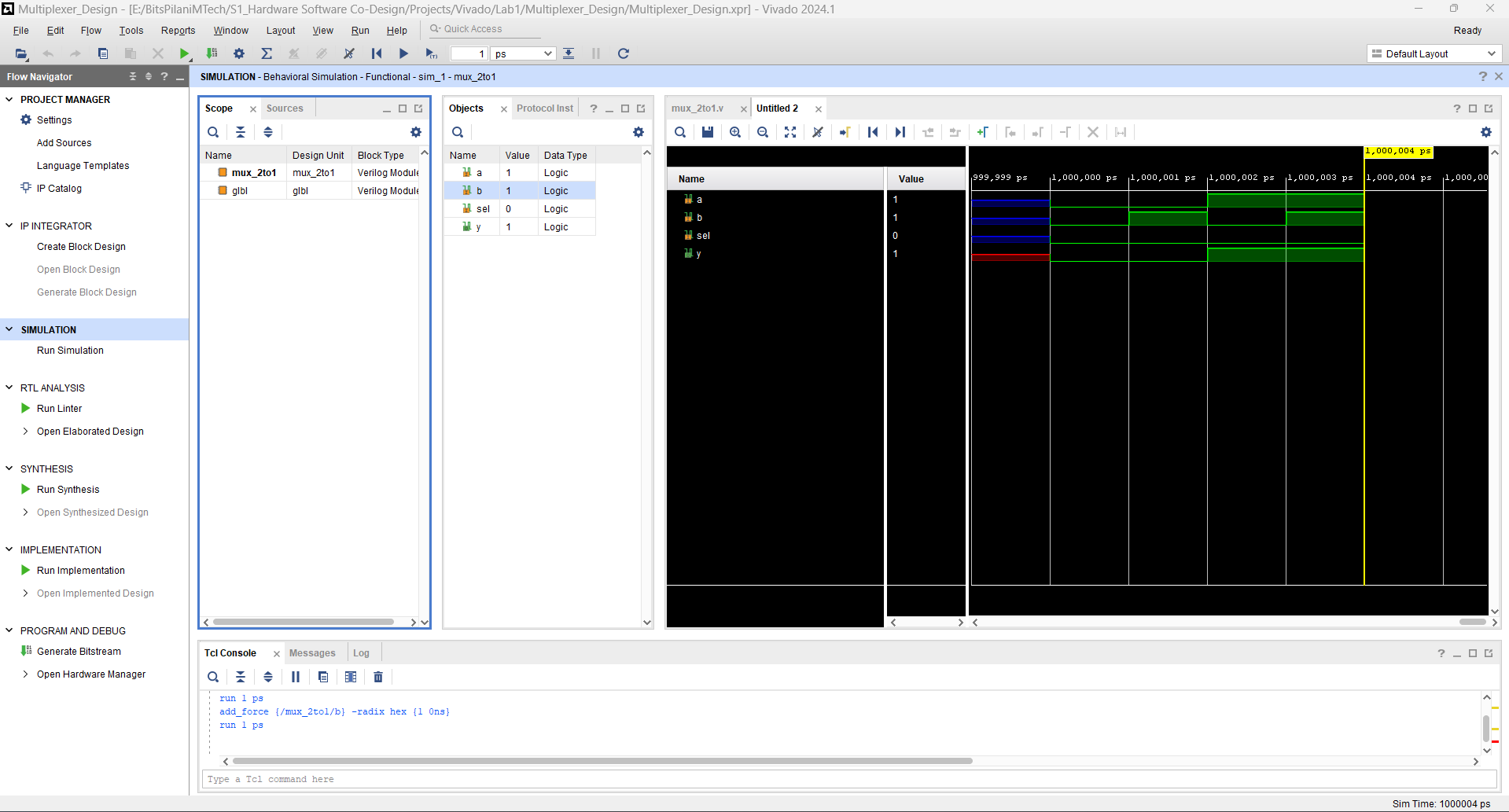
SIMULATION RESULTS 3 >>

|  |  |  |  |
| --- | --- | --- | --- |
| Sel | a | b | Y |
| 0 | 1 | 0 | 1 |



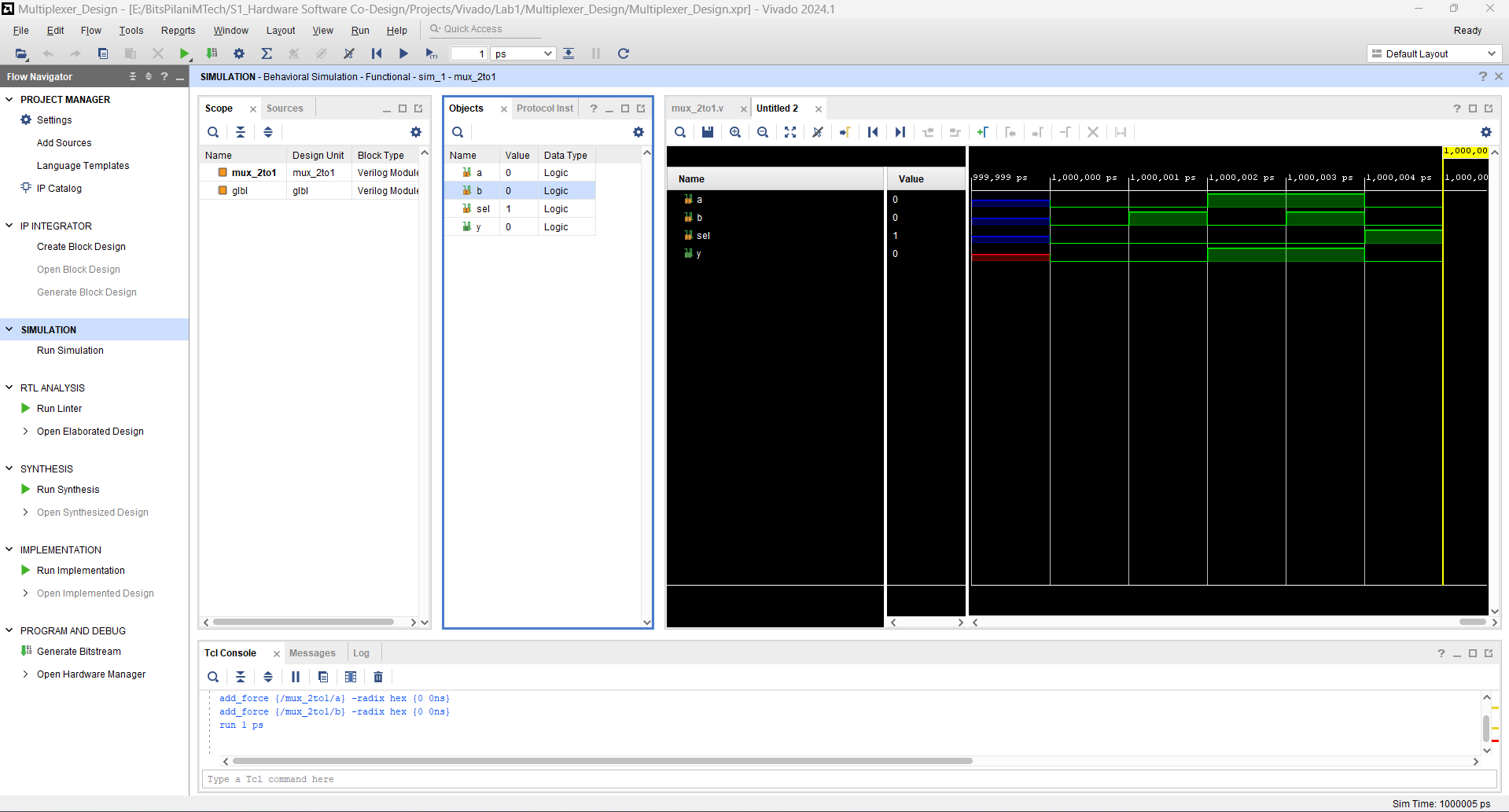
SIMULATION RESULTS 4 >>

|  |  |  |  |
| --- | --- | --- | --- |
| Sel | a | b | Y |
| 0 | 1 | 1 | 1 |



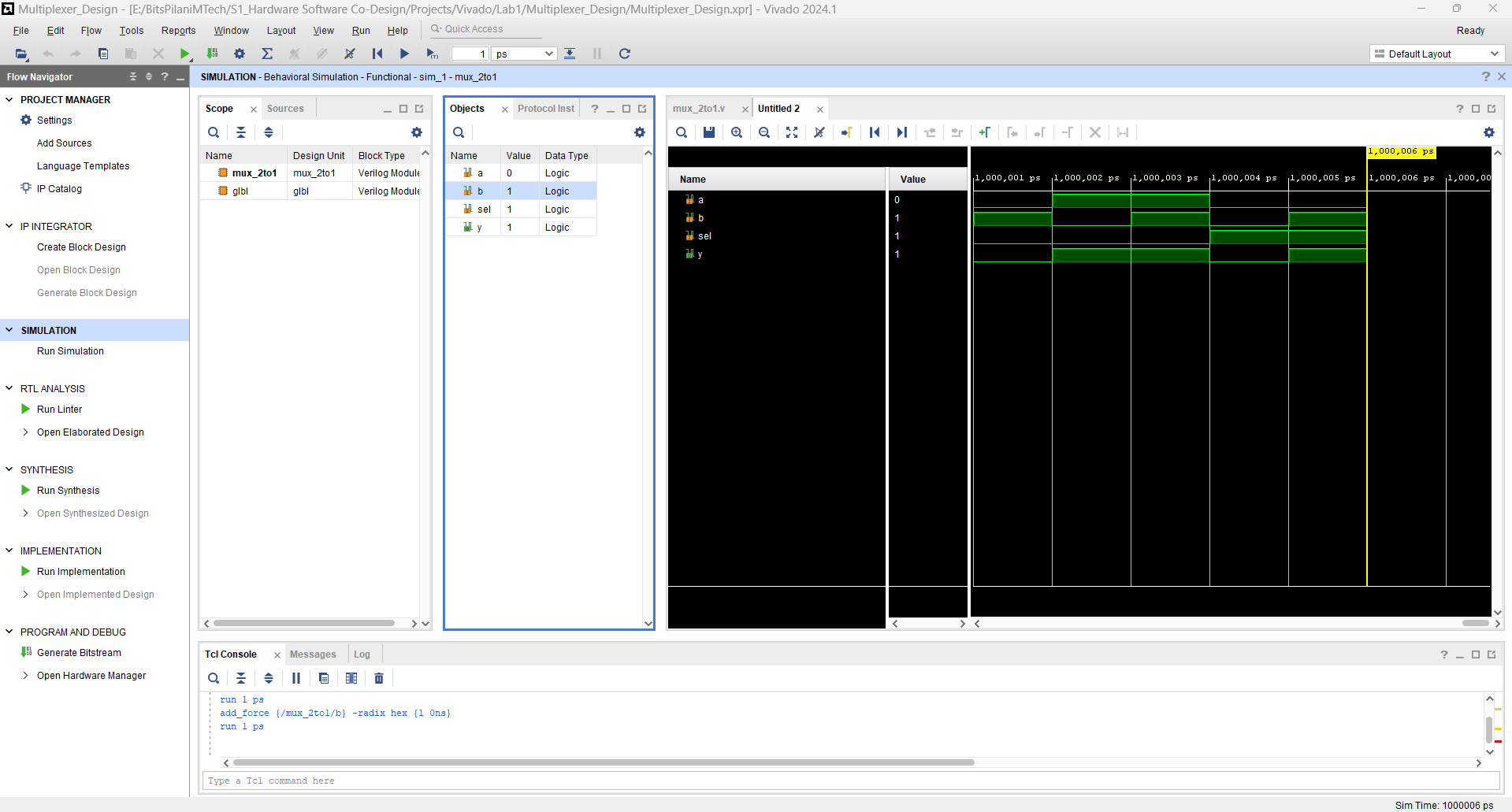
SIMULATION RESULTS 5 >>

|  |  |  |  |
| --- | --- | --- | --- |
| Sel | a | b | Y |
| 1 | 0 | 0 | 0 |



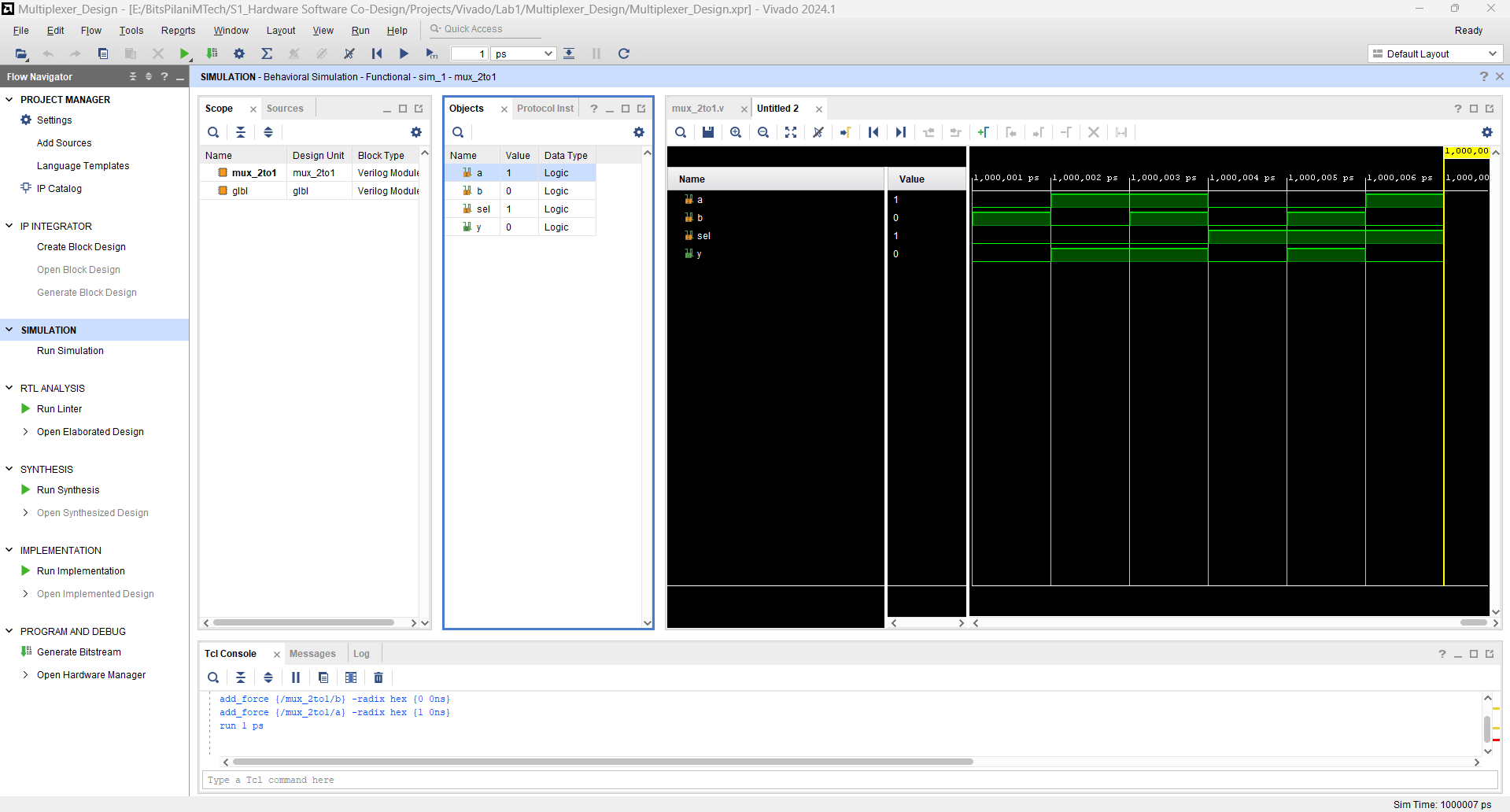
SIMULATION RESULTS 6 >>

|  |  |  |  |
| --- | --- | --- | --- |
| Sel | a | b | Y |
| 1 | 0 | 1 | 1 |



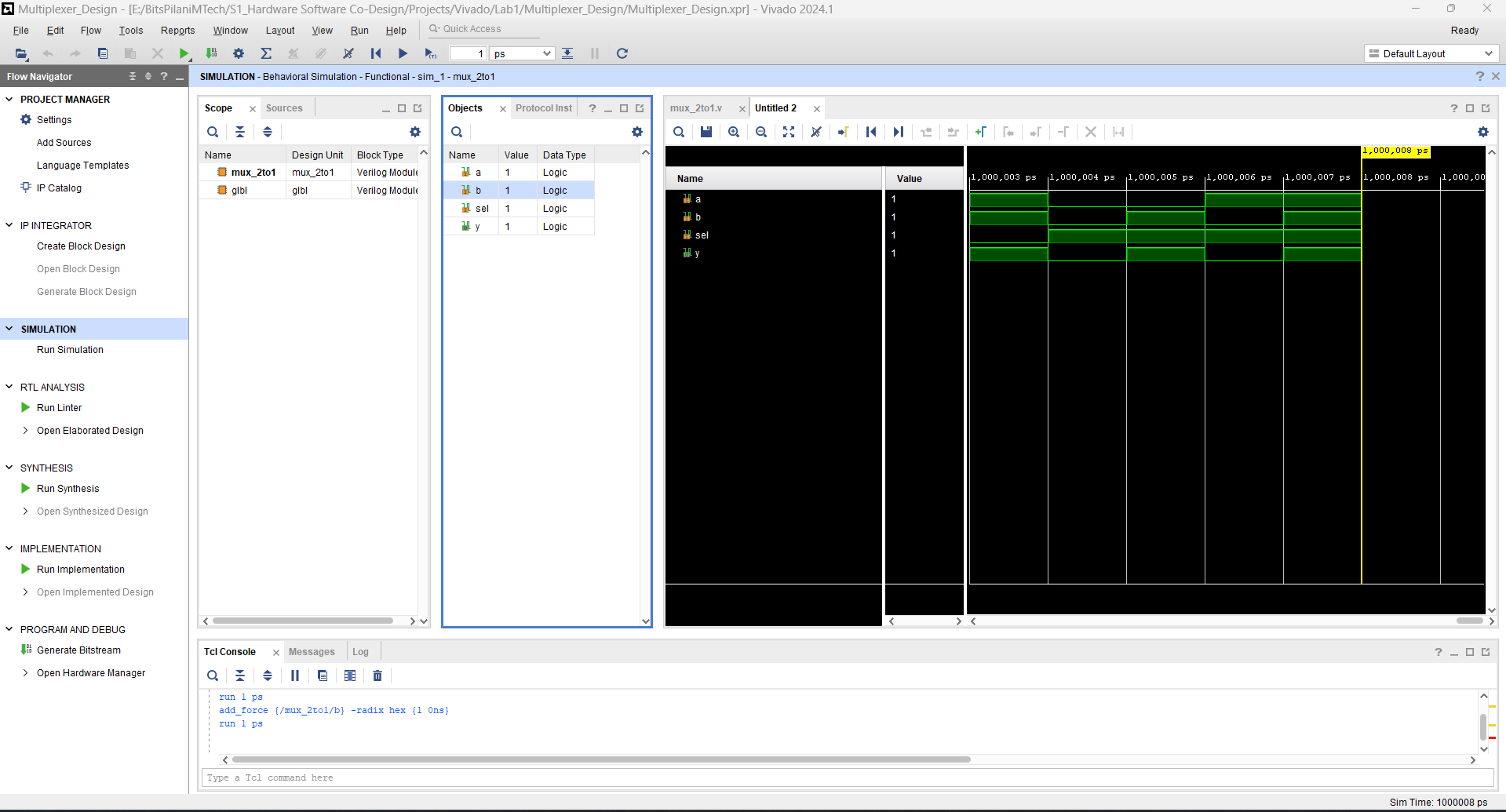
SIMULATION RESULTS 7 >>

|  |  |  |  |
| --- | --- | --- | --- |
| Sel | a | b | Y |
| 1 | 1 | 0 | 0 |

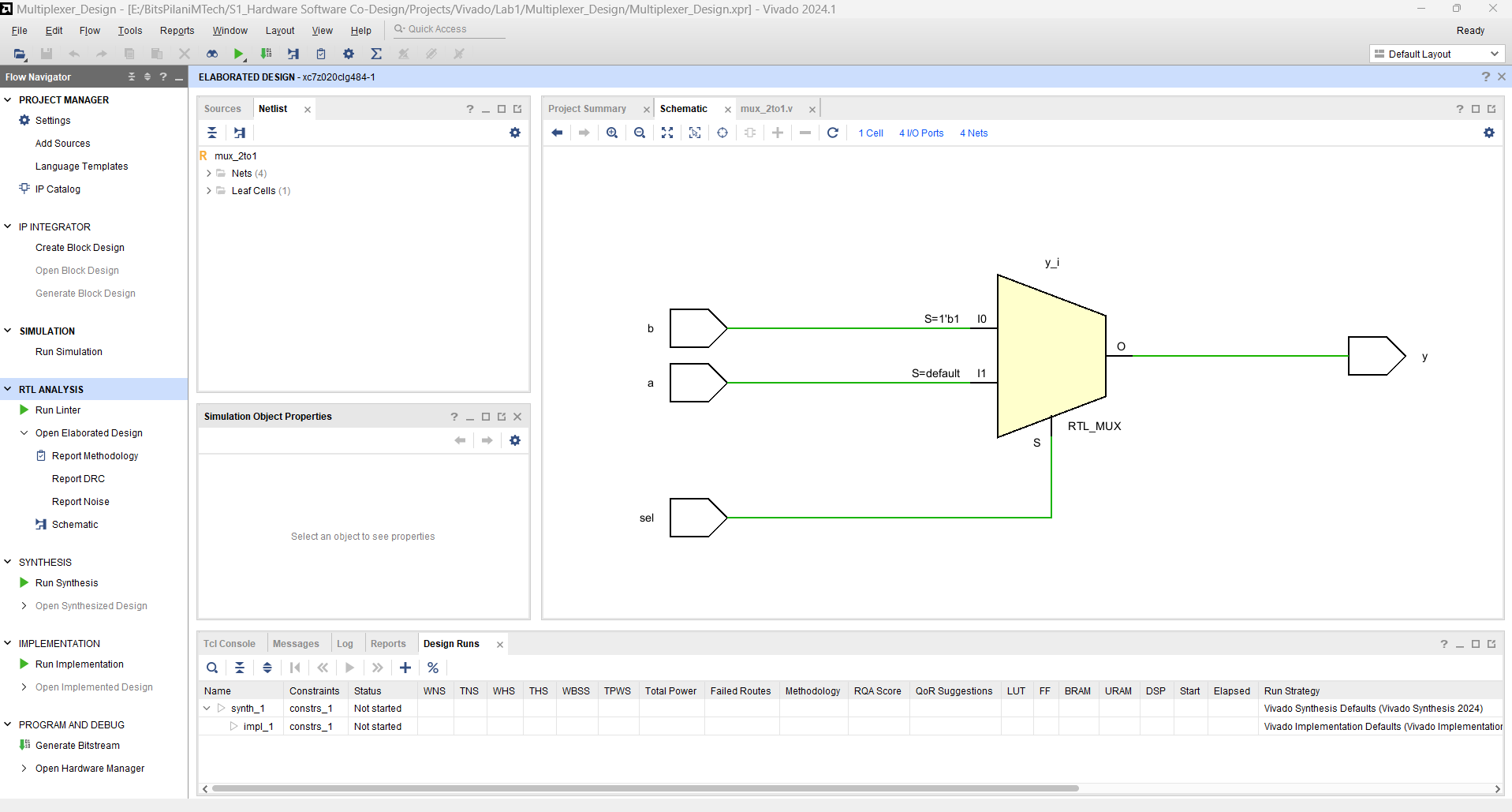


SIMULATION RESULTS 8 >>

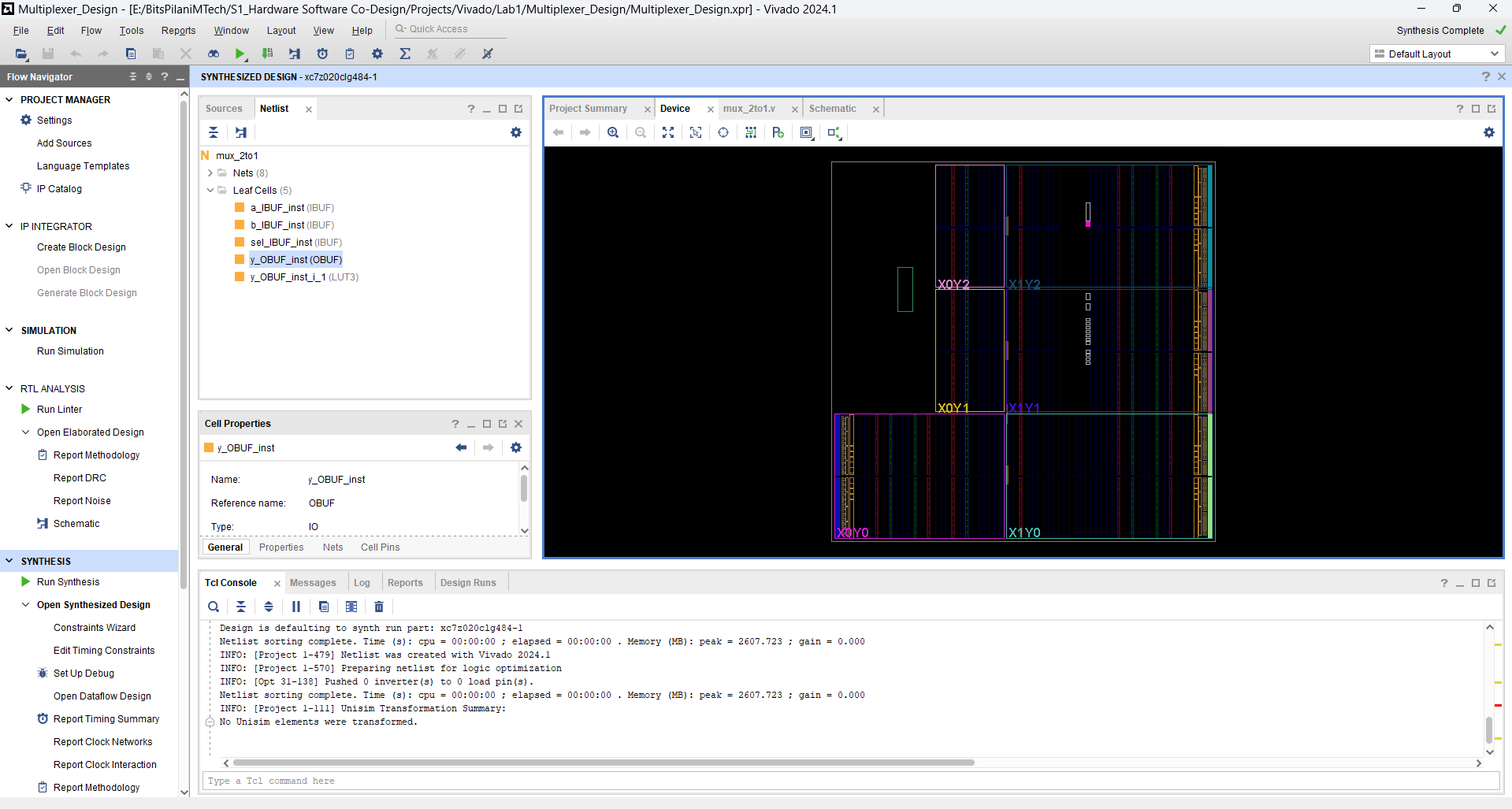
|  |  |  |  |
| --- | --- | --- | --- |
| Sel | a | b | Y |
| 1 | 1 | 1 | 1 |



ELABORATED DESIGN >>



SYNTHESIZED DESIGN >>



**Task 2 : Design 4-to-1 Multiplexer**

4x1

Mux

a Truth Table

|  |  |  |
| --- | --- | --- |
| s1 | s0 | y |
| 0 | 0 | a |
| 0 | 1 | b |
| 1 | 0 | c |
| 1 | 1 | d |

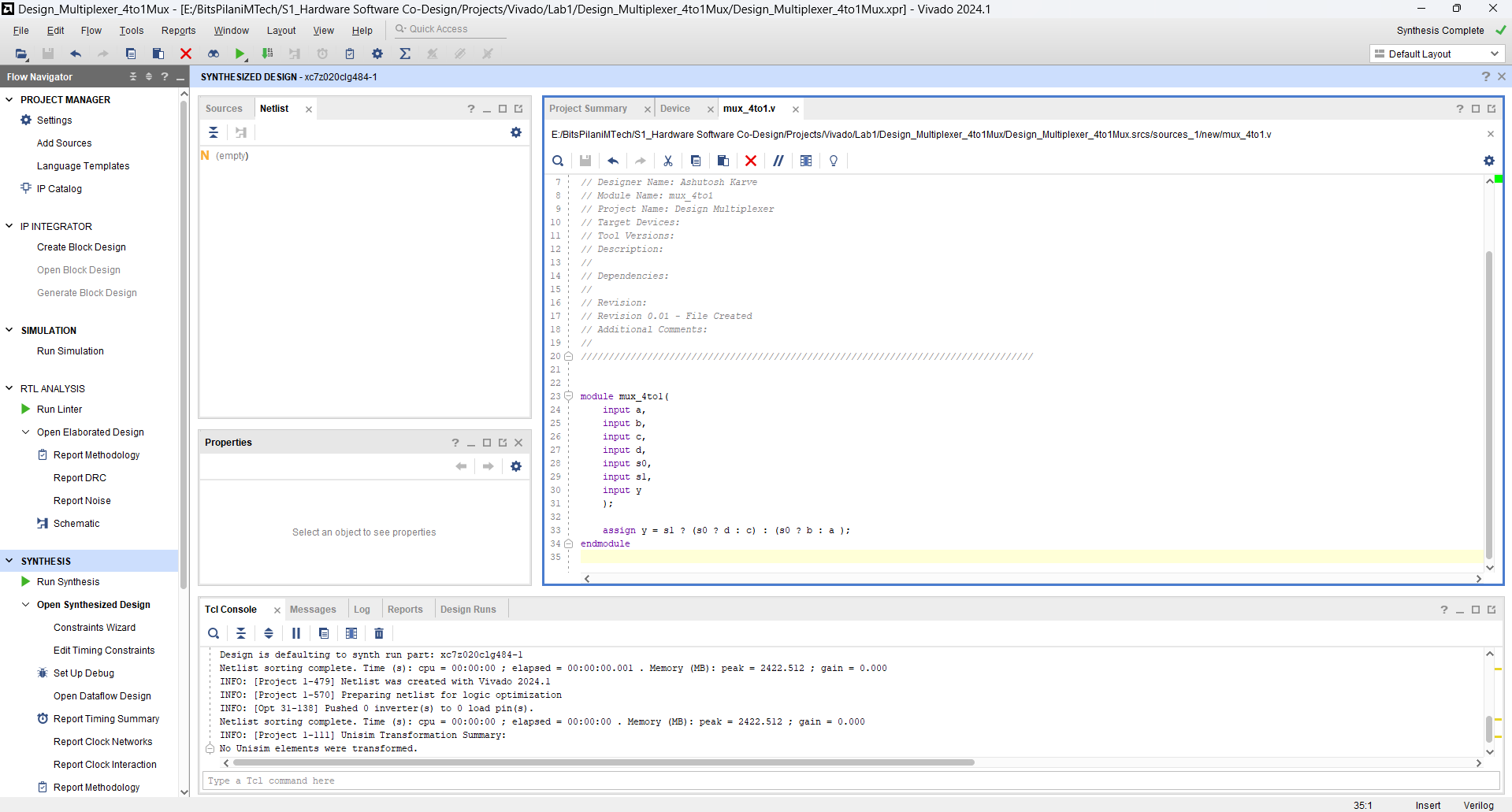
b y

c

d

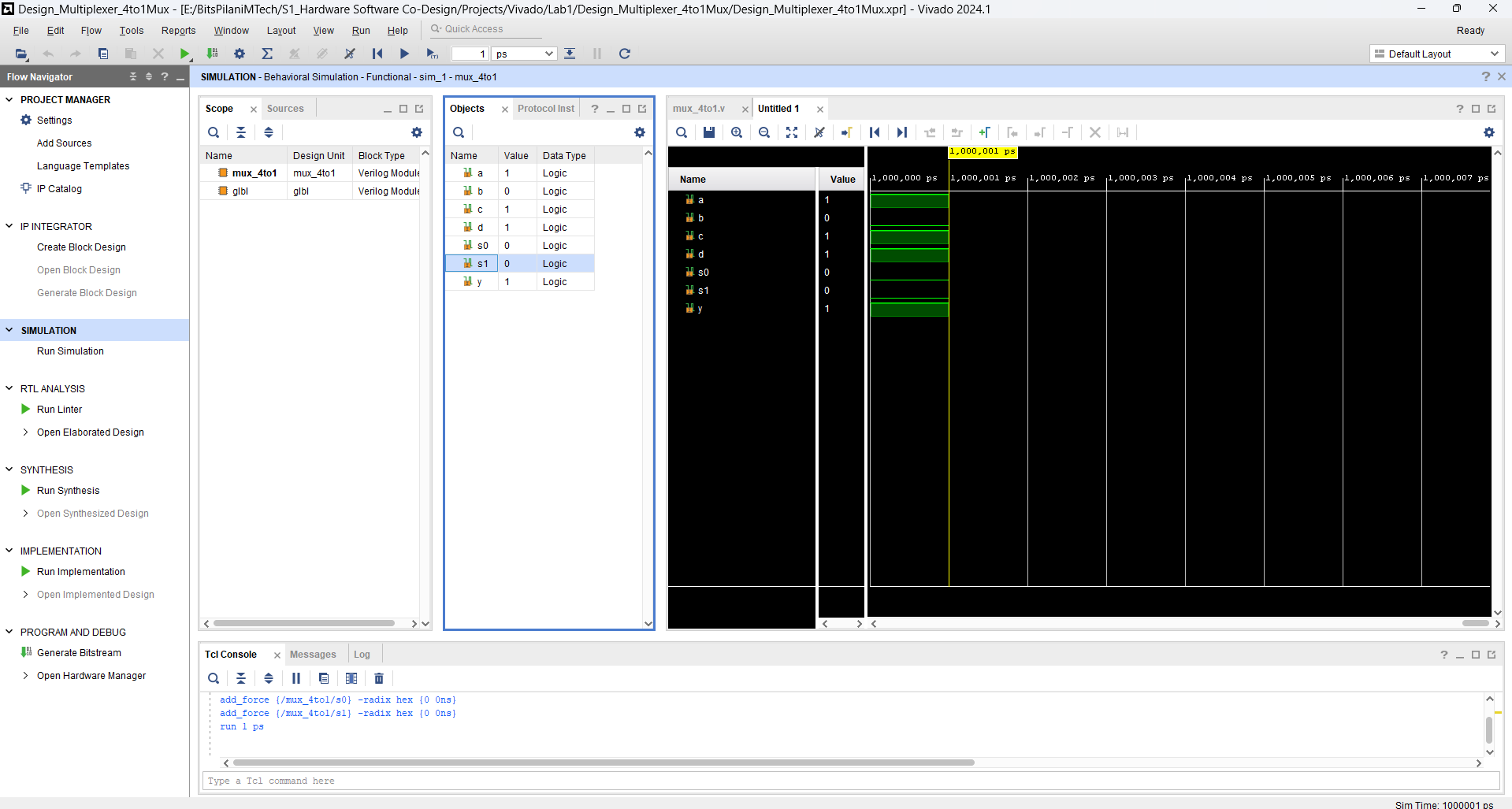
s0 s1

DESIGN SOURCE CODE >>



SIMULATION RESULTS 1 >>

|  |  |  |
| --- | --- | --- |
| s1 | s0 | y |
| 0 | 0 | a |



SIMULATION RESULTS 2 >>

|  |  |  |
| --- | --- | --- |
| s1 | s0 | y |
| 0 | 1 | b |

A screenshot of a computer

Description automatically generated

SIMULATION RESULTS 3 >>

|  |  |  |
| --- | --- | --- |
| s1 | s0 | y |
| 1 | 0 | c |

A screenshot of a computer

Description automatically generated

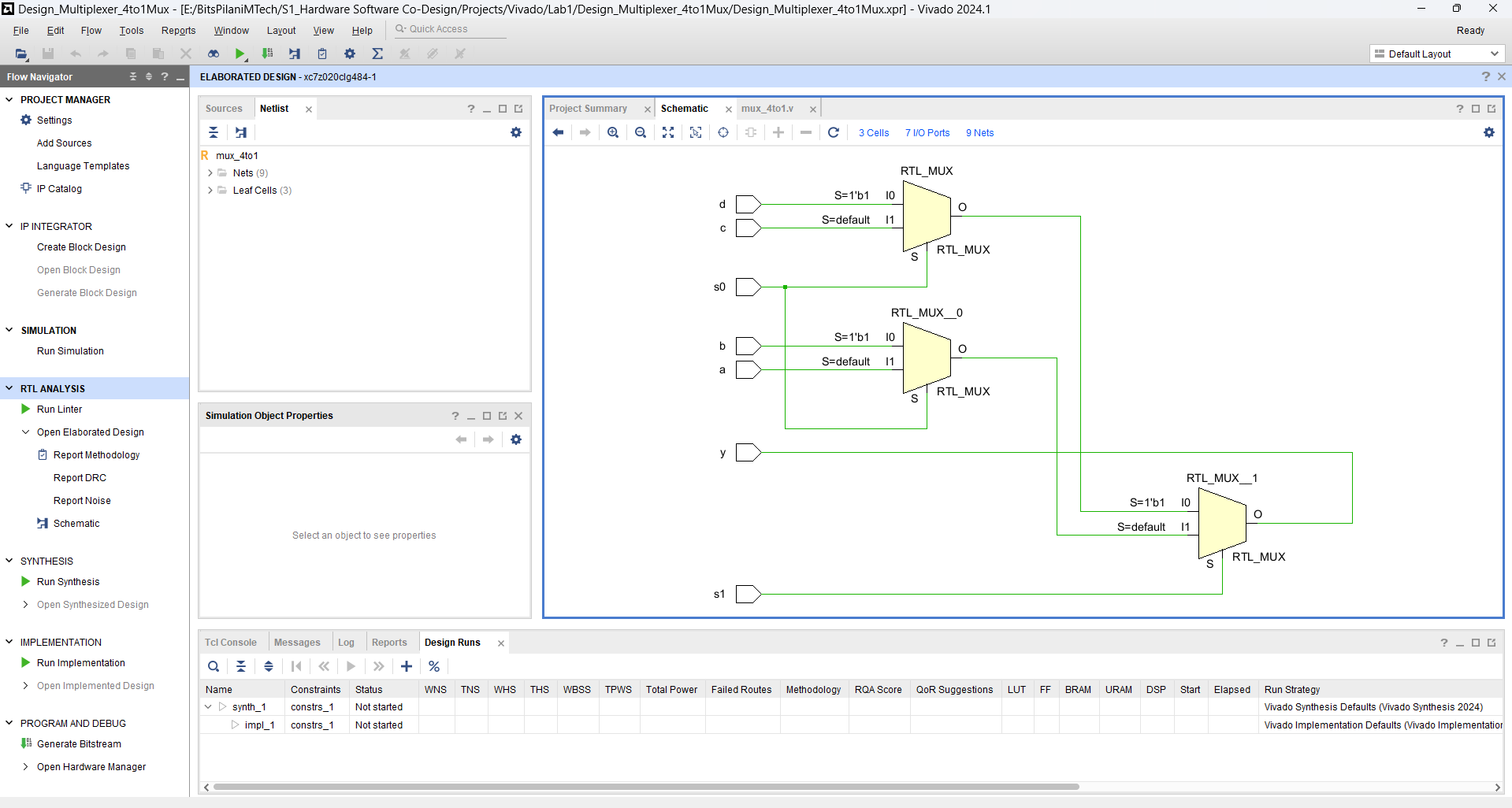
SIMULATION RESULTS 4 >>

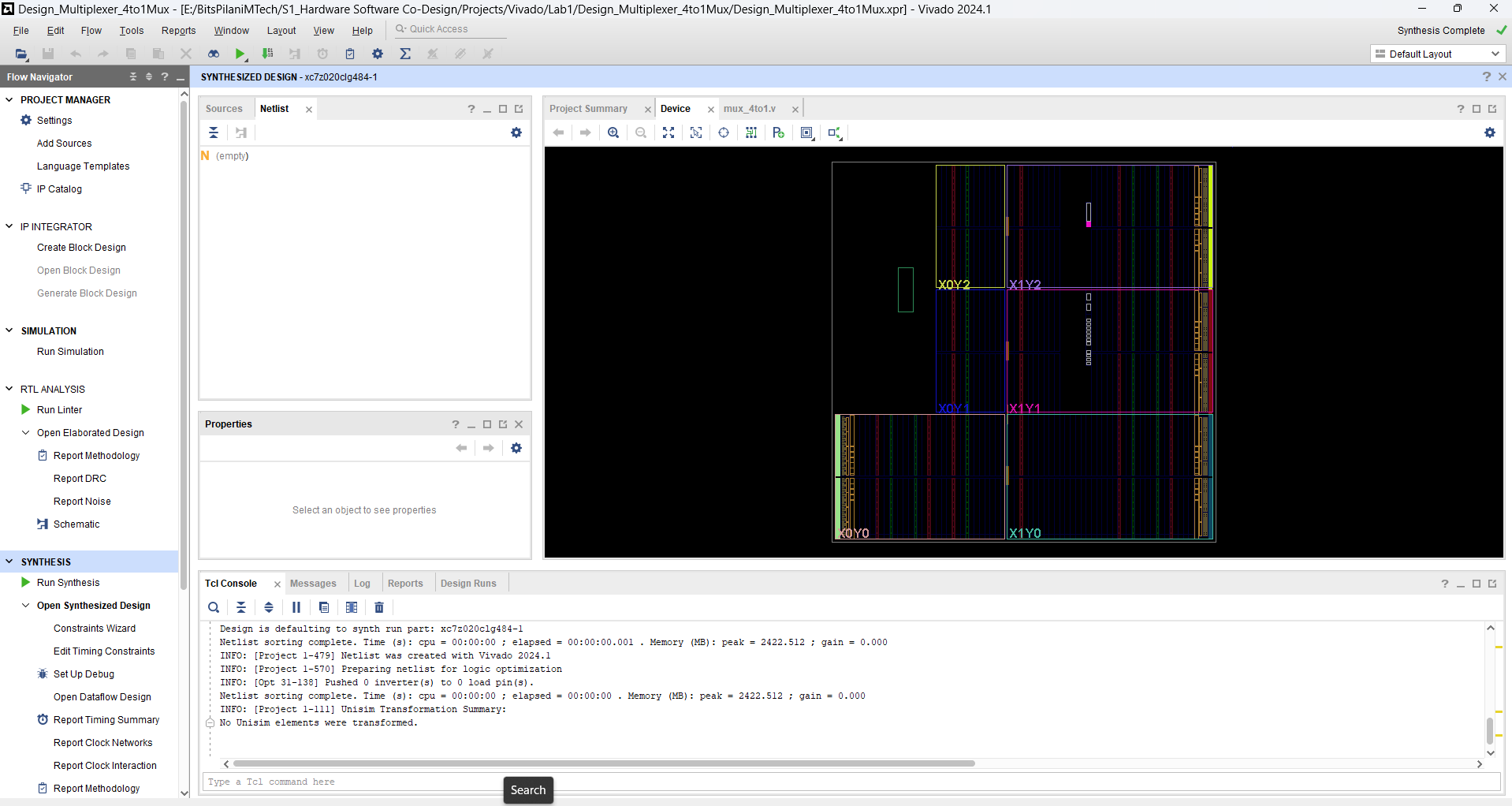
|  |  |  |
| --- | --- | --- |
| s1 | s0 | y |
| 1 | 1 | d |

A screenshot of a computer

Description automatically generated

ELABORATION DESIGN >>

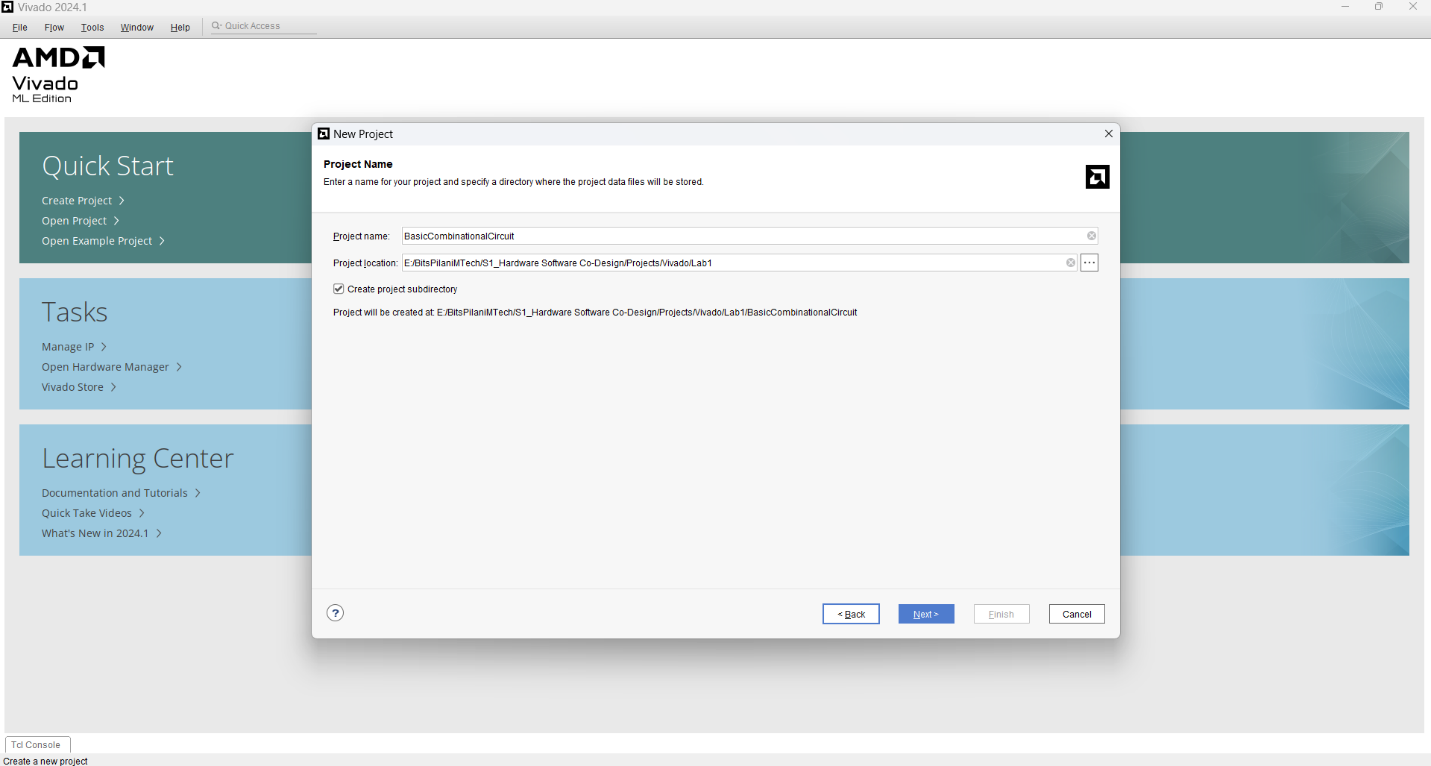


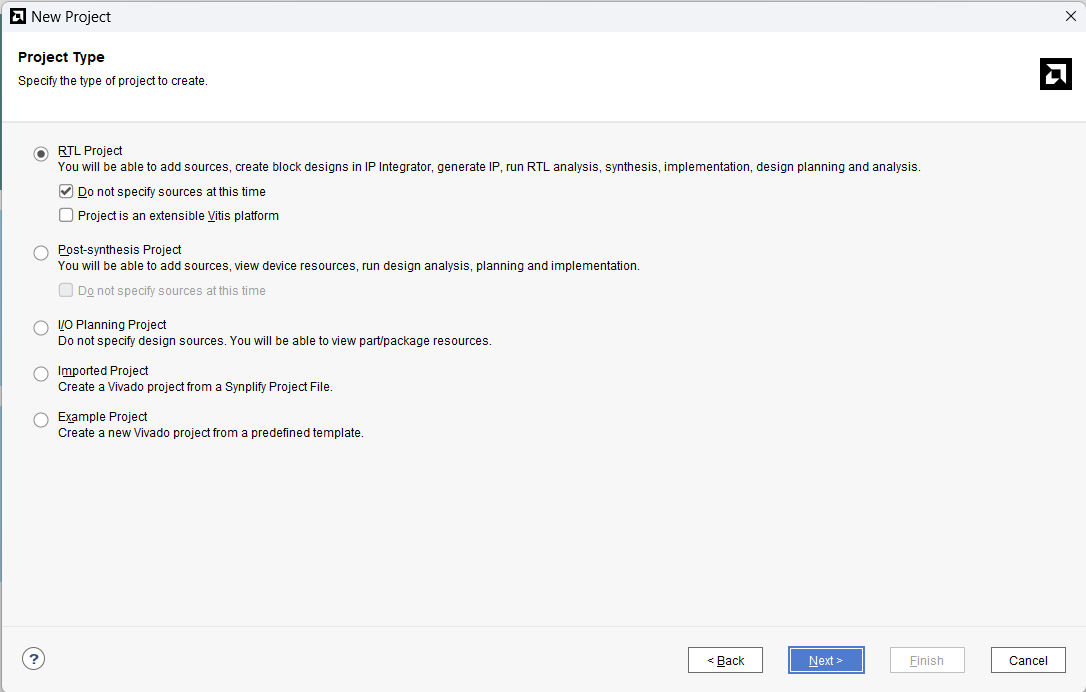
SYNTHESIZED DESIGN >>

++++++++++++++++++++++++++++ASSIGNMENT END++++++++++++++++++++++++++++++++++++

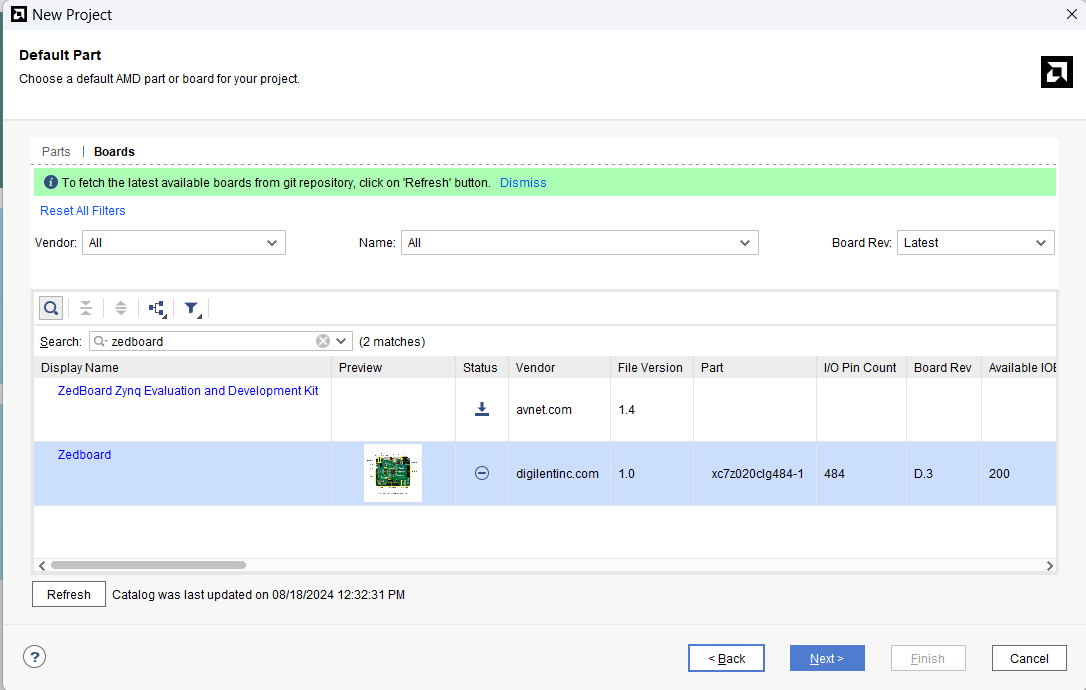
**<< BASIC HOW TO CREATE PROJECT IN VIVADO >>**

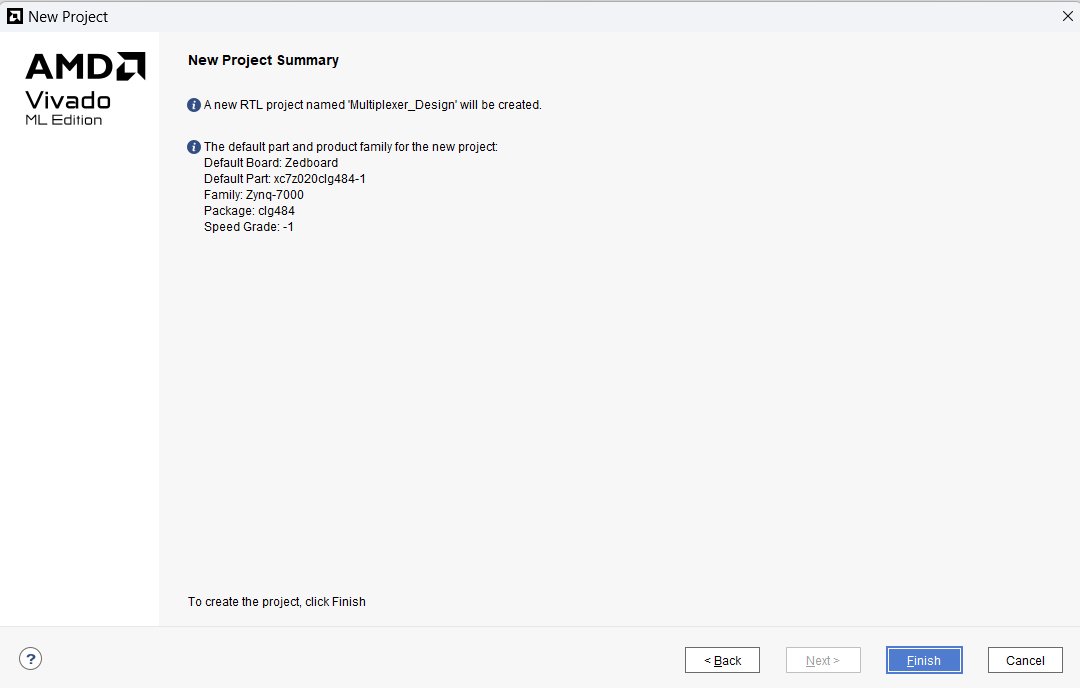
**Creating New Project on vivado FPGA >>**  
Files >> New Proejct



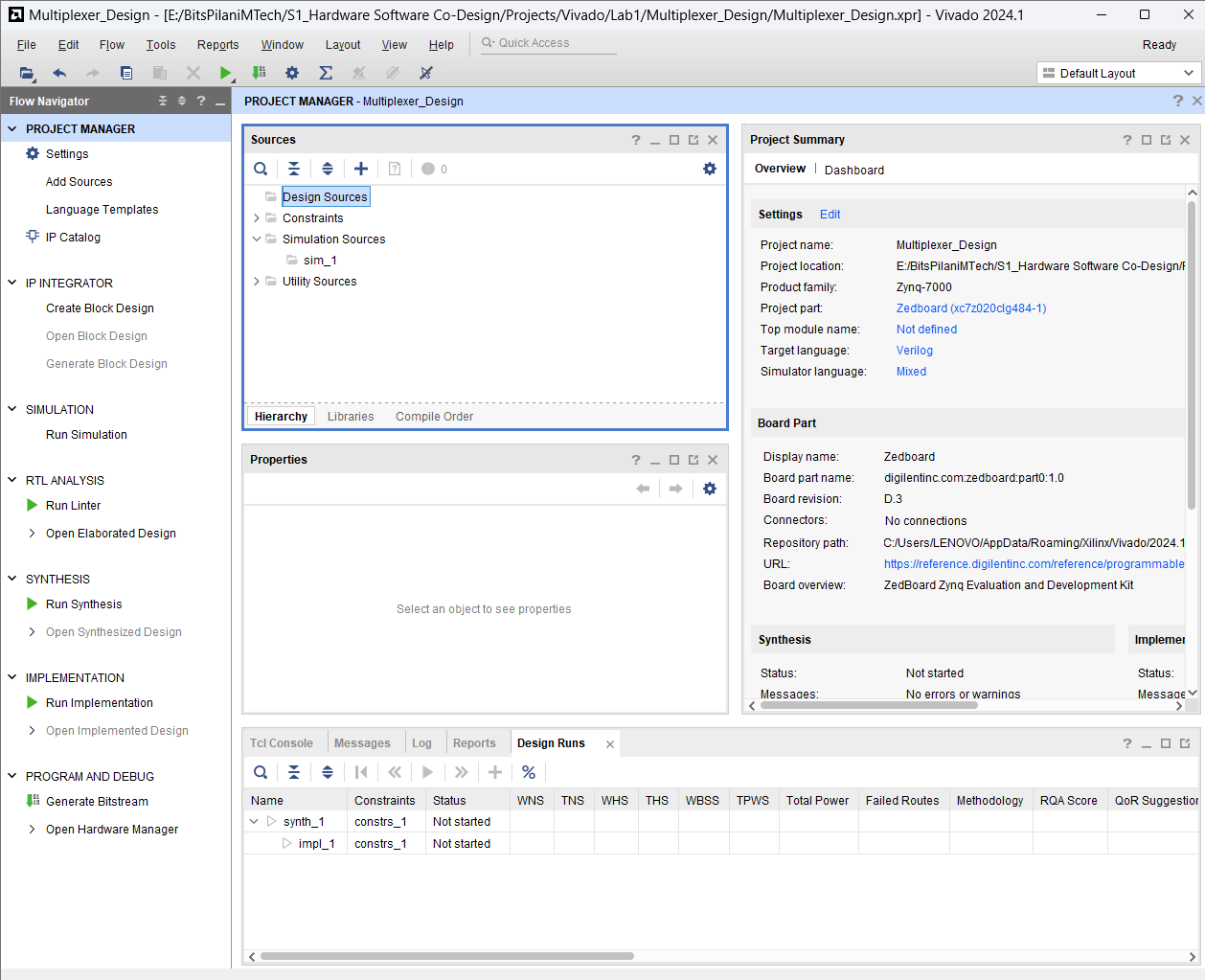


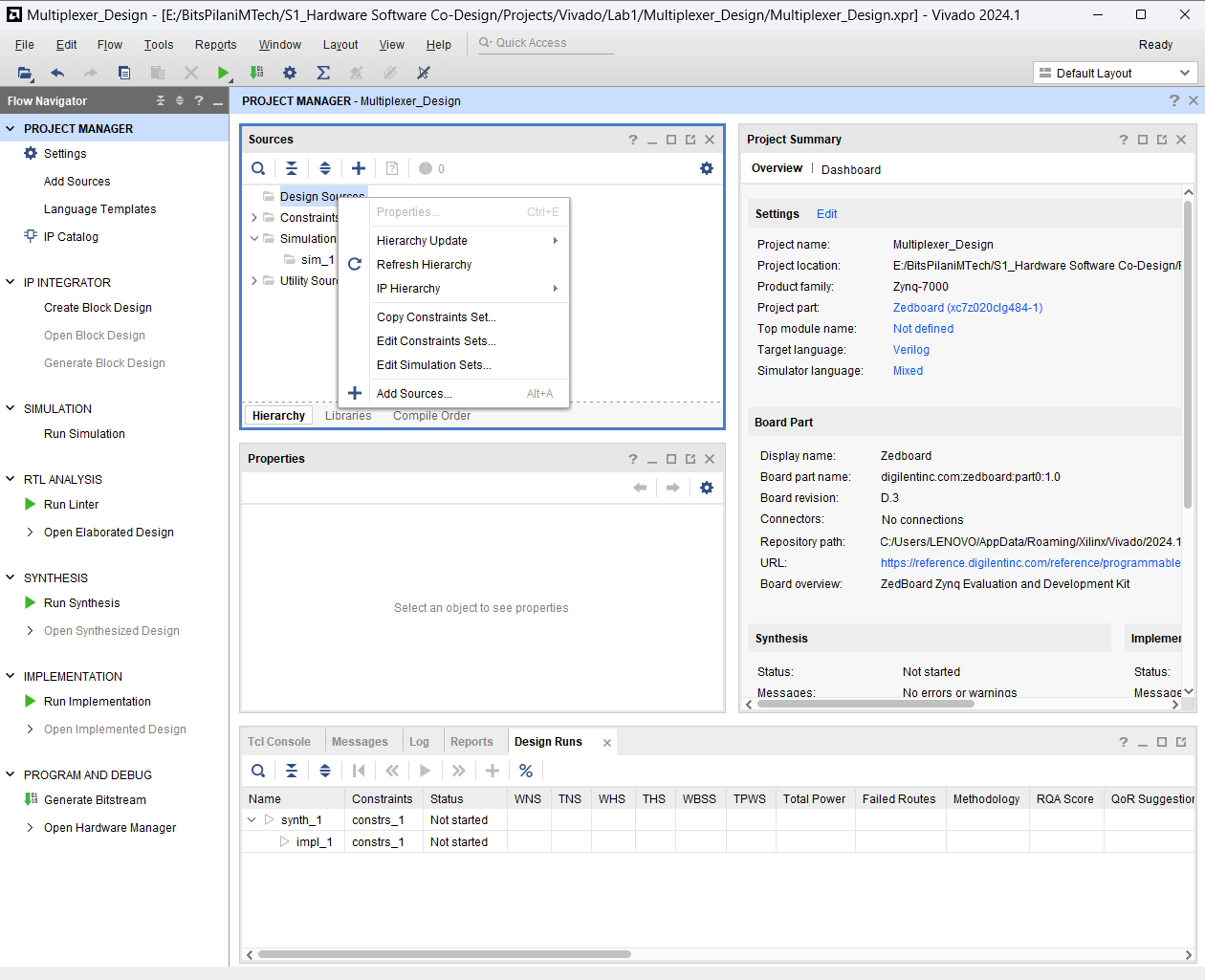
Search for ZedBoard >>



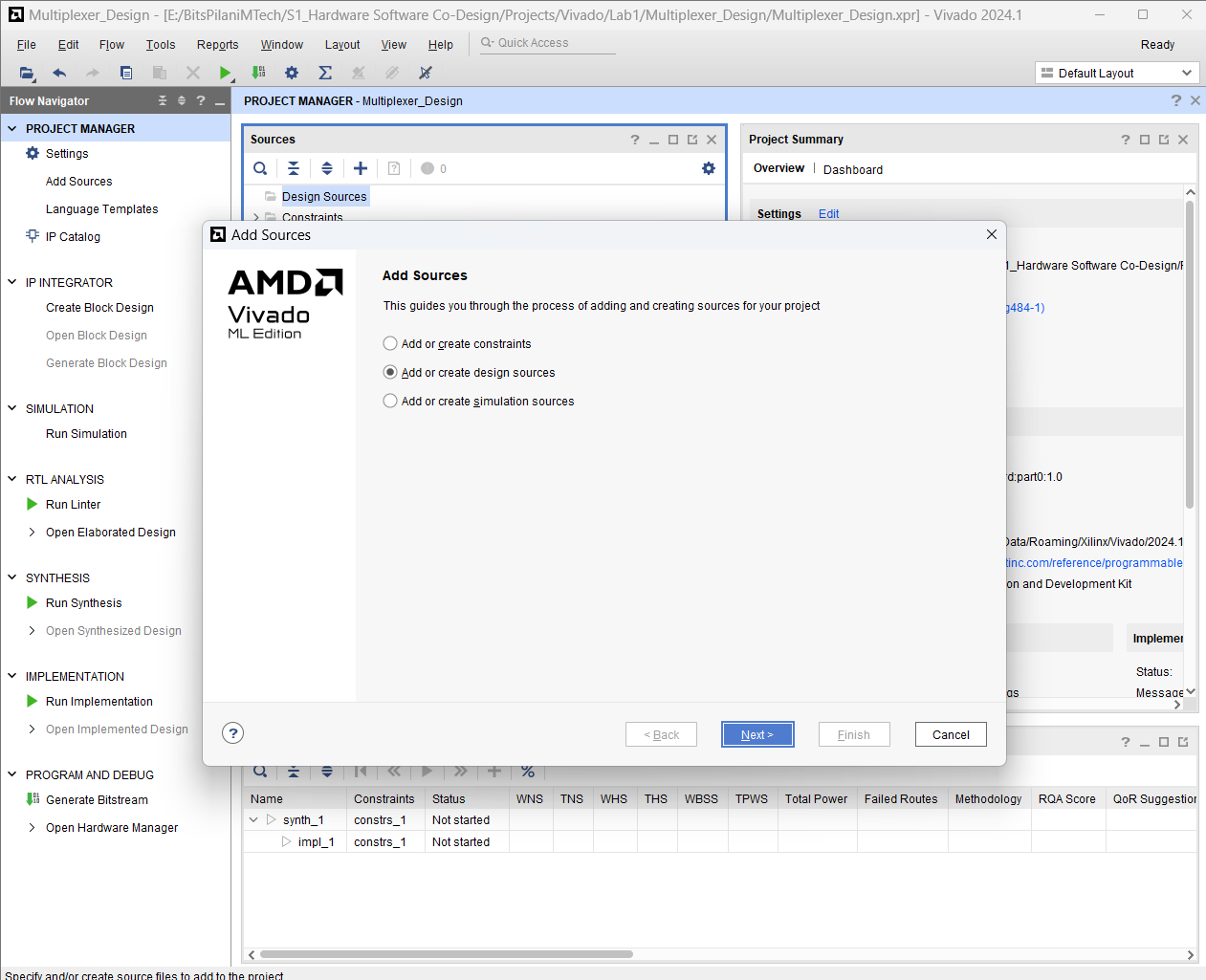


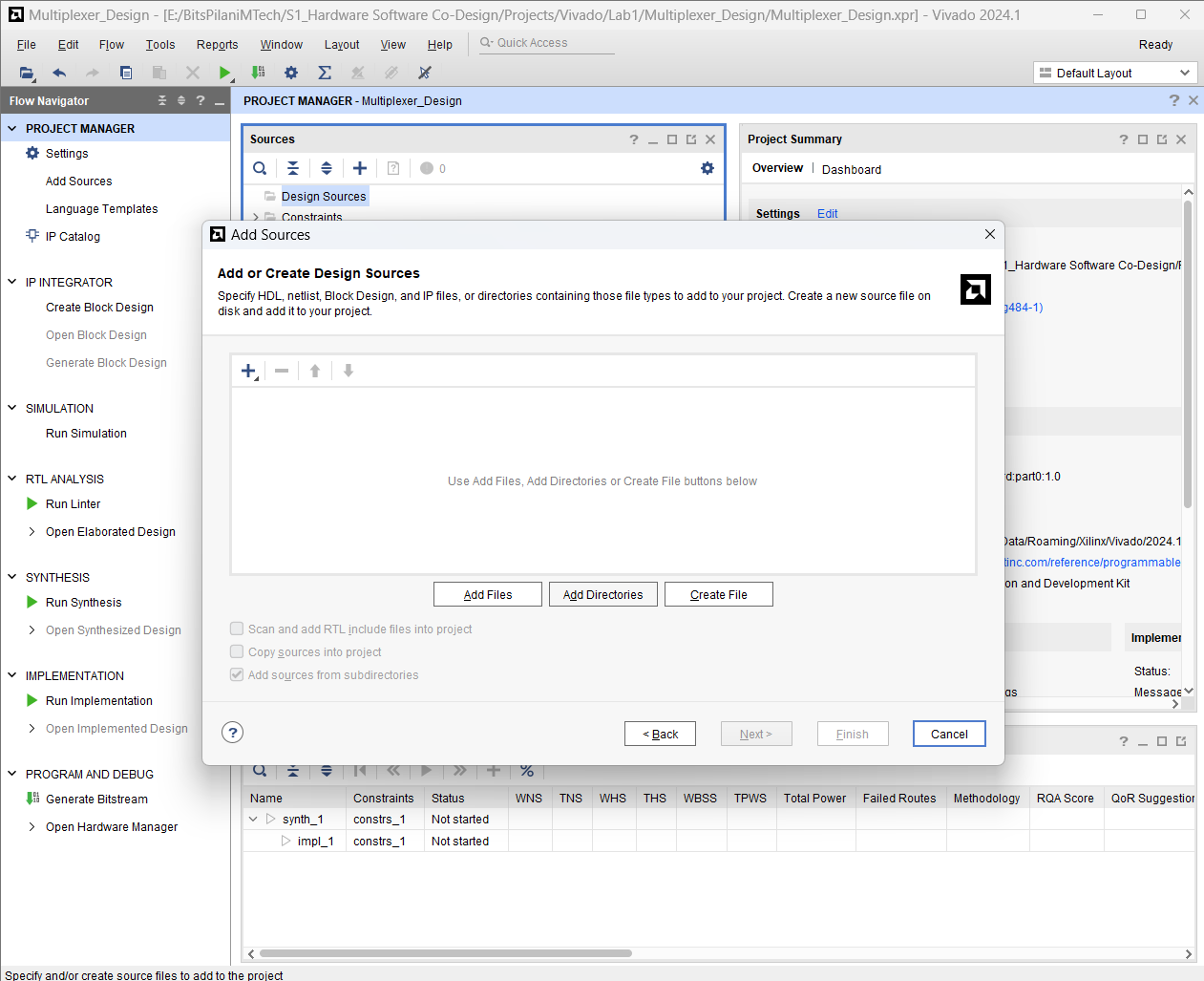
Right Click on >> Design Sources



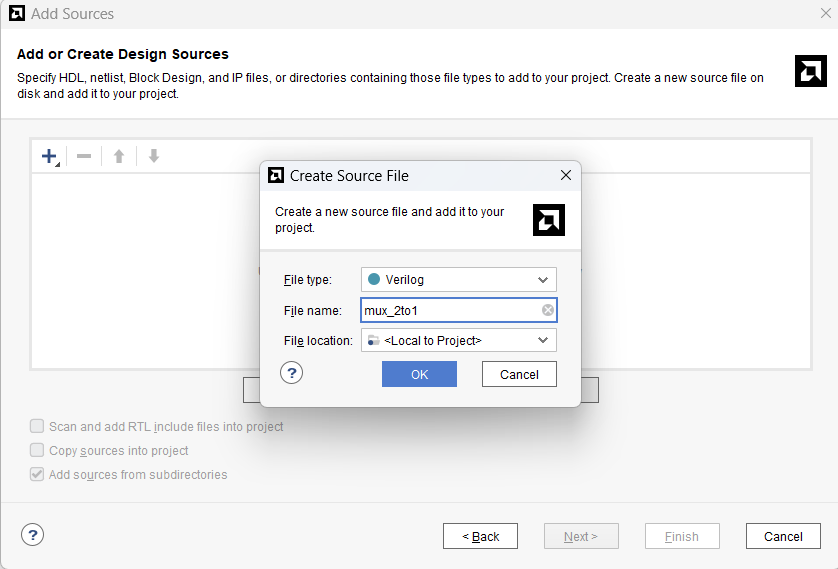


Select + Add Sources >> Add or create design sources >> Next





Click >> create File >> File name >> OK



Click >> Finish

