Electronic Devices & Circuits I 2EI4
Project 4

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1. Circuit Design

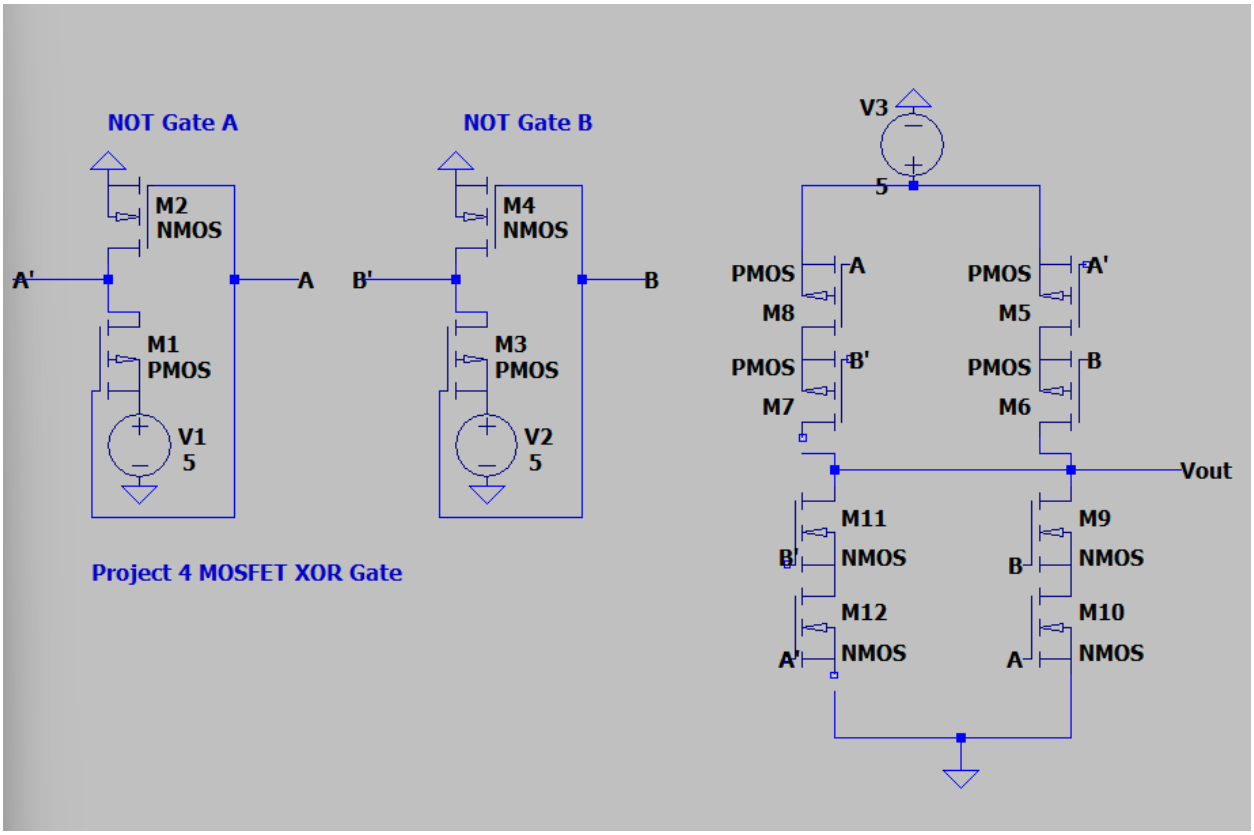
i. XOR Truth Table

A	B	F = A⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

ii. XOR Function

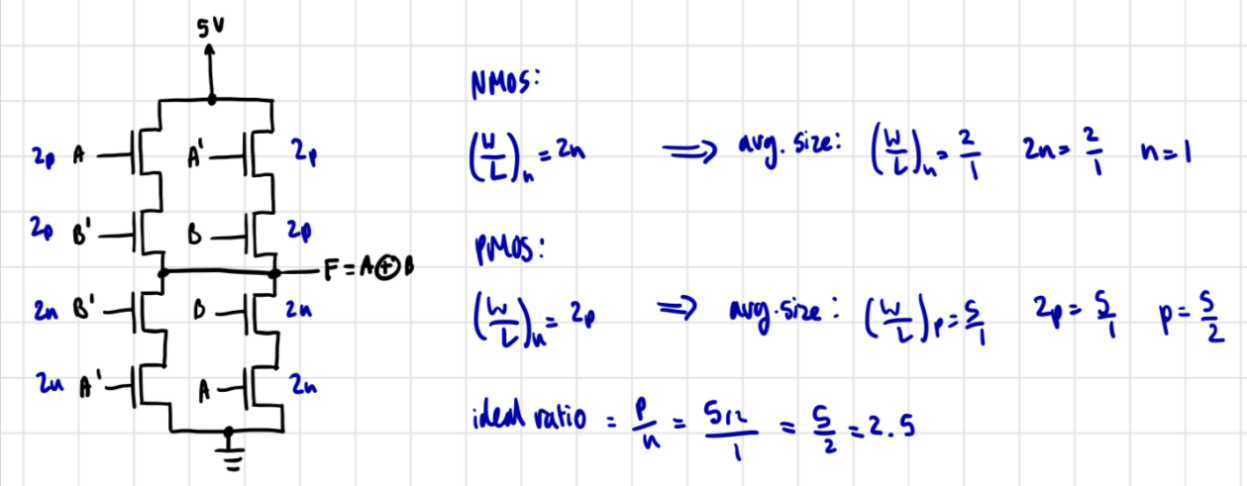
Using DeMorgan's theorem, the function can be determined where: F = A ⊕ B = AB' + A'B = ((AB')' + (A'B)')' = ((A' + B) (A + B'))' = (A'B' + AB)'

iii. Circuit Schematic



2. Idea Sizing

i. Ideal Ratio

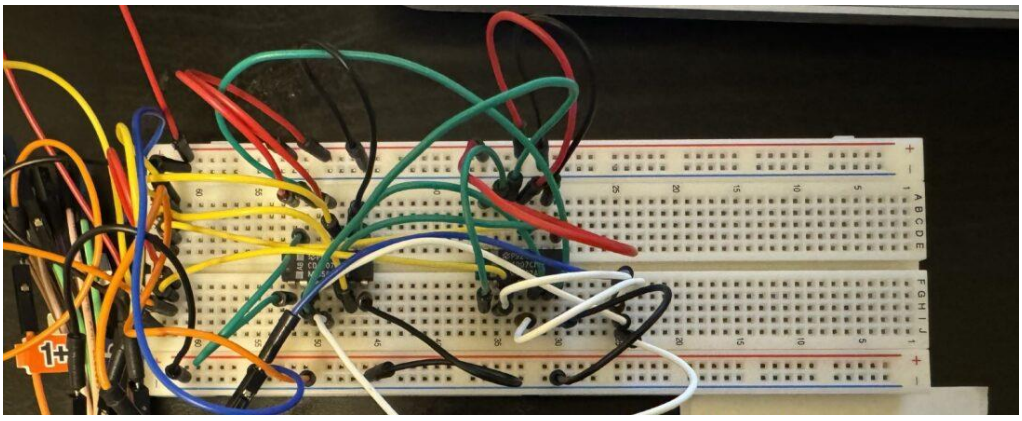


ii. Real Sizing

The ideal sizing can be implemented in the hardware design given the assumption that the n-type MOSFETs have $\left(\frac{W}{L}\right) = \frac{2}{1}$ and the p-type MOSFETs have $\left(\frac{W}{L}\right) = \frac{5}{1}$ where the longest path is from VDD to GND, resulting in the sizing ratio of 2.5 equal to that of the ideal scenario. This qualitatively has no impact on the performance, especially since symmetrical inverters are used in the circuit.

3. Testing

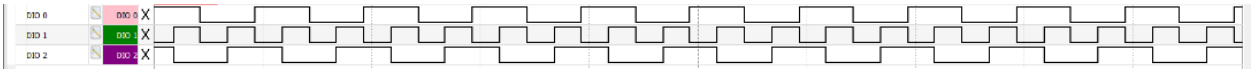
i. Circuit Implementation



ii. Functional Testing

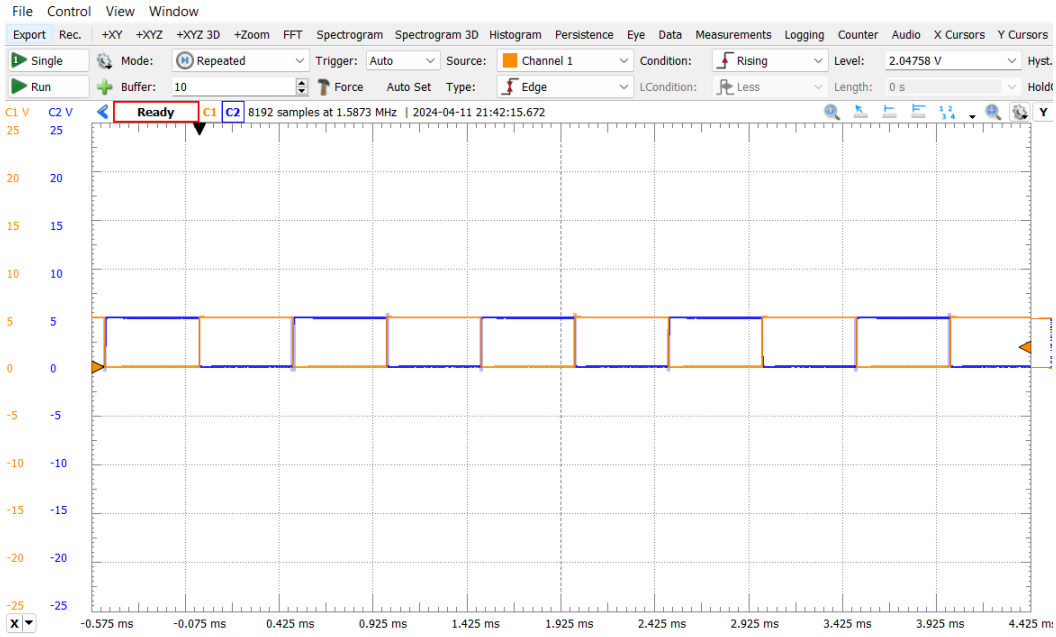
The result of the functional testing corresponds to the truth table for a XOR, as shown in the table below:

DIO0	DIO1	DIO2
0	0	0
0	1	1
1	0	1
1	1	0

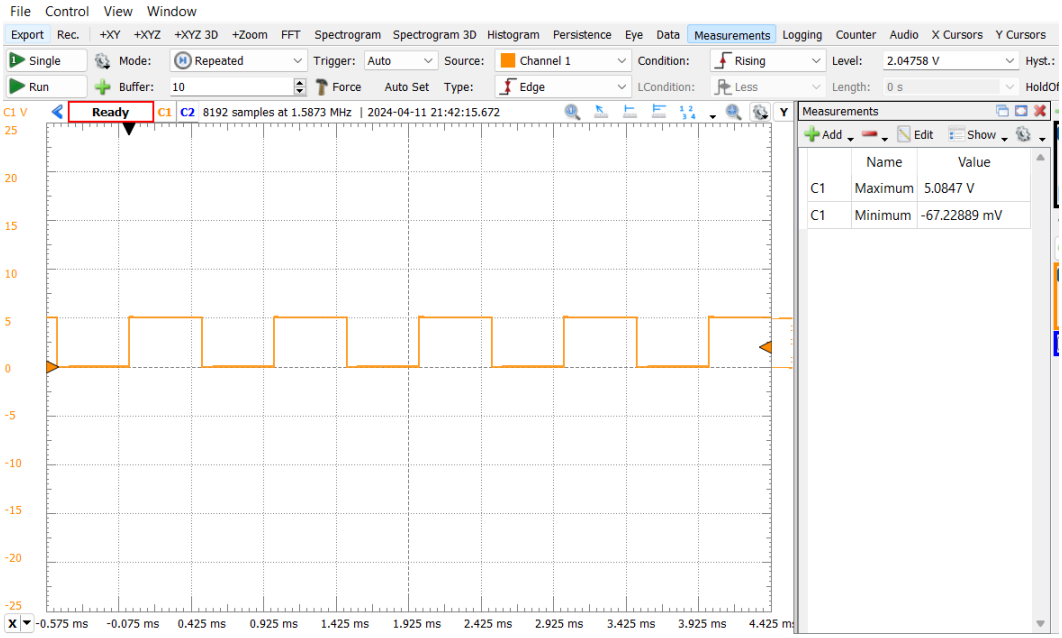


iii. Static Level Testing

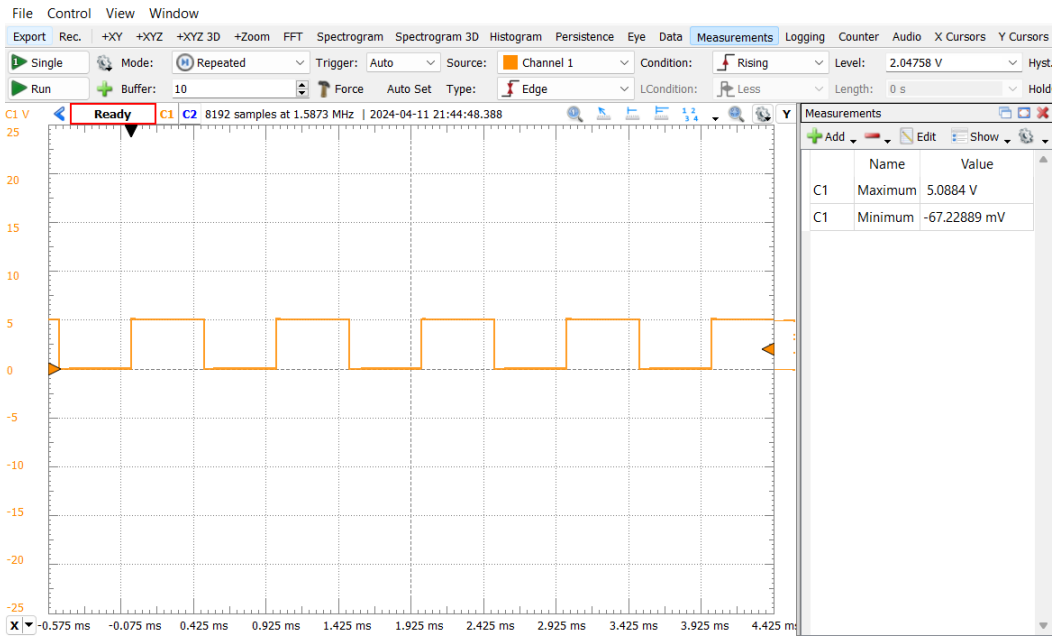
The static level testing demonstrates that the MOSFET XOR gate takes the input (C1) and inverses the output (C2), as shown in the AD2 measurements below.



The first waveform was generated with input A as a square wave between 0V and 5V and input B as 5V, where V_H = 5.0847 V and V_L = -67.22889 mV.



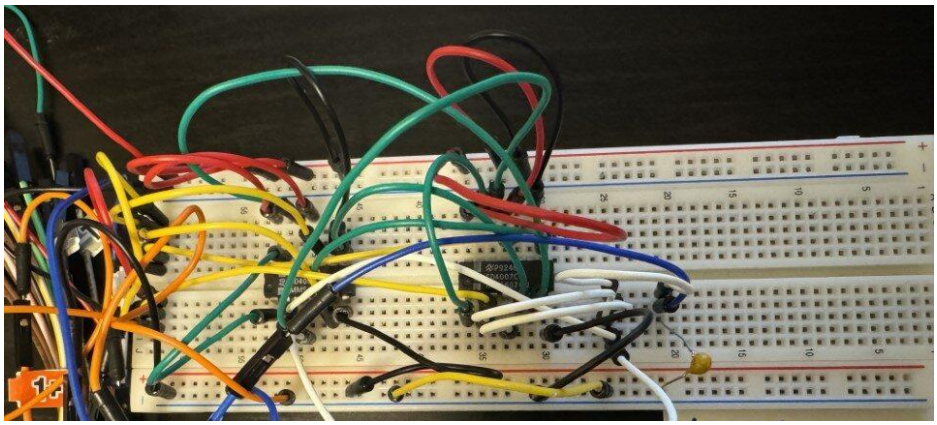
The second waveform was generated with input A as 5V and input B as a square wave between 0V and 5V , where V_H = 5.0884 V and V_L = -67.22889 mV.



Based on these results, it is evident that the values remain the same with minor variation.

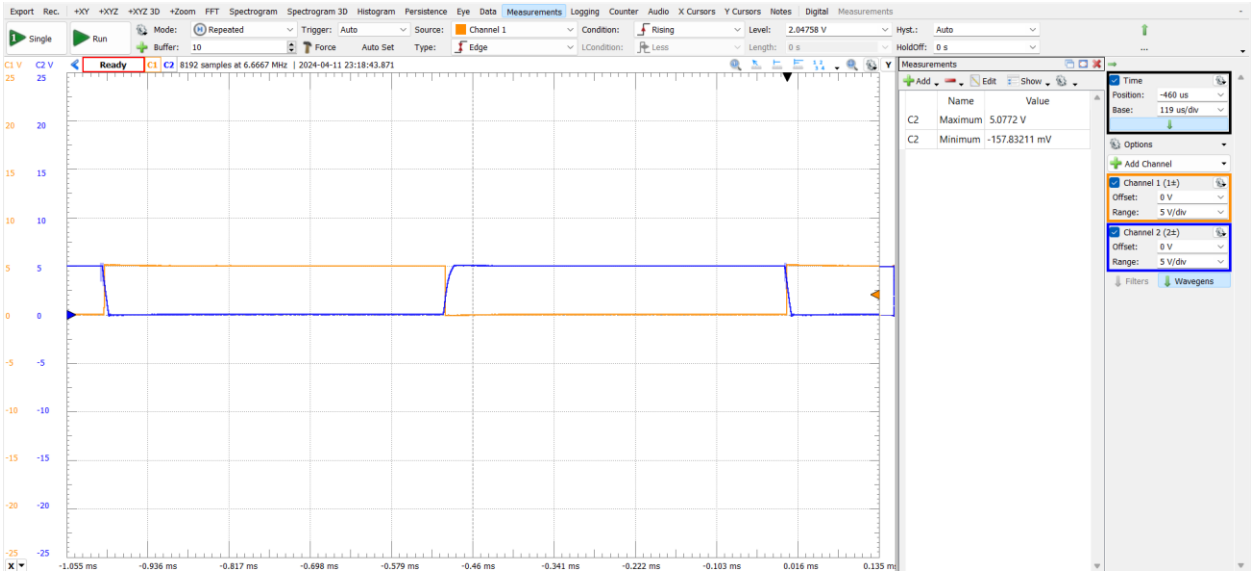
4. Testing

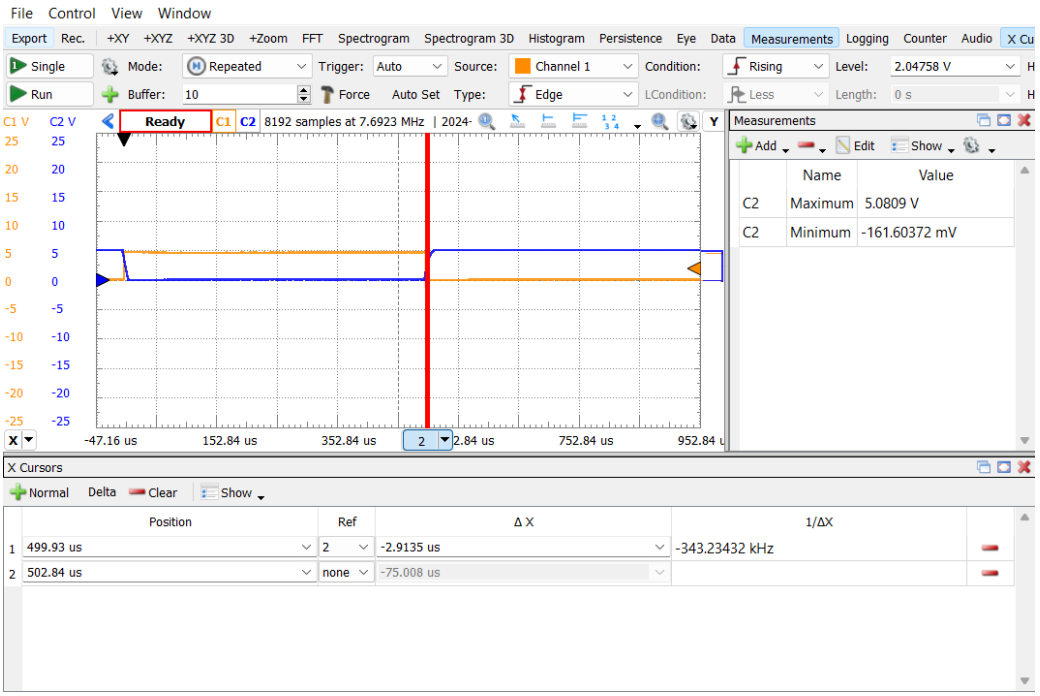
i. Circuit Implementation

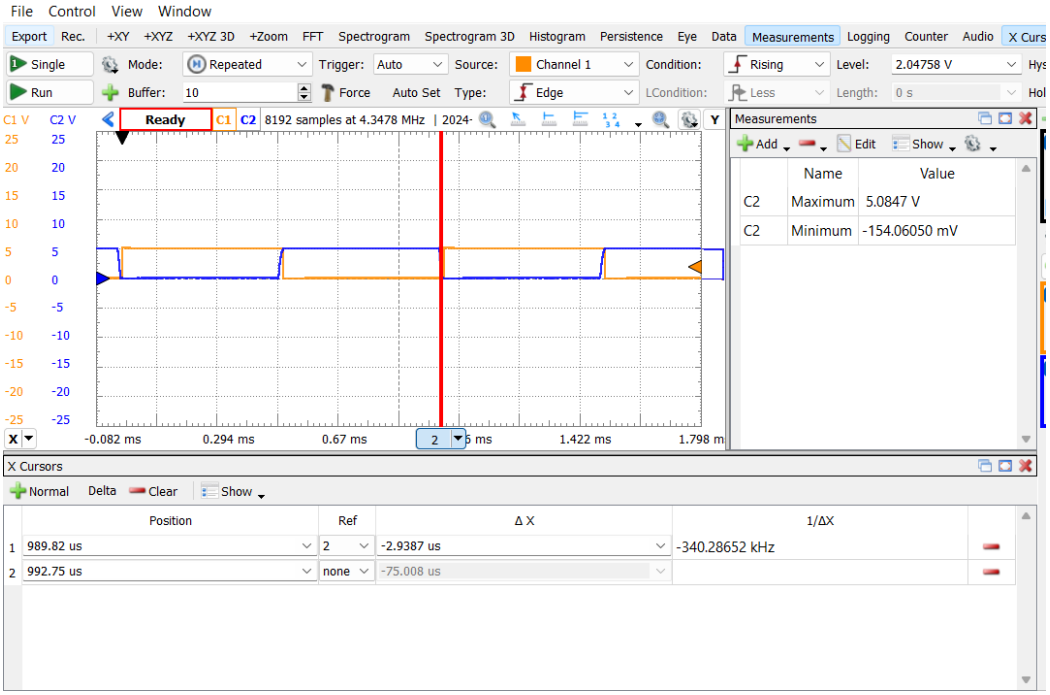


ii. Rise and Fall Times

A capacitance load of 100nF was used to produce the waveform, as shown below.







Based on the AD2 measurements, the rising and falling times were determined by taking the difference between the maximum and minimum values of the waveforms. The rising time was 2.9135 us and the falling time was 2.9387 us.

iii. $\tau_{PLH}, \tau_{PHL}, \tau_P$

According to the AD2 waveforms, the t_{PHL} can be determined by finding the time where the input reaches it maximum and XOR gate reaches 50% of its range, which was 183.87 us. The t_{PLH} can be determine by finding the where the input reaches it minimum and XOR gate reaches 50% of its range, which was 153.48 us. t_P can then be calculated by taking the average where $t_P = (t_{PHL} + t_{PLH}) / 2 = 168.66$ us.

References

[1] “CD4007CN Datasheet (PDF) – Fairchild Semiconductor,” *AllDatasheet*. Available: https://pdf1.alldatasheet.com/datasheet-pdf/view/50834/FAIRCHILD/CD4007CN.html. [Accessed April 10, 2024].