Mid-circuit Measurement/Reset

Quantum Computing ECE-592

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1. Problem Statement:

Typically, measurements in Quantum Circuits are performed at the end of the simulation to gather final information about the state of qubits(result in Classical terminology). The circuit is simulated multiple times(shots) and the measurement records the states of qubits. The states with the highest shots give the possible solutions.

Mid-circuit measurement along with reset enables the programmer to reuse the same qubits or ancilla qubits for the next connected circuit or in the same circuit itself. In this way, we can save the number of qubits we reserve for executing the job.

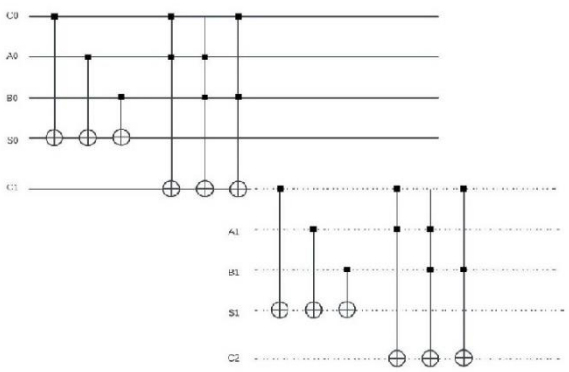
In general, the Quantum circuits get affected by various noise factors coming from idleness and quantum gates themselves. So, a stabilizer-based mid-circuit measurement and reset/set of the qubit corrects the deviation maintaining fidelity.

1.1 QC optimization using Mid measurement/reset:

We are planning to implement an n-bit Full adder circuit to show how mid-measurement and reset help to optimize the qubits usage. The textbook implementation of the n-bit full adder asigns each qubit to each bit of the inputs. Our approach induces a mid-circuit measurement and reset. Once the full addition operation is finished, the qubits are measured and reused for the next bit fulladder.

Mid-circuit measurement and reset can be significant in reducing the total number of qubits used in a quantum circuit. Implementing a n-bit Full-adder circuit can be a plausible way to demonstrate the decrease in the need of additional qubits. Typically, for Implementing a 1-bit full-adder, 5 qubits are needed. With increase in the width of the input, the number of qubits required increases at the rate of ‘4’ qubits where ’n’ is the width of the input bits.

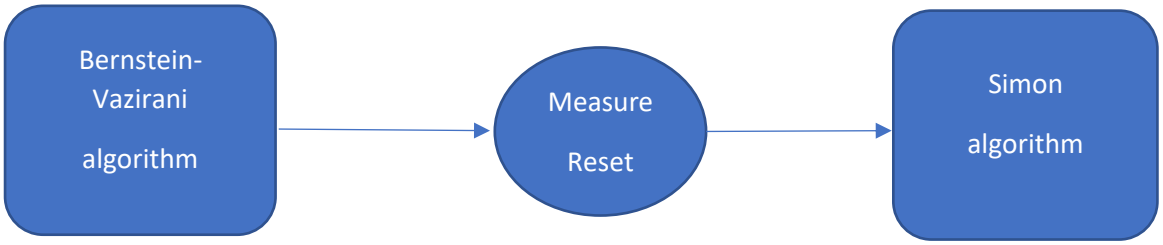
With the use of Mid-circuit measurement and reset, the sum bit can be measured and reset for storing consequent values of sum. The carry bit and input bits can also be reset and reused with the consequent carry and the input bits. Single resetting of the qubits can affect the fidelity. In order to prevent errors in the circuit, the reset is usually performed multiple times. But this significantly increases the depth of the circuit and hence the execution time. Below is description of typical n-bit full adder circuit. With the new approach, we reset the input A0,B0 and carry C0 and reuse them for all An, Bn and Cn.



1.2 Circuits fusing using Mid measurement/reset:

In this we are planning to fuse two Quantum circuits into a single module and analyse whether this gives any improvement on wait-times on actual hardware job queues. We plan to implement Bernstein-Vazirani and Simon's algorithms as the circuits. After first circuit completes its execution, we do a measure and reset the qubits for the next circuit implementation. Firstly, we want to run the circuits individually and note the results. Later, we want to merge the operations and run as a single job to monitor the improvements in the wait time. We are assuming monitoring the wait times on a set of IBMQ-s give more generalized and sophisticated results.

Also, we need to monitor if there is any fidelity issues caused by doing a mid-measurement and reset operation in between the circuits.

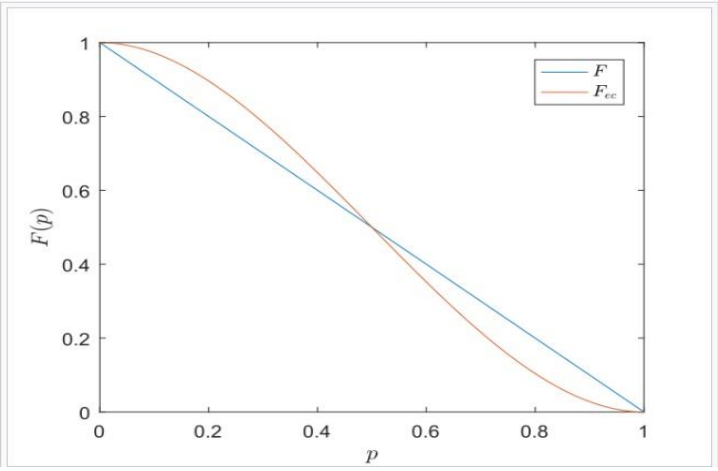


1.3 QEC for Mid measurement/reset noise:

As explained in the problem statement, Quantum circuits are susceptible to qubit and gate noise. We are planning to implement a repetition code based error correction technique. And after doing a mid circuit measurement on a noisy circuit, if we detect any error, we fix it by doing a conditional reset. This mid circuit measurement and reset might effect the fidelity of circuit and lead to errors which needs to be analysed. Effects of fidelity on QEC is as below:

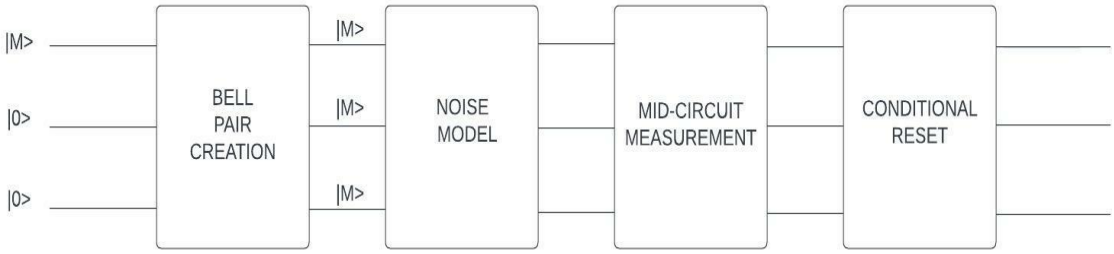
F : Fidelity without QEC F_ec: Fidelity with QEC.

P : Probability of error in qubit.



Note: Taken from Wikipedia: https://en.wikipedia.org/wiki/Quantum_error_correction

Block diagram of QEC using a mid-circuit measurement and reset:



2 Approach timeline:

S.NO	Milestones	Date
1	Using Measurement and reset to reduce the number of qubits used in a circuit	30th Oct 2022
2	Combining multiple circuits, performing measurements after each circuit and combining the circuit by reusing the qubits	30th Oct 2022
3	Implementing Quantum Error Correction.	12th Nov 2022
4	Implementing a channel that randomly injects errors into the circuit and implementing a QEC algorithm to correct the errors.	17th Nov 2022
5	The QEC algorithm will be optimized using mid-circuit measurement and reset.	23rd Nov 2022

3 Bibliography:

1. https://www.ibm.com/blogs/research/2021/02/quantum-mid-circuit-measurement/
2. https://qiskit.org/textbook/ch-quantum-hardware/error-correction-repetition-code.html
3. https://nonhermitian.org/posts/2021/2021-10-27-dynamic_BV.html
4. https://qiskit.org/textbook/ch-algorithms/bernstein-vazirani.html
5. https://qiskit.org/textbook/ch-algorithms/simon.html.
6. https://quantum-computing.ibm.com/lab/docs/iql/manage/systems/midcircuit-measurement/
7. https://journals.aps.org/pra/pdf/10.1103/PhysRevA.105.022441

4. UPDATES:

Current status & individual contributions:

1. Finished coding the #1 #2 sections of above timeline.
2. We came up with the ideas on how to implement above sections #1 and #2 and decided to implement a n-bit full adder for demonstrating the utilization of mid measure and reset. And implement a BV+Simon fused circuit to demonstrate waiting time improvements on launching multiple circuits as a single job.
3. Pradeep Vetapalem worked on fusing the quantum circuits BV and Simon and trying to run the jobs to check for waiting time improvements.
4. Ashwin Karthik worked coding the n-bit full adder circuit by just reusing 4 qubits for any lengths of input strings.
5. We also added the support of multiple resets in to the design expecting a better fidelity.

Challenges:

1. We are implementing an n-bit full adder by reusing the same qubits with the help of a mid-circuit measure and reset.
   But due to the large depth of circuits, we are seeing wrong answers with high frequencies on the actual hardware. The aer/qasm simulators are giving the correct answers.

2. We tried doing multiple resets expecting better results. But it is actually worsening the results. We read a few articles/publications where multiple resets give a better reset than a single reset. Not sure why it is not happening here.

3. We are seeing long waiting delays after launching the jobs. We tried on multiple imbqs like Toronto/Quito/Cairo/Kolkatta. All these queues are setting the jobs into longer waiting lists.

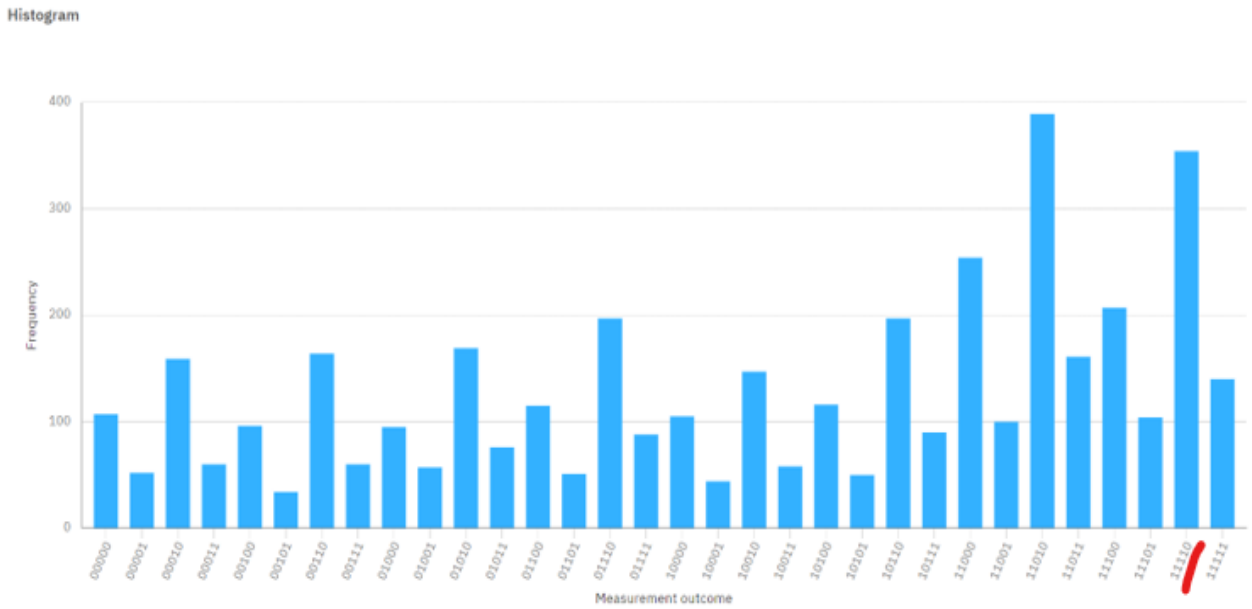
Pending Tasks:

1. Fix the above mentioned challenges by 12/12.
2. Model the error correction using mid circuit measure and reset by 12/12
3. Get the metrics for both #1 and #2 from Milestone sections by 12/19.

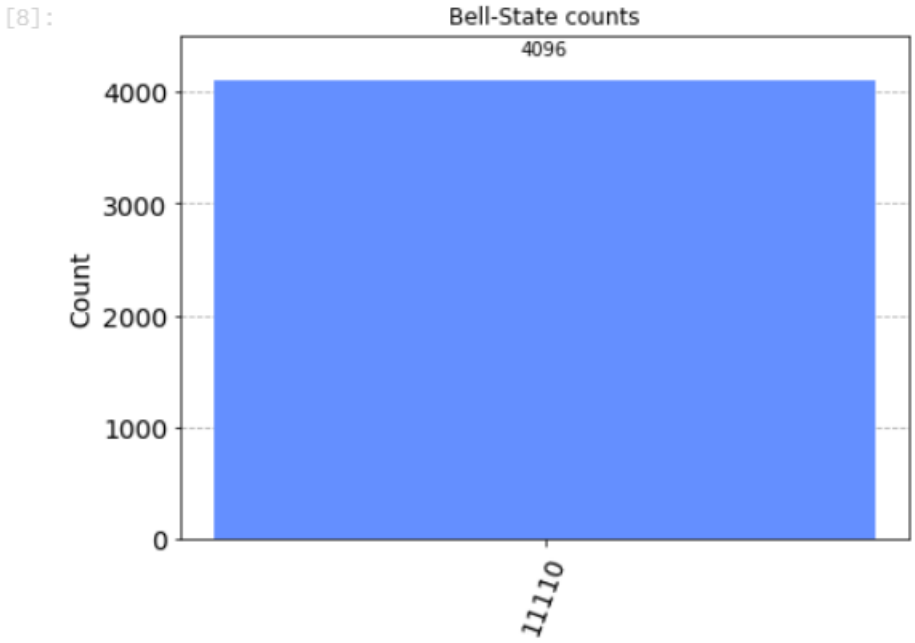
Graphs:

#1. Full adder:

IBMQ Hardware:



AER Simulator:



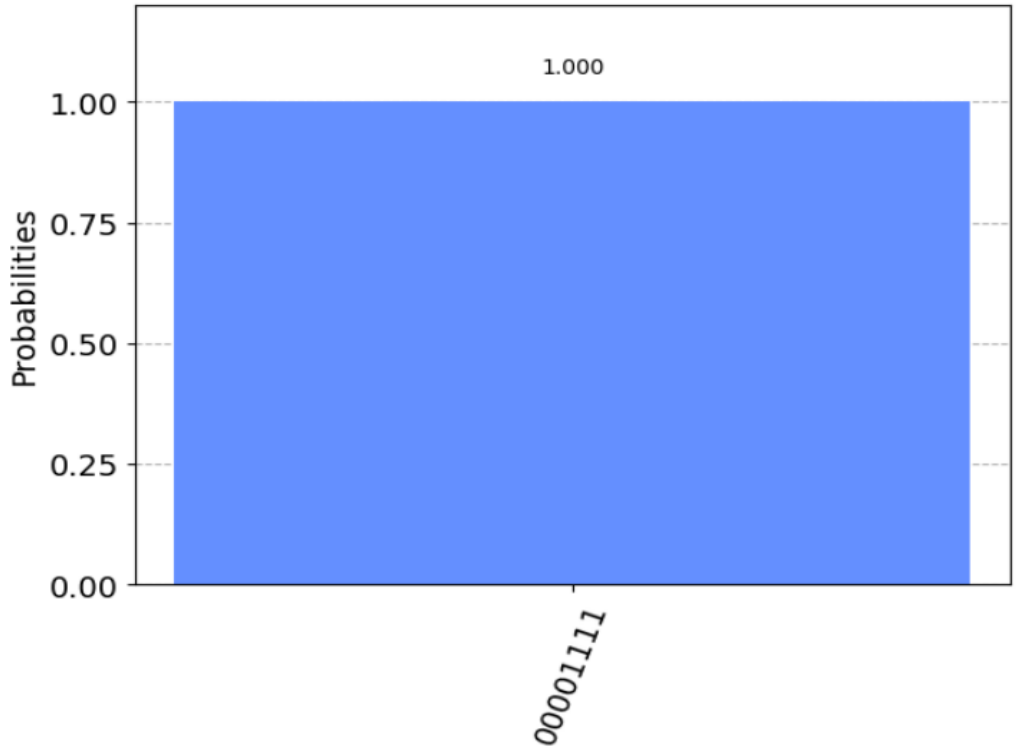
Because of decoherence and high depth of circuit, we observed frequency distribution on the other answers as well. Running with more number of shots might give us better results.

#2. BV/Simon/BV+Simon:

String: '1111'

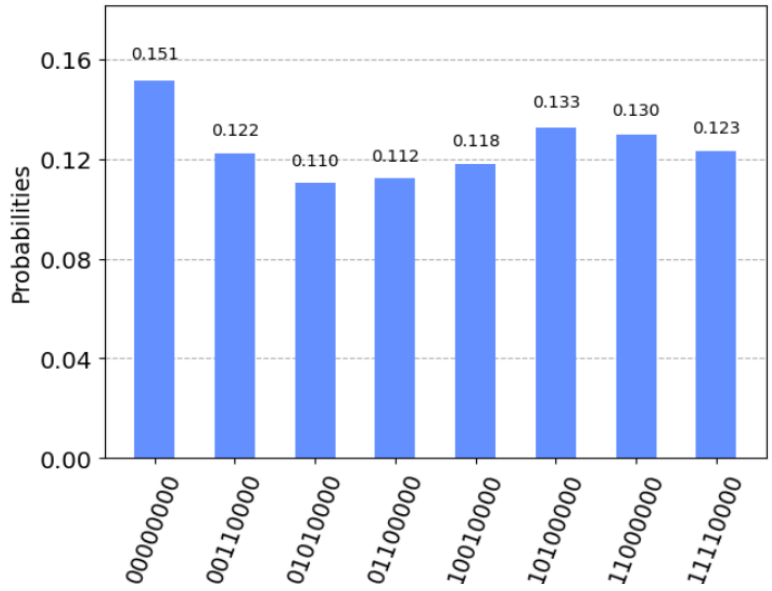
BV plot:

```
{'00001111': 1024}
```



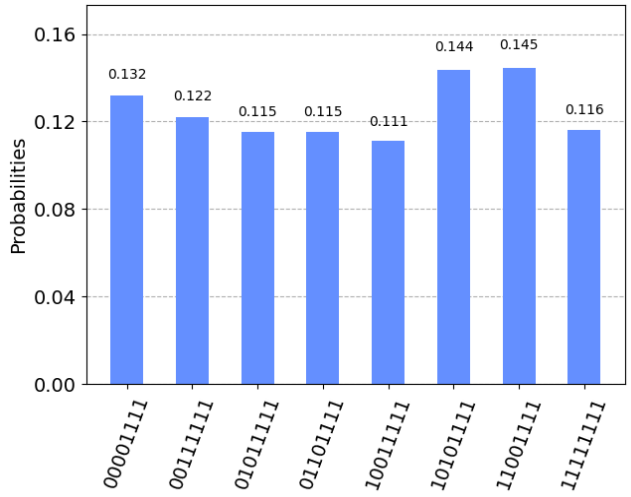
Simon plot:

```
(1111 dot 10010000)%2 = 0
(1111 dot 10100000)%2 = 0
(1111 dot 01100000)%2 = 0
(1111 dot 11110000)%2 = 0
(1111 dot 00110000)%2 = 0
(1111 dot 11000000)%2 = 0
(1111 dot 01010000)%2 = 0
(1111 dot 00000000)%2 = 0
```



BV+Simon plot:

```
{'10011111': 114, '10101111': 147, '11111111': 119, '01101111': 118, '00111111': 125, '11001111': 148, '01011111': 118, '000011
11': 135}
(1111 dot 10011111)%2 = 0
(1111 dot 10101111)%2 = 0
(1111 dot 11111111)%2 = 0
(1111 dot 01101111)%2 = 0
(1111 dot 00111111)%2 = 0
(1111 dot 11001111)%2 = 0
(1111 dot 01011111)%2 = 0
(1111 dot 00001111)%2 = 0
```



Actual hardware runtime plot: